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(54) Title: SAMPLING DEVICE WITH TIME-INTERLEAVED OPTICAL CLOCKING

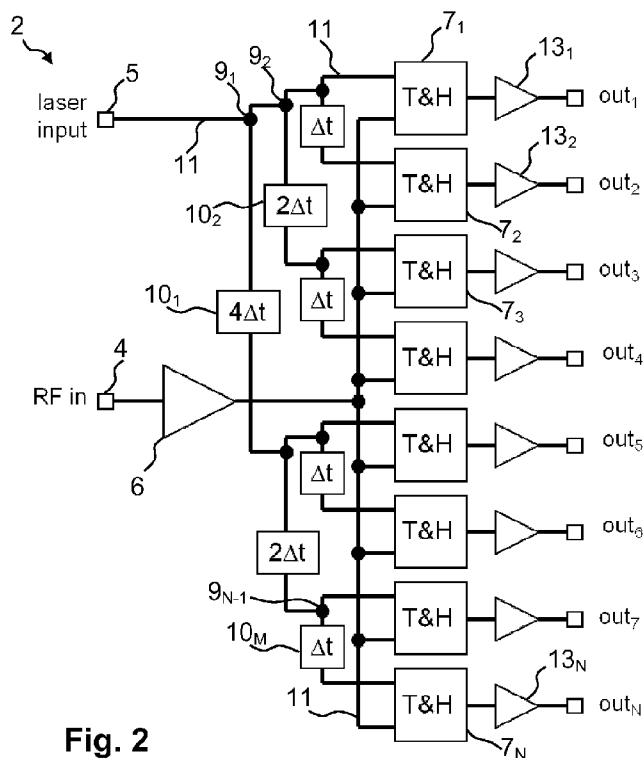


Fig. 2

(57) Abstract: A sampling device (2) comprising a
first input port (4) and a second input port (5),
wherein an input-signal is fed to the first input port
(4) and wherein an optical clock signal is fed to the
second input port (5). The sampling device (2) com-
prises a plurality of track and hold units ($7_1, 7_2, 7_N$),
wherein each of the plurality of track and hold units
($7_1, 7_2, 7_N$) is connected to the first input port (4).
The plurality of the track and hold units ($7_1, 7_2, 7_N$)
is further connected to the second input port (5)
through an optical waveguide (11) in such a manner
that the plurality of track and hold units ($7_1, 7_2, 7_N$)
operate in a time-interleaved mode.



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Sampling device with time-interleaved optical clocking

The invention relates to a sampling device which comprises a plurality of track-and-hold-units that are operated in a
5 time-interleaved mode.

The increasing need for wideband communication systems drives an increasing demand for suitable measurement systems. For analyzing those communication systems, the
10 measurement systems need a really high bandwidth and a good jitter performance. In order to obtain a measurement system having such a good jitter performance, the whole clock tree has to be stabilized.

15 The publication E. W Jacobs et al. "Optically clocked track-and-hold for high-speed, high-resolution analog-to-digital conversion" IEEE MWP '04, 2004, pages 190 - 192, describes a track-and-hold-unit that can be used within an analogue-to-digital-converter, wherein the track-and-hold-
20 unit receives an optical clock. The track-and-hold-unit therefore comprises two photodiodes that are used for generating an electrical current which is fed into a diode circuit thereby turning off a lower current from two current sources. Whenever an optical pulse is received by
25 the two photodiodes, a high frequency signal is kept constant at the output of the diode bridge.

It is a drawback of the publication that the sampling rate is limited, because the necessary hold-times for the
30 analog/digital-converter cannot be reduced anymore.

It is therefore the object of the present invention to create a sampling device that has a very high sampling rate as well as a good jitter performance.

This object is solved by the features of the independent claim 1 relating to a sampling device. Any beneficial further developments of the invention are defined in the dependent claims.

The inventive sampling device comprises a first input port and a second input port, wherein an input-signal is fed to the first input port and wherein an optical clock signal is fed to the second input port. The sampling device further comprises a plurality of track-and-hold-units, wherein each of the plurality of the track-and-hold-units is connected to the first input port and wherein the plurality of the track-and-hold-units is also connected to the second input port through an optical waveguide in such a manner that the plurality of the track-and-hold-units operate in a time-interleaved mode. It is very advantageous that a plurality of track-and-hold-units are used and that a single optical clock signal can be forwarded to those plurality of track-and-hold-units, so that only one light source is needed. It is further beneficial that the plurality of the track-and-hold-units operate in a time-interleaved mode. This ensures that the input-signal is captured by the plurality of the track-and-hold-units at different times, thereby allowing each of the plurality of the track-and-hold-units to store a part of the input-signal for a longer time.

It is also very advantageous if the optical waveguide comprises delay units, wherein the delay units delay the optical clock signal by a period of $\Delta t = 1/(N \cdot f_{\text{clk}})$, wherein f_{clk} is the frequency of the optical clock signal and wherein N is the number of the plurality of the track-and-hold-units. Therefore, each track-and-hold-unit has N

times more time to hold a part of the input-signal for the following analogue-to-digital-conversion circuit, thereby increasing the sampling frequency by the factor of N.

- 5 It is very advantageous if each delay unit is a part of the optical waveguide and if each delay unit has the shape of a meander and/or if each delay unit has segments that are parallel to each other and if each delay unit has other segments that connect the parallel segments to each other, wherein the other segments are round having a diameter that is equal or larger than the distance between the two parallel segments. The use of such delay units, that have the shape of a meander having parallel segments as well as the use of the other round segments connecting the parallel segments to each other, ensure that the power loss of the optical clock signal is minimized. However, no corners or other disadvantageous changeovers are used within the delay units.
- 10
- 15
- 20 It is further beneficial if the delay unit is a part of the optical waveguide and if this part of the optical waveguide, which forms the delay unit, has the shape of a spiral, wherein an inner segment of the delay unit which is also an inner segment of the spiral is lead to the outside within a straight line, thereby crossing the other segments at an angle of about 90° . If an angle of 90° is maintained, it is possible that the optical clock signal in different segments of the optical waveguide can cross itself without interfering itself. Therefore, the optical waveguide can be applied very easily.
- 25
- 30

It is also very advantageous, if the optical waveguide comprises N-1 optical power dividers, wherein N is the number of the plurality of the track-and-hold-units,

wherein each optical power divider splits the optical waveguide into a first branch and a second branch, and/or if the ratio of the signal power at each branch can be selected by adjusting the divergency angle of the first
5 branch and the divergency angle of the second branch with respect to an incoming signal line of the optical power divider. The use of such optical power dividers is very helpful, because the jitter performance is not degraded. It is also very useful, if the signal power at each branch
10 can be adjusted, because it can be guaranteed that each of the plurality of the track-and-hold-units receives the same signal level.

It is also very beneficial if the N-1 optical power
15 dividers are connected in the structure of a binary tree whose root is located at the second input port and whose N terminal branches connect to the N track-and-hold units. The terminal branches are also the leaf nodes of the binary tree. It should be noted, that all kinds of binary
20 trees can be used, like a perfect binary tree or a complete binary tree.

Furthermore, it is advantageous, if at least one delay unit is arranged within the second branch of each of the
25 N-1 optical power dividers. This ensures that every track-and-hold-unit operates at a different time, so that every track-and-hold-unit captures a different part of the input-signal.

30 It is further beneficial if the depths of all branches of the tree-structure comprising all descendants of the first optical power divider are the same and/or if the number of the delay units that are ranged within the second branch of every optical power divider equals the number of the

track-and-hold-units that are connected as descendants to that respective branch and/or if no delay unit is arranged within the first branch of every optical power divider. This ensures that all N-1 optical power dividers are
5 arranged symmetrically so that the only difference in the various branches is the number of the delay units. This allows that the signal power can be adjusted more easily within the N-1 optical power dividers, so that each of the plurality of the track-and-hold-units receives
10 approximately the same signal level.

It is also very advantageous if the sampling device comprises a plurality of opto-electronic flip-flops, wherein each of the plurality of the opto-electronic flip-
15 fops transforms the optical clock signal into an electrical clock signal, wherein each of the plurality of the opto-electronic flip-flops connects each of the track-and-hold-units to the optical waveguide. This ensures that the electrical clock signal has a duty cycle of
20 approximately 50%, wherein the light pulses of the optical clock signal are much smaller.

It is also very beneficial if the optical waveguide is made of a layer of germanium or SiO₂ and/or if the optical
25 waveguide, the optical power splitters and the delay units are made of germanium or SiO₂ and if they are arranged on a first part of the wafer and if the plurality of the track-and-hold-units and the opto-electronic flip-flops are made of SiGe and if they are arranged on a second part
30 of the wafer and if the opto-electric flip-flop comprises a photodiode that is arranged in between the two parts of the wafer. This ensures that the wafer can be used by the optic elements as well by the electronic elements. This allows that all of the aforementioned components can be

integrated within a single chip, thereby reducing the unit costs.

It is further beneficial if a mode locked laser is used to generate the optical clock signal and if the mode locked laser is connected through an optical fiber to the second input port. A mode locked laser has very good jitter performance as well as an output power on the order of 30 mW.

10

Different embodiments of the present invention are described exemplary in the following with reference to the description. This is done by the way of example only, without limitation. Identical elements have the same reference signs. The figures in the drawings show:

15

Fig. 1 a high speed sampling unit comprising an embodiment of the sampling device according to the present invention and a plurality of track-and-hold-units which are operated in a time-interleaved mode;

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Fig. 2 a sampling device according to an embodiment of the present invention;

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Fig. 3 a simplified layout of the sampling device according to an embodiment of the present invention;

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Fig. 4 a simplified layout of the sampling device according to another embodiment of the present invention;

- Fig. 5A an embodiment of an optical power divider according to the present invention;
- 5 Fig. 5B an embodiment of an optical waveguide operating as delay unit according to the present invention;
- 10 Fig. 5C another embodiment of an optical waveguide operating as delay unit according to the present invention;
- Fig. 6 an embodiment of an opto-electronic flip-flop used as an electronic clock generator;
- 15 Fig. 7 an embodiment of a simplified track and hold unit; and
- 20 Fig. 8 an embodiment of a simplified chip structure carrying the sampling device according to the present invention.

Fig. 1 shows a high-speed sampling unit 1 comprising the sampling device 2, which in turn comprises track-and-hold-units 7_1 , 7_2 to 7_N which are operated in a time-interleaved

25 mode. In some cases, the high-speed sampling unit 1 can be integrated within a single chip or ASIC. However, it is also possible that the sampling device 2 can be integrated on a chip of its own while the analog/digital-converters 3_1 , 3_2 to 3_N are located on separate chips. It should be

30 noted, that the analog/digital-converters 3_1 , 3_2 to 3_N are only incorporated within Fig. 1 for a better understanding and that they are not a necessary part of the invention. The sampling device 2 further comprises a first input port 4 and a second input port 5. An electrical input-signal,

i.e. a RF-signal, is fed to the first input port 4. The RF-signal is a high-frequency signal having a bandwidth of approximately up to 30 GHz and above.

5 The RF-signal is then amplified by at least one amplifier 6. However, if N is small, for example four or eight the RF-signal does not need to be amplified. The amplification factor of the at least one amplifier 6 is preferably adjustable. The amplified RF-signal is then fed to each of
10 a plurality of the track-and-hold-units 7_1 , 7_2 to 7_N . The amplified RF-signal can therefore be split up for example by using a 3-dB hybrid-coupler. It is also possible to abstain from using a 3-dB hybrid-coupler within a chip, because the signal lines should be short enough.

15

Furthermore, the high-speed sampling unit 1 comprises an optical clock source 8. The optical clock source is preferably a mode locked laser 8. The mode locked laser 8 is difficult to integrate within a chip together with the
20 other components of the high-speed sampling unit 1. The mode locked laser 8 generates an optical clock signal having a frequency f_{clk} of, for example, 10 GHz. The energy for each pulse exceeds for example 3 pJ and the timing jitter is smaller than 20 fs RMS.

25

The sampling device 2 preferably comprises the at least one amplifier 6, the plurality of the track-and-hold-units 7_1 , 7_2 to 7_N as well as at least one optical power divider 9 and at least one delay unit 10_1 , 10_2 .

30

The mode locked laser 8 is connected to the second input port by using an optical fiber. Within the sampling device 2 which can also be within a chip, an optical waveguide 11 is used to lead the optical clock signal to each of the

plurality of the track-and-hold-units $7_1, 7_2$ to 7_N . It is very important that the optical clock signal is fed to the plurality of the track-and-hold-units $7_1, 7_2$ to 7_N in such a manner that the plurality of the track-and-hold-units
5 are operated in a time-interleaved mode.

The second input port 5 which is connected to the optical waveguide 11 is connected to a first optical power divider 9. A first branch of the first optical power divider is
10 connected to the first track-and-hold-unit 7_1 . A second branch of the first optical power divider 9 is connected to a first delay unit 10_1 . The first delay unit 10_1 is further connected to a another delay unit 10_M , wherein $M \geq 1$ and $M \in \mathbb{N}$. Within the first delay unit 10_1 there is
15 also another optical power divider which splits up the optical clock signal into a signal that is fed to the second track-and-hold-unit 7_2 . Another signal of the another optical power divider is then fed to the other track-and-hold-units 7_N , wherein $N \geq 2$ and $N \in \mathbb{N}$.

20

It should also be noted that all branches which extend from every optical power divider 9 still belong to the optical waveguide 11.

25 Every delay unit 10_1 to 10_M delays the optical clock signal by a period $\Delta t = 1/(N \cdot f_{\text{clk}})$, wherein f_{clk} is the frequency of the optical clock signal. If the number for N is three for example, each delay unit 10_1 to 10_M delays the optical clock signal by the factor of $1/3$ period. This
30 means that the track-and-hold-units $7_1, 7_2$ to 7_N can store a part of the RF-signal for a whole clock period, thereby ensuring that the RF-signal is sampled with a frequency that is three times higher than the frequency of the optical clock signal.

Each of the plurality of the track-and-hold-units $7_1, 7_2$ to 7_N comprises further a plurality of opto-electronic flip-flops $12_1, 12_2$ to 12_N which transform the optical clock
5 signal into an electrical clock signal. The plurality of the opto-electronic flip-flops $12_1, 12_2$ to 12_N therefore connect each of the track-and-hold-units $7_1, 7_2$ to 7_N to the optical waveguide 11. The plurality of the opto-electronic flip-flops $12_1, 12_2$ to 12_N also enhance the duty
10 cycle of the electrical clock signal to approximately 50%. The opto-electronic flip-flops $12_1, 12_2$ to 12_N can be integrated within the track-and-hold-units $7_1, 7_2$ to 7_N , but they can also be separated from the respective track-and-hold-units $7_1, 7_2$ to 7_N . Thus they can be integrated
15 somewhere in the sampling device 2.

The output of each of the plurality of the track-and-hold-units $7_1, 7_2$ to 7_N is preferably connected to an amplifier $13_1, 13_2$ to 13_N . The amplifiers $13_1, 13_2$ to 13_N drive the
20 inputs of the analog/digital converters. Furthermore, the analog/digital-converters $3_1, 3_2$ to 3_N are preferably arranged outside of the chip, because the chip may not be large enough. Each of the analog/digital-converters $3_1, 3_2$ to 3_N has a plurality of parallel output ports which can
25 be used for a high-speed data transfer.

Fig. 2 shows a sampling device 2 according to the present invention. The sampling device 2 comprises a plurality of track-and-hold-units $7_1, 7_2$ to 7_N . In this case the
30 interleaving factor N equals eight, which also means that there are eight track-and-hold-units $7_1, 7_2$ to 7_N . It can also be seen that there is a plurality of delay units 10_1 to 10_M . Each delay unit $10_1, 10_M$ is a part of the optical waveguide 11 which is explained in detail below.

The optical waveguide 11 further comprises N-1 optical power dividers 9_1 to 9_{N-1} wherein N is the interleaving factor as well as the number of the plurality of the track-and-hold-units $7_1, 7_2$ to 7_N . Each optical power divider 9_1 to 9_{N-1} splits the optical waveguide 11 into a first branch and into a second branch. If the optical waveguide 11 is nearly lossless, each branch should get half the incoming optical power. In practice, the optical waveguide may have substantial losses, whereby a larger attenuation will occur on a branch with a large delay compared to a branch with a small delay. In this case, it is preferable to provide more power to the branch with a large delay so that the power at the output of each branch will be substantially equal. The ratio of the signal power at each branch can be selected by adjusting the divergency angle of the first branch and the divergency angle of the second branch with respect to the incoming signal line of the respective optical power divider 9_1 to 9_{N-1} . These details will also be explained below.

The ratio of the signal power of all N-1 optical power dividers 9_1 to 9_{N-1} is adjusted in such a way that the signal power at each end node of the optical waveguide 11 or at each of the plurality of the track-and-hold-units $7_1, 7_2$ to 7_N is approximately the same. More precisely, the ratio of the signal power of all N-1 optical power dividers 9_1 to 9_{N-1} has to be adjusted in such a way that the signal power should be the same at the input port of the plurality of the opto-electronic flip-flops $12_1, 12_2$ to 12_N , wherein the opto-electronic flip-flops $12_1, 12_2$ to 12_N are integrated within the track-and-hold-units $7_1, 7_2$ to 7_N or wherein the opto-electronic flip-flops 12_1 to 12_N

are arranged in front of the track-and-hold-units 7_1 , 7_2 to 7_N , i.e. upstream in the signal path.

Fig. 2 describes a symmetrical tree-structure of the optical waveguide 11. This means that the depth of all branches of the tree-structure is the same, wherein the tree-structure comprises all descendants of the first optical power divider 9_1 . The descendants comprise the further optical power dividers 9_2 to 9_{N-1} as well as the plurality of the delay units 10_1 , 10_2 to 10_M . The descendants are connected to the first branch or the second branch of the first optical power divider 9_1 . The first optical power divider 9_1 is thereby connected to the second input port 5. In the embodiment of Fig. 2 the depth of the tree-structure is three.

Furthermore, the number of the delay units 10_1 to 10_M arranged within a second branch of every optical power divider 9_1 to 9_{N-1} equals the number of the track-and-hold-units 7_1 , 7_2 to 7_N that are connected as descendants to the respective branch. For example, the second branch of the first optical divider 9_1 comprises four delay units 10_1 . This is indicated by the number "4" before Δt . However, the second branch of the first optical divider 9_1 is connected to four track-and-hold-units 7_1 , 7_2 to 7_N at the end. The same also applies to the second branch of the second optical divider 9_2 . The second branch of the second optical divider 9_2 is connected to two track-and-hold-units 7_1 , 7_2 to 7_N , which means that two delay units 10_2 are incorporated within the second branch of the second optical power divider 9_2 .

A branch is a line segment of the optical waveguide 11 that extends from the output of each of the optical power

dividers 9_1 to 9_{N-1} and ends at the input of the descendant optical power divider 9_1 to 9_{N-1} or at the input port of the opto-electronic flip-flop 12_1 to 12_N or at the input port of the track-and-hold-unit 7_1 , 7_2 to 7_N . Into each
 5 branch a delay unit 10_1 to 10_M can be incorporated. As described in detail below the delay unit 10_1 to 10_M is an integral part of the optical waveguide 11 having a special wiring.

- 10 In the embodiment of Fig. 2 according to the present invention no delay units 10_1 to 10_M are arranged within the first branch of every optical power divider 9_1 to 9_{N-1} . It is clear that the optical clock signal, which is fed to the first track-and-hold-unit 7_1 , is only delayed by the
 15 length of the optical waveguide 11 from the second input port 5 to the respective input port of the opto-electronic flip-flop 12_1 of the first track-and-hold-unit 7_1 . However, the optical clock signal of the second track-and-hold-unit 7_2 is delayed by one delay unit by a period $\Delta t = 1/(N \cdot f_{clk})$.
 20 If the period has a length of 100 ps the optical clock signal for the second track-and-hold-unit 7_2 is delayed by 12.5 ps. It is also clear that the clock signal for the third track-and-hold-unit 7_3 is delayed by 25 ps compared to the clock signal fed to the first track-and-hold-unit
 25 7_1 .

When calculating the division ratio of the optical power dividers 9_1 to 9_{N-1} the amount of the descendant branches have to be taken into account comprising the amount of the
 30 descendant delay units 9_1 to 9_{N-1} . For example, the first branch of the first optical power divider 9_1 comprises four descendant delay units 10_1 to 10_M , wherein the second branch of the first optical power divider 9_1 comprises eight delay units 10_1 to 10_M . Putting all this information

together, the division ratio of all the optical power dividers 9_1 to 9_{N-1} can be calculated, so that the input signal level is the same for all of the plurality of the opto-electronic flip-flop 12_1 to 12_N or for the plurality of the track-and-hold-units 7_1 , 7_2 to 7_N .

However, it should be clear that the tree-structure described above can also be brought forward to a sampling device 2 having more or less track-and-hold-units 7_1 , 7_2 to 7_N than shown in Fig. 2.

There are also other tree-structures possible that do not have to be symmetrical. However, all tree-structures have in common that the root-node is connected to the second input port 5 and that a plurality of end-nodes are connected to the plurality of the track-and-hold-units 7_1 , 7_2 to 7_N or to the plurality of the opto-electronic flip-flops 12_1 to 12_N . The at least one delay unit 10_1 to 10_M delays the optical clock signal in such a manner that each of the plurality of the track-and-hold-units 7_1 , 7_2 to 7_N captures a part of the RF (radio frequency)-input-signal at a different time.

As already mentioned other tree-structures for the optical waveguide 11 can also be used. For example, the $N-1$ optical power dividers 9_1 to 9_{N-1} can be connected in series so that each optical power divider 9_1 to 9_N is connected to the second branch of a respective parent optical power divider 9_1 to 9_{N-1} , wherein the first optical power divider 9_1 is connected to the second input port 5 and wherein the first branch of each of the $N-1$ optical power dividers 9_1 to 9_{N-1} is connected to the respective track-and-hold-unit 7_1 , 7_2 to 7_N . Such a structure is shown in Fig. 1 for example.

Furthermore, one delay unit 10_1 to 10_M is arranged within the second branch of each of the $N-1$ optical power dividers 9_1 to 9_{N-1} . This kind of tree-structure can preferably be used if the number of the track-and-hold-units $7_1, 7_2$ to 7_N is small. Thus, the division ratio within the first optical power divider 9_1 can easily be adjusted. However, if there are, for example, 32 track-and-hold-units $7_1, 7_2$ to 7_N the first optical power divider 9_1 should have a division ratio of at least 1:32 which is difficult to obtain.

The plurality of the track-and-hold-units $7_1, 7_2$ to 7_N are connected to the plurality of amplifiers 13_1 to 13_N , wherein the output of the plurality of the amplifiers 13_1 to 13_N is preferably also the output of the chip.

Fig. 3 shows a simplified layout of the sampling device 2 according to an embodiment of the present invention. As already mentioned an RF-signal is fed to the first input port 4. Within an RF-distribution circuit 30, the RF-signal is split into N individual signals which are fed to the plurality of the track-and-hold-units $7_1, 7_2$ to 7_N . The RF-distribution circuit 30 comprises several amplifiers 6 for amplifying each of the individual RF-signals. It should be noted that the RF-distribution circuit 30 is matched with respect to the first input port 4.

Furthermore, as already described, an optical clock signal is fed to the second input port 5. This optical clock signal is preferably generated by a mode locked laser 8. The optical clock signal is then split up by a first optical power divider 9_1 which is part of the optical waveguide 11.

In order to simplify the arrangement, the plurality of opto-electronic flip-flops 12_1 to 12_N which transform an optical clock signal into an electrical clock signal are
5 not shown within Fig. 3.

The plurality of the delay units 10_1 to 10_M are also shown within the layout of Fig. 3. The delay units 10_1 to 10_M which are part of the optical waveguide 11 have the shape
10 of a meander. It has to be noted that the corners of the meander of the delay units 10_1 to 10_M are illustrated disproportionately. As described below, the meander structure has only round segments which connect the parallel segments to each other. The meander structure
15 thereby increases the light length with respect to the typically straight lines of the optical waveguide 11. It can clearly be seen that the optical clock signal for the first track-and-hold-unit 7_1 does not travel through any delay unit 10_1 to 10_M . The optical clock signal for the
20 last track-and-hold-unit 7_N travels through $N-1$ delay units 10_1 to 10_M .

If the clock signal has a period of 100 ps each output port is delayed to the respective adjacent output port by
25 12.5 ps. Because a mode locked laser has a very good jitter performance, the difference between the delay times of each output port is constant.

Fig. 4 shows a simplified layout of the sampling device 2
30 according to another embodiment of the invention. The interleaving factor N is higher in Fig. 4 compared to the interleaving factor in Fig. 2. The interleaving factor N equals 16 so that there are also 16 track-and-hold-units $7_1, 7_2$ to 7_N . It can also be seen that an RF-signal is fed

to the first input port 4. The RF-signal is then split into two signal paths, wherein each signal path comprises an amplifier 6. Each signal path is then further split, so that a part of the RF-signal which is fed to the first
5 input port 4 also applies at the input port of each of the plurality of the track-and-hold-units $7_1, 7_2$ to 7_N .

Fig. 4 also shows the second input port 5 which is connected through an optical fiber to the mode locked
10 laser 8. The input port 5 consists of a grating, which couples the incident light into the optical waveguide 11. This ensures that as much power of the light pulses as possible can be injected into the optical waveguide 11. Other forms which also reduce the power loss of the
15 optical clock signal at the second input port 5 are also suitable.

As already described, the optical waveguide 11 is split by first optical power divider 9_1 into a first branch and a
20 second branch. As already described a plurality of delay units 10_1 to 10_M are formed within the optical waveguide 11. Each delay unit 10_1 to 10_M is separated from the adjacent delay unit 10_1 to 10_M as indicated by a dotted line. The number of the delay units 10_1 to 10_M which are
25 arranged within the second branch of the first optical power divider 9_1 also equals the number of the track-and-hold-units $7_1, 7_2$ to 7_N that are connected as descendants to the respective branch. In this case eight track-and-hold-units $7_1, 7_2$ to 7_N are connected as descendants to the
30 second branch of the first optical power divider 9_1 . Thus, there are eight delay units inserted within the second branch. The same also applies for example for the second optical power divider 9_2 . In this case there are four track-and-hold-units $7_1, 7_2$ to 7_N that are connected to the

second branch of the second optical divider 9_2 . Therefore, the second branch of the second optical power divider 9_2 comprises four delay units 10_1 to 10_M . On the other hand, as already mentioned, the first branch of every optical power divider 9_1 to 9_{N-1} does not comprise any delay unit 10_1 to 10_M .

Fig. 4 also shows the plurality of the opto-electronic flip-flops 12_1 to 12_N . Each of the opto-electronic flip-flops 12_1 to 12_N is arranged at an input port of a track-and-hold-units $7_1, 7_2$ to 7_N . Each opto-electronic flip-flop 12_1 to 12_N transforms an optical clock signal to an electronic clock signal that is fed to the respective track-and-hold-unit $7_1, 7_2$ to 7_N . It is also desirable that the optical clock signal has about the same power level at every opto-electronic flip-flop 12_1 to 12_N . This goal is achieved by a suitable angle between the first and the second branch of each of the optical power dividers 9_1 to 9_{N-1} with respect to the input port of the optical power divider 9_1 to 9_{N-1} .

Fig. 5A shows a simplified embodiment of the optical power divider 9_1 to 9_{N-1} . It can be seen that the optical power divider 9_1 to 9_{N-1} has one incoming signal line 50 which is part of the optical waveguide 11. The incoming signal line 50 is split into a first branch 51_1 and a second branch 51_2 . The ratio of the signal power at each branch $51_1, 51_2$ can be selected by adjusting the divergency angle 52_1 of the first branch and the divergency angle 52_2 of the second branch 51_2 with respect to the incoming signal line 50 of the optical power divider 9_1 to 9_{N-1} . If the starting point of the first branch 51_1 and the second branch 51_2 is in the middle of the incoming signal line and if both divergency angles are 45° , the optical power divider 9_1 to

9_{N-1} divide the optical clock signal into two clock signals both having the same signal power level.

Furthermore, a corner 53 which connects the first branch 51₁ to the second branch 51₂ can be slid along the width of the incoming signal line 50 to further adjust the division ratio which allows building optical power dividers 9₁ to 9_{N-1} that have a very high division ratio of for example 1:30 or above. Those kind of optical power dividers 9₁ to 9_{N-1} can be used if an asymmetrical tree-structure of the optical waveguide 11 should be realized.

The first branch 51₁ and the second branch 51₂ shown in the embodiment of Fig. 5A have a smaller width than the incoming signal line 50. It should be clear that the first branch 51₁ and the second branch 51₂ can also have a width that equals the width of the incoming signal line 50 or they can have a width that is larger than the one of the incoming signal line 50.

As already mentioned, the incoming signal line 50 as well as the first branch 51₁ and the second branch 51₂ of each optical power divider 9₁ to 9_{N-1} are part of the optical waveguide 11 and are therefore made of a transparent layer of germanium or SiO₂. The optical power divider 9₁ to 9_{N-1} as well as the whole optical waveguide 11 can easily be structured on a common wafer. Furthermore it is also possible to create an optical power divider that has more than two branches.

Fig. 5B shows an embodiment of a part of an optical waveguide 11 operating as delay unit 10₁ to 10_M according to the present invention. Within Fig. 3 and Fig. 4 it is shown that the delay unit 10₁ to 10_M is part of the

optical waveguide 11 and that this part of the optical waveguide 11 has the shape of a meander. However, the delay units 10_1 to 10_M can also have the shape of a spiral, wherein an inner segment 55 of the delay unit 10_1 to 10_M is lead to the outside by using a straight line 56 thereby crossing the other segments 57_1 , 57_2 at an angle of about 90° . An angle of 90° ensures that the delayed clock signal on the straight line 56 does not interfere with the more or less delayed clock signals on the other segments 57_1 , 57_2 . As already mentioned it has to be assured that no corners are used.

The larger the radius of all parts of the spiral shaped delay units 10_1 to 10_M is, the more can the loss of the optical power be reduced.

Fig. 5C shows another embodiment of an optical waveguide 11 operating as a delay unit 10_1 to 10_M according to the present invention. As mentioned above, the delay unit 10_1 to 10_M can have the shape of a meander, wherein the delay unit 10_1 to 10_M has segments 60_1 , 60_2 that are parallel to each other and wherein the delay unit 10_1 to 10_M has other segments 61 that are round, thereby connecting the parallel segments 60_1 , 60_2 to each other. The radius of the other segments 61 can be equal to the distance between the two parallel segments 60_1 , 60_2 as shown in Fig. 4. However, the diameter of the other segments can also be larger than the distance between the two parallel segments 60_1 , 60_2 as shown in Fig. 5C. If the other segment 61 has a radius that is larger than the distance between the two parallel segments, the optical power loss is further reduced.

Fig. 6 shows an embodiment of an opto-electronic flip-flop 12₁ to 12_N that can be used as an electronic clock generator. The opto-electronic flip-flop 12₁ to 12_N comprises several transistors 60₁, 60₂, 60₃, 60₄. The
5 emitters of the transistors 60₁, 60₂ are connected to a photodiode 61, which, for its part, is connected to a negative supply voltage, which can also be connected to ground. Data inputs D and $\overline{D}$ are connected to the base terminals of the transistors 60₁, 60₂. The collectors of
10 the transistors 60₁, 60₂ are each connected by means of a resistor 62₁, 62₂ to a positive supply voltage.

The photodiode 61 in this circuit is connected in such a manner that only minimal leakage current flows, as long as
15 no light falls on the photodiode 61. As soon as light falls onto the photodiode 61, a photocurrent passes from an n-doped to a p-doped region of the photodiode. The intensity of the photocurrent is, in a good approximation, proportional to the luminous power of the laser pulse.

20

Fig. 6 shows also a differential pair of transistors 60₃, 60₄ which form a latch. The base terminals of this differential pair are connected crosswise to the collector terminals of the transistors 60₁, 60₂. That is to say, the
25 base terminal of the transistor 60₃ is connected to the collector terminal of the transistor 60₁. The base terminal of the transistor 60₄ is connected to the collector terminal of the transistor 60₂. Moreover, the collector terminal of the transistor 60₃ is connected to
30 the collector terminal of the transistor 60₂. The collector terminal of transistor 60₄ is also connected to the collector terminal of transistor 60₁. The emitter terminals of the transistors 60₃, 60₄ are connected via a current source 63 to a negative supply voltage, which can

also be connected to ground. As a result of the crosswise wiring, a positive feedback is generated, and accordingly, the logical status of the latch is maintained. In this context, the zero-signal current of the latch generated by
5 the current source 63 must be significantly smaller than the photocurrent which is generated by the photodiode 61. Only if this condition is fulfilled, can the photocurrent of the photodiode 61 exceeds the zero-signal current of the current source 63 and accordingly varies the logical
10 status of the latch.

The optically controlled D-flip-flop, also called the opto-electronic flip-flop 12_1 , 12_2 to 12_N , illustrated here can be used for a plurality of applications. In
15 particular, it is suitable for use in a high-precision clock generator that can be used i.e. within a sampling device 2 according to the present invention. In order to generate an electrical clock signal, of which the clock statuses provide the same length (duty cycle 50%), a
20 feedback loop has also to be implemented.

Fig. 6 shows also a delaying device 64. The delaying device 64 comprises two transistors 65_1 , 65_2 , a current source 66 and two resistors 67_1 , 67_2 . The two resistors
25 67_1 , 67_2 are each connected between a positive supply voltage and the collector of one of the transistors 65_1 , 65_2 as load resistors. The emitters of the transistors 65_1 , 65_2 are each connected to the current source 66, which is connected to a negative supply voltage, which can
30 also be connected to ground. The base of the transistor 65_1 is connected to the base of the transistor 60_4 . The base of the transistor 65_2 is connected to the base of the transistor 60_3 . Moreover, the collector of the transistor 65_1 is connected to the base of the transistor 60_1 as a

feedback. Similarly, the collector of the transistor 65₂ is connected to the base of the transistor 60₂.

Fig. 7 shows an embodiment of a simplified track-and-hold-unit 7₁, 7₂ to 7_N. It can be seen that the simplified track-and-hold-unit 7₁, 7₂ to 7_N has three input ports. An RF-signal is fed to the first input port 70, wherein a clock signal is fed to a second input port 71, wherein a clock-not-signal is fed to the third input port 72. The first input port of the track-and-hold-unit 7₁ to 7_N is connected to one end of a resistor 73, wherein the other end of the resistor 73 is connected to a supply voltage. Furthermore, the first input port 70 is also connected to a base of a transistor 74 and to a collector of another transistor 75. The collector of the transistor 74 is also connected to the supply voltage. The emitter of the transistor 74 is connected to a collector of a further transistor 76 and to one end of a capacitor 77, wherein the other end of the capacitor 77 is connected to a supply voltage that can be ground for example. The base of the further transistor 76 is connected to the second input port 71 of the simplified track-and-hold-unit 7₁ to 7_N, wherein the base of the other transistor 75 is connected to the third input port 72 of the simplified track-and-hold-unit 7₁ to 7_N. The emitters of the other transistor 75 and the further transistor 76 are connected together and to a current source 79.

However, instead of connecting the third input port 72 of the simplified track-and-hold-unit 7₁ to 7_N to a clock-not-signal, the third input port 72 can also be connected to a constant voltage source, if the voltage is lower than the logic "high" level of the electric clock signal and higher than the logic "low" level of the electrical clock

signal, wherein the electrical clock signal is fed to the second input port 71. Otherwise, a clock-not-signal can be input to the third input port 72 too, wherein the clock-not-signal has a phase shift of 180° with respect to the electrical clock signal which is input to the second input port 71.

If the logic level of the electrical clock signal is "high", the further transistor 76 is in a conducting state. Thus, the capacitor 77 is charged with a part of the RF-signal, wherein the part equals the RF-signal minus the voltage U_{BE} of the transistor 74. If the logic level of the electrical clock signal is "low" at the second input port 71 of the simplified track-and-hold-unit 7_1 to 7_N , the other transistor 75 is in a conducting state which ensures that the transistor 74 is not in a conducting state. The resistor 73 enhances this effect.

Fig. 8 shows an embodiment of a chip structure carrying the sampling device 2 according to the present invention. The chip comprises a silicon wafer as a ground structure. Furthermore, the optical waveguide 11 comprising the optical power splitters 9_1 to 9_{N-1} and the delay units 10_1 to 10_M are arranged on a first part 80_1 of the wafer. The optical waveguide 11 together with the aforementioned components are made of a layer which is transparent for the respective wavelength of the light source, i.e. germanium or SiO_2 . It should be mentioned that other materials that can be deposited on a wafer and that have a transparent structure can be used as well for creating the optical waveguide 11.

On the other side the plurality of the track-and-hold-units 7_1 to 7_N and the opto-electronic flip-flops 12_1 to

12_N are arranged on a second part 80₂ of the wafer. It should be noted that the photodiode 61 within the optoelectronic flip-flop 12₁ to 12_N is preferably arranged at the changeover between the first part 80₁ and the second
5 part 80₂ of the wafer. The components of the second part 80₂ are preferably made of SiGe. It should be clear that other materials can be used as well if they can be deposited on a wafer and if they are suitable for high-speed data rates.

10

Instead of using the optical delay units 10₁ to 10_M it is also possible to delay the electrical RF-signal which is input at the first input port 4. This could be done in a limited range by a proper insertion of varactors, for
15 example by insertion of voltage-dependent capacitors.

The invention is not restricted to the exemplary embodiment presented. All of the features described above or illustrated in the drawings can be advantageously
20 combined with one another as required within the scope of the invention. Other transistors, such as PNP bipolar transistors, NMOS or PMOS transistors or even other FET transistors can be used instead of NPN transistors. Other light sources instead of a mode locked laser can be used,
25 such as stroke lamps, LEDs or other kind of lasers, such as semiconductor lasers. A semiconductor laser might be integrated on the same chip if layers of a III-V-semiconductor, such as InGaAs is applied on the Si-substrate by MBE for example.

30

Claims

1. A sampling device (2) comprising a first input port (4) and a second input port (5),
5 wherein an input-signal is fed to the first input port (4) and wherein an optical clock signal is fed to the second input port (5),
characterized in that,
the sampling device (2) comprises a plurality of track and
10 hold units ($7_1, 7_2, 7_N$), wherein each of the plurality of track and hold units ($7_1, 7_2, 7_N$) is connected to the first input port (4) and
that the plurality of track and hold units ($7_1, 7_2, 7_N$) is connected to the second input port (5) through an optical
15 waveguide (11) in such a manner that the plurality of track and hold units ($7_1, 7_2, 7_N$) operate in a time-interleaved mode.
2. A sampling device according to claim 1,
20 **characterized in that,**
the optical waveguide (11) is arranged in a tree-structure, wherein a root-node is connected to the second input port (5) and wherein each of a plurality of end-nodes is connected to one of the track and hold units ($7_1,$
25 $7_2, 7_N$), wherein the optical waveguide (11) comprises at least one delay unit ($10_1, 10_2, 10_M$) that delays the optical clock signal so that each of the plurality of track and hold units ($7_1, 7_2, 7_N$) captures the RF-signal at a different time.
- 30
3. A sampling device according to claim 2,
characterized in that,
each delay unit ($10_1, 10_2, 10_M$) delays the optical clock signal by a period $\Delta t = 1/(N \cdot f_{clk})$, wherein N is the number

of the plurality of the track and hold units ($7_1, 7_2, 7_N$) and wherein f_{clk} is the frequency of the optical clock signal.

- 5 4. A sampling device according to claim 2 or 3,
characterized in that,
each delay unit ($10_1, 10_2, 10_M$) is a part of the optical waveguide (11) and that this part of the optical waveguide (11) has the shape of a meander and/or
10 that each delay unit ($10_1, 10_2, 10_M$) has segments ($60_1, 60_2$) that are parallel to each other and that the delay unit ($10_1, 10_2, 10_M$) has other segments (61) that connect the parallel segments ($60_1, 60_2$) to each other, wherein the other segments (61) are round having a diameter that
15 is equal or larger than the distance between the two parallel segments ($60_1, 60_2$).

5. A sampling device according to claim 2 to 4,
characterized in that,
20 each delay unit ($10_1, 10_2, 10_M$) is a part of the optical waveguide (11) and that this part of the optical waveguide (11) has the shape of a spiral, wherein an inner segment (55) of the delay unit ($10_1, 10_2, 10_M$) is lead to the outside within a straight line (56) thereby preferably
25 crossing other segments ($57_1, 57_2$) of the spiral at an angle of about 90 degree.

6. A sampling device according to claim 2 to 5,
characterized in that,
30 the optical waveguide (11) comprises N-1 optical power dividers ($9; 9_1, 9_2, 9_{N-1}$) wherein N is the number of the plurality of the track and hold units ($7_1, 7_2, 7_N$), wherein each optical power divider ($9; 9_1, 9_2, 9_{N-1}$) splits the

optical waveguide (11) into a first branch (51₁) and a second branch (51₂).

7. A sampling device according to claim 6,

5 **characterized in that,**

that the ratio of the signal power at each branch (51₁, 51₂) can be selected by adjusting the divergency angle of the first branch (51₁) and the divergency angle of the second branch (51₂) with respect to an incoming signal
10 line (50) of the optical power divider (9; 9₁, 9₂, 9_{N-1}).

8. A sampling device according to claim 7,

characterized in that,

that the ratio of the signal power of all N-1 optical
15 power dividers (9; 9₁, 9₂, 9_{N-1}) is adjusted in such a way that the signal power at each end-node or at each of the plurality of track and hold units (7₁, 7₂, 7_N) is approximately the same.

20 9. A sampling device according to any of the claims 6 to 8,

characterized in that,

the N-1 optical power dividers (9; 9₁, 9₂, 9_{N-1}) are connected in series so that each optical power divider (9;
25 9₁, 9₂, 9_{N-1}) is connected to the second branch (51₂) of a respective parent optical power divider (9; 9₁, 9₂, 9_{N-1}) and that the first optical power divider (9; 9₁) is connected to the second input port (5) and that the first branch (51₁) of the N-1 optical power dividers (9; 9₁, 9₂,
30 9_{N-1}) is connected to the respective track and hold unit (7₁, 7₂, 7_N).

10. A sampling device according to any of the claims 6 to 9,

characterized in that,

one delay unit (10_1 , 10_2 , 10_M) is arranged within the second branch (51_2) of each of the N-1 optical power dividers (9 ; 9_1 , 9_2 , 9_{N-1}).

5

11. A sampling device according to claim 6 to 8,

characterized in that,

a depth of all branches (51_1 , 51_2) of the tree-structure comprising all descendants of the first optical power

10 divider (9 ; 9_1) is the same and/or

that the number of delay units (10_1 , 10_2 , 10_M) arranged within the second branch (51_2) of every optical power divider (9 ; 9_1 , 9_2 , 9_{N-1}) equals the number of the track and hold units (7_1 , 7_2 , 7_N) that are connected as

15 descendants to that respective branch (51_2) and/or

that no delay unit (10_1 , 10_2 , 10_M) is arranged within the first branch (51_1) of every optical power divider (9 ; 9_1 , 9_2 , 9_{N-1}).

20 12. A sampling device according to claim 6 to 8 or claim 11,

characterized in that,

the N-1 optical power dividers (9 ; 9_1 , 9_2 , 9_{N-1}) are connected in the structure of a binary tree whose root is located at the second input port (5) and whose N terminal branches (51_1 , 51_2) connect to the N track-and-hold units (7_1 , 7_2 , 7_N).

25

13. A sampling device according to any of the preceding claims,

30

characterized in that,

the sampling device (2) comprises a plurality of opto-electronic flip-flops (12_1 , 12_2 , 12_N), wherein each of the plurality of the opto-electronic flip-flops (12_1 , 12_2 , 12_N)

transforms the optical clock signal into an electrical clock signal, wherein each of the plurality of the opto-electronic flip-flops (12_1 , 12_2 , 12_N) connects each of the track and hold units (7_1 , 7_2 , 7_N) to the optical waveguide (11) and/or wherein the electrical clock signal has a duty cycle of approximately 50%.

14. A sampling device according to claim 13,
characterized in that,
each of the plurality of track and hold units (7_1 , 7_2 , 7_N) captures a part of the input-signal at the rising or falling edge of the respective optical clock signal or the respective transformed electrical clock signal for the duration of one clock period and/or
that the maximum frequency of the optical clock signal is equal to a maximum sampling frequency of a plurality of analog/digital-converters (3_1 , 3_2 , 3_N) wherein each of the analog/digital-converters (3_1 , 3_2 , 3_N) is connected to one of the plurality of the track and hold units (7_1 , 7_2 , 7_N).

15. A sampling device according to claim 13 or 14 and 3 and 6,
characterized in that,
the optical waveguide (11) is made of a layer of germanium or SiO_2 and/or
that the optical waveguide (11), the optical power splitters (9 ; 9_1 , 9_2 , 9_{N-1}) and the delay units (10_1 , 10_2 , 10_M) are made of germanium or SiO_2 and are arranged on a first part (80_1) of a wafer and that the plurality of track and hold units (7_1 , 7_2 , 7_N) and the opto-electronic flip-flops (12_1 , 12_2 , 12_N) are made of SiGe heterojunction bipolar transistors and are arranged on a second part (80_2) of the wafer and that the opto-electronic flip-flops

(12₁, 12₂, 12_N) comprise a photodiode that is placed between the two parts (80₁, 80₂) of the wafer.

16. A sampling device according to any of the preceding
5 claims,

characterized in that,

a mode locked laser (88) is used to generate the optical clock signal and that the mode locked laser (8) is connected with an optical fiber to the second input unit
10 (5).

17. A sampling device according to claim 13,

characterized in that,

the opto-electronic flip-flop (10₁, 10₂, 10_M) comprises a
15 differential pair of first transistors (60₁, 60₂) and two load resistors (62₁, 62₂),

that the load resistors (62₁, 62₂) are connected between a supply voltage terminal and collectors of the first transistors (60₁, 60₂), and

20 that emitters of the first transistors (60₁, 60₂) are connected to the photodiode (61) and/or

that the opto-electronic flip-flop (10₁, 10₂, 10_M) comprises a differential pair of second transistors (60₃, 60₄) and a first current source (63),

25 that the first current source (63) is connected between emitters of the second transistors (60₃, 60₄),

that base terminals of the second transistors (60₃, 60₄) are connected crosswise to collectors of the second transistors (60₃, 60₄), and

30 that the collectors of the second transistors (60₃, 60₄) are each connected to a collector of the first transistors (60₁, 60₂) and/or

that the opto-electronic flip-flop (10₁, 10₂, 10_M) comprises a differential pair of third transistors (65₁,

65₂), two load resistors (67₁, 67₂) and a second current source (66),
that the load resistors (67₁, 67₂) are connected between a supply voltage terminal and collectors of the third
5 transistors (65₁, 65₂),
that emitters of the third transistors (65₁, 65₂) are connected to the second current source (66), and
that base terminals of the third transistors (65₁, 65₂) are connected to at least one output (Q, $\overline{Q}$) of the opto-
10 electronic flip-flop (10₁, 10₂, 10_M).

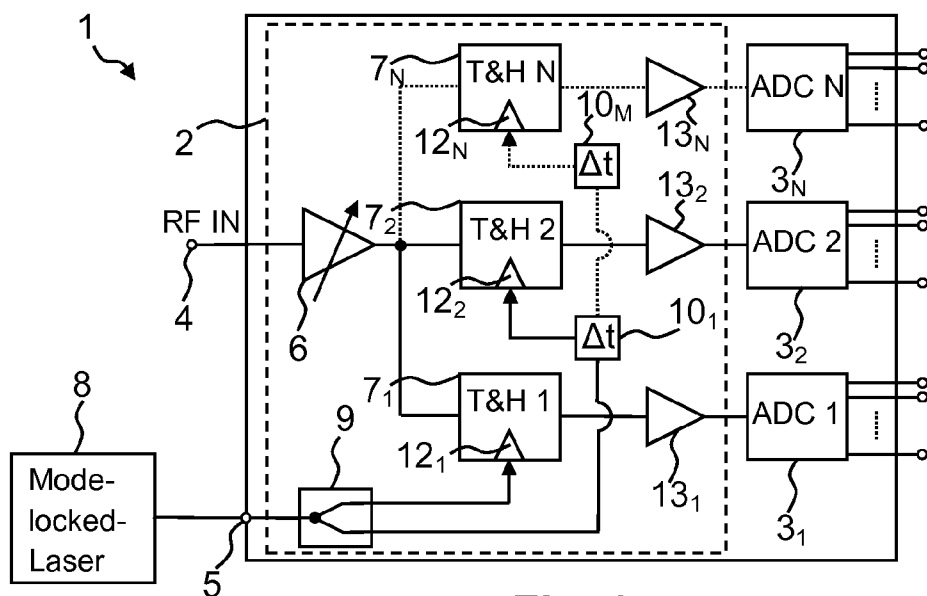


Fig. 1

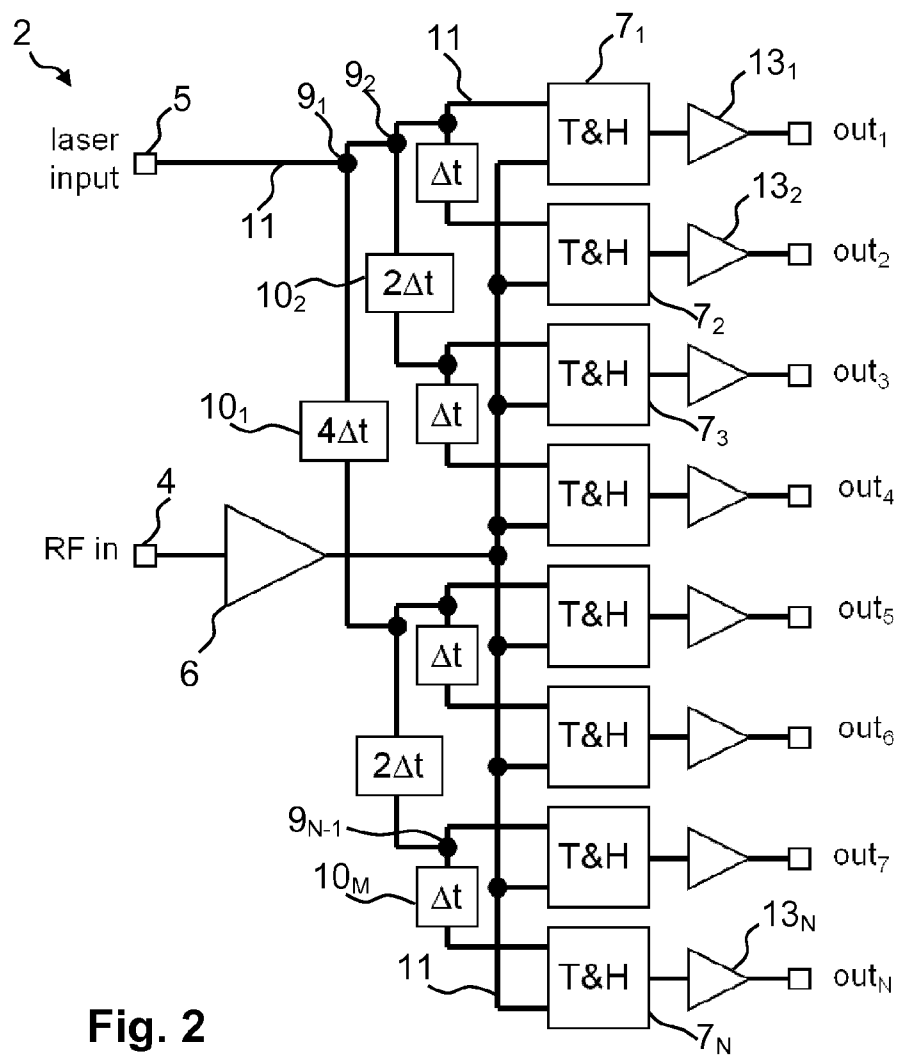


Fig. 2

2

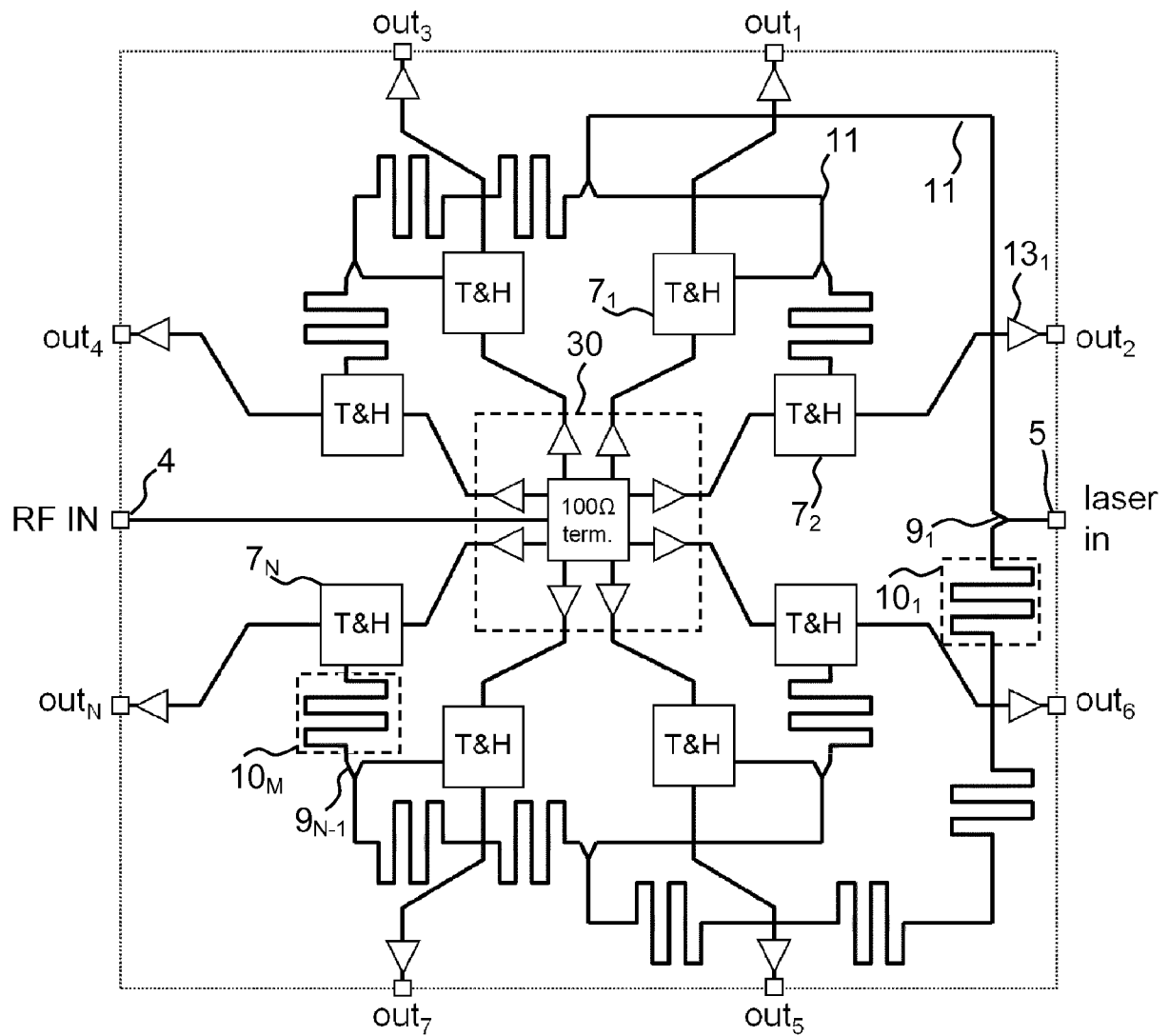
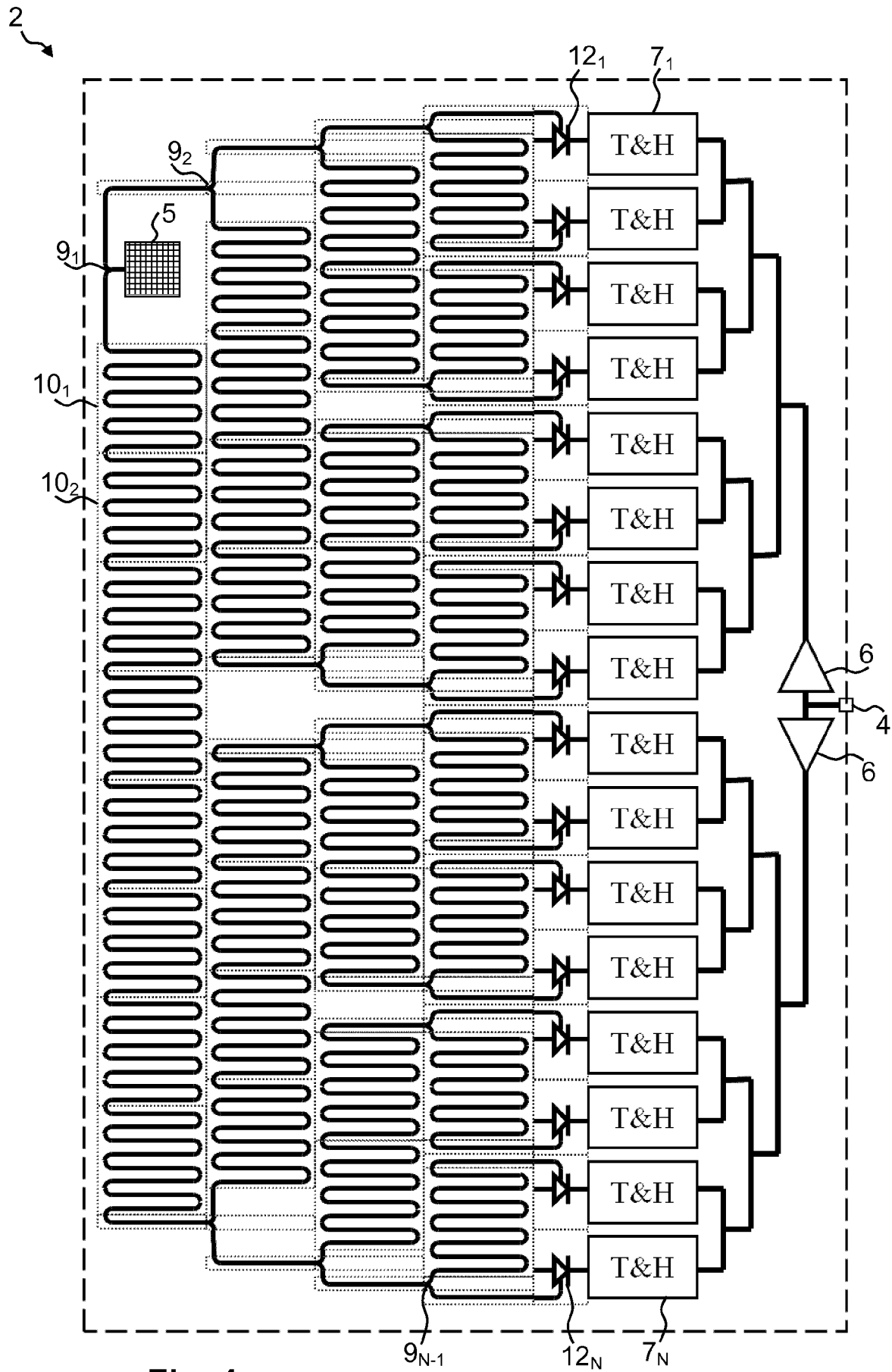


Fig. 3



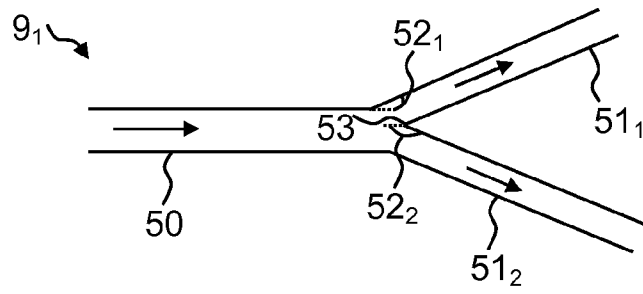


Fig. 5A

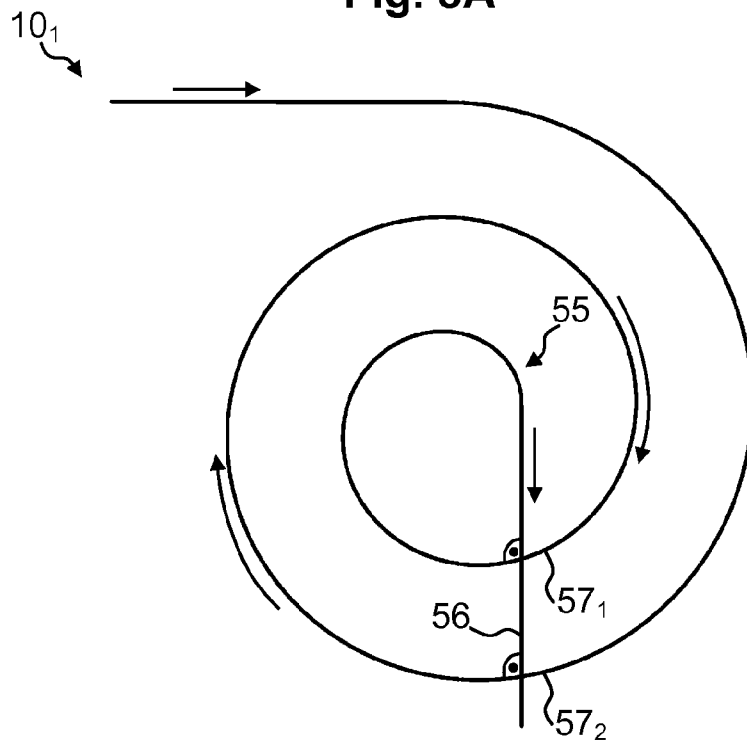


Fig. 5B

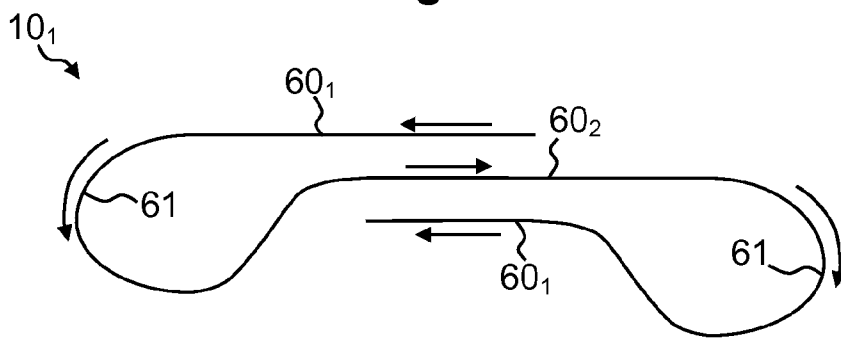


Fig. 5C

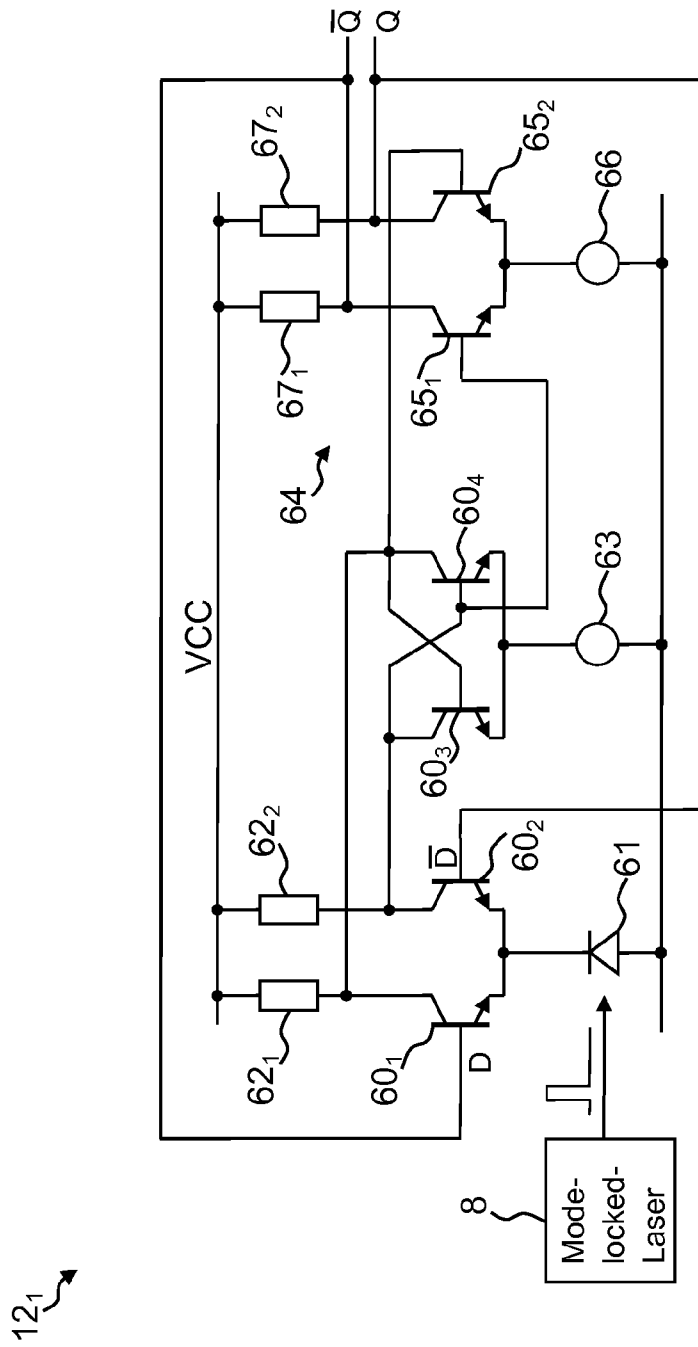
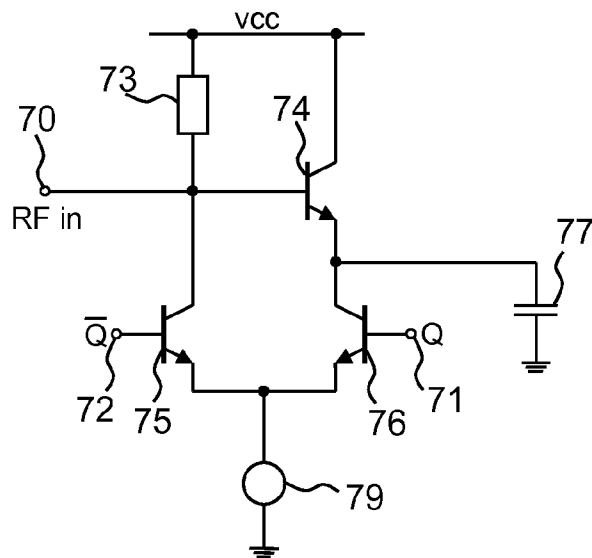
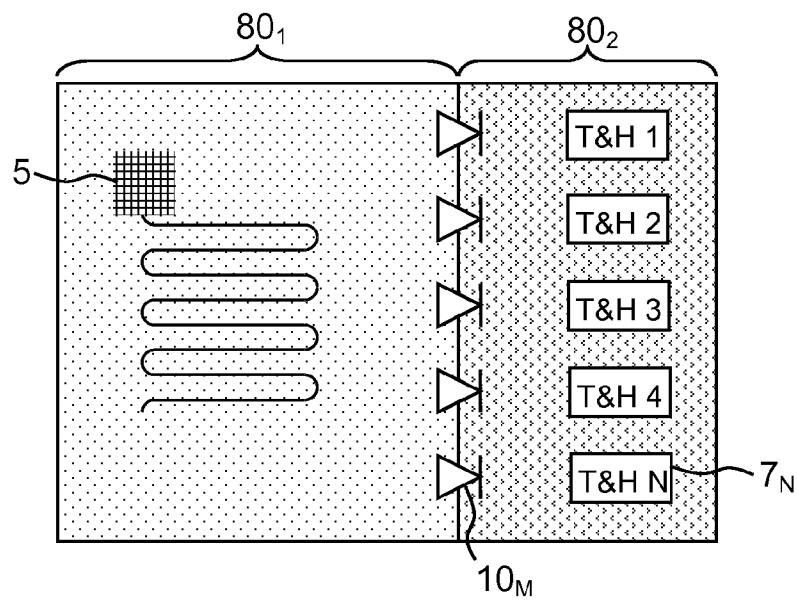


Fig. 6

7₁**Fig. 7****Fig. 8**

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2013/058362

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C27/02 H03M1/12 H03K3/42 G02F7/00 G02B6/125
ADD. G11C13/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C H03M H03K G02F H04B G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/277354 A1 (LEE JAESIK [US] ET AL) 4 November 2010 (2010-11-04)	1-5, 8-12, 14-16
Y	paragraph [0014] - paragraph [0015]; claims 1-3; figure 2	6,7,13, 14,17
Y	DE 10 2010 025782 A1 (ROHDE & SCHWARZ [DE]) 5 January 2012 (2012-01-05) paragraph [0024]; figure 4	13,14,17
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Further documents are listed in the continuation of Box C.



See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

4 June 2013

Date of mailing of the international search report

12/06/2013

Name and mailing address of the ISA/

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Authorized officer

Colling, Pierre

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2013/058362

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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