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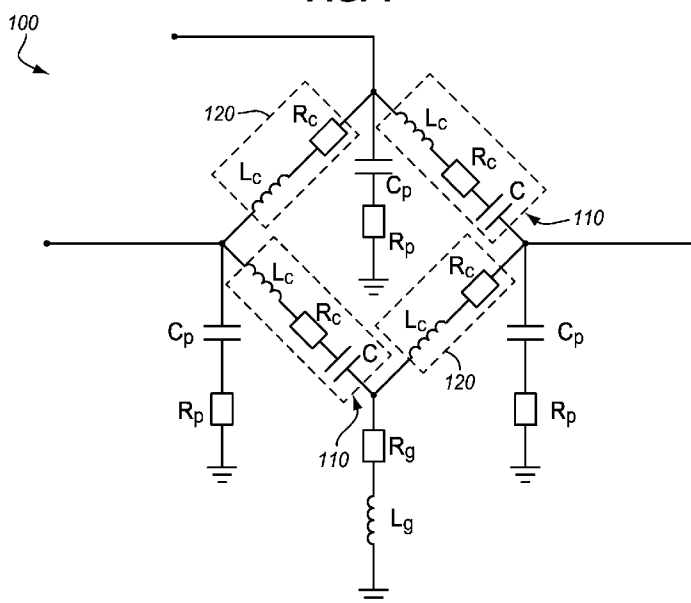
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FIG. 1



(57) Abstract: An integrated circuit (IC) comprises one or more intra-metal finger to finger capacitors having a closed loop and one or more inter-metal plate to plate capacitors integrated with the one or more intra-metal finger to finger capacitors.



HIGH QUALITY FACTOR CAPACITOR

FIELD

The present disclosure generally relates to millimeter wave field-effect applications.

BACKGROUND

Millimeter-wave circuits having antenna beamforming arrays may be designed for a range of applications in the microwave electromagnetic spectrum. Millimeter-wave microstrip patch antennas or endfire antennas are designed to operate in the electromagnetic spectrum ranging from 30 GHz to 300 GHz, corresponding to wavelengths ranging from 10 mm to 1 mm. Applications for these circuits include personal area networking (PAN), broadband wireless networking and communication, wireless portable devices, wireless computers, servers, workstations, laptops, ultra-laptops, handheld computers, telephones, cellular telephones, pagers, walkie-talkies, routers, switches, bridges, hubs, gateways, wireless access points (WAP), personal digital assistants (PDA), televisions, motion picture experts group audio layer 3 devices (MP3 player), global positioning system (GPS) devices, electronic wallets, optical character recognition (OCR) scanners, medical devices (e.g., cancer diagnostics), cameras, security screening (e.g., people screening at airports and security areas like hotels, conference rooms, sport stadiums, etc.), radar for range and velocity detection in cars (e.g., self autonomous driving cars) or for gesture sensing radar-sensors (e.g., replacing the keyboard device for tactile internet experience) and so forth.

Circuits operating in the mm-Wave frequency range implement power efficient broadband architecture capacitors with a high quality factor (Q) and high resonance frequency. The resonance frequency should be at least around twice as large as the sum of carrier center frequency and half of the bandwidth of the information containing signal. A high Q capacitor is difficult to achieve at increasing frequencies because the quality factor decreases with increasing frequency. Conventional capacitors using high resistive lower level thin metals of the digital metal stack in a complementary metal–oxide–semiconductor (CMOS) fail to provide a high Q at mm-Wave frequencies.

Capacitors formed in the thicker metal levels of the power routing provide lower resistance at lower capacitance, which leads to higher Qs. However, these capacitors fail to achieve high resonance frequency required for operation at mm-Wave frequencies due to the associated high parasitic inductances. Accordingly, mostly narrowband transformer based architectures are used today for mm-Wave circuits in advanced CMOS because of the lack of appropriate capacitors.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a schematic of one embodiment of a broadband circuit at which a high Q capacitor is implemented.

Figures 2A – 2C illustrate embodiments of a closed loop finger capacitor.

Figures 3A & 3B illustrate embodiments of a cross section schematic of a high Q capacitor configuration.

Figures 4A – 4C illustrate different views of one embodiment of a high Q capacitor configuration.

Figures 5A – 5D illustrate embodiments of layers of a high Q capacitor.

Figures 6A – 6E illustrate additional embodiments of layers of a high Q capacitor.

Figures 7A & 7B illustrate still additional embodiments of layers of a high Q capacitor.

Figures 8A – 8F illustrate embodiments of sidewall transformers and transformer loops within layers of a high Q capacitor.

Figures 9A – 9C illustrate embodiments of current loops within layers of a high Q capacitor.

Figure 10 illustrates a system in which a high Q capacitor may be implemented.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth in order to provide a thorough understanding of various embodiments. However, various embodiments of the invention may be practiced without the specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to obscure the particular embodiments of the invention.

Figure 1 illustrates a schematic of one embodiment of a broadband circuit 100. In one embodiment, broadband refers to a signal having a frequency bandwidth of larger than 700 MHz, or >1 GHz, >2, >3, >4, >5, >6, >7, >8, >9, >10, >11, >12, >13, >14, >15, >20, >40, >60 GHz. In one embodiment, circuit 100 is a lattice balun that implements distributed capacitor elements 110 and inductive elements 120 (e.g. coils, transformers, transmission lines (TML), slow-wave TML). In one embodiment, the balun provides a high impedance transformation ratio that enables high radio frequency (RF) output power at an antenna with low supply voltage of advanced CMOS.

In one embodiment, inductive elements 120 (e.g., in L_c and R_c) represent a coil. In some embodiments, the inductive element may be a transmission line, where R_c and L_c are lumped modeling elements of an (possibly distributed) inductive element. In a further embodiment, capacitor element 120 (e.g., in L_c and R_c) represents a capacitor. Similarly,

Rc, Lc and C may be lumped elements for modeling a distributed high Q capacitor. Further p stands for parasitic capacitance to ground (g). Accordingly, Cp and Rp are modeled elements for a lossy capacitance.

According to one embodiment, capacitors 110 are high Q capacitor capacitors. In such an embodiment, capacitors 110 comprise closed loop finger capacitances. In a further embodiment, the closed loop fingers provide sidewall transformers for inductance cancellation. As described herein, inductance cancellation does not necessarily equate to complete inductance elimination, but may also be defined as inductance reduction.

Figure 2A illustrates one embodiment of such a closed loop finger capacitance 200. As shown in **Figure 2A**, capacitor 200 includes finger capacitors 210 and transformers 220. As discussed above, transformers 220 are built into capacitors 210 in order to cancel inductance. Accordingly, the capacitor 200 configuration provides for higher resonance frequency. In some embodiments, inductance cancelation can be applied in instances in which only one component/electrode of capacitor 200 includes the closed loops.

In one embodiment, capacitor 200 combines intra-metal finger to finger (or lateral finger) capacitors having high aspect ratio metals and vertical parallel plate capacitors using thinner dielectrics and metals. In a further embodiment, the lateral finger capacitor electrodes having closed loop fingers that form sidewall transformers and cancel the inductance via mutual inductance. Accordingly, capacitor 200 avoids, at least partially, the low-k dielectrics (e.g., dielectric with dielectric constant < 3.9 of pure silicon oxide) or air-gaps used in lower metal levels of advanced CMOS.

According to one embodiment, a ground shield or closed loop transformer winding(s) may be placed at the bottom below a finger to finger capacitor, or placed above the finger to finger capacitor, or by flipping the ground shield or closed loop transformer winding by approximately 90° placed/arranged at/around the two sides of a conductive line or finger to finger capacitor and forming the sidewall ground shields or sidewall closed loop transformer winding(s). Embodiments of the sidewall closed loop transformer windings can be included/incorporated into the finger to finger capacitor (**See Figure 2B**). Other embodiments of sidewall closed loop transformer windings may be separated from the finger to finger capacitors and be un-connected (or floating), as one shown in **Figure 2C**. Such a configuration may be regarded as an inductance canceling fill structure. Fill structures are implemented in modern scaled semiconductor technologies to provide a means for planarization.

Figure 3A illustrates one embodiment of a cross section of a closed loop finger capacitor 200. As shown in **Figure 3A**, capacitor 200 includes a lateral finger capacitor

configuration separated by a spacing (s), and inter-metal plate-to plate (or vertical plate) capacitors separated by a spacing (d). Integrating lateral finger capacitors together with vertical plate capacitors together allows for increase of the capacitance per area, which makes the layout more compact; but may also allow for tailoring the capacitance accuracy

of the total capacitance since the manufacturing process variability may be different for lateral finger capacitors compared to vertical plate capacitors. A sufficient capacitance tolerance $\sigma C/C$ (e.g., σC being the one sigma distribution value of the manufacturing statistical capacitance variation and C the capacitance value) may be less than 20%, equal or less than 15%, equal or less than 10%, equal or less than 7.5%, or equal or less than 5%.

In one embodiment, the metal to metal spacing s of the finger capacitors are selected at minimum. Alternatively, spacing s may be selected according to metal density rules. In a further embodiment, the finger capacitors use metals with large aspect ratio h/s embedded in a high-k dielectric (e.g., dielectric constant > 3.9 (3.9 is dielectric constant of Silicon oxide SiO_2)).

In one embodiment, the aspect ratio h/s of parallel finger capacitors that are not forming parallel plate capacitors is 2 or larger (e.g., > 2.5, >3, >3.5, >4, >4.5, or > 5). Further, the aspect ratio h/s may be defined for metals having a height of larger than 0.2 μm (e.g., > 0.25 μm , >0.3 μm , >0.4 μm , >0.5 μm). In a further embodiment, the spacing d in subsequent layers is 200nm or smaller (e.g., 150 nm or smaller, 100nm, or smaller, 75 nm or smaller, 50 nm or smaller). In one embodiment the spacing d may be larger than 10nm, > 20nm, > 30nm, > 40nm, >50nm.

Additionally, the vertical parallel plate capacitors have a defined width of metal level to inter-metal distance (width/d) ratio. For instance, the width/d ratio is represented as a width of a metal level (x) with spacing d to a next metal level (x-1) nearer to the substrate. In such an embodiment, the metal level x and x-1 forming the vertical parallel plate capacitor is 2 or larger (e.g., >3, >4, > 5, >6, >8, >10, >12, >14, >16, >18, >20, >22, >24, >26, >27, >28, > 29, >30). In one embodiment, the ratio width/d is 100 or smaller (e.g., <80, <60, <50 or <40).

The width of lower level metals forming the parallel plate capacitors is limited by the pitch of the parallel finger capacitors above. The pitch of metal fingers is the sum of finger (metal) width and finger to finger spacing. The finger to finger spacing of upper metal level finger to finger capacitor (e.g., in M7 in **Figures 3**) may be 1 μm or less. The width of the finger of upper level finger to finger capacitors may be selected according the skin-depth (skin-effect) at the required frequency. At 30 GHz the skin-depth in copper or aluminum is 0.5 μm or less. In one embodiment, the width of the finger may be 3 to 4

times the skin-depth (e.g., the width of upper metal level fingers may be selected 2 μm or less, 1.9 μm or less, 1.8 μm or less, 1.7 μm or less, 1.6 μm or less, 1.5 μm or less at 30 GHz and may be less for higher frequencies). In a further embodiment, the maximum width of the metal fingers forming lower level parallel plate capacitors may be selected smaller than the pitch of the upper metal levels (e.g., width of lower level metal may be selected equal to or smaller than 3 μm which is the sum of 2 μm for the finger width of upper metal levels plus 1 μm for the finger to finger spacing of upper metal level finger to finger capacitors).

In one embodiment, capacitor 200 includes a top metal layer (M8) capacitor, second metal layer (M7) capacitors and third metal layer (M6) capacitors coupled to metal layer M7 using vias 320, where + and – in layers M8 and M7 denote electrode electrical polarity. In one embodiment, the + electrode in layer M7 is a finger electrode coupled to layer M8 by a via 410 (represented by * in **Figures 3** and visible in **Figures 4B&C**), while the - electrode in layer M7 is an island electrode (as shown below in **Figure 4C**). Metal layers M6 and M5 are coupled using vias 330. However in some embodiments metal layers M6 and M5 may be coupled without the use of vias 330. In such an embodiment, a grounded shield may be implemented to couple layers M1-M5, or layers M1-M4, or layers M1-M3, or layers M1-M2, or layer M1 only.

Capacitor 200 includes fourth and fifth metal layers, (M5) and (M4), respectively. According to one embodiment, layer M8 is a non-floating capacitor coupled conductively to a nearby M7 finger and forming a vertical capacitance with an underlying M7 island, while metal layer M4 is a floating ground shield. In such an embodiment, layer M4 increases capacitance and shields a maybe lossy (e.g., silicon) substrate (not shown) from the other capacitor 200 plates. Further, layer M4 carries eddy currents that reduce inductance and forms a closed loop bottom plate transformer winding for the finger capacitors above. Moreover, the floating layer M4 configuration increases break down voltage. **Figure 3B** illustrates an alternative embodiment in which metal layers M5 and M4 are coupled using vias 340. In such an embodiment, layer M4 is an electrode.

In one embodiment, metal layer M1 is positioned below layer M4. In such an embodiment, layer M1 is a grounded shield that may include layers M1-M3, or layers M1-M2 connected by vias forming a bottom plate closed loop transformer winding for the finger capacitors above. The forming of a grounded M1 ground shield (or omission) depends on the application. In case one electrode of the capacitor is connected to ground (referring to the – sign in **Figures 3A & B**), such a M1 or M1-M2 or M1-M3 grounded ground shield provides additional capacitance and maybe wishful. In case of a signal that is not coupled to ground, the signal may be transmitted from one electrode of the capacitor

to the other electrode. In such an instance the grounded ground shield maybe omitted to reduce parasitic capacitance, which lowers the amplitude of the signal at the electrode exiting the capacitor or maybe formed only in M1 to provide a inductance cancellation to the lateral finger capacitors but minimize the parasitic capacitance.

5 In one embodiment, a low-k dielectric (dielectric constant < 3.9) (not shown) is positioned below the bottom plate layer M4. However in other embodiments, air-gaps (e.g., air holes within the (inter metal) dielectric to reduce the dielectric constant of the dielectric) are formed below the layer M4, and metal filling with area filling density of less than 25%, or less than 15% is used to lower parasitic capacitances. In such embodiments,
 10 metal fill shapes in subsequent metal levels between the floating M4 shield and the grounded shield or a maybe lossy substrate are not overlapping to reduce parasitic capacitance; and there is no via fill. In a further embodiment, a floating or via high impedance ($> 1\text{k}\Omega$) connected Nwell in a p-type semiconductor substrate, or floating or via high impedance ($> 1\text{k}\Omega$) connected Pwell in floating or high impedance ($> 1\text{k}\Omega$)
 15 connected N-well in p-type semiconductor substrate (triple-well: p-well in n-well in p-substrate) maybe placed below the floating shield layer M4 to reduce parasitic capacitance.

In one embodiment the semiconductor substrate below the capacitor may have an area density of shallow trench isolation (STI) of 60% or more (e.g., 70% or more, or 79% or more, or 80% or more), and the area density of gates is less than 40% (e.g., $< 30\%$, or $< 20\%$ or $< 15\%$, or $< 11\%$). The gates may be preferably placed over the STI regions only. The STI is a hole etched into the silicon substrate and filled with a dielectric with a dielectric constant, typically for silicon around 3.9 and smaller than the dielectric constant of the semiconductor (e.g. for silicon 11.9) to isolate different devices (e.g. field effect transistors (FETs), varactors, diodes, etc.) from each other. Within this document the term
 25 gate denotes the gate conductor material used for field effect transistors (FET), which could be poly silicon, doped poly silicon, silicided poly silicon, silicide or a metal like (e.g. TiN used in high-k metal gate FETs in advanced CMOS technologies).

Figures 4A – 4C illustrate different views of one embodiment of a high Q capacitor 200. As shown in **Figure 4A**, an electrical connection path flows from the - electrode of metal layer M8 down to layer M6 through the finger electrodes of layer M7. Subsequently,
 30 the path returns to layer M7 at the island electrodes before completion at the + electrode of layer M8. **Figure 4B** illustrates one embodiment of a side view of capacitor 200 showing vias 410, 320 and 330, coupling metal layers M8 to M7, M7 to M6 and M6 to M5, respectively. **Figure 4C** illustrates capacitor 200 without metal layer M8. As shown in
 35 **Figure 4C**, layer M7 includes finger electrodes and island electrodes.

Figures 5A – 5D illustrate embodiments of layers of capacitor 200. **Figure 5A** illustrates one embodiment of a layout of top metal layer M8. As shown in **Figure 5A**, layer M8 includes slotted fingers to mitigate resistance increase due to skin-effect. In addition, layer M8 includes vias 410 to couple with layer M7. Further, tapers 504 are provided to allow optimum connection to transmission lines (TML). In one embodiment, the TML is a slow-wave TML formed in M8. According to one embodiment, layer M8 includes closed loops for transformer based inductance cancellation (or “top plate transformer”).

A bottom plate transformer occurs when a conductive line performs a transformer action with a grounded ground shield or floating ground shield allowing closed loop currents within the shield to cancel the inductance of the conductive line running above the shield. In such an embodiment, the current running through the conductive line induces eddy currents in the floating or grounded ground shield, which creates magnetic fields that cancel the magnetic fields of the conductive line above the shield and so cancel the inductance of the conductive line above. Accordingly, inductance of the lines above the floating ground shield is reduced. **Figure 5A** represents a quasi-top ground shield (e.g., the lines below the slotted M8 structure perform a transformer action with the M8 structure; further the slotted M8 top plate performs as a shorted second transformer winding towards the lines below and so reduces the inductance of the lines below).

Figure 5B illustrates one embodiment of a layout of a second metal layer M7. As shown in **Figure 5B**, layer M7 forms lateral finger capacitors 505 and island capacitors 506. In one embodiment, layer M7 may also include a taper that provides a M7 taper to M8 taper vertical plate to plate capacitor, a M7 transmission line above a grounded or floating ground shield, and provides a means for closing a loop to provide a sidewall closed loop transformer winding (see **Figures 8A-D** below for more detail). However in such an embodiment, the M7 taper is smaller than the M8 taper 504 (e.g., enclosed by M8 taper 504). **Figure 5C** illustrates one embodiment of a layout of the top metal layer M8 imposed over second metal layer M7, best visualized by overlaying **Figure 5A** with **Figure 5B**. As discussed above, layer M8 serves as a non floating metal electrode to increase the vertical capacitance between M7 and M8. **Figure 5D** illustrates another embodiment of a layout of the top metal layer M8 imposed over second metal layer M7.

In **Figure 5D**, the arrows define a different connection direction in the case of the capacitor being used in a differential application (e.g., when connecting to a differential transformer or differential coil). In such an embodiment, the taper would be minimized (e.g., leaving only sufficient metal for closing the loops) or even omitted. The width1,

height1 and width2, height2 of both tapers in M7 only, or each of M7 and M8 tapers, for the + and – electrodes may be used to make the capacitances of both electrodes towards the ground equal for a balanced/differential mode excitation (e.g., voltages at + and – electrodes in **Figure 5D** are 180° out of phase to each other).

Figures 6A – 6D illustrate embodiments of metal layers M6 and M5 of capacitor 200. **Figure 6A** illustrates one embodiment of metal layer M6, while **Figure 6B** illustrates an embodiment of metal layer M6 with vias 320. **Figure 6C** illustrates one embodiment of metal layer M5, while **Figure 6D** illustrates metal layer M5 with vias 330. **Figure 6E** illustrates one embodiment of metal layers M6 and M5 with vias 330.

Figure 7A illustrates an embodiment of a metal layer M4 of capacitor 200. As discussed above, metal layer M4 is a floating shield. According to one embodiment, the floating shield comprises a meshed bottom floating shield to cancel inductance through the transformer action with the above lines of the finger capacitor, and provides a vertical capacitor to increase the capacitance and shield the substrate.

In one embodiment, the floating shield provides a low ohmic path (e.g., compared to a semiconductor substrate), and, increases the capacitance and shields the capacitance from the substrate. The eddy currents induced from lines above the shield generate a magnetic field that cancels the magnetic fields from the lines above (which leads to inductance cancellation), which in turn increases the resonance frequency of the capacitance. In a further embodiment, the floating shield may be formed from one metal level only. However other embodiments may feature a shield having several metal levels connected in parallel. In yet a further embodiment, wider layer M5 lines are placed parallel to metal shapes in layer M4 to increase the parallel plate capacitance between the M5 line and the metal shape in M4.

In yet another embodiment more narrow M5 lines (than the M6 lines) are placed over the M4 shield (or M4 electrode according to **Figure 3B**) to tailor the contribution of the M5 to M4 parallel plate capacitor to the total capacitance of the broadband high-Q capacitor. Such adjustment of contribution may be useful to adjust the value of the total capacitance, and to also adjust a statistical variation of the capacitance value due to process variations, as the statistical process variations may be different for vertical plate and lateral finger capacitors. **Figure 7B** illustrates a detailed zoom of the embodiment of metal layer M4 shown in **Figure 7A**. As shown in **Figure 7B**, the width (W) should align with the widths of M5 or M6. Thus, W is as wide as the wider of the M6 or M5 finger width. The M5 or M6 finger is centered above the M4 finger shape inside the meshed floating ground shield.

Figure 8A illustrates one embodiment of transformer loops formed within layers of a high Q capacitor. As shown in a layout of metal layers M7 and M6 in **Figure 8A**, vias 320 form sidewall transformer loops 810 and 820. In one embodiment, loop 810 is a closed loop path forming a first transformer winding, while loop 820 is a closed loop path forming a second transformer winding. In one embodiment, transformer loops 810 and 820 running interleaved side by side provide the inductance canceling feature of a ground shield (e.g. for a line running above or below such a ground shield on bottom or top) to each other that has much lower resistance as the layer M4 ground shield (e.g., see above-descriptions with reference to **Figures 3B** and **Figures 7A&B**). As used herein, the term sidewall ground shield or sidewall closed loop transformer winding is used for describing this inductance cancelation feature. Thus, eddy currents will flow in transformer loops 810 and 820 rather than M4, which maybe improves the quality factor of the capacitor.

Figure 8B illustrates one embodiment of localized via 320 placement to provide transformer loops 810 and 820. In this embodiment, via 320 placement is localized at the ends of M7 fingers and M7 islands. According to one embodiment, placement of vias only in certain regions, instead of continuously distributed via placement, enables generation of well defined current paths in different layers. Such current path shaping reduces inductance. **Figures 8C & 8D** illustrate other embodiment of via 320 placement.

Figures 8E & 8F illustrate one embodiment of transformer loops within layers of a high Q capacitor. As shown in a layout of metal layers M7 and M6 in **Figure 8A**, vias 320 form sidewall transformer loops 810 and 820. **Figure 8E** illustrates one embodiment of capacitor electrodes connected in M7 forming vertical transformers in metal levels 8 and metal level 6 in the opposite electrodes of the capacitor. **Figure 8F** illustrates yet another embodiment in which capacitors with capacitor electrodes connected in M7 form vertical transformers in M8 and M6 in the opposite electrodes of the capacitor, and form additional vertical capacitors with finger structures in M6 and M8 in the opposite capacitor electrodes.

Figures 9A – 9C illustrate one embodiment of current loops within layers of a high Q capacitor. **Figure 9A** shows current loops formed in metal layers M8, M7 and M6 using a localized via placement according **Figure 8B**. As shown in **Figure 9A**, current flows in from one (+) electrode via layer M8 to M7 (finger), and subsequently to layer M6. From layer M6, the current travels to M7 (island) before exiting at the other (-) electrode via layers M7 (finger) and M8 of the (-) electrode.

According to one embodiment, additional metal levels may be included to achieve a larger amount of current running in opposite directions. **Figure 9B** shows an embodiment

where more metal layers are arranged to provide more canceling currents with opposite directions. Layers can be connected in parallel to lower the resistance. Additionally, there may be metal layers near the semiconductor substrate that are not used to reduce parasitic capacitance (e.g., the most bottom layer may include layers M1 to M3 connected in parallel, or layers M2 plus layer M3 connected in parallel). The induction cancellation performance increases as the distance between currents running in opposite directions gets smaller, e.g., opposite running currents in different metal layers cancel each other (inductance) the better the more closely spaced, laterally or vertically, they are.

Figure 9C shows cancelling current flows having associated magnetic fields that occur in metal layers M8, M7 and M6. Arrows 910, 920, 930 and 940 represent currents in layers M8, in M7 beside M8, in M6 below M8 and M6 below M7, respectively. As shown in **Figure 9C**, currents 940 and 920 cancel one another due to inductance cancelation through opposite running currents flowing in M7 and M6. Currents 910 flowing in M8 and currents 920 flowing in M7 cancel each other, while currents 930 and 940 add to one another.

Figure 10 illustrates one embodiment of a block diagram of a system 1000 in which broadband circuit 100 may be implemented. System 1000 may comprise, for example, a communication system having multiple nodes. A node may comprise any physical or logical entity having a unique address in system 1000. Examples of a node may include, but are not necessarily limited to, a computer, server, workstation, laptop, ultra-laptop, handheld computer, telephone, cellular telephone, personal digital assistant (PDA), router, switch, bridge, hub, gateway, wireless access point (WAP), and so forth. The unique address may comprise, for example, a network address such as an Internet Protocol (IP) address, a device address such as a Media Access Control (MAC) address, and so forth. The embodiments are not limited in this context.

The nodes of system 1000 may be arranged to communicate different types of information, such as media information and control information. Media information may refer to any data representing content meant for a user, such as voice information, video information, audio information, text information, alphanumeric symbols, graphics, images, and so forth. Control information may refer to any data representing commands, instructions or control words meant for an automated system. For example, control information may be used to route media information through a system, or instruct a node to process the media information in a predetermined manner.

The nodes of system 1000 may communicate media and control information in accordance with one or more protocols. A protocol may comprise a set of predefined rules or instructions to

control how the nodes communicate information between each other. The protocol may be defined by one or more protocol standards as promulgated by a standards organization, such as the Internet Engineering Task Force (IETF), International Telecommunications Union (ITU), the Institute of Electrical and Electronics Engineers (IEEE), the 3rd Generation Partnership Project (3GPP), 5th generation mobile networks (5G), and so forth.

The high-Q capacitance, circuits, systems, and methods described herein are beneficial in devices, circuits and systems compliant with millimeter wave based wireless communication and connectivity standards such as: 5th generation wireless systems (5G); 802.11ad, WiGig; next-generation 60 GHz connectivity; IEEE 802.11ay (WiGig 2); millimeter wave sensors such as millimeter wave based radar and imaging.

System 1000 may be implemented as a wireless communication system and may include one or more wireless nodes arranged to communicate information over one or more types of wireless communication media. An example of a wireless communication media may include portions of a wireless spectrum, such as the radio-frequency (RF) spectrum or frequency spectrum in the millimeter wave range (30-300 GHz). Carrier frequencies used in the system may include frequencies between 24.25 GHz till 27 GHz, or include/contain frequencies at 27.5, 28, 29, 30, 31, 37.5, 38, 39, 40, 41, 50, 66, 71, 76, 81, 86 GHz or frequencies above 86 GHz. The wireless nodes may include components and interfaces suitable for communicating information signals over the designated wireless spectrum, such as one or more antennas, wireless transmitters/receivers ("transceivers"), amplifiers, filters, control logic, and so forth. Examples for the antenna may include an internal antenna, an omni-directional antenna, a monopole antenna, a dipole antenna, an end fed antenna, a circularly polarized antenna, a micro-strip antenna, a micro-strip patch antenna, an endfire antenna, a diversity antenna, a dual antenna, an antenna array for beamforming reasons or electronic beam steering functionality, and so forth.

Referring again to **Figure 10**, system 1000 may comprise node 1002, 1004, and 1006 to form a wireless communication network, such as, a PAN, for example. Although **Figure 10** is shown with a limited number of nodes in a certain topology, it may be appreciated that system 1000 may include more or less nodes in any type of topology as desired for a given implementation. The embodiments are not limited in this context.

In one embodiment, system 1000 may comprise node 1002, 1004, and 1006 each may comprise a transceiver 1008, 1010, and 1012, respectively, and a CMOS integrated circuit device 1050. The CMOS integrated circuit device 1050 may comprise any one of antenna systems to form a wireless communication network through wireless links 1052, 1054, 1056, for example. In some embodiment, the CMOS integrated circuit device 1050 may be replaced by other semiconductor technology as (silicon) CMOS. The CMOS integrated circuit device 1050 maybe

integrated within a system in package (SIP), which comprises any one of antenna systems to form a wireless communication or sensor network through wireless links 1052, 1054, 1056.

The embodiments are not limited to planar bulk silicon CMOS integration but can include usage of semiconductor/silicon on insulator (SOI) technology. The capacitor structure could be used not only in silicon CMOS technology but also be integrated within Bipolar or BiCMOS technologies. Semiconductor materials can include any one of, silicon, germanium, silicon-germanium (SiGe), GaAs, InAs, GaN, InN, AlN, InSb, InP. The embodiments are not limited to the integration within semiconductor technologies but could be realized also in package technologies (e.g. wafer level bonding technologies, etc.)

References to “one embodiment”, “an embodiment”, “example embodiment”, “various embodiments”, etc., indicate that the embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Further, some embodiments may have some, all, or none of the features described for other embodiments.

In the following description and claims, the term “coupled” along with its derivatives, may be used. “Coupled” is used to indicate that two or more elements co-operate or interact with each other, but they may or may not have intervening physical or electrical components between them.

As used in the claims, unless otherwise specified the use of the ordinal adjectives “first”, “second”, “third”, etc., to describe a common element, merely indicate that different instances of like elements are being referred to, and are not intended to imply that the elements so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

The following clauses and/or examples pertain to further embodiments or examples. Specifics in the examples may be used anywhere in one or more embodiments. The various features of the different embodiments or examples may be variously combined with some features included and others excluded to suit a variety of different applications. Examples may include subject matter such as a method, means for performing acts of the method, at least one machine-readable medium including instructions that, when performed by a machine cause the machine to performs acts of the method, or of an apparatus or system for facilitating hybrid communication according to embodiments and examples described herein.

Some embodiments pertain to Example 1 that includes an integrated circuit (IC) comprising one or more intra-metal finger to finger capacitors having a closed loop and one or more inter-metal plate to plate capacitors integrated with the one or more intra-metal finger to finger capacitors

Example 2 includes the subject matter of Example 1, wherein the lateral finger capacitors comprise electrodes that form sidewall transformers to cancel inductance.

Example 3 includes the subject matter of Examples 1 and 2, wherein the one or more intra-metal finger to finger capacitors are comprised within a plurality of metal layers of the IC.

5 Example 4 includes the subject matter of Examples 1-3, wherein the plurality of metal layers comprise a first metal layer, a second metal layer positioned on the first metal layer, a third metal layer positioned on the second metal layer, a fourth metal layer positioned on the third metal layer and maybe a fifth metal layer positioned on the fourth metal layer.

10 Example 5 includes the subject matter of Examples 1-4, wherein the fourth metal layer is electrically coupled to the fifth metal layer by first vias, the third metal layer is electrically coupled to the fourth metal layer by second vias, the second metal layer is electrically coupled to the third metal layer by third vias, and the first metal layer is electrically coupled to the second metal layer by fourth vias.

15 Example 6 includes the subject matter of Examples 1-5, wherein the first metal layer comprises an unconnected shield and the fifth metal layer comprises a connected capacitor.

Example 7 includes the subject matter of Examples 1-6, wherein the unconnected ground shield cancels inductance through a plate transformer.

20 Example 8 includes the subject matter of Examples 1-7, wherein the unconnected ground shield further provides a capacitance to increase the capacitance of the one or more closed loop intra-metal finger to finger capacitors and shield a substrate.

Example 9 includes the subject matter of Examples 1-8, further comprising a dielectric positioned below the unconnected ground shield.

Example 10 includes the subject matter of Examples 1-9, further comprising one or more air gaps formed below the mesh floating ground shield.

25 Example 11 includes the subject matter of Examples 1-10, wherein the fifth metal layer comprises one or more closed loops for transformer based inductance cancellation.

Example 12 includes the subject matter of Examples 1-11, wherein the transformers comprise a first closed loop path forming a first transformer winding and a second closed loop path forming a second transformer winding.

30 Example 13 includes the subject matter of Examples 1-12, wherein the first and second transformer windings operate as an inductance canceling ground shield, wherein a resistance in the upper metal layers forming the sidewall transformer is lower compared to the ground shield formed in a thinner lower metal level.

35 Example 14 includes the subject matter of Examples 1-13, wherein the fifth metal layer comprises slotted fingers to mitigate resistance increase due to skin-effect.

Example 15 includes the subject matter of Examples 1-14, wherein the fourth metal layer comprises a plurality of finger electrodes and a plurality of island electrodes.

Some embodiments pertain to Example 16 that includes an integrated circuit (IC) comprising a broadband circuit, including a plurality of inductive elements and one or more high quality factor closed loop finger capacitors, each capacitor comprising one or more intra-metal finger to finger capacitors having a closed loop and one or more inter-metal plate to plate capacitors integrated with the one or more intra-metal finger to finger capacitors.

Example 17 includes the subject matter of Example 16, wherein the one or more intra-metal finger to finger capacitors comprise electrodes that form sidewall transformers to cancel inductance.

Example 18 includes the subject matter of Examples 16 and 17, wherein the one or more intra-metal finger to finger capacitors are comprised within a plurality of metal layers of the IC.

Example 19 includes the subject matter of Examples 16-18, wherein the plurality of metal layers comprise a first metal layer, a second metal layer positioned on the first metal layer, a third metal layer positioned on the second metal layer, a fourth metal layer positioned on the third metal layer and a fifth metal layer positioned on the fourth metal layer.

Example 20 includes the subject matter of Examples 16-19, wherein the first metal layer comprises an unconnected shield and the fifth metal layer comprises a connected capacitor.

Example 21 includes the subject matter of Examples 16-20, wherein the unconnected ground shield cancels inductance, provides a capacitance to increase the capacitance of the one or more closed loop intra-metal finger to finger capacitors and shield a substrate.

Example 22 includes the subject matter of Examples 16-21, wherein the fifth metal layer comprises one or more closed loops for transformer based inductance cancellation.

Example 23 includes the subject matter of Examples 16-22, wherein the transformers comprise a first closed loop path forming a first transformer winding and a second closed loop path forming a second transformer winding.

Some embodiments pertain to Example 24 that includes a millimeter-wave antenna comprising a plurality of inductive elements and one or more high quality factor closed loop finger capacitors, each capacitor comprising one or more intra-metal finger to finger capacitors having a closed loop and one or more inter-metal plate to plate capacitors integrated with the one or more intra-metal finger to finger capacitors.

Example 25 includes the subject matter of Example 24, wherein the one or more intra-metal finger to finger capacitors are comprised within a plurality of metal layers, wherein the plurality of metal layers comprise a first metal layer, a second metal layer positioned on the first

metal layer, a third metal layer positioned on the second metal layer, a fourth metal layer positioned on the third metal layer and a fifth metal layer positioned on the fourth metal layer.

Although embodiments of the invention have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed subject matter
5 may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.

CLAIMS

What is claimed is:

1. An apparatus comprising:
 - one or more intra-metal finger to finger capacitors having a closed loop; and
 - 5 one or more inter-metal plate to plate capacitors integrated with the one or more intra-metal finger to finger capacitors.
2. The IC of claim 1, wherein the one or more intra-metal finger to finger capacitors comprise one or more electrodes that form sidewall transformers to cancel inductance.
3. The IC of claim 2, wherein the one or more intra-metal finger to finger capacitors are
10 comprised within a plurality of metal layers of the IC.
4. The IC of claim 3, wherein the plurality of metal layers comprise:
 - a first metal layer;
 - a second metal layer positioned on the first metal layer;
 - a third metal layer positioned on the second metal layer;
 - 15 a fourth metal layer positioned on the third metal layer; and
 - a fifth metal layer positioned on the fourth metal layer.
5. The IC of claim 4, wherein the fourth metal layer is electrically coupled to the fifth metal layer by first vias, the third metal layer is electrically coupled to the fourth metal layer by second vias, the second metal layer is electrically coupled to the third metal layer by third vias, and the
20 first metal layer is electrically coupled to the second metal layer by fourth vias.
6. The IC of claim 5, wherein the first metal layer comprises an unconnected shield and the fifth metal layer comprises a connected capacitor.
7. The IC of claim 6, wherein the unconnected shield cancels inductance through a plate transformer.

8. The IC of claim 7, wherein the unconnected shield further provides a capacitance to increase the capacitance of the one or more closed loop intra-metal finger to finger capacitors and shield a substrate.
9. The IC of claim 7, further comprising a dielectric positioned below the unconnected
5 shield.
10. The IC of claim 7, further comprising one or more air gaps formed below the unconnected shield.
11. The IC of claim 3, wherein the fifth metal layer comprises one or more closed loops for transformer based inductance cancellation.
- 10 12. The IC of claim 11, wherein the transformers comprise:
a first closed loop path forming a first transformer winding; and
a second closed loop path forming a second transformer winding.
13. The IC of claim 12, wherein the first and second transformer windings operate as a shield, wherein a resistance in the upper metal layers forming the sidewall transformer is lower
15 compared to the shield positioned on the finger capacitors.
14. The IC of claim 12, wherein the fifth metal layer comprises:
slotted fingers to mitigate resistance increase due to skin-effect.
15. The IC of claim 14, wherein the fourth metal layer comprises:
a plurality of finger electrodes; and
20 a plurality of island electrodes.
16. An integrated circuit (IC) comprising:
a broadband circuit, including:
a plurality of inductive elements; and

one or more high quality factor closed loop finger capacitors, each capacitor comprising:

one or more intra-metal finger to finger capacitors having a closed loop; and

one or more inter-metal plate to plate capacitors integrated with the one or more

5 intra-metal finger to finger capacitors.

17. The IC of claim 16, wherein the one or more intra-metal finger to finger capacitors comprise electrodes that form sidewall transformers to cancel inductance.

18. The IC of claim 17, wherein the one or more intra-metal finger to finger capacitors are comprised within a plurality of metal layers of the IC.

10 19. The IC of claim 18, wherein the plurality of metal layers comprise:

a first metal layer;

a second metal layer positioned on the third metal layer;

a third metal layer positioned on the second metal layer;

a fourth metal layer positioned on the third metal layer; and

15 a fifth metal layer positioned on the fourth metal layer.

20. The IC of claim 19, wherein the first metal layer comprises an unconnected shield and the fifth metal layer comprises a connected capacitor.

21. The IC of claim 20, wherein the unconnected shield cancels inductance, provides a capacitance to increase the capacitance of the one or more closed loop intra-metal finger to
20 finger capacitors and shield a substrate.

22. The IC of claim 20, wherein the fifth metal layer comprises one or more closed loops for transformer based inductance cancellation.

23. The IC of claim 22, wherein the transformers comprise:

a first closed loop path forming a first transformer winding; and
a second closed loop path forming a second transformer winding.

24. A millimeter-wave antenna comprising, including:

a plurality of inductive elements; and

5 one or more high quality factor closed loop finger capacitors, each capacitor comprising:

one or more intra-metal finger to finger capacitors having a closed loop; and

one or more inter-metal plate to plate capacitors integrated with the one or more
intra-metal finger to finger capacitors.

25. The antenna of claim 24, wherein the one or more intra-metal finger to finger capacitors

10 are comprised within a plurality of metal layers, wherein the plurality of metal layers comprise:

a first metal layer;

a second metal layer positioned on the first metal layer;

a third metal layer positioned on the second metal layer;

a fourth metal layer positioned on the third metal layer; and

15 a fifth metal layer positioned on the fourth metal layer.

FIG. 1

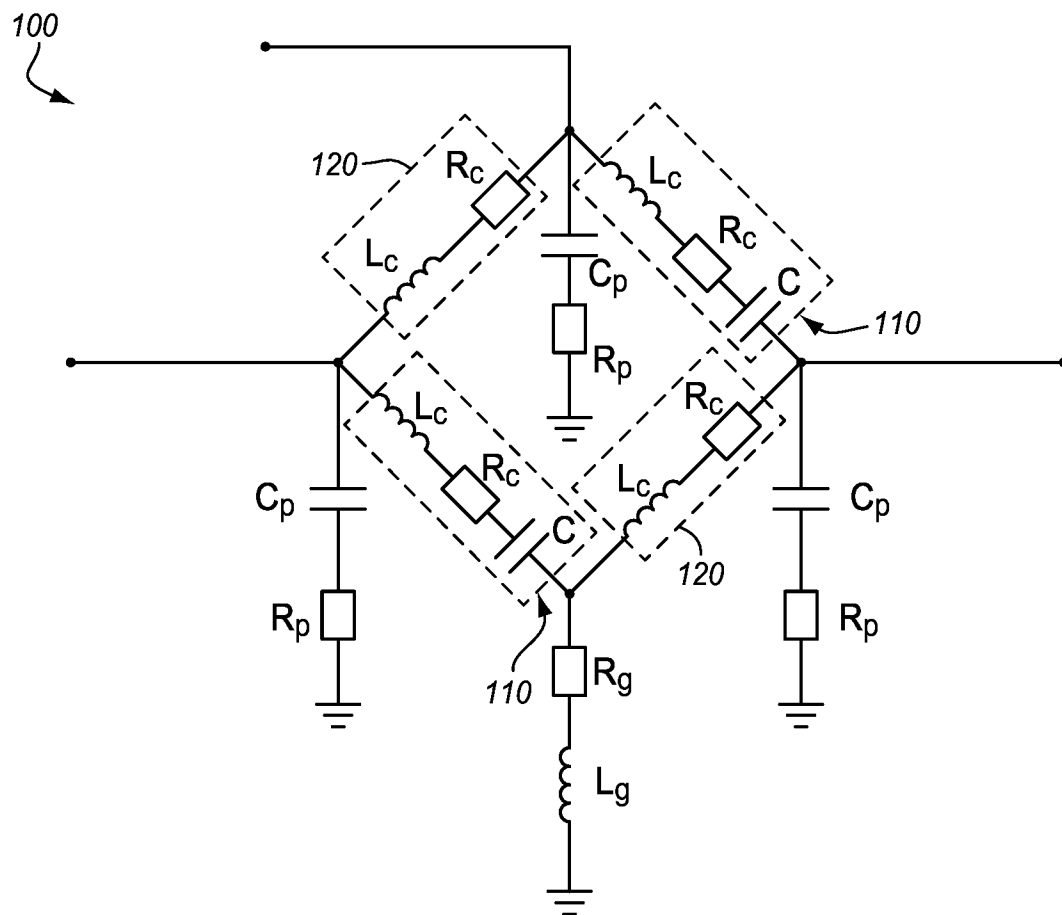


FIG. 2A

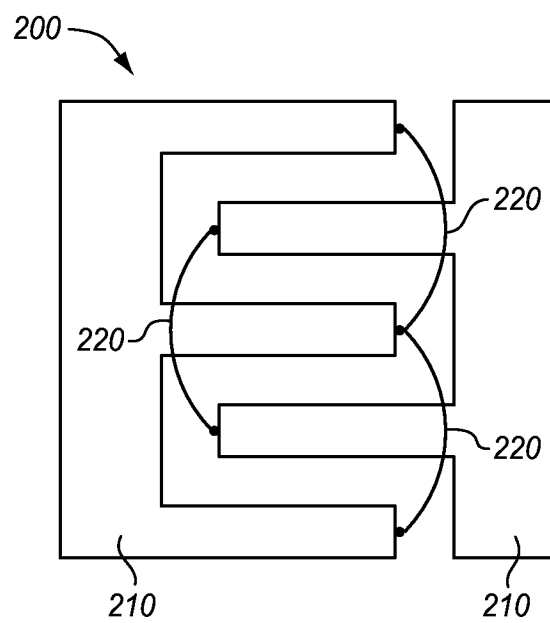
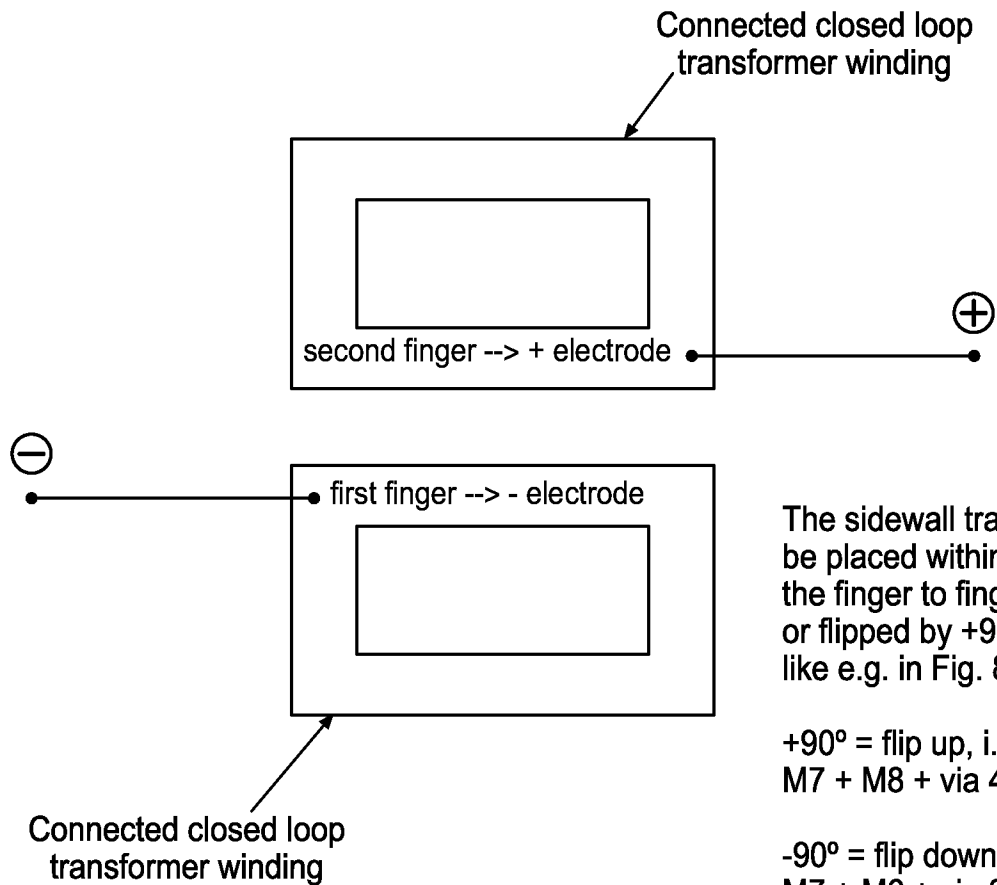


**FIG. 2B**

All structures e.g. in metal M7



The sidewall transformers can be placed within the plane where the finger to finger capacitors lie or flipped by $+90^\circ$ or -90° like e.g. in Fig. 8E or 8F

$+90^\circ$ = flip up, i.e. loop using M7 + M8 + via 410

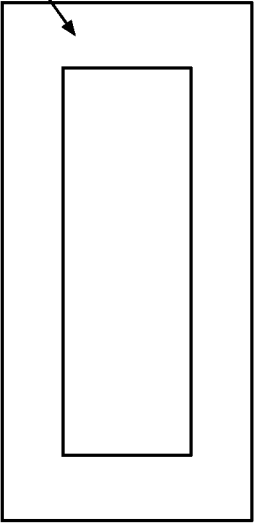
-90° = flip down, i.e. loop using M7 + M6 + via 320



FIG. 2C

All structures e.g. in metal M7

Floating closed loop transformer winding
= inductance canceling fill structure



⊖

first finger --> - electrode

⊕

second finger --> + electrode

The sidewall transformers can be placed within the plane where the finger to finger capacitors lie or flipped by +90° or -90° like e.g. in Fig. 8E or 8F

+90° = flip up, i.e. loop using M7 + M8 + via 410

-90° = flip down, i.e. loop using M7 + M6 + via 320

Floating closed loop transformer winding
= inductance canceling fill structure

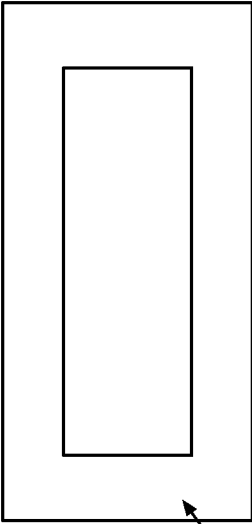




FIG. 3A

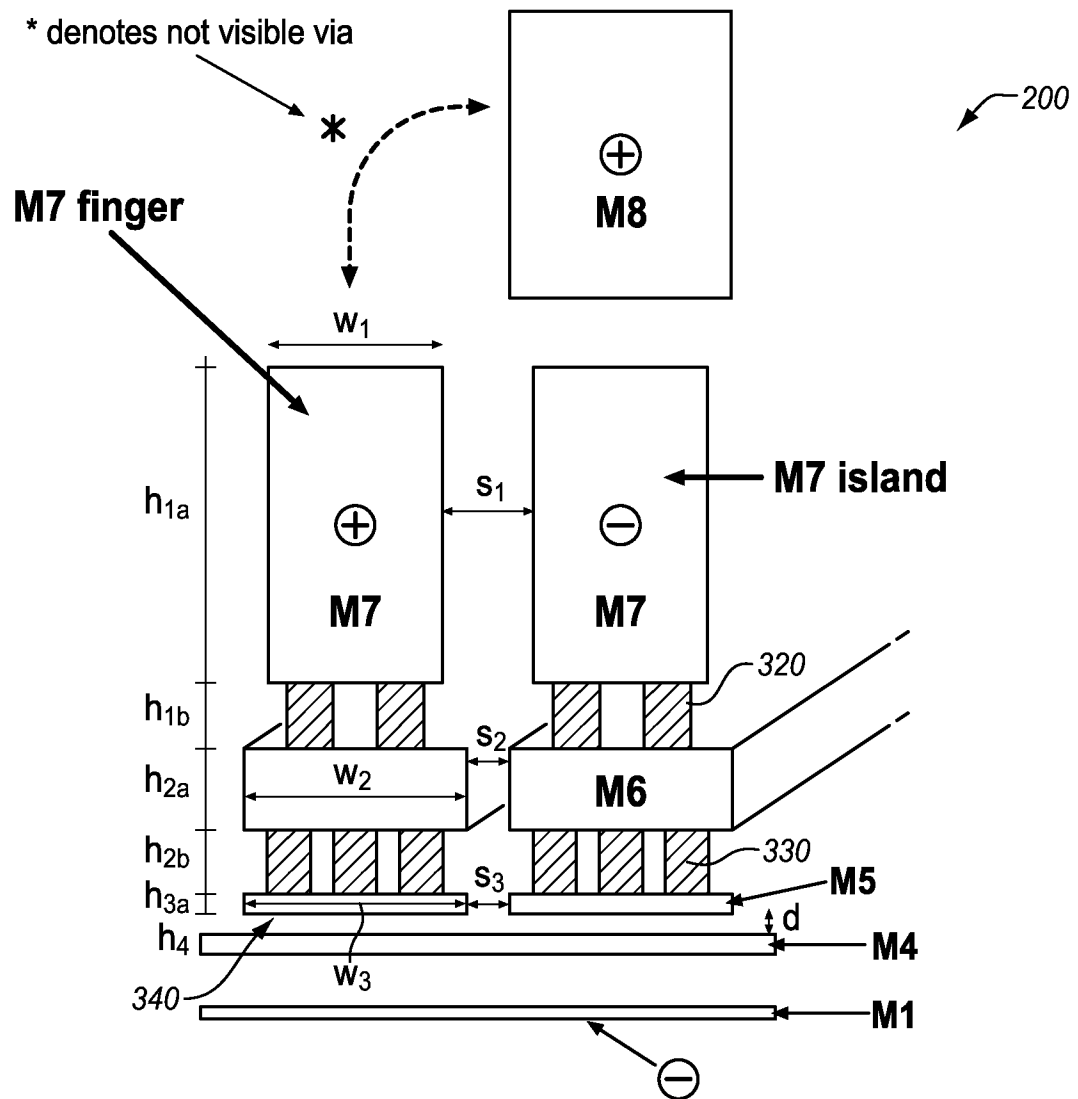


FIG. 4A

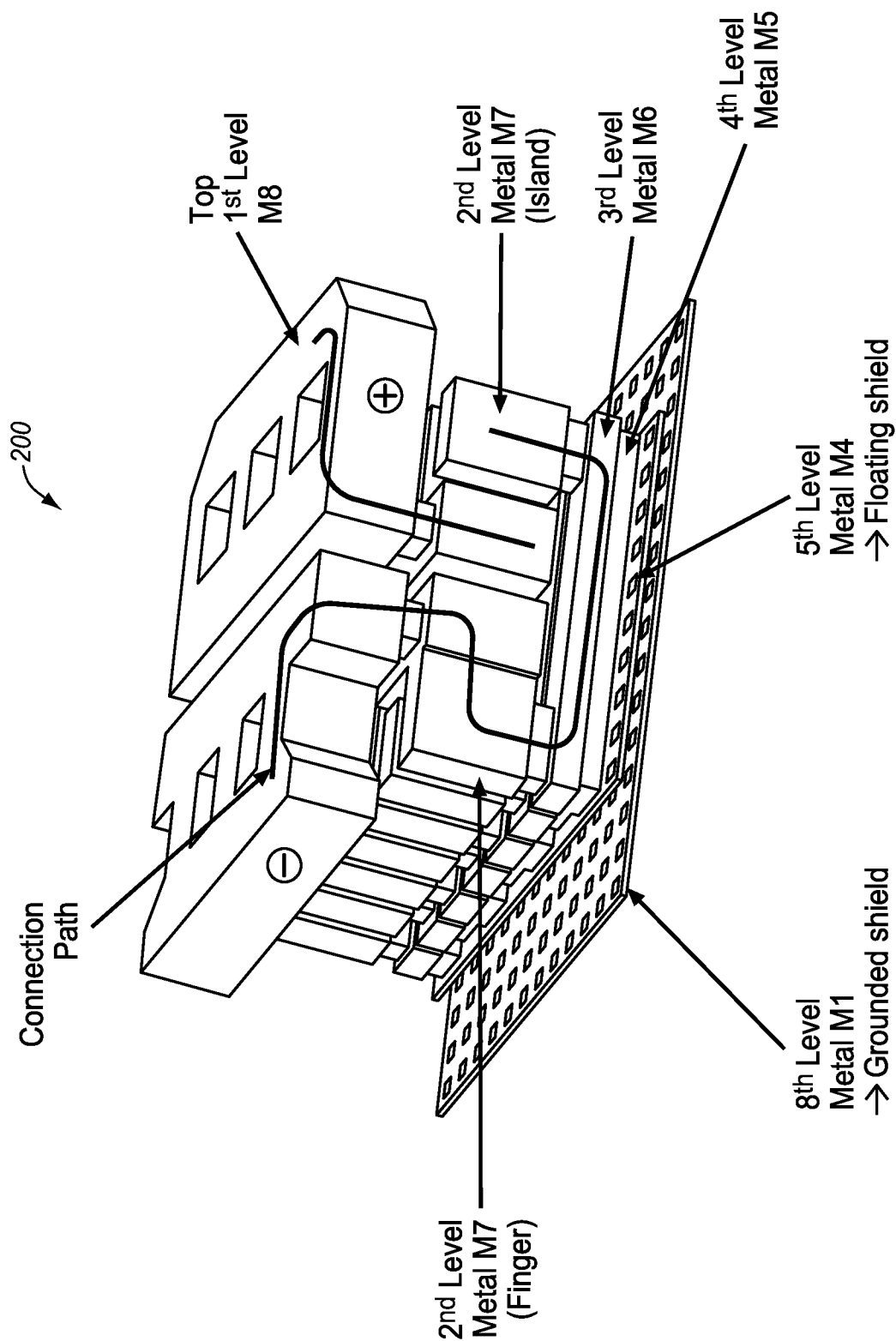


FIG. 4B

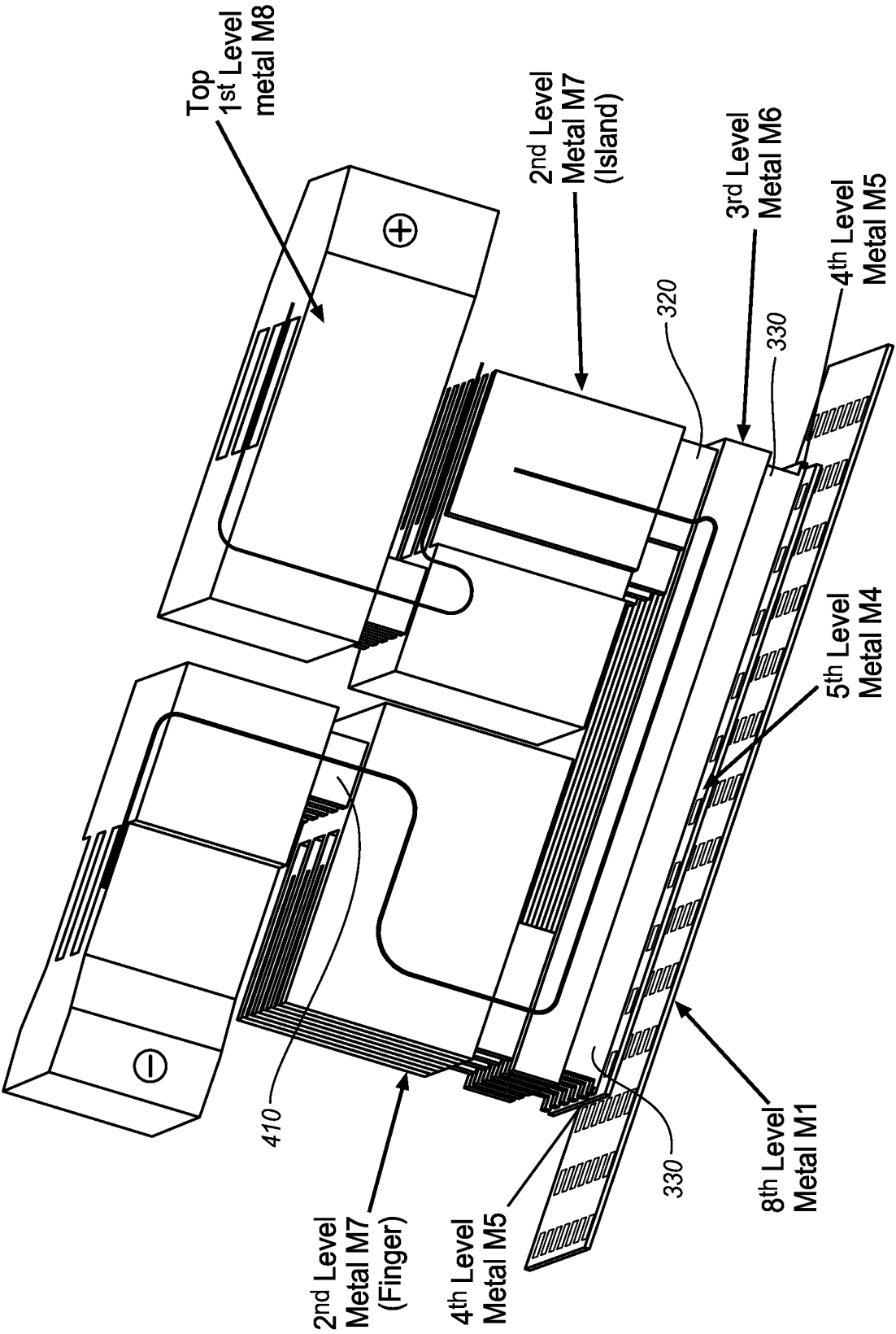


FIG. 4C

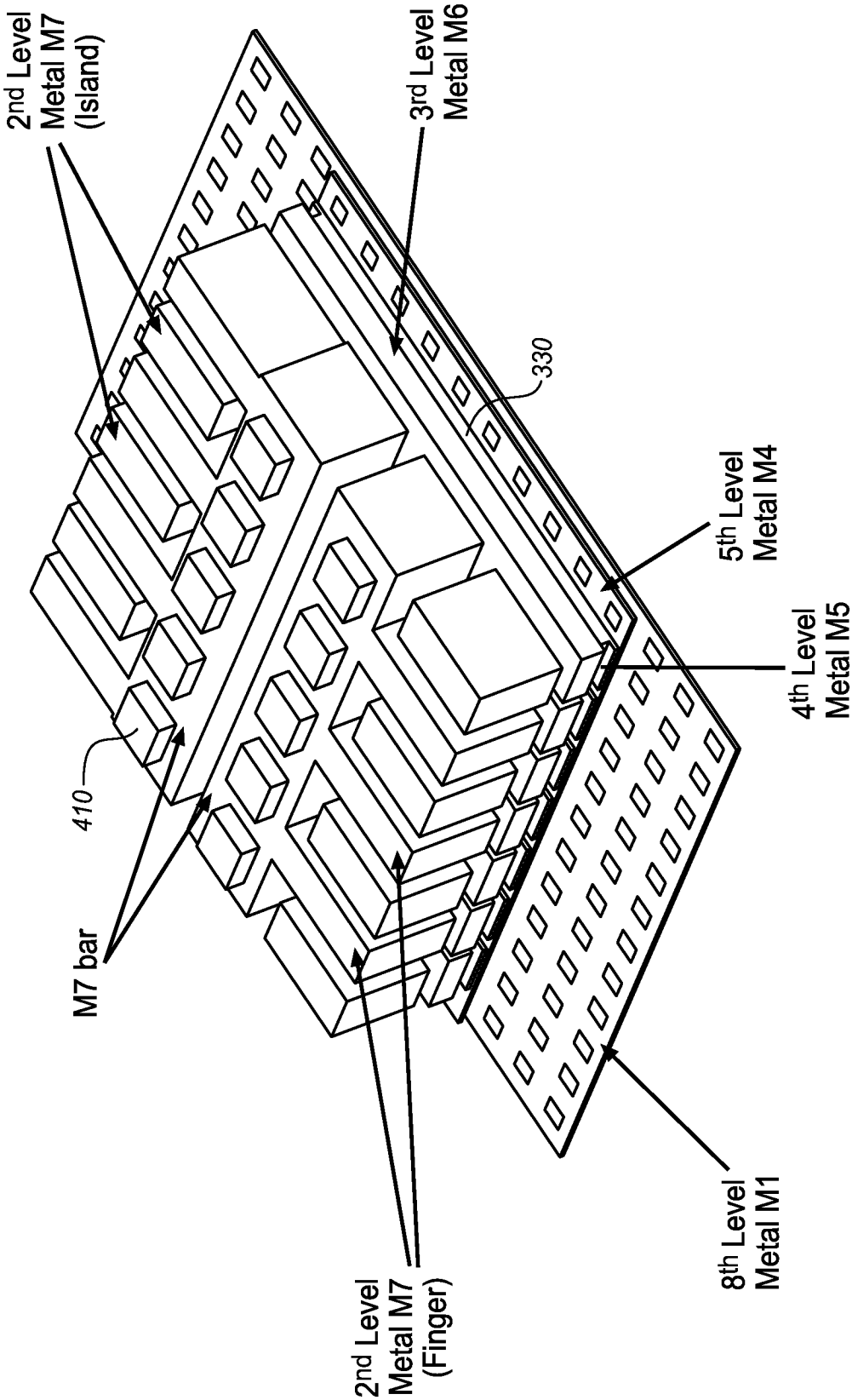




FIG. 5A

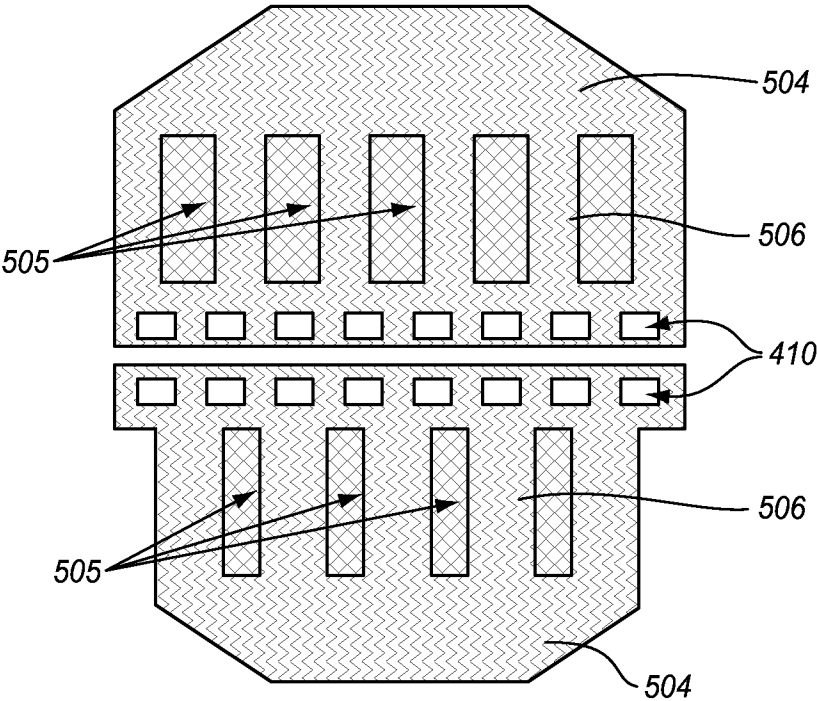
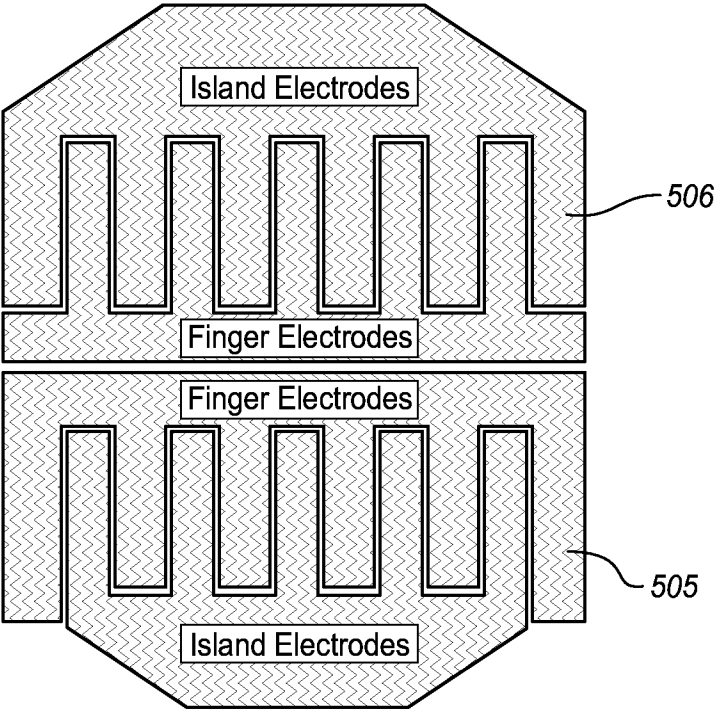


FIG. 5B



10/21

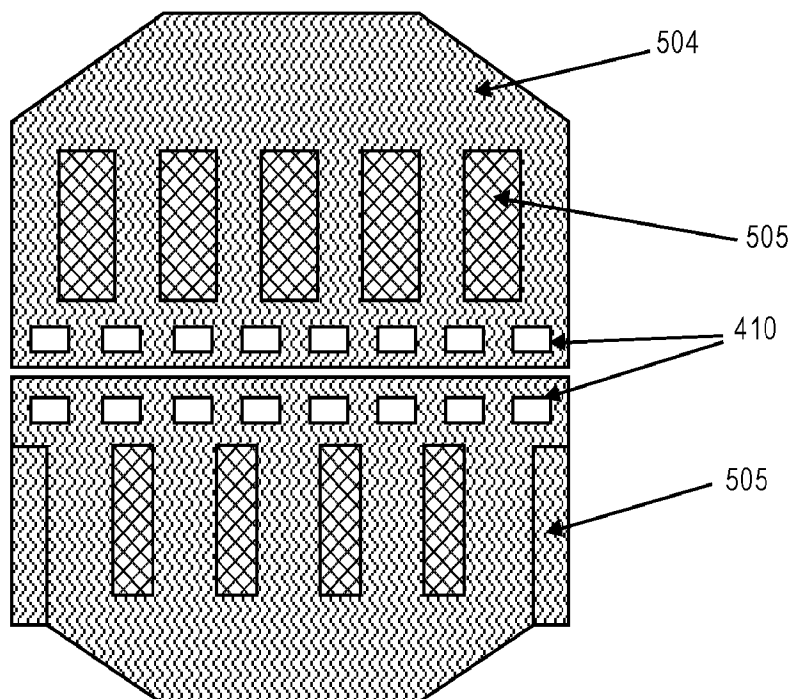


FIG. 5C

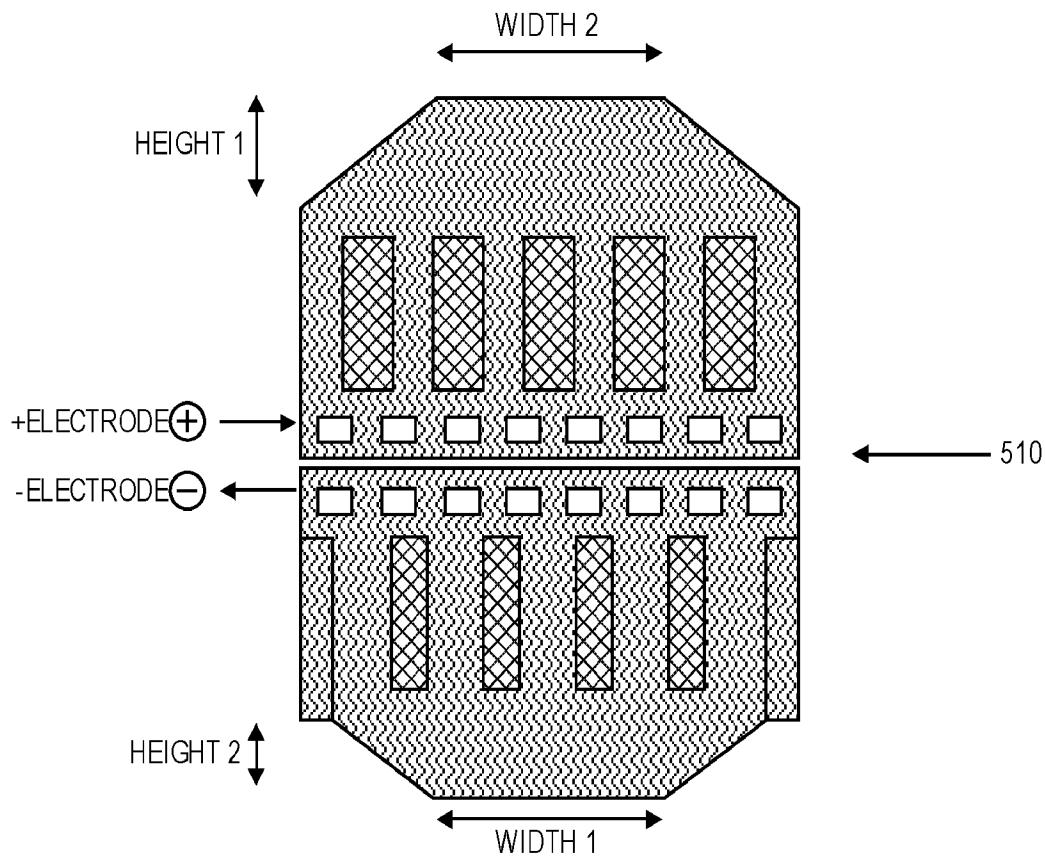


FIG. 5D



FIG. 6A

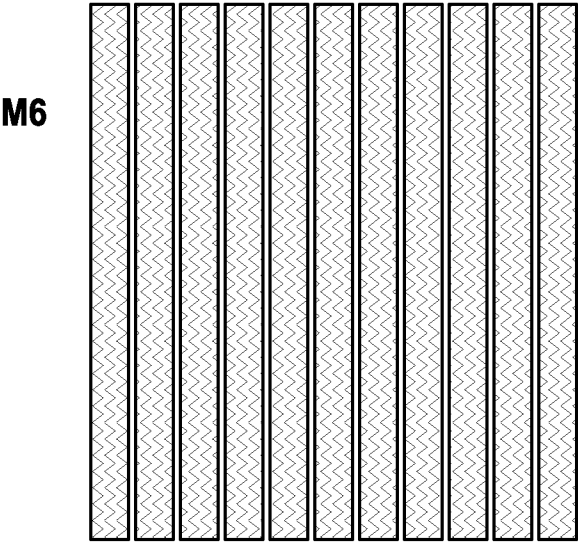


FIG. 6B

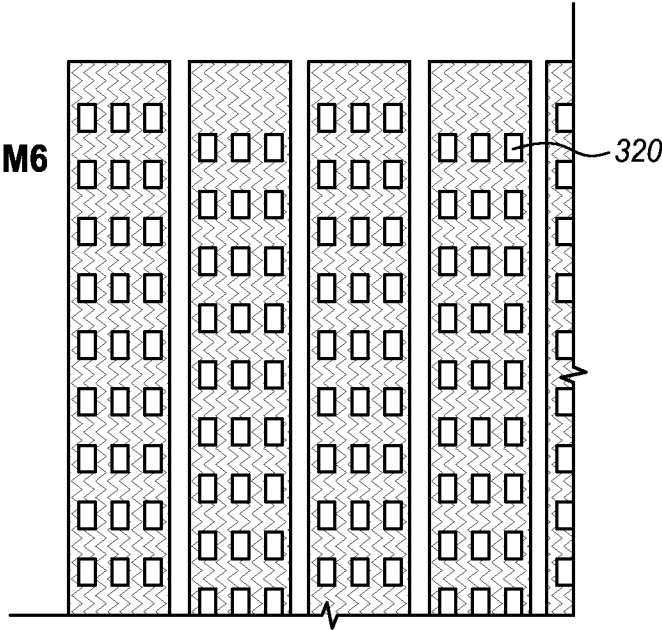




FIG. 6C

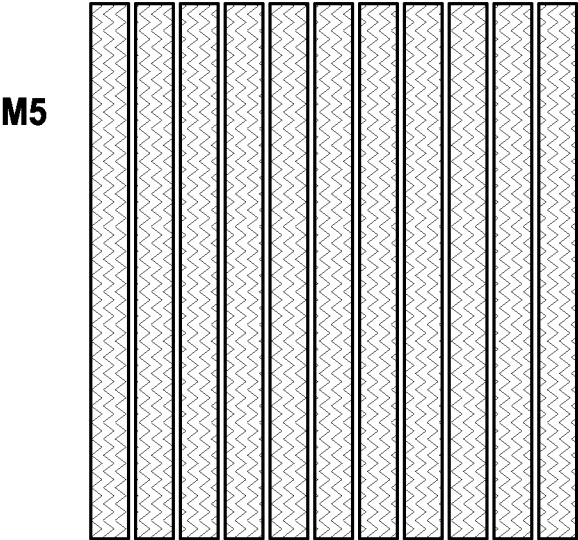


FIG. 6D

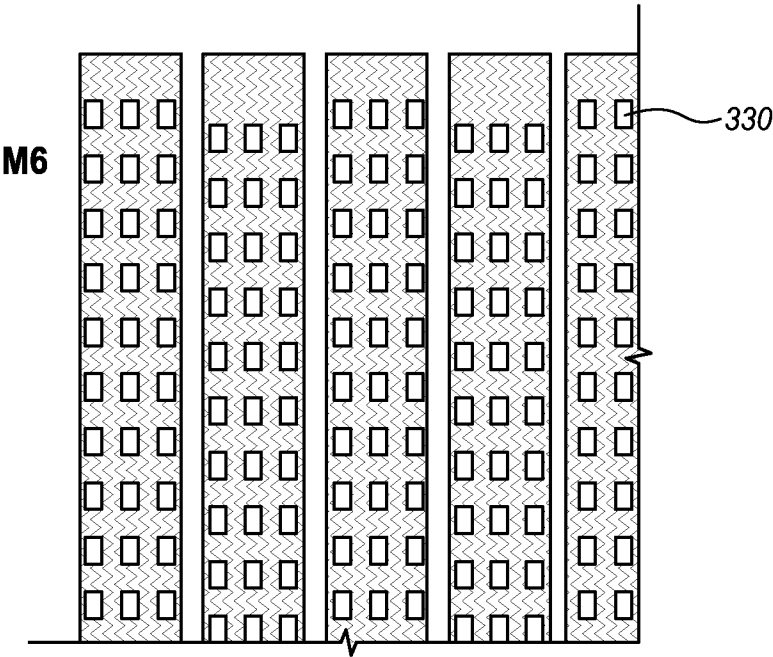




FIG. 6E

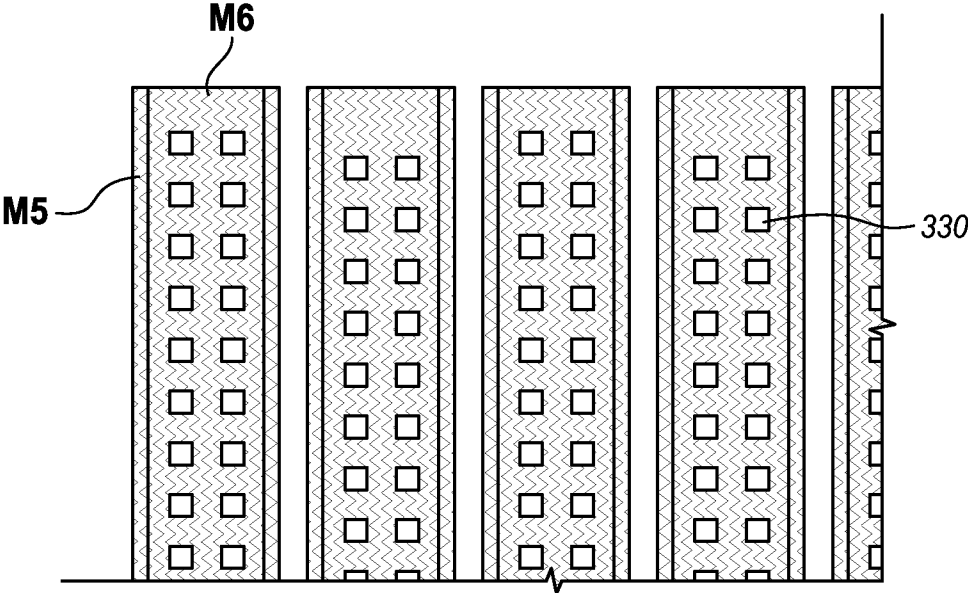




FIG. 7A

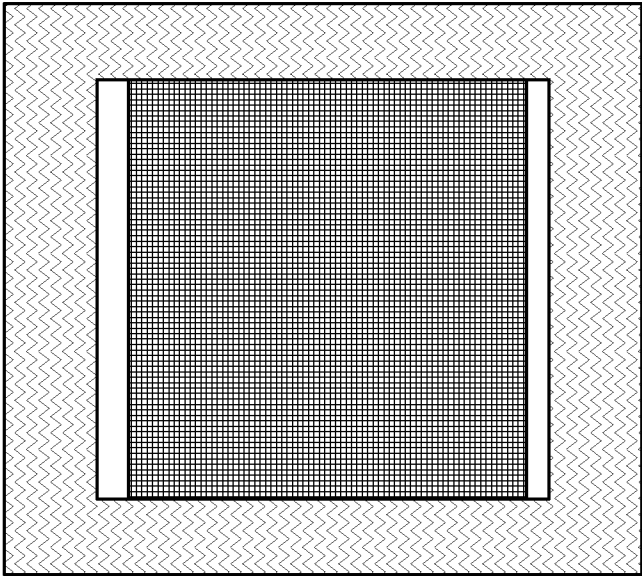


FIG. 7B

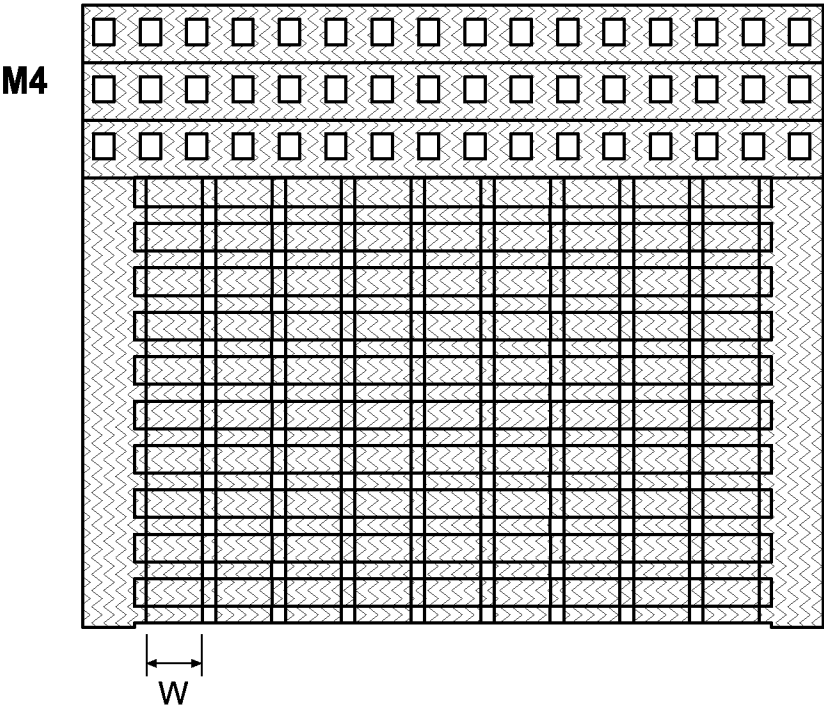




FIG. 8A

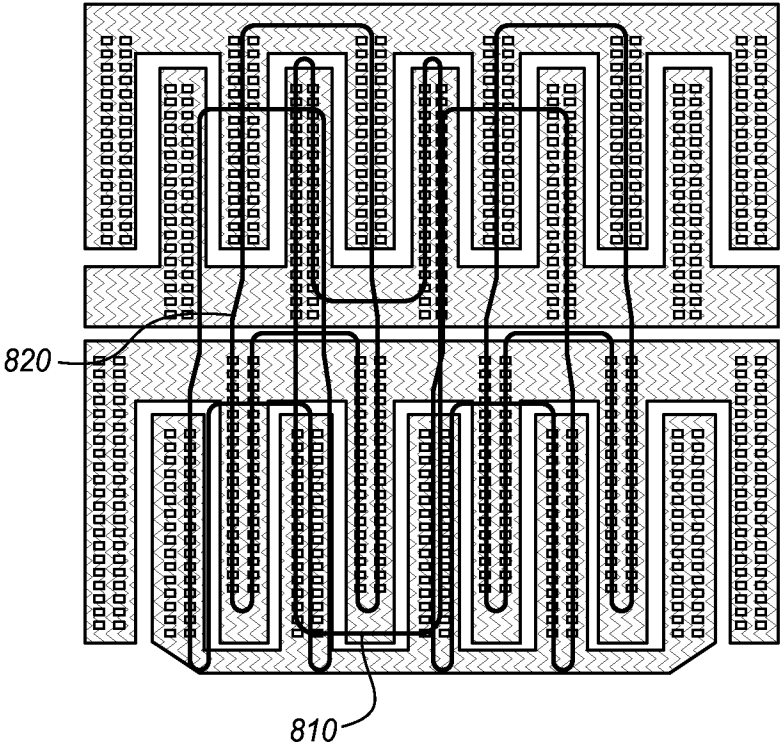


FIG. 8B

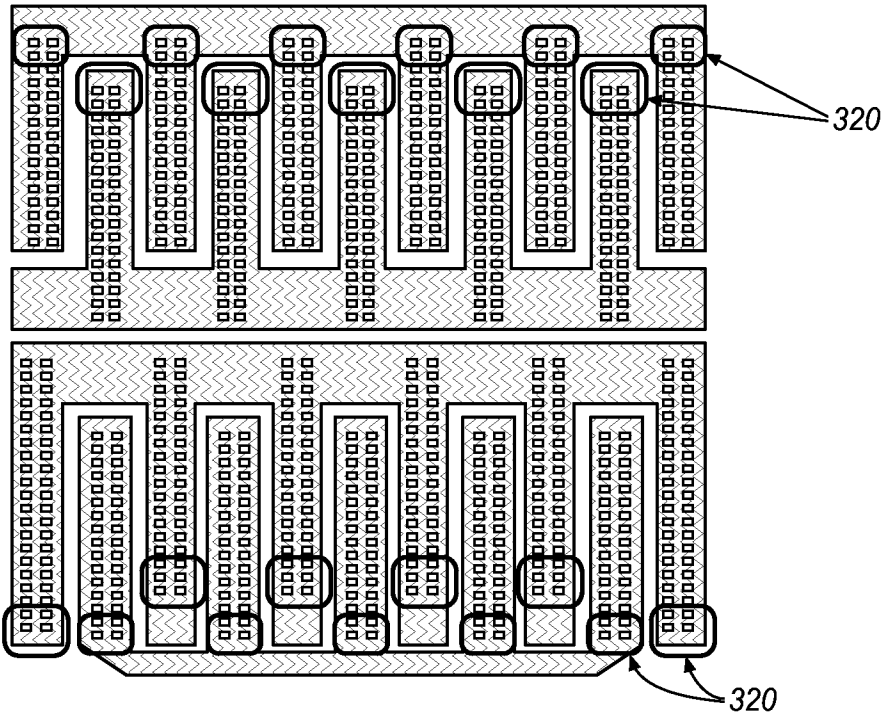


FIG. 8C

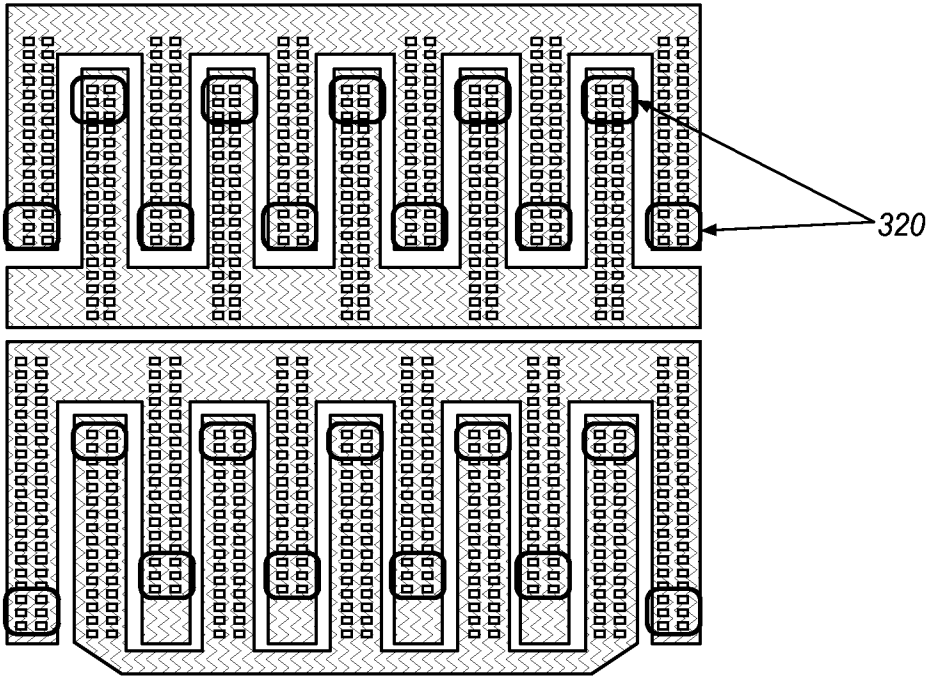
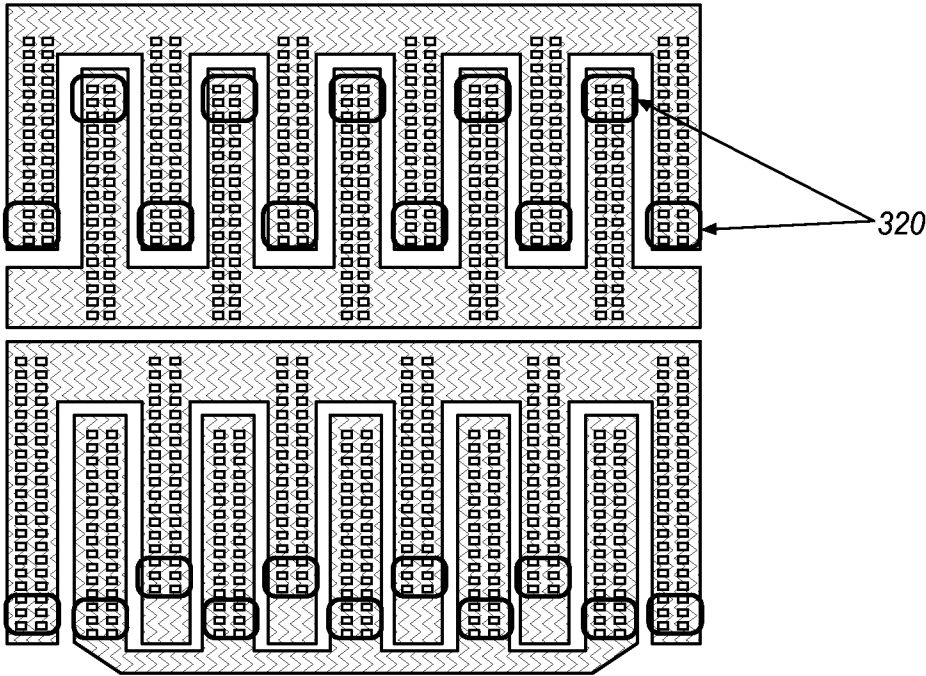


FIG. 8D



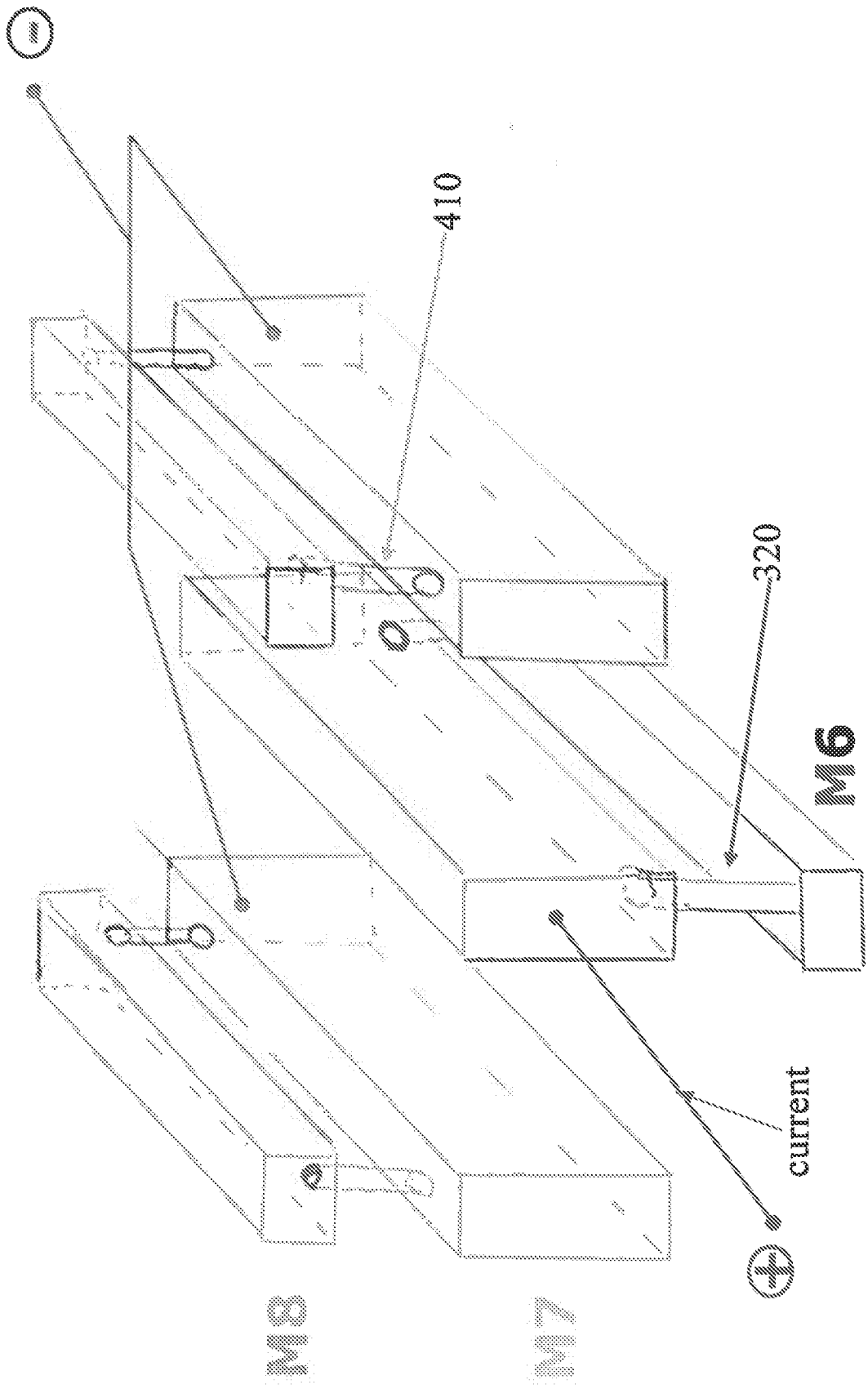


Figure 8E

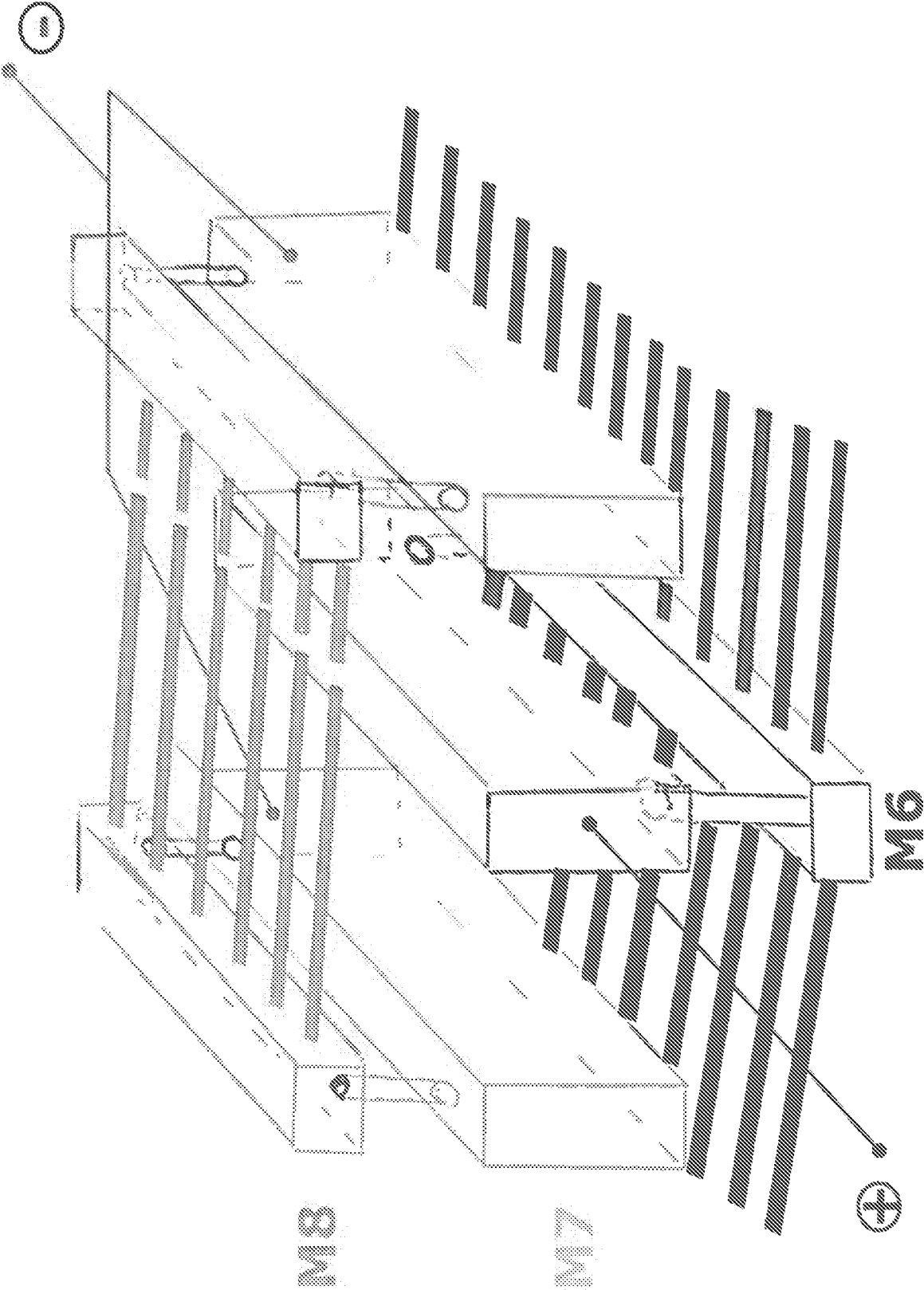


Figure 8F

FIG. 9A

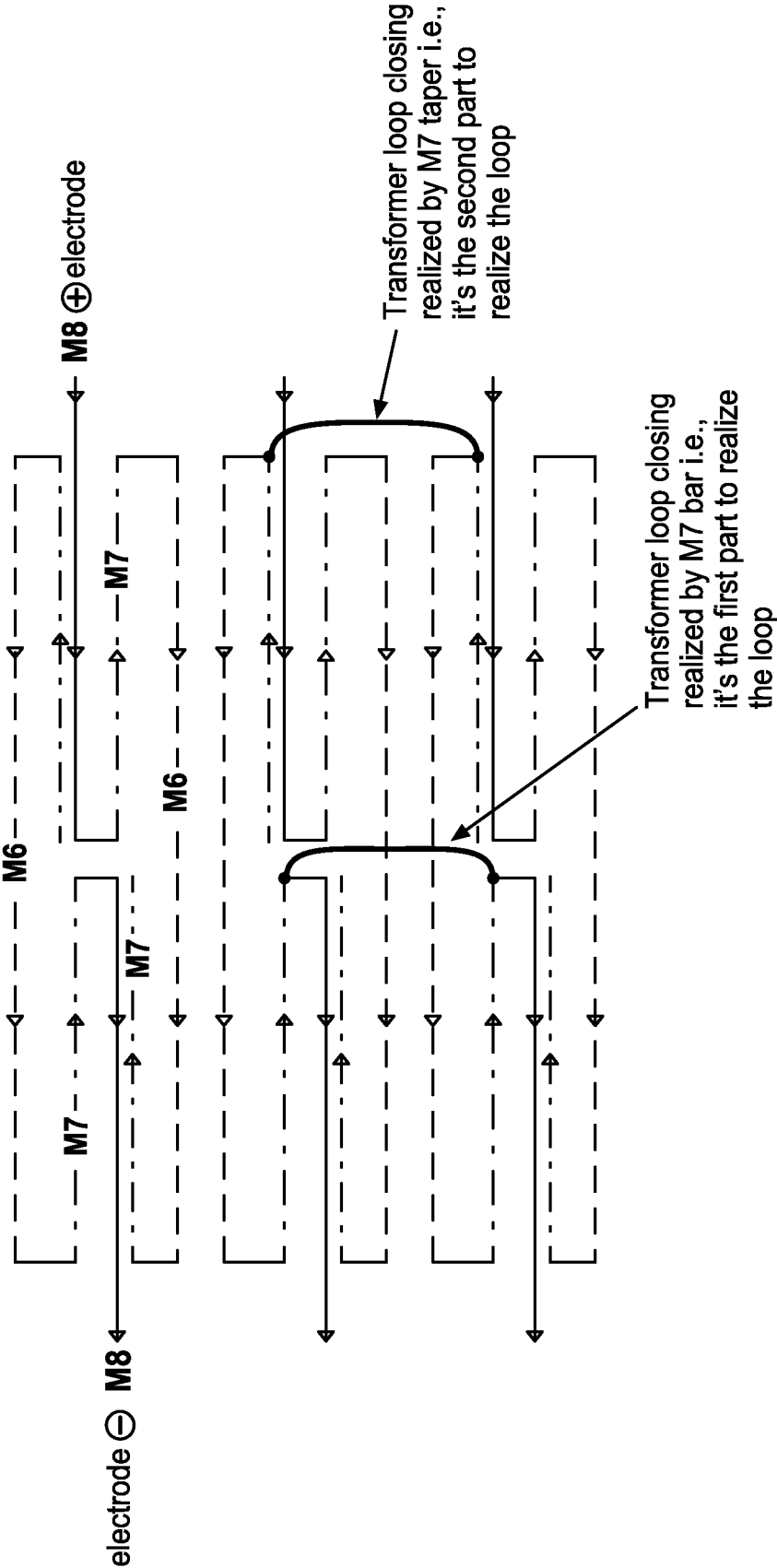




FIG. 9B

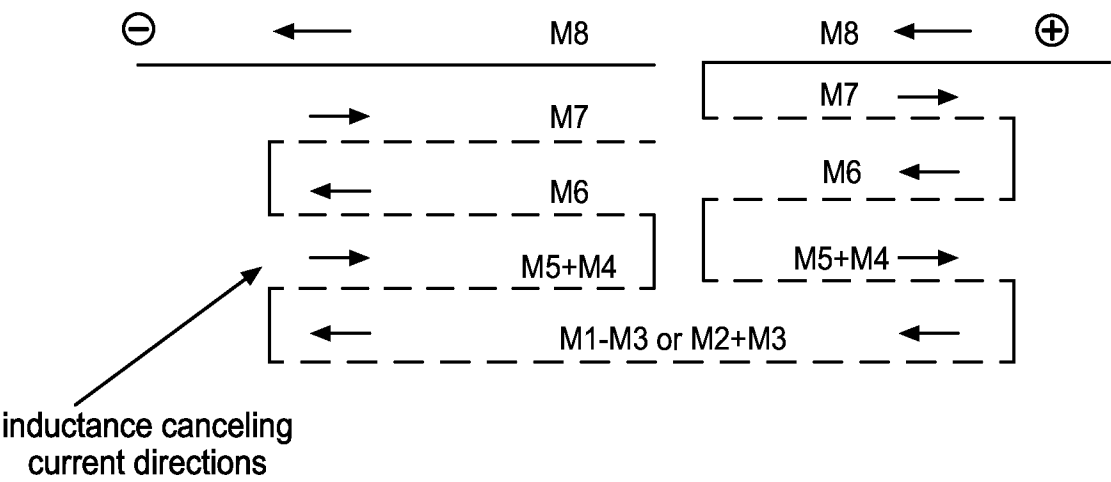


FIG. 9C

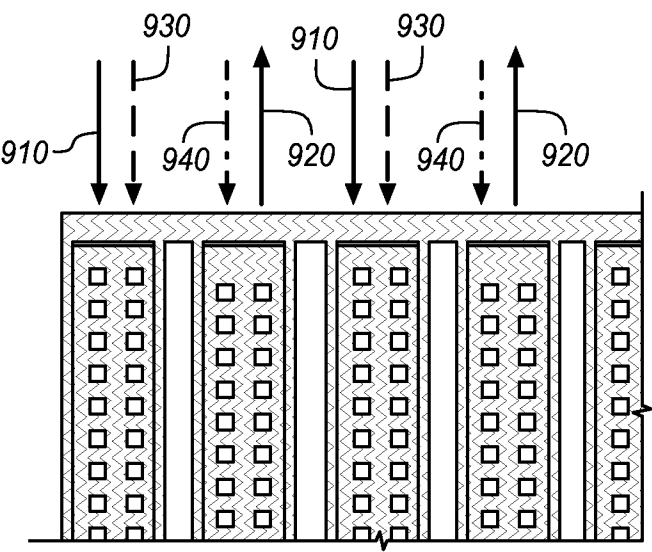
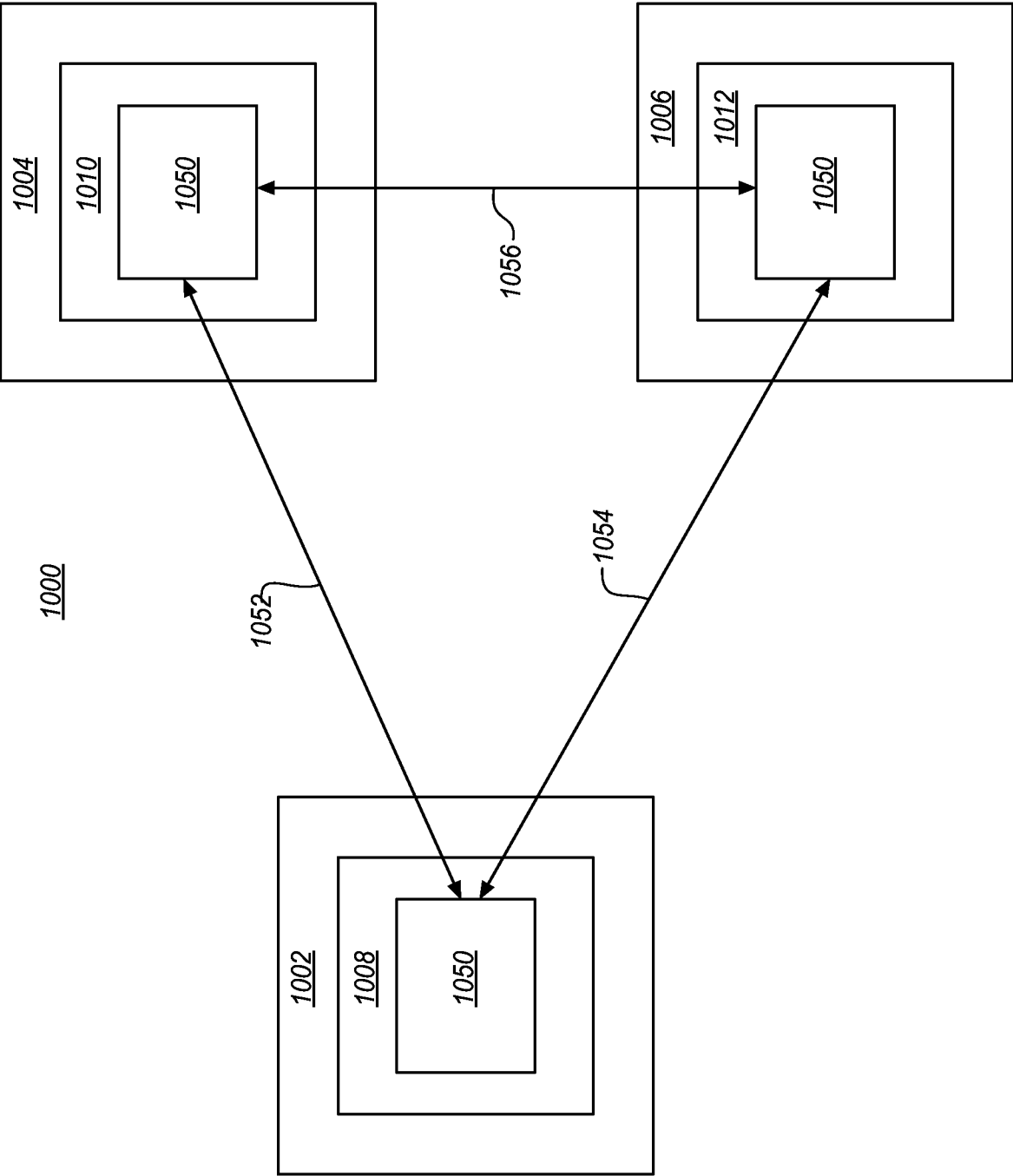


FIG. 10



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/040036**A. CLASSIFICATION OF SUBJECT MATTER****H01G 4/005(2006.01)i, H01L 49/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01G 4/005; H01G 4/38; H01G 4/30; H01L 27/082; H01L 23/522; H03H 7/01; H03H 3/00; H01G 13/00; H01L 49/02; H04B 1/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: finger to finger capacitor, closed loop, plate to plate capacitor, sidewall transformer, inductance, metal layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2016-025260 A1 (XILINX, INC.) 18 February 2016 See abstract, pages 5-10, claim 1 and figures 1-8.	1-25
A	US 2015-0145615 A1 (XILINX, INC.) 28 May 2015 See paragraphs [0035]-[0053], claim 1 and figures 1-5.	1-25
A	US 2011-0151803 A1 (EDWIN VAN DER HEIJDEN et al.) 23 June 2011 See paragraphs [0023]-[0035], claim 1 and figures 1-4.	1-25
A	US 2008-0304205 A1 (DAVID BANG) 11 December 2008 See paragraphs [0022]-[0029], claim 1 and figures 3-4.	1-25
A	US 2007-0228520 A1 (GREG WINN et al.) 04 October 2007 See paragraphs [0029]-[0042], claim 1 and figures 2A-4B.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

16 March 2017 (16.03.2017)

Date of mailing of the international search report

17 March 2017 (17.03.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

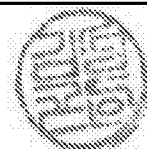
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/040036

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