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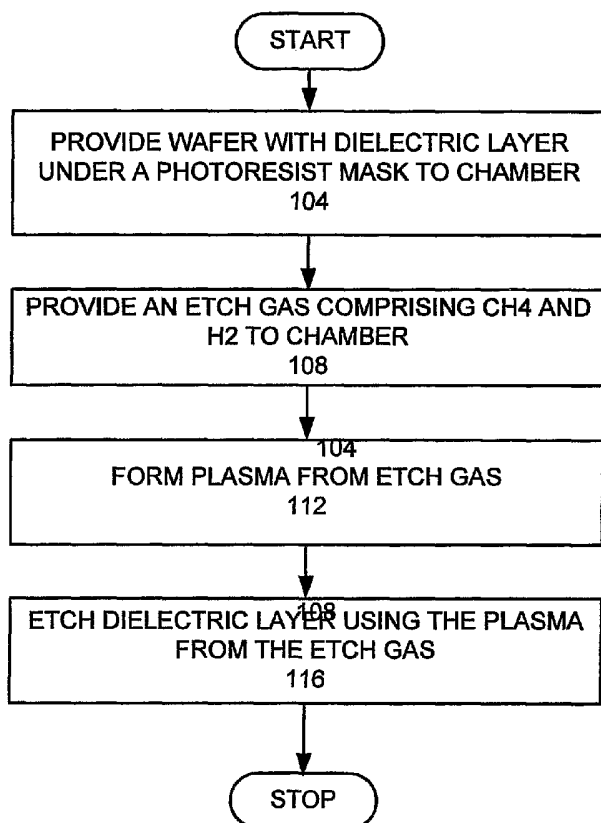
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[Continued on next page]

(54) Title: LOW-K DIELECTRIC ETCH



(57) Abstract: A method for etching a dielectric layer below a photoresist mask is provided. A wafer with the dielectric layer disposed below a photoresist mask is provided in an etch chamber. An etch gas comprising CF₄ and H₂ is provided into the etch chamber wherein the CF₄ has a flow rate and the H₂ has a flow rate, wherein the flow rate of H₂ is greater than the flow rate of CF₄. A plasma is formed from the etch gas. Features are etched into the dielectric layer through the etch mask using the plasma formed from the etch gas.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

LOW-K DIELECTRIC ETCH

BACKGROUND OF THE INVENTION

[0001] The present invention relates to the formation of semiconductor devices.

[0002] During semiconductor wafer processing, features of the semiconductor device are defined in the wafer using well-known patterning and etching processes. In these processes, a photoresist (PR) material is deposited on the wafer and then is exposed to light filtered by a reticle. The reticle is generally a glass plate that is patterned with exemplary feature geometries that block light from propagating through the reticle.

[0003] After passing through the reticle, the light contacts the surface of the photoresist material. The light changes the chemical composition of the photoresist material such that a developer can remove a portion of the photoresist material. In the case of positive photoresist materials, the exposed regions are removed, and in the case of negative photoresist materials, the unexposed regions are removed. Thereafter, the wafer is etched to remove the underlying material from the areas that are no longer protected by the photoresist material, and thereby define the desired features in the wafer.

[0004] Various generations of photoresist are known. 193 nm photoresist and 157 nm photoresist and smaller generation photoresist are desired to provide smaller device sizes and increased device density. 193 nm and 157 nm photoresist may be softer than previous generation photoresist and may be more like polymer and especially, low-k dielectric polymer, which would decrease the selectivity of an etch of a low-k dielectric with respect to the photoresist.

SUMMARY OF THE INVENTION

[0005] To achieve the foregoing and in accordance with the purpose of the present invention a method for etching a dielectric layer below a photoresist mask is provided. A wafer with the dielectric layer disposed below a photoresist mask is provided in an etch chamber. An etch gas comprising CF_4 and H_2 is provided into the etch chamber wherein the CF_4 has a flow rate and the H_2 has a flow rate, wherein the flow rate of H_2 is greater than the flow rate of CF_4 . A plasma is formed from the etch gas. Features are etched into the dielectric layer through the etch mask using the plasma formed from the etch gas.

[0006] In another manifestation of the invention, a method for etching an etch layer below an organic material mask is provided. A wafer with the etch layer disposed below the organic material mask is provided in an etch chamber. An etch gas comprising CF_4 and H_2 is provided into the etch chamber wherein the CF_4 has a flow rate and the H_2 has a flow rate, wherein the flow rate of H_2 is greater than the flow rate of CF_4 . A plasma is formed from the etch gas. Features are etched into the etch layer through the organic material mask using the plasma formed from the etch gas.

[0007] These and other features of the present invention will be described in more detail below in the detailed description of the invention and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0009] FIG. 1 is a high level flow chart of a process that may be used in an embodiment of the invention.

[0010] FIG.'S 2A-C are cross sectional view of a wafer during various steps of the inventive process.

[0011] FIG. 3 is a schematic view of a plasma processing chamber 300 that may be used for depositing the layer, etching, and stripping that may be used by the invention.

[0012] FIG.'S 4A and 4B illustrate a computer system, which is suitable for implementing a controller used in embodiments of the present invention.

[0013] FIG.'S 5A and 5B are photographs of cross-sections of layers etched using the inventive etch.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0014] The present invention will now be described in detail with reference to a few preferred embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures

have not been described in detail in order to not unnecessarily obscure the present invention.

[0015] The invention provides an etch process that is able selectively etch a dielectric layer, especially a low-k dielectric layer, with respect to a 197 nm or smaller generation photoresist with a high selectivity. The selectivity may approach infinity.

[0016] To facilitate understanding, FIG. 1 is a high level flow chart of a process that may be used in an embodiment of the invention. A wafer with a dielectric layer disposed under a photoresist mask is placed into a process chamber (step 104). An etch gas comprising CH₄ and H₂ is provided to the etch chamber (step 108). The etch gas has a H₂ flow rate that is greater than the flow rate of the CF₄ of the etch gas. A plasma is formed from the etch gas (step 112). Features are etched into the dielectric layer through the etch mask using the plasma from the etch gas (step 116).

Example

[0017] In an example of the inventive process for forming a trench, a wafer with a dielectric layer disposed under a photoresist mask is placed into a process chamber (step 104). In an example of the invention, FIG. 2A is a cross sectional view of a wafer 204 with a dielectric layer 208, disposed below a bottom antireflective coating (BARC) 210, disposed below a photoresist mask 212. Preferably, the dielectric layer 208 is a low-k dielectric, which has a $k < 3.0$. In addition, the photoresist that forms the photoresist mask 212 is a 193 nm or less generation photoresist, so that the photoresist is not greater than a 193 nm generation photoresist. Because of the high selectivity of the inventive etch the photoresist mask may have an applied thickness 216 of less than 3000 Å. In this example, the low-k dielectric material is an organosilicate glass, such as Coral, Black Diamond, or Aurora.

[0018] FIG. 3 is a schematic view of a plasma processing chamber 300 that may be used for depositing the layer, etching, and stripping that may be used in this example. The plasma processing chamber 300 comprises confinement rings 302, an upper electrode 304, a lower electrode 308, a gas source 310, and an exhaust pump 320. Within plasma processing chamber 300, the wafer 204 is positioned upon the lower electrode 308. The lower electrode 308 incorporates a suitable substrate chucking mechanism (e.g., electrostatic, mechanical clamping, or the like) for holding the wafer 204. The reactor top 328 incorporates the upper electrode 304 disposed immediately opposite the lower electrode 308. The upper electrode 304, lower electrode 308, and

confinement rings 302 define the confined plasma volume. Gas is supplied to the confined plasma volume by the gas source 310 and is exhausted from the confined plasma volume through the confinement rings 302 and an exhaust port by the exhaust pump 320. A first RF source 344 is electrically connected to the upper electrode 304. A second RF source 348 is electrically connected to the lower electrode 308. Chamber walls 352 surround the confinement rings 302, the upper electrode 304, and the lower electrode 308. Both the first RF source 344 and the second RF source 348 may comprise a 27 MHz power source and a 2 MHz power source. Different combinations of connecting RF power to the electrode are possible. In the case of a 2300 Flex™ or a Exelan HPT or a 2300™ Exelan, made by LAM Research Corporation™ of Fremont, California, which may be used in a preferred embodiment of the invention, both the 27 MHz and 2 MHz power sources make up the second RF power source 348 connected to the lower electrode, and the upper electrode is grounded. A controller 335 is controllably connected to the RF sources 344, 348, exhaust pump 320, and the gas source 310.

[0019] FIG. 4A and 4B illustrate a computer system 800, which is suitable for implementing a controller 335 used in embodiments of the present invention. FIG. 4A shows one possible physical form of the computer system. Of course, the computer system may have many physical forms ranging from an integrated circuit, a printed circuit board, and a small handheld device up to a huge super computer. Computer system 800 includes a monitor 802, a display 804, a housing 806, a disk drive 808, a keyboard 810, and a mouse 812. Disk 814 is a computer-readable medium used to transfer data to and from computer system 800.

[0020] FIG. 4B is an example of a block diagram for computer system 800. Attached to system bus 820 is a wide variety of subsystems. Processor(s) 822 (also referred to as central processing units, or CPUs) are coupled to storage devices, including memory 824. Memory 824 includes random access memory (RAM) and read-only memory (ROM). As is well known in the art, ROM acts to transfer data and instructions uni-directionally to the CPU and RAM is used typically to transfer data and instructions in a bi-directional manner. Both of these types of memories may include any suitable of the computer-readable media described below. A fixed disk 826 is also coupled bi-directionally to CPU 822; it provides additional data storage capacity and may also include any of the computer-readable media described below.

Fixed disk 826 may be used to store programs, data, and the like and is typically a secondary storage medium (such as a hard disk) that is slower than primary storage. It will be appreciated that the information retained within fixed disk 826 may, in appropriate cases, be incorporated in standard fashion as virtual memory in memory 824. Removable disk 814 may take the form of any of the computer-readable media described below.

[0021] CPU 822 is also coupled to a variety of input/output devices, such as display 804, keyboard 810, mouse 812 and speakers 830. In general, an input/output device may be any of: video displays, track balls, mice, keyboards, microphones, touch-sensitive displays, transducer card readers, magnetic or paper tape readers, tablets, styluses, voice or handwriting recognizers, biometrics readers, or other computers. CPU 822 optionally may be coupled to another computer or telecommunications network using network interface 840. With such a network interface, it is contemplated that the CPU might receive information from the network, or might output information to the network in the course of performing the above-described method steps. Furthermore, method embodiments of the present invention may execute solely upon CPU 822 or may execute over a network such as the Internet in conjunction with a remote CPU that shares a portion of the processing.

[0022] In addition, embodiments of the present invention further relate to computer storage products with a computer-readable medium that have computer code thereon for performing various computer-implemented operations. The media and computer code may be those specially designed and constructed for the purposes of the present invention, or they may be of the kind well known and available to those having skill in the computer software arts. Examples of computer-readable media include, but are not limited to: magnetic media such as hard disks, floppy disks, and magnetic tape; optical media such as CD-ROMs and holographic devices; magneto-optical media such as floptical disks; and hardware devices that are specially configured to store and execute program code, such as application-specific integrated circuits (ASICs), programmable logic devices (PLDs) and ROM and RAM devices. Examples of computer code include machine code, such as produced by a compiler, and files containing higher level code that are executed by a computer using an interpreter. Computer readable media may also be computer code transmitted by a

computer data signal embodied in a carrier wave and representing a sequence of instructions that are executable by a processor.

[0023] In this example, the bottom antireflective coating (BARC) 210 is opened before the etching of the dielectric layer. The opening of the BARC 210 reduces the thickness of the photoresist mask to a remaining photoresist mask thickness 218, as shown in FIG. 2B. The photoresist mask may have a remaining mask thickness of less than 2000 Å. In this example, the BARC opening is through a process where a pressure of 100 mTorr is maintained in the chamber 300. 200 watts at 27 MHz and 0 watts at 2 MHz of power is provided. A BARC open gas of 100 sccm CF₄ is provided. The BARC open process is maintained for 49 seconds. FIG. 5A is a photograph of a cross-sectional view of a dielectric layer disposed below a photoresist mask and a BARC layer 504 after the BARC has been opened and before the main etch. The photoresist and BARC have a photoresist and BARC thickness 508 of about 182 nm.

[0024] Next an etch gas comprising CF₄ and H₂ is provided from the gas source 310 (step 108). In this example, the etch gas provides a flow of 60 sccm CF₄, 70 sccm H₂, and 300 sccm Ar. A plasma is generated from the etch gas (step 112). In this example, the chamber pressure is maintained at 80 mTorr. 600 watts are provided at 27 MHz and 200 watts are provided at 2 MHz. The plasma formed from the etch gas is used to etch features in the dielectric layer 208 (step 116). This process is maintained for 60 seconds to etch a 2681 Å feature depth. This example provides no loss of photoresist, but instead adds polymer to the photoresist, while etching features in the dielectric layer, which thus provides a dielectric to photoresist etch selectivity of infinity. FIG. 2C is a cross-sectional view of the wafer 204 after the etching of features 222 in the dielectric layer 208 is completed. It should be noted that the thickness 220 of the combined remaining photoresist mask and polymer added during the etch is greater than the remaining photoresist mask thickness 218 before etching. FIG. 5B is a photograph of a cross-sectional view of a dielectric layer disposed below a photoresist mask and a BARC layer 504 after the main etch, using the above etch parameters. The photoresist and BARC have a photoresist and BARC thickness 512 of about 229 nm. So, the added polymer has increased the thickness of the photoresist during the etching process.

[0025] The photoresist mask is then stripped.

[0026] Such an inventive process may be used to provide infinite selectivity. The inventive process is able to add to the thickness of the photoresist, while etching.

[0027] In other embodiments of the invention, other organic layers may be used as an etch mask instead of 193 nm or higher generation photoresist masks. It has been found that the remaining organic layer before the etch may be less than 2000 Å. More preferably, the remaining organic or photoresist layer before the etch is less than 1000 Å. Most preferably the remaining organic or photoresist layer before the etch is less than 500 Å. By allowing the use of thinner photoresist masks of higher generation photoresists, the critical dimensions can be decreased, since thinner photoresist masks of higher generation photoresist provide higher resolution.

[0028] It is preferred that the flow rate of H_2 be greater than the flow rate of CF_4 . It is more preferable that the flow rate of H_2 (x) be greater than the flow rate of CF_4 (y) and less than five times the flow rate of CF_4 (5y), so that $5y > x > y$. It is more preferable that the flow rate of H_2 (x) be either between five times the flow rate of CF_4 (5y) and three times the flow rate of CF_4 (3y) or two times the flow rate of CF_4 (2y) and the flow rate of CF_4 (y), such that $5y > x > 3y$ or $2y > x > y$.

[0029] For a flow rate of 60 sccm CF_4 , it is preferred that the flow rate of H_2 would be between 60 sccm and 120 sccm providing an H_2 to CF_4 flow ratio of between about 1:1 to 2:1. The most preferable flow rate is 80 sccm H_2 . For a flow rate of 35 sccm CF_4 , it is preferable that the flow rate of H_2 would be between 100 to 175 sccm H_2 , providing an H_2 to CF_4 flow ratio between about 3:1 to 5:1. The other most preferred flow rate is 120 sccm H_2 .

[0030] For etching a low-k dielectric, the above recipes may be used with the addition of N_2 gas. A preferred flow rate for N_2 that may be added to the above recipes is 5 sccm to 40 sccm N_2 . A most preferred flow rate is about 20 sccm N_2 .

[0031] In an example of a recipe that uses N_2 , during a main etch a pressure of 90 mTorr is maintained in the chamber. An etching gas consisting essentially of 40 sccm CF_4 , 50 sccm H_2 , 20 sccm N_2 , and 100 sccm Ar is provided into the chamber. 800 Watts are provided at 27 MHz. 400 Watts are provided at 2 MHz. This recipe provided an etch where the thickness of the mask increased, and in addition no striation (sidewall polymer deposition) was found, and where the feature had a very vertical profile.

[0032] It is preferred that the power ranges for the higher frequency power source (i.e. 27MHz power source) be between 200W~1500W and for the lower frequency power source (i.e. 2MHz power source) be from 0W~1000W. It is more preferred that the power ranges for the higher frequency power source be between 500W~1200W and for the lower frequency power source be between 200W~800W. It is most preferred that the power ranges for the higher frequency power source be between 800W~1000W and for the lower frequency power source be between 300W~600W. Another example of a recipe that uses the above power ranges for etching a low-k via provides a pressure of 90 mTorr, with a high frequency power of 1000W and a lower frequency power of 400W.

[0033] Without being bound by theory, it is believed that CF_4 is a strong etchant providing four fluorine atoms for etching for each carbon atom. As a result, H_2 is added to protect the photoresist. It was believed that such a combination would cause etch stop. It was unexpectedly found that such a combination does not cause etch stop.

[0034] In other embodiments N_2 may be added to the etch gas at a flow rate of between 5-40 sccm, when a low-k dielectric is being etched. It is believed that N_2 provides a leaner etch gas that scavenges carbon during a low-k dielectric etch for organosilicate glass (OSG), such as Coral (manufactured by Novellus of San Jose, CA, Black Diamond manufactured by Applied Materials Inc. of Santa Clara, CA), and Aurora (manufactured by ASM Japan KK of Tokyo), which results in the formation of less polymer.

[0035] It has been found that the inventive process provides etching rates of over 1 micron per minute. The inventive etch process has been found to provide an etch of up to about 1.3 microns per minute. Even higher etch rates may be achieved with higher powers.

[0036] Too fast an etch rate may be too hard to control. Argon may be added to slow down etch rates. This allows for greater control of etch rates by controlling the flow of argon.

[0037] It is preferred that the etch time using the inventive etch gas is greater than 10 seconds. It is more preferred that the etch time is greater than 20 seconds.

[0038] It has been unexpectedly found that the inventive process reduces striation. It is believed that striation is reduced because this process not only deposits on PR but

also deposits a thin layer of sidewall polymer. This sidewall polymer is believed to reduce the formation of striation.

[0039] The invention may be used for various applications, such as in the formation of vias, formation of trenches, and the opening of silicon nitride hard mask. The hard mask may be above a low-k dielectric. The inventive process would then allow a thin photoresist mask to be used for both opening the hard mask and etching the dielectric layer, especially low-k dielectric layers.

[0040] While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and various substitute equivalents, which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and various substitute equivalents as fall within the true spirit and scope of the present invention.

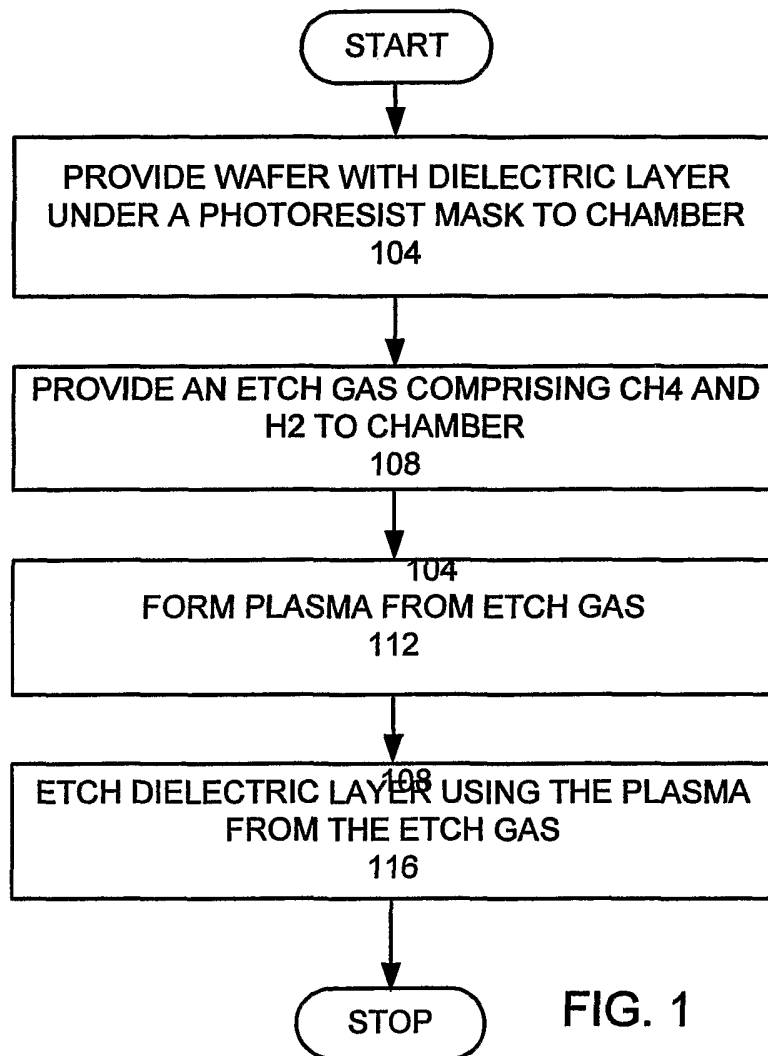
CLAIMS

What is claimed is:

1. A method for etching a dielectric layer below a photoresist mask, comprising:
providing a wafer with the dielectric layer disposed below a photoresist mask
5 into an etch chamber;
providing an etch gas comprising CF_4 and H_2 into the etch chamber wherein
the CF_4 has a flow rate and the H_2 has a flow rate, wherein the flow rate of H_2 is
greater than the flow rate of CF_4 ;
forming a plasma from the etch gas; and
10 etching features into the dielectric layer through the etch mask using the
plasma formed from the etch gas.
2. The method, as recited in claim 1, wherein the photoresist mask has a
thickness of less than 2000 Å before etching the feature.
3. The method, as recited in any of claims 1-2, the photoresist is not greater than
15 a 193 nm generation photoresist.
4. The method, as recited in any of claims 1-3, wherein the etching features into
the dielectric layer adds polymer on the photoresist mask during the etching so that a
thickness of the mask increases to provide infinite etch selectivity for etching the
dielectric layer with respect to the photoresist mask.
- 20 5. The method, as recited in any of claims 1-4, wherein the flow rate of the H_2 is
less than five times the flow rate of CF_4 .
6. The method, as recited in any of claims 1-5, wherein the photoresist mask has
a thickness of less than 500 Å before etching the feature.
7. The method, as recited in any of claims 1-6, wherein the flow rate of H_2 is
25 greater than three times the flow rate of CF_4 .
8. The method, as recited in any of claims 1-7, wherein the etch gas further
comprises N_2 .
9. The method, as recited in any of claims 1-8, wherein the dielectric layer is a
low-k dielectric layer.
- 30 10. The method, as recited in any of claims 8-9, wherein the N_2 has a flow rate
between 5-40 sccm.
11. The method, as recited in any of claims 1-10, wherein the etching provides an
etch rate greater than 1 micron per minute.

12. The method, as recited in any of claims 1-11, wherein the etch gas further comprises argon.
13. The method, as recited in any of claims 1-12, wherein the etching the feature is performed for more than 20 seconds.
- 5 14. The method, as recited in any of claims 1-13, wherein the flow rate of H₂ is less than two times the flow rate of CF₄.
15. The method, as recited in any of claims 1-14, wherein the etching features into the dielectric layer further deposits polymer on sidewalls of the features, which reduces striation.
- 10 16. A semiconductor device formed by the method of any of claims 1-15.
17. An apparatus for performing the method of any of claims 1-15.
18. A method for etching an etch layer below an organic material mask, comprising:
- providing a wafer with the etch layer disposed below the organic material
- 15 mask into an etch chamber;
- providing an etch gas comprising CF₄ and H₂ into the etch chamber wherein the CF₄ has a flow rate and the H₂ has a flow rate, wherein the flow rate of H₂ is greater than the flow rate of CF₄;
- forming a plasma from the etch gas; and
- 20 etching features into the etch layer through the organic material mask using the plasma formed from the etch gas.
19. The method, as recited in claim 18, wherein the organic material mask has a thickness of less than 2000 Å before etching the feature.
20. The method, as recited in any of claims 18-19, wherein the etching features
- 25 into the etch layer adds polymer on the organic material mask during the etching so that a thickness of the mask increases to provide infinite etch selectivity for etching the etch layer with respect to the organic material mask.
21. The method, as recited in any of claims 18-20, wherein the flow rate of the H₂ is less than five times the flow rate of CF₄.
- 30 22. The method, as recited in any of claims 18-21, wherein the organic material mask has a thickness of less than 500 Å before etching the feature.
23. The method, as recited in any of claims 18-22, wherein the flow rate of H₂ is greater than three times the flow rate of CF₄.

24. The method, as recited in any of claims 18-23, wherein the etch gas further comprises N₂.
25. The method, as recited in claim 24, wherein the N₂ has a flow rate between 5-40 sccm.
- 5 26. The method, as recited in any of claims 18-25, wherein the dielectric layer is a low-k dielectric layer.
27. The method, as recited in any of claims 18-26, wherein the etching provides an etch rate greater than 1 micron per minute.
28. The method, as recited in any of claims 18-27, wherein the etching the feature
10 is performed for more than 20 seconds.
29. The method, as recited in any of claims 18-28, wherein the flow rate of H₂ is less than two times the flow rate of CF₄.
30. The method, as recited in any of claims 18-29, wherein the etching features into the dielectric layer further deposits polymer on sidewalls of the features, which
15 reduces striation.



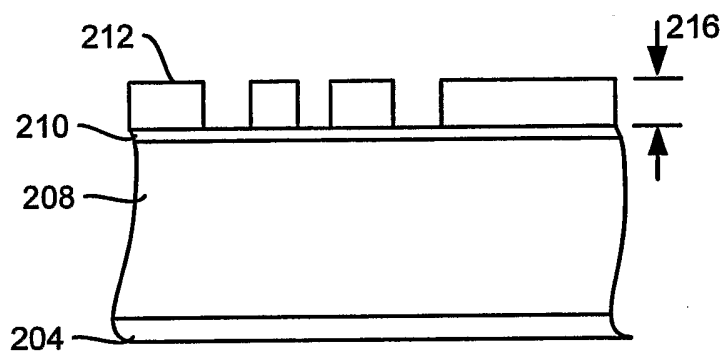


FIG. 2A

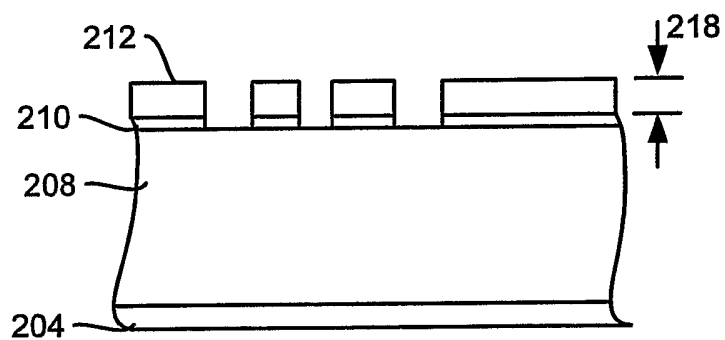


FIG. 2B

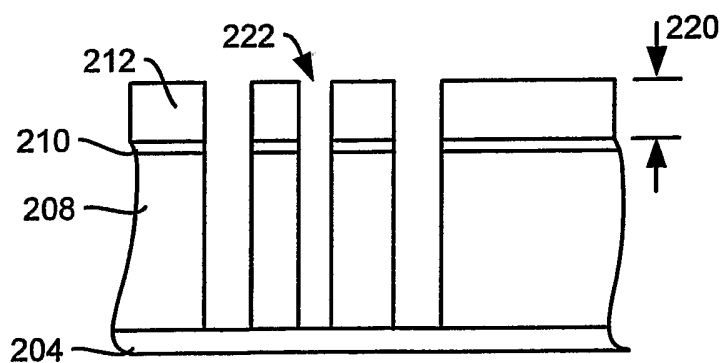


FIG. 2C

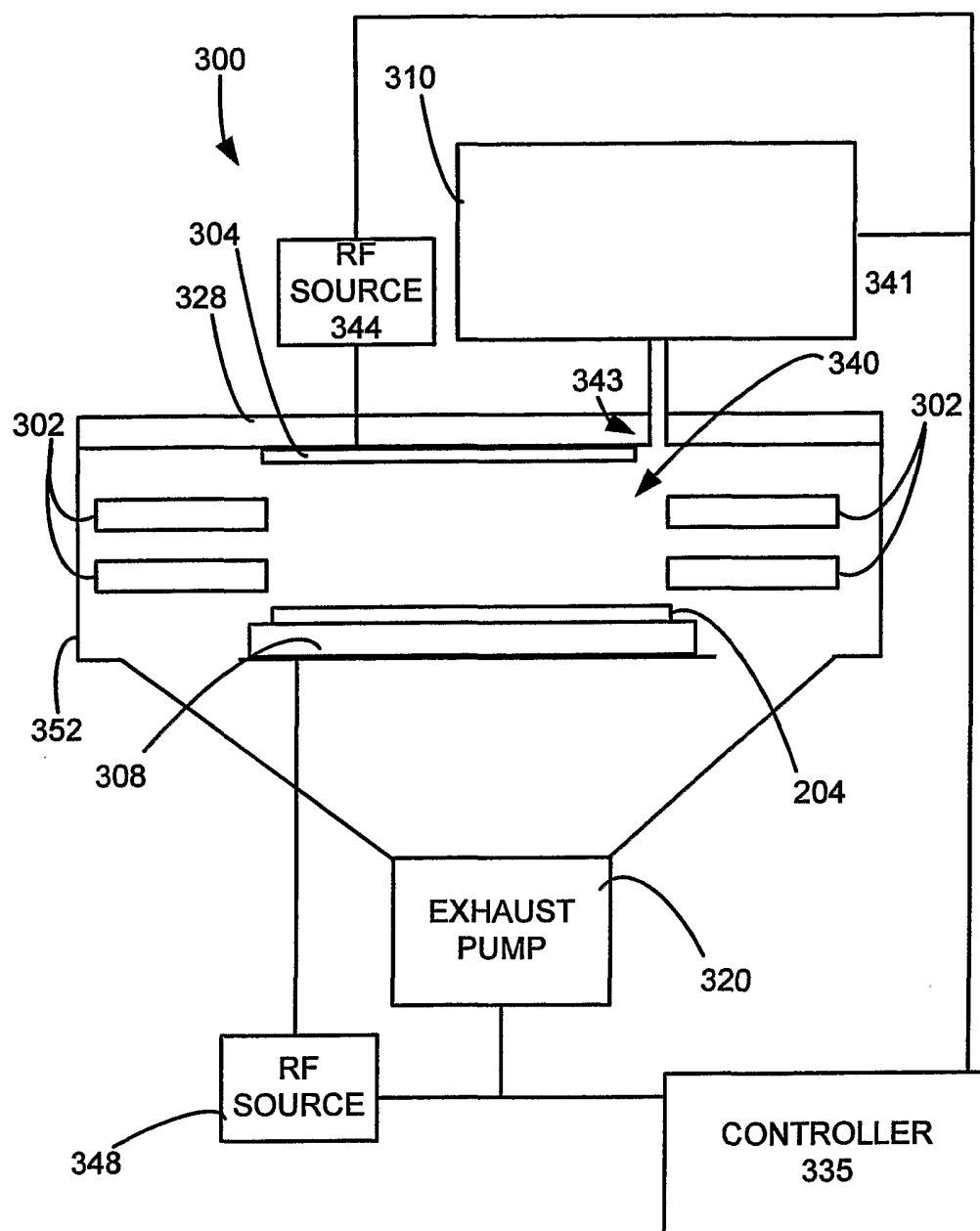
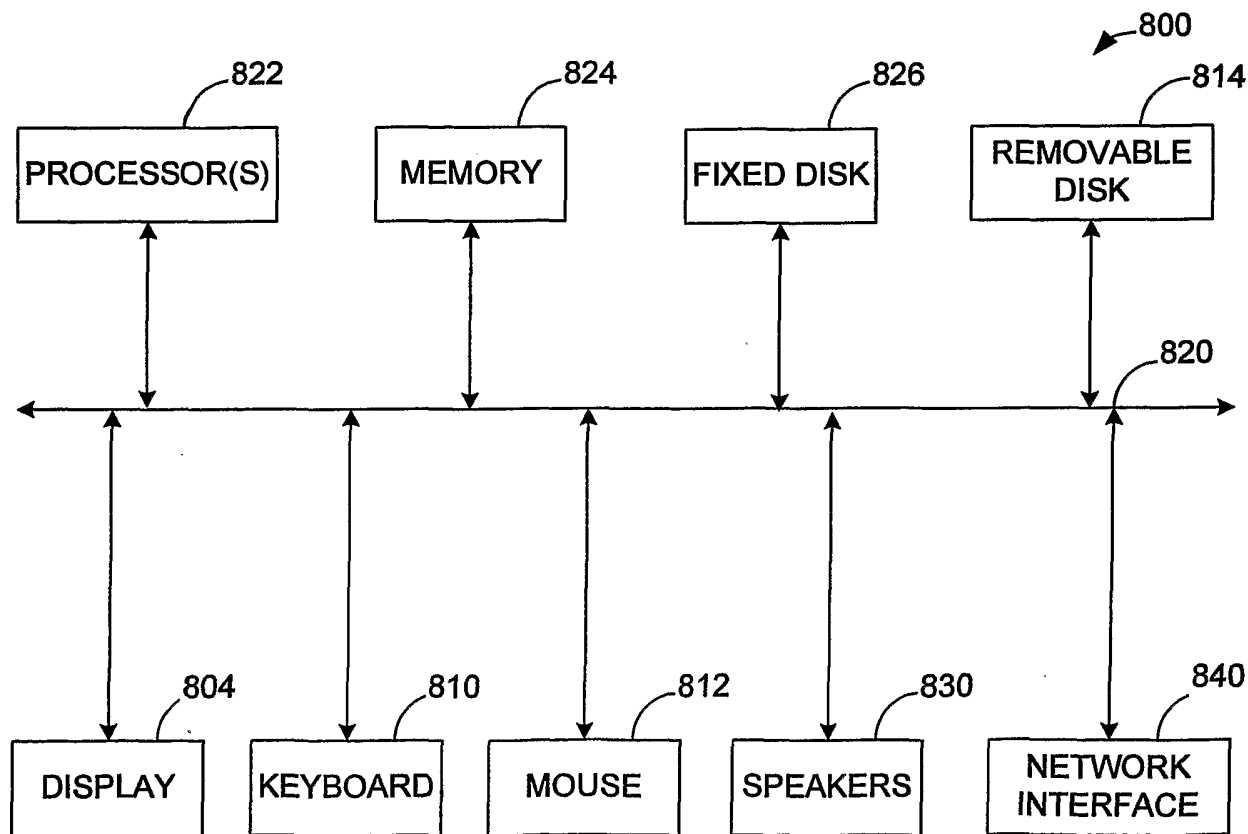
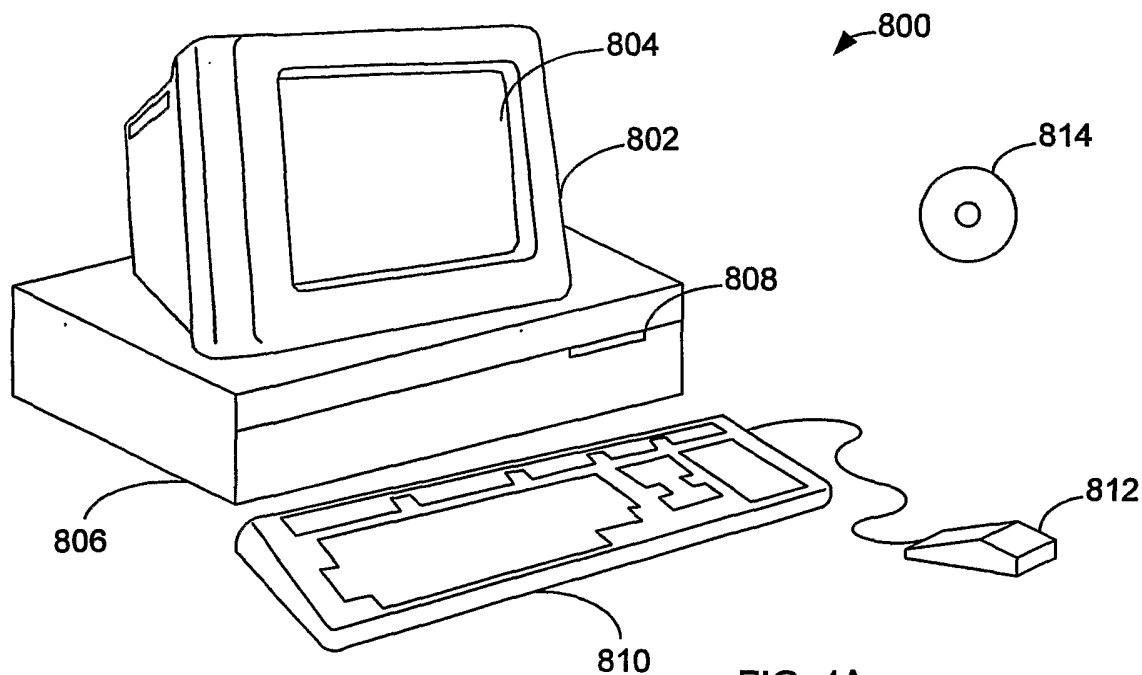


FIG. 3



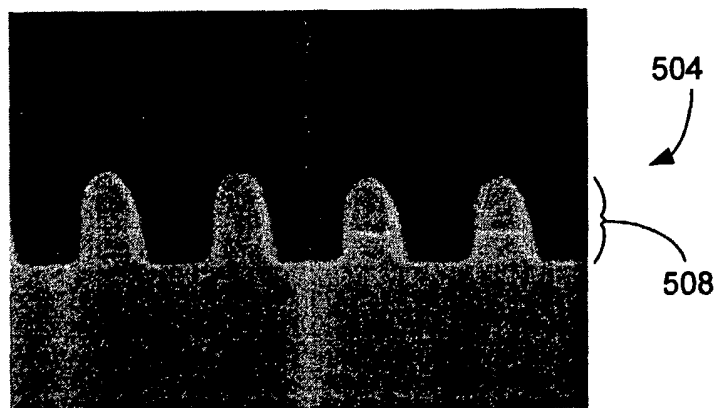


FIG. 5A

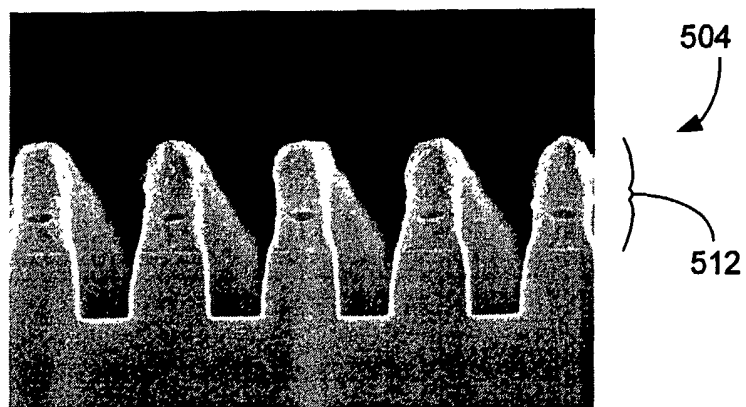


FIG. 5B

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/024905

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/311

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, WPI Data, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2004/003988 A (TOKYO ELECTRON LIMITED; YAMAGUCHI, TOMOYO; FUSE, TAKASHI; FUJIMOTO, KI) 8 January 2004 (2004-01-08) pages 30-36	1-30
X	US 5 310 454 A (OHIWA ET AL) 10 May 1994 (1994-05-10) column 5, line 60 - column 9	1,4,5,7, 8,10-18, 20,21, 23-25, 27-30
X	US 6 265 320 B1 (SHI JIANOU ET AL) 24 July 2001 (2001-07-24) the whole document	1,4, 7-13,15, 16,18, 20, 23-28,30

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

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