

Oct. 21, 1947.

P. J. HERBST

2,429,228

ELECTRONIC COMPUTER

Filed June 11, 1945

4 Sheets-Sheet 1

Fig. 1.

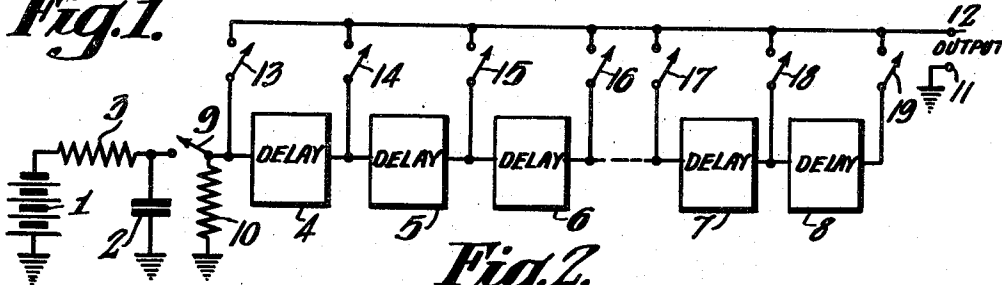


Fig. 2.
MULTIPLIER

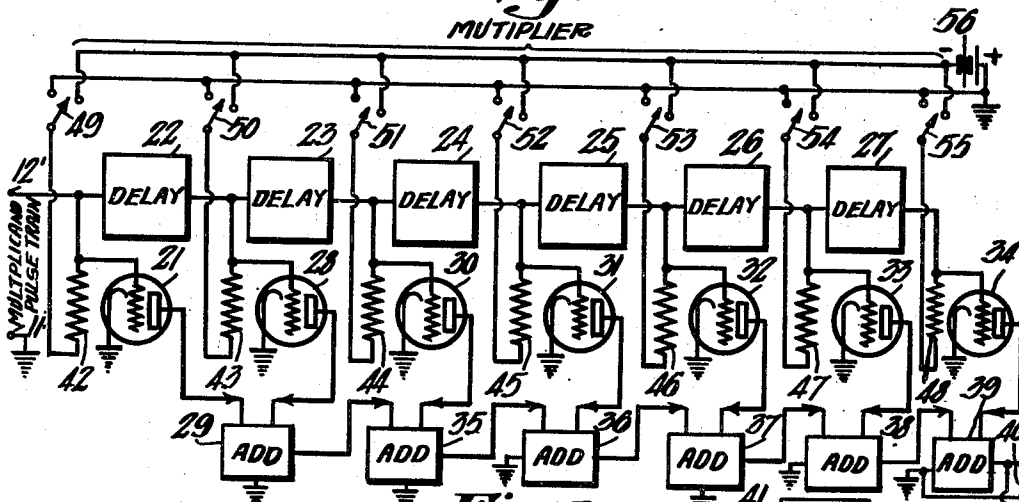
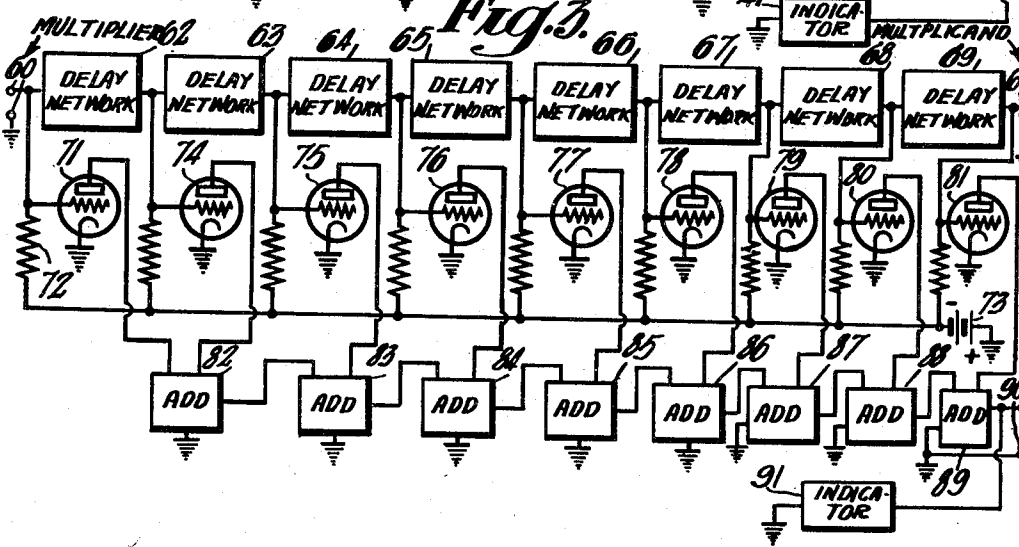


Fig. 3.



Inventor
Philip J. Herbst

CD Pucka
Attorney

Oct. 21, 1947.

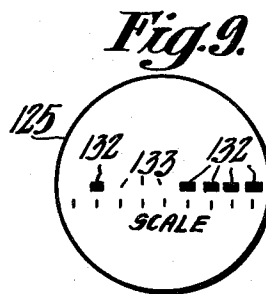
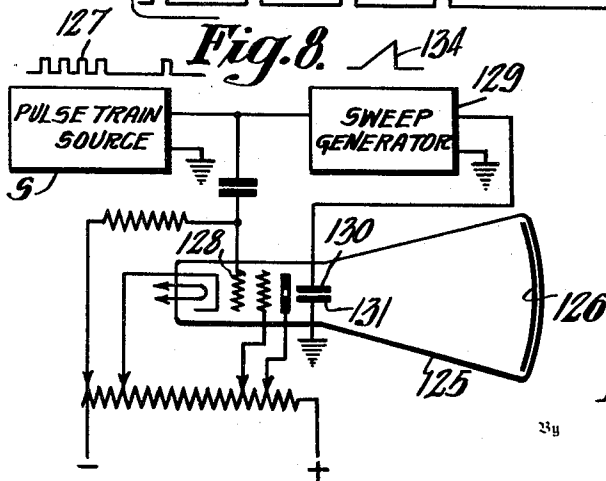
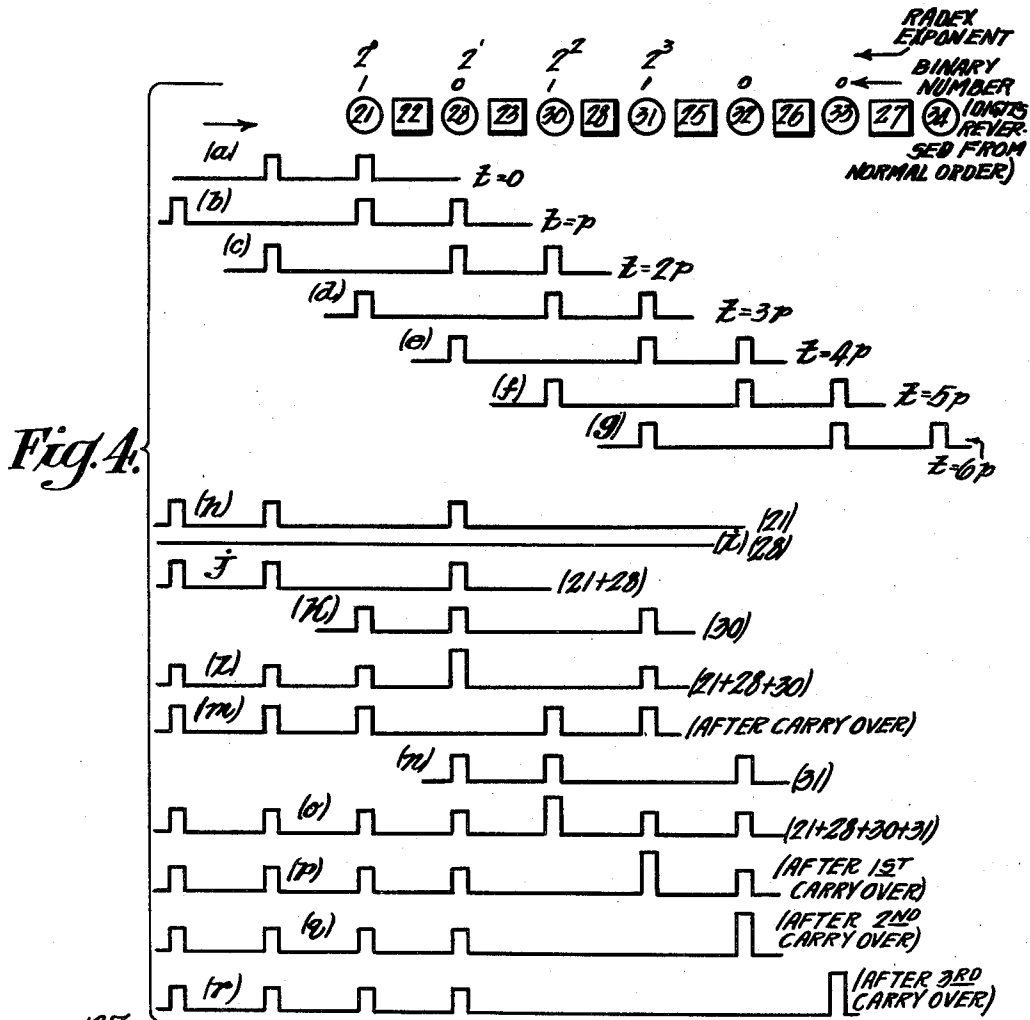
P. J. HERBST

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ELECTRONIC COMPUTER

Filed June 11, 1945

4 Sheets-Sheet 2



Philip J. Herbst ^{Inventor}

CD Puska

Attorney

Oct. 21, 1947.

P. J. HERBST

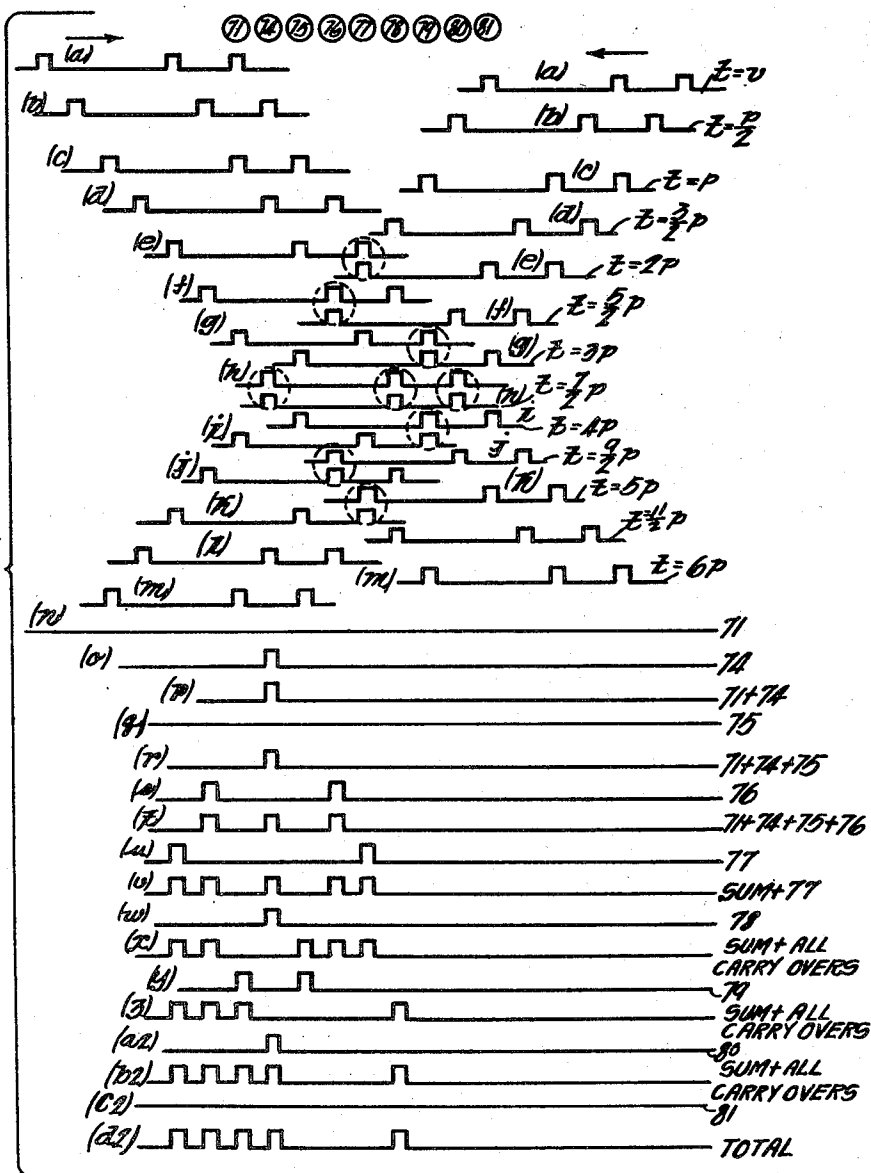
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Filed June 11, 1945

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Fig. 5



Inventor
Philip J. Herbst

By

CD Mucka

Attorney

Oct. 21, 1947.

P. J. HERBST

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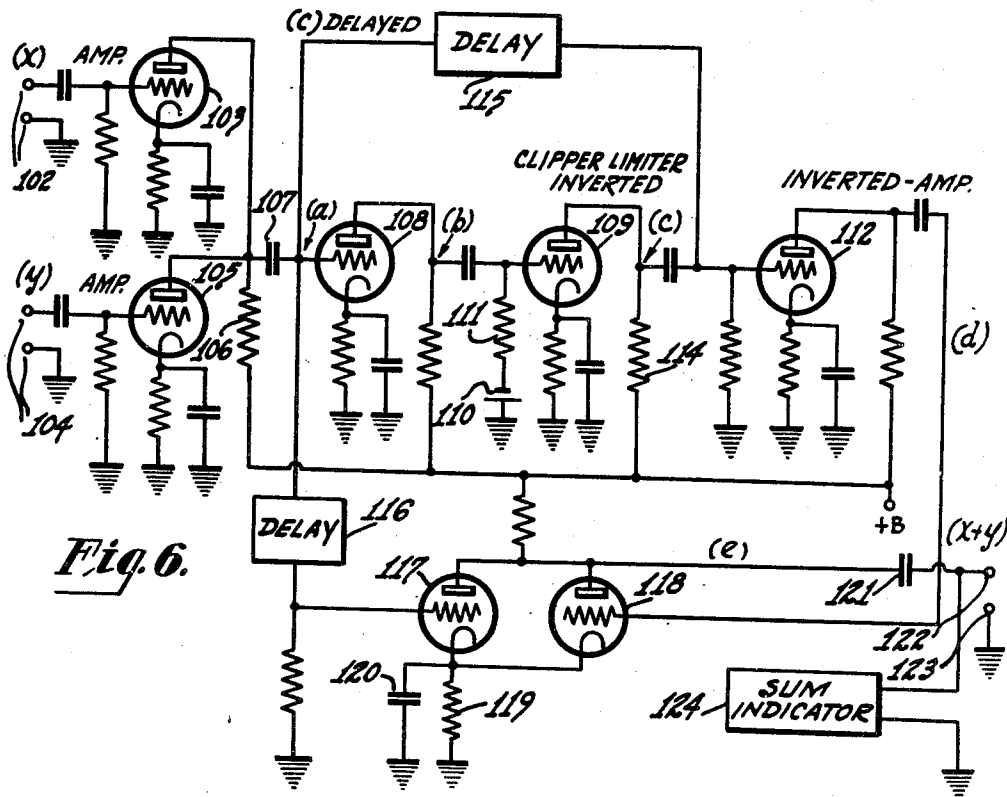


Fig. 6.

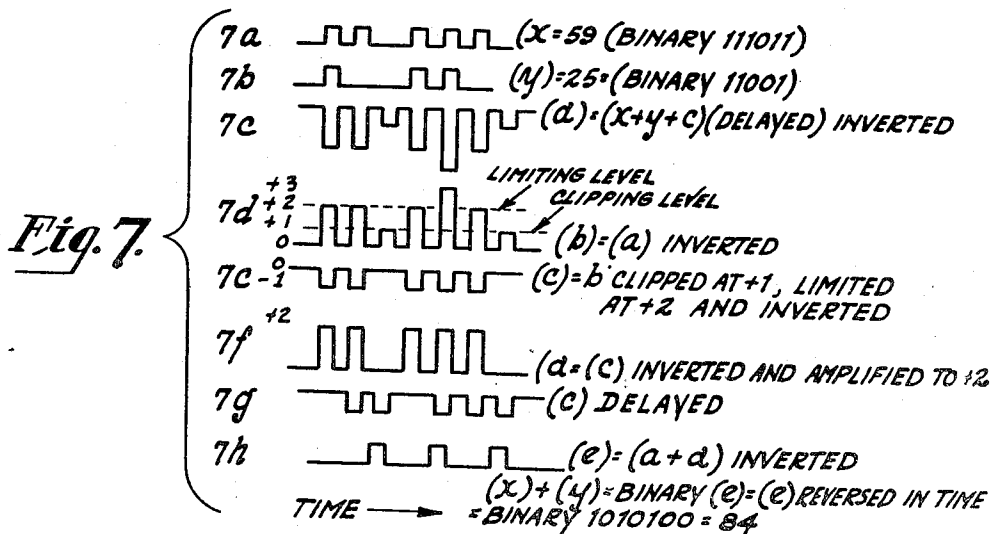


Fig. 7.

INVENTOR
 PHILIP J. HERBST
 BY *C. A. Huska*
 ATTORNEY

UNITED STATES PATENT OFFICE

2,429,228

ELECTRONIC COMPUTER

Philip J. Herbst, Princeton, N. J., assignor to
Radio Corporation of America, a corporation
of Delaware

Application June 11, 1945, Serial No. 598,702

20 Claims. (Cl. 235—61)

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This application is a continuation-in-part of my copending application Serial No. 488,801, filed May 26, 1943, for "Electronic computer."

This invention relates generally to electronic computers and more particularly to an electronic computing system for deriving the product of at least two quantities, each of which are represented by separate groups of voltages characteristic of the binary values of each of the quantities.

The binary system of computation is particularly suited to electronic computation, since a complete binary term of a binary number may be expressed in terms (a) of conducting condition or (b) of the cut-off condition of the anode circuit of a conventional vacuum tube. A saving in the number of tubes required for a given quantity is also possible in a ratio of 3:1 over a numerical system utilizing a radix of 10. Furthermore, binary quantities may be expressed in terms of voltage pulse trains having pulses of unit magnitude which are indicative of the presence of a binary 1 term and the absence of unit magnitude pulses indicative of binary 0 terms. A description of the binary system of computation may be found in "Elementary Number Theory," by Uspenski and Heaslet.

Briefly, the instant invention comprises two distinct methods of deriving the product of two quantities by means of the systems described in detail hereinafter.

First method

The first method comprises generating a pulse train in which unit magnitude pulses bear a time relation indicative of the binary number corresponding to one of the quantities. For example, the binary number 1101 would be represented by a pulse train having two unit magnitude pulses separated by the width of a pulse, followed at an interval of three pulse widths by a third unit magnitude pulse. The pulses will therefore correspond to binary 1 terms and the absence of a pulse between the second and third pulses would correspond to a binary 0 term. The multiplicand would be represented by a pulse train, of the type described, which would be applied to a group of cascaded delay circuits each of which provides a delay equal to the pulse period.

A plurality of blocking amplifiers are connected to the delay circuits in a manner whereby the pulse train applied to successive delay circuits also is applied to the control electrode of a corresponding one of the blocking amplifiers. The respective blocking amplifiers are connected

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to a plurality of switches whereby normal bias, or cut-off bias, may be applied to each of the respective amplifiers. Cut-off bias is applied to an amplifier if a corresponding term of the multiplier is binary 0, while normal bias is applied thereto if the corresponding term of the binary multiplier is binary 1. Therefore, if the binary multiplier is 1001, the first and fourth blocking amplifiers would receive normal bias, while the second and third amplifiers would be biased beyond anode current cut-off.

The amplifiers will therefore be non-conductive except at such times as a pulse of the applied multiplier pulse train is applied to the control electrode of one of the normally biased amplifiers. In the latter instance, the anode circuit of the normally biased amplifier will include a pulse train indicative of the corresponding sub-total of the multiplication process. Sub-total pulse trains derived from the first two blocking amplifiers may be added by means of a pulse train adding circuit of the type described in applicant's copending U. S. application Serial No. 485,308, filed May 1, 1943. Similarly, the output pulse train derived from the first adding circuit is applied to a second similar adding circuit which also receives a sub-total pulse train from the third blocking amplifier. The output pulse train of the second adding circuit is combined with the sub-total output pulse train of the fourth blocking amplifier and applied to a third adding circuit. This process is continued through additional adding circuits until the output pulse trains from all blocking amplifiers have been included in the final total which is derived as a final pulse train in the last of the cascaded adding circuits.

Second method

The second method includes means for generating separate pulse trains indicative of the binary values of each of the quantities to be multiplied. These pulse trains are applied at opposite ends of a group of cascaded delay networks in which each network provides a delay equal to one-half of the pulse period of the pulse trains. A plurality of blocking amplifiers which are normally biased beyond anode current cut-off condition, are respectively connected to the input of each successive delay network. The various blocking amplifiers are arranged to pass no anode current except when unit magnitude pulses from both the multiplier and the multiplicand applied pulse trains coincide in time on the control electrode of the respective amplifiers. The pulse

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trains derived from the anode circuits of each of the blocking amplifiers are combined in pulse train adding circuits of the type disclosed in applicant's copending application mentioned heretofore, in the same manner as described heretofore for applicant's first method of multiplication.

Among the objects of the invention are to provide an improved method of and means for deriving electronically the product of two quantities. Another object of the invention is to provide an improved method of and means for generating voltage pulse trains characteristic of the binary value of one or more quantities and combining said pulse trains to provide an output pulse train characteristic of the binary value of the product of said quantities. Another object of the invention is to provide an improved method of and means for deriving the product of two quantities wherein one of said quantities is represented by a pulse train indicative of the binary value of said quantity, the other of said quantities is represented by different values of bias voltages applied to a plurality of cascaded blocking amplifiers, said pulse train is applied to said amplifiers at successive time intervals, and pulse trains derived from each of said amplifiers are combined to provide an output pulse train indicative of the binary value of the product of said quantities.

An additional object of the invention is to provide an improved method of and means for generating separate pulse trains indicative of the binary values of two quantities, delaying each of said pulse trains, combining said pulse trains to derive sub-total pulse trains and combining said sub-total pulse trains to derive an output pulse train which is indicative of the binary value of the product of said quantities. An additional object of the invention is to provide an improved method of and means for deriving electronically the product of two quantities which are represented by separate groups of voltages indicative of the binary values of said quantities, deriving an output pulse train indicative of the product of said quantities and indicating said product.

The invention will be described in further detail by reference to the accompanying drawings of which Figure 1 is a schematic circuit diagram of a pulse train generator; Figure 2 is a schematic circuit diagram of one embodiment of applicant's multiplying system; Figure 3 is a schematic circuit diagram of a second embodiment of applicant's multiplying system; Figure 4 is a family of graphs indicating the circuit operation of Figure 2; Figure 5 is a family of graphs indicating the circuit operation of Figure 3; Figure 6 is a schematic circuit diagram of the adding circuit forming a component of the circuits of both Figure 2 and Figure 3; Figure 7 is a family of graphs indicative of the circuit operation of Figure 6; Figure 8 is a schematic circuit diagram of a binary indicator; and Figure 9 is an elevational view of the type of indication provided thereby on a cathode ray oscilloscope. Similar reference numerals are applied to similar elements throughout the drawing.

Apparatus for first multiplier method

Referring to Figure 1, a pulse train generator, for deriving pulse trains indicative of a particular quantity to be multiplied, includes a source of voltage such as, for example, a battery 1, which is connected to a capacitor 2 through a series resistor 3 in such a manner that a capacitor

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2 is normally charged by the voltage source 1. A plurality of delay circuits 4, 5, 6, 7, 8 are connected in cascade arrangement. The first delay circuit 4 is connected through a first switch 9 to the common terminals of the capacitor 2 and the resistor 3. The input of the first delay circuit 4 is also connected, through a second resistor 10, to the common grounded terminals of the battery 1 and the capacitor 2. One output terminal 11 is grounded, and a second output terminal 12 is connected to the input and output circuits of the various delay networks through separate output switches 13, 14, 15, 16, 17, 18 and 19, respectively.

In operation, if a pulse train corresponding to the number 1101 is desired, the switches 13, 15 and 16 are closed. When the switch 9 is closed, a single pulse train having the desired characteristics may be derived from the output terminals 11, 12, which are connected effectively across the second, or load, resistor 10. If then the switch 9 is opened, the capacitor 2 will again be charged by the voltage source 1. A second voltage pulse train having characteristics determined by the positions of the output switches 13, 14, 15, 16, 17, 18 and 19 may thereafter be derived from the output terminals 11, 12 when the switch 9 is again closed.

In Figure 2 the output pulse train, derived from the circuit of Figure 1, is applied to input terminals 11', 12' which apply the pulses to the control electrode of a first blocking amplifier 21 and to the input of the first of a plurality of serially connected delay circuits 22, 23, 24, 25, 26 and 27. The delay provided by each of the delay circuits is equivalent to the pulse period of the pulse train. The control electrode of a second blocking amplifier 28 is connected to the output of the first delay circuit 22. The anode circuits of the first and second blocking amplifiers 21, 28, respectively, are connected to the input of a first pulse train adding circuit 29, which will be described in detail hereinafter.

Similarly, the output of the second delay circuit 23 is applied to the control electrode of a third blocking amplifier 30, and the outputs of the third, fourth, fifth, and sixth delay circuits 24, 25, 26, 27, respectively, are connected to the control electrodes of the fourth, fifth, sixth, and seventh blocking amplifiers 31, 32, 33 and 34, respectively. The anode circuit of the third blocking amplifier 30 and the output of the first pulse train adding circuit 29 are applied to the input of a second pulse train adding circuit 35. Similarly, the anode circuit of the fourth blocking amplifier 31 and the output of the second pulse train adding circuit 35 are applied to the input of a third pulse train adding circuit 36. The anode circuit of the fifth blocking amplifier 32 and the output of the third adding circuit 36 are applied to the input of a fourth adding circuit 37. Likewise, the anode circuit of the sixth blocking amplifier 33 and the output of the fourth adding circuit 37 are applied to the input of the fifth adding circuit 38. Also, the anode circuit of the seventh blocking amplifier 34 and the output of the fifth adding circuit 38 are applied to the input of the sixth adding circuit 39. The output of the sixth adding circuit 39 is connected to the output terminals 40 from which a pulse train may be derived which is characteristic of the binary number corresponding to the product. An indicator 41, which may be of the type described in the circuit of Figure 6, may

be connected across the output terminals 40, if the product is to be indicated directly.

The control electrode circuits of the blocking amplifiers 21, 28, 30, 31, 32, 33 and 34 are connected to grid resistors 42, 43, 44, 45, 46, 47 and 48, respectively. The remaining terminals of the grid resistors are each connected to the movable contacts of one of a plurality of bias control switches 49, 50, 51, 52, 53, 54 and 55, respectively. One of the fixed contacts of each of the bias control switches is grounded, and the remaining fixed contacts of these switches are connected to the negative terminal of a source of bias voltage, 56. The positive terminal of the source of bias voltage is grounded. The cathodes of all of the blocking amplifiers also are grounded.

Mode of operation—Method I

The pulse train applied to the input terminals 11', 12' is indicative of the value of the binary number corresponding to the multiplicand. The position of the bias control switches 49, 50, 51, 52, 53, 54 and 55 is indicative of the value of the binary number corresponding to the multiplier. For example, if the multiplier is the binary number 1011, switches 49, 50, and 52 (because the switches are set up from right to left) will be connected to the grounded contact, and switches 51, 53, 54 and 55 will be connected to the contacts which are at negative potential derived from the voltage source 56. The value of this negative potential is selected to provide anode current cut-off of all blocking amplifier tubes to which it is applied. It should be understood that the number of delay circuits, blocking amplifiers and adding circuits required will depend upon the number of binary digits in the numbers to be multiplied.

In operation, the multiplicand pulse train applied to the input terminals 11', 12' will provide anode current only in the blocking amplifiers 21, 28, 31, of which the bias control switches 49, 50, 52 are at ground potential. The pulse train in the output of these normally biased amplifiers will be of magnitude proportional to the magnitude of the applied pulse train and the time relation thereof will be dependent upon the total delay provided by the delay circuits intermediate the input terminals and the particular tube control electrode. The voltage pulse trains in the anode circuits of the respective blocking amplifiers will be combined or added in the adding circuits as described in detail hereinafter. It will be seen that only two pulse trains are applied to each adding circuit, and that these pulse trains are derived from either two blocking amplifier anode circuits, or from one anode circuit and a preceding pulse train adding circuit.

Example: Product of 13×11 (binary $1101 \times$ binary 1011)

Figure 4 is a family of graphs indicating the progress of the applied pulse train through the several blocking amplifiers, delay circuits and adding circuits described herein for the circuit of Figure 2. It is assumed that the switches 49, 51 and 52 are connected to the grounded contacts thereof, so that the blocking amplifiers 21, 30 and 31 are supplied with normal grid bias. Therefore, the blocking amplifiers 28, 32, 33 and 34 would be biased by the voltage from the source 56 and would not be responsive to the pulse train.

Graph (a) shows the first pulse of the pulse

train actuating the first blocking amplifier 21. Graph (b) shows the pulse train at a later interval of one pulse period reaching the second blocking amplifier 28. Graph (c) shows the pulse train after an interval of two pulse periods reaching the third blocking amplifier 30. Graph (d) shows the first pulse of the pulse train reaching the fourth blocking amplifier 31, and graphs (e), (f), and (g) show the progress of the pulse train through the remaining blocking amplifiers.

Graph (h) shows the pulse train transmitted by the normally-biased first blocking amplifier 21. Graph i illustrates the fact that no pulse train is transmitted by the overbiased second blocking amplifier 28. Graph j illustrates the combined pulse train derived from the first adding circuit 29, which pulse train is equivalent to the sum of the pulse trains shown in graphs h and i. Graph k shows the pulse train derived from the third blocking amplifier 30. Graph l shows the combined pulse train in the second adding circuit 35 which is equivalent to the sum of the pulse trains derived from the third blocking amplifier and the first adding circuit 29. Graph m is the pulse train derived from the output of the second adding circuit 35 after the carryover of the double magnitude pulse in graph l.

Graph n is the pulse train derived from the fourth blocking amplifier tube 31. Graph o is the pulse train in the third adding circuit 36 which is equivalent to the sum of the pulse trains derived from the fourth amplifier 31 and the second adding circuit 35. Graph p is equivalent to graph o after the first carryover of the double amplitude pulse in graph o. Graph q is equivalent to graph p after the carryover of the double amplitude pulse in graph p; and graph r is equivalent to graph q after the carryover of the double amplitude pulse of graph q.

Since the fifth, sixth and seventh blocking amplifiers 32, 33, 34 do not transmit the pulse train, the pulse train represented by graph r is merely repeated through the fourth, fifth and sixth adding circuits 37, 38, 39. It may be derived from the output terminals 40, or indicated on the indicator 41. The time relation is indicated by the scale below graph r, and the equivalent binary number 10001111, corresponding to the product, may be derived by reading the pulse train r on a reversed time scale; i. e., from right to left.

Apparatus for second multiplier method

Figure 3, comprising the circuit required for performing applicant's second method, includes a first pair of input terminals 60, to which are applied a pulse train characteristic of one of the quantities to be multiplied. The circuit also includes a second pair of input terminals 61 to which are applied, simultaneously with the application of the first pulse train to the terminals 60, a second pulse train characteristic of the binary value of the second number to be multiplied. The simultaneous application of both pulse trains may be effected by ganging the control switches 9 of the two pulse generating circuits of the type described in Fig. 1. A plurality of delay networks 62, 63, 64, 65, 66, 67, 68, 69, each providing a delay equal to one half the pulse period of the applied pulse trains, are connected in series between the pulse train input terminals 60, 61. The control electrode circuit of a first blocking amplifier tube 71 is connected to the input terminals 60, and also is connected through a control electrode bias resistor 72 to the negative terminals

of a source of bias potential 73. The positive terminal of the source of bias potential 73 is grounded, and the value of the bias voltage is selected to provide anode current cut-off in the absence of the coincidence of applied voltage pulses of both of the pulse trains.

Similarly, the control electrode of a second blocking amplifier tube 74 is connected to the output of the first delay network 62, the control electrode of a third blocking amplifier 75 is connected to the output of the second delay network 63, and the control electrodes of fourth, fifth, sixth, seventh and eighth blocking amplifiers 76, 77, 78, 79, 80, respectively, are connected to the output of the third, fourth, fifth, sixth and seventh delay networks 64, 65, 66, 67, and 68, respectively. The control electrode of the ninth blocking amplifier 81 is connected to the ungrounded terminal 61 of the eighth delay network 69. Similarly, the control electrodes of the blocking amplifiers 76, 77, 78, 79, 80, and 81 are connected through separate grid resistors to the negative terminal of the source of bias potential 73. The cathodes of all of the blocking amplifiers are grounded.

The anode circuits of the first and second blocking amplifiers 71, 74 are connected to the input of a first pulse train adding circuit 82. The output of the first pulse train adding circuit 82, and the anode circuit of the third blocking amplifier 75 are connected to the input of a second pulse train adding circuit 83. The output of the second pulse train adding circuit 83 and the anode circuit of the fourth blocking amplifier 76 are connected to the input of a third pulse train adding circuit 84. Similarly, the output of the third pulse train adding circuit 84 and the anode circuit of the fifth blocking amplifier 77 are applied to the input of a fourth pulse train adding circuit 85. Also, the output of the adding circuit 85 and the anode circuit of the tube 78 are applied to the input of a fifth pulse train adding circuit 86. The output of the adding circuit 86 and the anode circuit of the tube 79 are applied to the input of a sixth pulse train adding circuit 87. The output of the sixth adding circuit 87 and the anode circuit of the eighth blocking amplifier tube 80 are applied to the input of a seventh pulse train adding circuit 88. Similarly, the output of the seventh adding circuit 88 and the anode circuit of the last amplifier tube 81 are applied to the input of an eighth pulse train adding circuit 89. The output of the last pulse train adding circuit 89 is applied to the output terminals 90, to derive therefrom an output pulse train which is characteristic of the binary number corresponding to the product of the two quantities to be multiplied. An indicator 91 may be connected across the output terminals 90 if the product is to be indicated directly. The pulse train adding circuits 82, 83, 84, 85, 86, 87, 88 and 89, and the indicator 91 are each of the types described in detail hereinafter in the circuit of Figure 6. It should be understood that the number of delay networks, blocking amplifiers and adding circuits will depend upon the number of binary digits of the numbers to be multiplied. In practice there necessarily will be one more blocking amplifier than delay network in order to combine fully delayed pulse trains traveling in both directions.

Mode of operation—Method II

In operation, a pulse train corresponding to the binary multiplicand is applied to the input

terminals 60, while simultaneously a pulse train corresponding to the binary multiplier is applied to the other input terminals 61. The two pulse trains are each delayed intervals equivalent to one half the pulse period as they progress in opposite directions through each of the delay networks. When pulses in both trains coincide in time at the input of any of the blocking amplifiers, the particular amplifier provides a unit magnitude pulse in its output circuit, which unit pulse is applied to the particular pulse train adding circuit connected thereto.

The several pulse train adding circuits 82, 83, 84, 85, 86, 87, 88 and 89 are so connected in series and to the separate blocking amplifiers that the proper time relations and carryovers are maintained for the unit pulses transmitted thereto by the several blocking amplifiers. The resultant pulse train derived from the output circuit of the last adding circuit 89 corresponds in magnitude and time relation to the value of the binary product.

Example: Product of 13×11 (binary 1101×binary 1011)

Figure 5 is illustrative of the progress of the two pulse trains applied respectively to the input terminals 60 and 61 of the circuit of Figure 3. The position of the blocking amplifiers and delay circuits are indicated by the numbered circles and squares, respectively, at the upper portion of the family of graphs. The time intervals are indicated on the right hand margin of the family of graphs. The pulse train applied to the input terminals 60 is read as a binary number from left to right, while the pulse train applied to the input terminals 61 is read as a binary number from right to left.

Graph *a* illustrates the two pulse trains applied simultaneously to the end blocking amplifiers 71, 81, respectively. Graph *b* illustrates the progress of the two pulse trains to the amplifiers 74, 80, respectively at a time delay of one half the pulse period. Graphs *c*, *d*, *e*, *f*, *g*, *h*, *i*, *j*, *k*, *l*, and *m* indicate successive progress of the two pulse trains toward the opposite ends of the bank of blocking amplifiers. The successive graphs indicate conditions at time intervals of one half the pulse period. The encircled pulses of the graphs *e*, *f*, *g*, *h*, *i*, *j* and *k* indicate the coincidence of pulses in a particular blocking amplifier whereby the amplifier is caused to transmit a pulse to the adding circuit connected thereto.

Graph *n* indicates that no pulses are transmitted by the first blocking amplifier 71. Graph *o* indicates that a single pulse is transmitted by the second blocking amplifier 74 at a time interval of 7/2 the pulse period. Graph *p* indicates the pulse derived from the first adding circuit 82 in response to the single pulse derived from the blocking amplifiers 71 and 74. Graph *q* indicates that no pulses are derived from the third blocking amplifier 75. Graph *r* indicates the single pulse which is therefore transmitted by the second adding circuit 83 in response to the single pulse applied thereto from the first adding circuit 82.

Graph *s* indicates the two pulses derived from the fourth blocking amplifier 76. Graph *t* indicates the three pulses derived from the third adding circuit 84 in response to the two pulses from the fourth amplifier 76 and the single pulse from the second adding circuit 83.

Graph *u* indicates the two pulses derived from the fifth blocking amplifier 77, while graph *v* indi-

ates the five pulses derived from the fourth adding circuit 85 in response to the two pulses from the fifth amplifier 77 and the three pulses from the third adding circuit 84.

Graph *w* indicates the single pulse derived from the sixth blocking amplifier 78 while graph *x* indicates the output pulse train from the fifth adding circuit 86 in response to the pulse trains *v* and *w* applied thereto. It will be seen that the coincidence of two pulses in the graphs *v* and *w* has provided a carryover to the next pulse period.

Graph *y* indicates the two pulses derived from the seventh blocking amplifier 79 while graph *z* indicates the pulse train derived from the sixth adding circuit 87 in response to the applied pulse trains *x* and *y*. It will be seen that three successive carryovers occurred in the adding circuit 87.

Graph *a2* indicates the single pulse derived from the eighth blocking amplifier 80, while graph *b2* indicates the pulse train derived from the seventh adding circuit 88 in response to applied pulse trains represented by the graphs *z* and *a2*.

Graph *c2* indicates that no pulses are transmitted by the last blocking amplifier 81 while graph *d2* indicates the output pulse train derived from the last adding circuit 89 which is identical to that derived from the seventh adding circuit 88. The output pulse train may be derived from the output terminals 90 or indicated on the indicator 91. It corresponds to the binary number 10001111 represented by the pulse train represented by graph *d2* on a reversed time scale—i. e., reading from right to left.

These various steps are set forth in the following tabulation wherein the first column shows the reference numerals of the various tubes, the second column shows the times at which these tubes conduct, the third column shows the output pulses, and the fourth column shows the carry pulses:

Tube	Time	Output	Carry
77	2	1	-----
78	2½	1	-----
79	3	1	-----
74	3½	1	-----
78	3½		-----
80	3½		1
79	4		1
78	4½	0	1
77	5	0	1
	5½	1	-----

Method of adding pulses

The principle employed is the summation of the pulses representing the numbers to be added, the generation of a control pulse train having pulses whenever the pulse train representing the summation exceeds the amplitude of one pulse and in which the amplitudes of the pulses in the control train are all of the same magnitude, the delay of this control train by a time equal to the interval between pulses in the train. The addition of this delayed train to the input so as to represent the carryover from one digit to the next and the subtraction of the undelayed control train from the total sum to accomplish the cancellation of pulses of double magnitude.

Briefly, the system comprises an improved method and means for adding the magnitudes of the voltage pulses of each of the input pulse trains to derive therefrom a combined pulse train. To the combined pulse train is added a delayed pulse train representing the carryover counts in the binary addition to derive a first control pulse train representing the binary sum but not in prop-

er form for normal use. The first control pulse train may contain pulses of zero, unity, double or triple amplitude. The method employed consists in utilizing these amplitudes to produce a pulse train representing the binary sum in correct form as follows: Amplitudes of unity produce a count in the output pulse train but introduce no carryover pulse in the circuit, double amplitudes produce a carryover pulse but no count in the output train, pulses of triple amplitude produce both carryover and count pulses. To accomplish this the first control pulse train is clipped at unit amplitude and limited at double amplitude to derive a second control pulse train which represents the carryover pulses used which is delayed and added to the combined pulse train as previously described to produce the first control pulse train. The second control pulse train is amplified to derive a third control pulse train of double amplitude. The third control pulse train is combined in opposing polarity with the first control pulse train to derive a fourth pulse train which is characteristic of the sum of the binary numbers to be added. The fourth pulse train may be applied to additional computing apparatus or the sum may be indicated directly.

The two pulse trains to be added are impressed upon the input of a thermionic tube circuit having a common load, to derive therefrom the first combined pulse train. The combined pulse train is applied to the grid of a conventional amplifier stage to which the delayed pulse train representing the carryover operation is also applied. The output of this stage constitutes the first control pulse train and is applied to a clipping-limiting stage, the output of which consists only of pulses of unit magnitude occurring whenever the magnitude of the pulses in the first control pulse train exceed unity and comprising the second control pulse train. This second control pulse train is applied to a conventional delay circuit which delays its pulses an amount equal to the time interval between pulses. The delayed pulses are combined with the combined pulse train to derive the first control pulse train as previously described. The second control pulse train is also applied to a conventional amplifier to derive a third control pulse train of double amplitude. The first and third control pulse trains are applied to the inputs of a summing stage. Since the pulses are applied in opposing polarity the pulses of the third control pulse train will tend to cancel those of the first control pulse train. However, for amplitudes of zero or unit magnitude in the first control pulse train, no pulses are present in the third, while for pulses of triple magnitude in the first, the presence of the double amplitude pulse in the third control train produces a partial cancellation which results in a pulse of unit amplitude in the output. When the pulse in the first control train is of double amplitude the cancellation is complete. The output of the summing stage is the fourth pulse train and represents the binary sum.

Apparatus for adding pulses

Referring to Figure 6 of the drawing, a voltage pulse train *x*, illustrated by Fig. 7a, corresponding to the number 59 expressed in terms of the binary number 111011, is applied to the input terminals 102 which are connected to the input of a first amplifier tube 103. A voltage pulse train *y*, corresponding to the quantity 25 in terms of the corresponding binary number 11001, is applied to a second group of input terminals 104 which are connected to the input of a second amplifier tube

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105. The anode circuits of the first and second amplifier tubes 103, 105, respectively, include a common load resistor 106 which is connected to a source of operating potential (not shown). The anodes of the amplifier tubes 103, 105 are connected, through an isolating capacitor, 107, to the control electrode of an amplifier tube 108, which inverts the polarity of the combined pulse train derived from the amplifier tubes 103, 105 and the output of the delay network 115. The output of the amplifier tube 108 is applied to the control electrode of a first limiter-inverter tube 109. The control electrode bias potential of tube 109 is selected so as to provide a threshold which will permit pulses of double and triple amplitude impressed on the input to produce an output in the plate circuit but discriminates against pulses of unit amplitude. The plate circuit of tube 109 is chosen so as to limit the amplitude of the pulses in the output to a fixed amplitude for all input pulses of double amplitude or greater. Figs. 3 and 4 of applicants' copending application Ser. No. 598,701 show the mutual characteristic of tube 109 and illustrate the clipping and limiting action of this tube. The plate current limiting is realized by employing a very high resistance 114 in the plate circuit. Other methods, such as reducing the applied plate voltage could be used.

The control electrode bias potential may be derived from a battery 110 connected, through a grid resistor 111, to the control electrode of the limiter-clipper-inverter tube 109. As an added refinement to accommodate wide variation in pulse rate without shifting of the location of the pulse peaks on the mutual characteristic, a means of maintaining the base line of the input pulses may be employed. This means may take the form of a rectifier or similar "locking circuit." One form of this circuit is shown in Fig. 7 of the above copending application which has the same filing date as the present application. This refinement is not essential if the pulse width is small compared to the spacing or if the width of the mutual characteristic is small compared to the pulse amplitude, i. e., if the shift in the A.-C. axis of the pulse train is not sufficient to cause a change in the limiting clipping action of tube 109. The output of tube 109 represents the carryover count in the binary addition and will henceforth be designated as the second control pulse train c.

The second control pulse train c is applied to the control electrode of an inverter amplifier tube 112. This amplification of this tube is established by selection of the values of its associated circuit components so that the pulse train in its output signal has a constant magnitude of double amplitude. This may be further insured by providing limiter-clipper action similar to tube 109 but is not essential to the fundamental operation of the circuit. The output of tube 112 represents the cancellation terms in the binary addition and will henceforth be designated as the third control pulse train d.

The second control pulse train c also is applied, through a conventional delay circuit 115, to the control electrode of the first inverter tube 108. The delay provided in the delay circuit 115 corresponds to the period of the pulses of the applied voltage pulse trains. The resultant pulse train applied to the control electrode of the first inverter tube 108 will, therefore, represent the sum of the applied pulse trains and the delayed second control pulse train, and will hereinafter be designated as the first control pulse train a.

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The first control pulse train a is applied to a delay circuit 116, which delays the pulse train an amount equivalent to the total delay in the circuits associated with the inverter and limiter tubes 108, 109 and 112. The output of the delay circuit 116 is applied to the control electrode of a triode 117. The third control pulse train d is applied to the control electrode of a triode 118. The triodes 117, 118, respectively, include common cathode and anode circuits and are self-biased by means of a cathode resistor 119 and cathode bypass capacitor 120 connected between the cathodes and ground. Any excessive delay which would tend to unduly separate the occurrence of pulses can be compensated by the addition of such delay in the delay networks between the separate addition circuits. Network 116 is merely a corrective measure taken to insure the proper coincidence of pulses applied to the grids of tubes 117 and 118. The anodes of the triodes 117, 118 are connected through an output capacitor 121 to an output terminal 122. The other output terminal 123 may be connected to ground or any suitable indicator 124, for indicating the binary number corresponding to the sum of the applied quantities x, y may be connected to the terminals 122—123.

The indicator 124, for example, may comprise, as shown in Figs. 8 and 9, a conventional oscilloscope tube 125, the beam of which is normally blanked off and normally deflected just off the fluorescent screen 126. The pulse train 127 to be indicated is derived from a source S such as the circuit of Fig. 6, and is applied to the tube control grid 128 to unblock the cathode ray at each occurrence of a positive pulse characteristic of a binary 1 term. The initial pulse is applied to key a conventional sweep voltage generator 129 to provide a relatively slower sweep voltage which may be applied to the tube deflection elements 130, 131 to sweep the ray across the fluorescent screen 126. The sweep voltage preferably should be of saw-tooth wave form 134 and the fluorescent screen 126 should be of the type providing sustained fluorescence. The indications on the fluorescent screen will be in the form of luminous dashes 132 separated by relatively wide dark spaces 133 corresponding to binary 0 terms.

Referring to Fig. 7, the first graph 7a illustrates the pulse train corresponding to the first applied quantity x. Reading from right to left, the pulses of unit amplitude, and the absence of pulses, correspond to the binary number 111011, which equals 59. Graph 7b similarly illustrates the pulse train corresponding to the second applied quantity y. Similarly reading from right to left, this pulse train corresponds to the binary number 11001, which equals 25. Graph 7c illustrates the first control pulse train a which is characteristic of the combined pulse trains x+y+c delayed. The c delayed pulse train, shown at 7g, is characteristic of carryover pulses occurring whenever two or more unit pulses occur coincidentally.

Graph 7d shows the pulse train b derived from the output of the first inverted tube 108, which is equivalent to the first control pulse train a inverted in polarity. Graph 7e represents the second control pulse train c, which is equivalent to the pulse train b clipped at an amplitude of +1 and limited at an amplitude +2, and inverted in polarity. Graph 7f illustrates the third control pulse train d derived from the output of the inverted tube 112, which is equivalent to double the amplitude of the second control pulse

train *c* clipped at a magnitude of binary 1 and inverted in polarity. Pulses occur in the pulse train *d* only when two or more pulses coincide in the first control pulse train *a*. Since the *a* pulse train has been triple inverted, the *d* pulse train will be of opposite polarity thereto. When combined, in the tubes 117, 118, the *d* pulse train will subtract double amplitude pulses from all double or triple amplitude pulses occurring in the *a* pulse train. Graph 7*g* illustrates the delayed second pulse train *c*.

Graph 7*h* represents the output pulse train *e* characteristic of the binary sum to be derived, and is equivalent to the combined, relatively delayed control pulse trains *a* + *d* inverted in polarity. Reading still from right to left, the graph 7*h* indicates a pulse train corresponding to the binary number 1010100, which equals the sum 84.

Thus the invention described comprises two methods of and means for deriving the product of two quantities represented by groups of voltages or pulse trains, or combinations thereof, corresponding to the values of the binary numbers representative of each of said quantities. The product may be derived in the form of pulse trains in which the pulses have magnitudes and time relations corresponding to the binary number representing said product.

I claim as my invention:

1. An electronic computer for deriving the product of two quantities represented by groups of voltages each of said groups being characteristic in magnitude and time relation of the binary values of different ones of said quantities including a plurality of thermionic tubes, means normally biasing all of said tubes to at least anode current cut-off condition, means for applying said voltage groups to each of said tubes in predetermined time relation to provide anode current in each of said tubes upon coincidence of predetermined magnitudes and time relations of the voltages of both of said groups, and means for deriving from said tube anode currents a voltage pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

2. The method of deriving electronically the product of two quantities comprising deriving separate voltage groups characteristic in magnitude and time relation of the binary values of each of said quantities, combining said voltage groups in predetermined time relation, deriving in response to said combined voltage groups currents characteristic of the coincidence of voltages of both of said groups, and deriving from said currents a voltage pulse train having pulses characteristic in time relation and magnitude of the binary value of said product.

3. An electronic computer for deriving the product of two quantities including means for deriving a voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of one of said quantities, a plurality of thermionic tubes, means for biasing different ones of said tubes in accordance with the values of different binary terms of the second of said quantities, means for applying said voltage pulse train to all of said tubes in predetermined time relation to provide anode current in each of said tubes upon coincidence of voltage pulses and predetermined tube bias voltages, and means for deriving from said anode currents a second voltage pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

4. Apparatus of the type described in claim 1 including means responsive to said pulse train for indicating the value of said product.

5. The method described in claim 2 including the step of indicating responsive to said pulse train the value of said product.

6. Apparatus of the type described in claim 3 including means responsive to said second pulse train for indicating the value of said product.

7. An electronic computer for deriving the product of two quantities represented by groups of voltages each of said groups being characteristic in magnitude and time relation of the binary values of different tones of said quantities including a plurality of thermionic tubes, means normally biasing all of said tubes to at least anode current cut-off condition, means including delay means for applying said voltage groups to each of said tubes in predetermined time relation to provide anode current in each of said tubes upon coincidence of predetermined magnitudes and time relations of the voltages of both of said groups, and means for deriving from said tube anode currents a voltage pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

8. An electronic computer for deriving the product of two quantities including means for deriving a voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of one of said quantities, a plurality of thermionic tubes, means for biasing different ones of said tubes in accordance with the values of different binary terms of the second of said quantities, means including delay means for applying said voltage pulse train to all of said tubes in predetermined time relation to provide anode current in each of said tubes upon coincidence of voltage pulses and predetermined tube bias voltages, and means for deriving from said anode currents a second voltage pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

9. An electronic computer for deriving the product of two quantities including means for deriving a first voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of one of said quantities, means for deriving a second voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of the other of said quantities, a plurality of thermionic tubes, means normally biasing all of said tubes to at least anode current cut-off condition, means for simultaneously applying said first and said second pulse trains in predetermined time relation to each of said normally biased tubes to provide anode current therein upon coincidence of predetermined magnitudes and time relations of the pulses of both of said applied pulse trains, and means responsive to the anode currents in said tubes for deriving a third pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

10. Apparatus of the type described in claim 9 including means responsive to said third pulse train for indicating the value of said product.

11. An electronic computer for deriving the product of two quantities including means for deriving a first voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of one of said quantities, means for deriving a second voltage pulse train having pulses characteristic in magnitude and time re-

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lation of the binary terms of the other of said quantities, a plurality of thermionic tubes, means normally biasing all of said tubes to at least anode current cut-off condition, a plurality of cascaded delay circuits each having a period equivalent to one-half the pulse interval of said pulse trains, means including said delay circuits for simultaneously applying said first and said second pulse trains in predetermined time relation to each of said normally biased tubes to provide anode current therein upon coincidence of predetermined magnitudes and time relations of the pulses of both of said applied pulse trains, and means responsive to the anode currents in said tubes for deriving a third pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

12. Apparatus of the type described in claim 11 including means responsive to said third pulse train for indicating the value of said product.

13. An electronic computer for deriving the product of two quantities including means for deriving a voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of one of said quantities, a plurality of thermionic tubes, means for biasing different ones of said tubes in accordance with the values of different binary terms of the second of said quantities, a plurality of cascaded delay circuits each having a period equivalent to the pulse interval of said pulse train, means including said delay circuits for applying said voltage pulse train to all of said tubes in predetermined time relation to provide anode current in each of said tubes upon coincidence of voltage pulses and predetermined tube bias voltages, and means for deriving from said anode currents a second voltage pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

14. An electronic computer for deriving the product of two quantities including means comprising a voltage discharge circuit including a plurality of delay elements for deriving a voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of one of said quantities, a plurality of thermionic tubes, means for biasing different ones of said tubes in accordance with the values of different binary terms of the second of said quantities, a plurality of cascaded delay circuits each having a period equivalent to the pulse interval of said pulse train, means including said delay circuits for applying said voltage pulse train to all of said tubes in predetermined time relation to provide anode current in each of said tubes upon coincidence of voltage pulses and predetermined tube bias voltages, and means for deriving from said anode currents a second voltage pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

15. An electronic computer for deriving the product of two quantities including means comprising a first voltage discharge circuit including a plurality of delay elements for deriving a first voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of one of said quantities, means comprising a second voltage discharge circuit including a plurality of delay elements for deriving a second voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of the other of said quantities, a plurality of thermionic tubes, means normally biasing all of said tubes to at least anode current cut-off

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condition, a plurality of cascaded delay circuits each having a period equivalent to one-half the pulse interval of said pulse trains, means including said delay circuits for simultaneously applying said first and said second pulse trains in predetermined time relation to each of said normally biased tubes to provide anode current therein upon coincidence of predetermined magnitudes and time relations of the pulses of both of said applied pulse trains, and means responsive to the anode currents in said tubes for deriving a third pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

16. An electronic computer for deriving the product of two quantities represented by groups of voltages each of said groups being characteristic in magnitude and time relation of the binary values of different ones of said quantities including a plurality of thermionic tubes, means normally biasing all of said tubes to at least current cut-off condition, means for applying said voltage groups to each of said tubes in predetermined time relation to provide anode current in each of said tubes upon coincidence of predetermined magnitudes and time relations of the voltages of both of said groups, and means including a plurality of pulse train combining circuits for deriving from said tube anode currents a voltage pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

17. An electronic computer for deriving the product of two quantities including means for deriving a voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of one of said quantities, a plurality of thermionic tubes, means for biasing different ones of said tubes in accordance with the values of different binary terms of the second of said quantities, a plurality of cascaded delay circuits each having a period equivalent to the pulse interval of said pulse train, means including said delay circuits for applying said voltage pulse train to all of said tubes in predetermined time relation to provide anode current in each of said tubes upon coincidence of voltage pulses and predetermined tube bias voltages, and means including a plurality of pulse train combining circuits for deriving from said anode currents a second voltage pulse train having pulses characteristic in magnitude and time relation of the binary value of said product.

18. An electronic computer for deriving the product of two quantities including means for deriving a first voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of one of said quantities, means for deriving a second voltage pulse train having pulses characteristic in magnitude and time relation of the binary terms of the other of said quantities, a plurality of thermionic tubes, means normally biasing all of said tubes to at least anode current cut-off condition, means for simultaneously applying said first and said second pulse trains in predetermined time relation to each of said normally biased tubes to provide anode current therein upon coincidence of predetermined magnitudes and time relations of the pulses of both of said applied pulse trains, and means including a plurality of pulse train combining circuits responsive to the anode currents in said tubes for deriving a third pulse train having pulses characteristic in magnitude in time relation of the binary value of said product.

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19. In a device for deriving the product of two quantities represented by groups of potentials each group of which is representative of the binary value of a different one of said quantities, the combination of a plurality of delay elements connected in series, means for applying said potentials to said delay elements, a plurality of adding circuits connected in series and each having first and second output terminals the first of which is connected to the input terminals of the next successive one of said adding circuits, a plurality of electron discharge devices having their input circuits connected at points each separated by a different one of said delay elements, means connecting the output circuits of the first two of said electron discharge devices to the input terminals of the first of said adding circuits, means connecting the output circuits of successive ones of said electron discharge devices to the second of the input terminals of successive ones of said adding circuits, and means for deriving from said adding circuits a voltage pulse train having pulses which are characteristic in magnitude and time relation of the binary value of said product.

20. In a device for deriving the product of two quantities represented by groups of potentials each group of which is representative of the binary value of a different one of said quantities, the combination of a plurality of delay elements connected in series, means for applying said poten-

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tials to said delay elements, a plurality of adding circuits connected in series and each having first and second output terminals the first of which is connected to the input terminals of the next successive one of said adding circuits, a plurality of electron discharge devices having their input circuits connected at points each separated by a different one of said delay elements, means connecting the output circuits of the first two of said electron discharge devices to the input terminals of the first of said adding circuits, means connecting the output circuits of successive ones of said electron discharge devices to the second of the input terminals of successive ones of said adding circuits, and means for deriving from said adding circuits a voltage pulse train having pulses which are characteristic in magnitude and time relation of the binary value of said product.

PHILIP J. HERBST.

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