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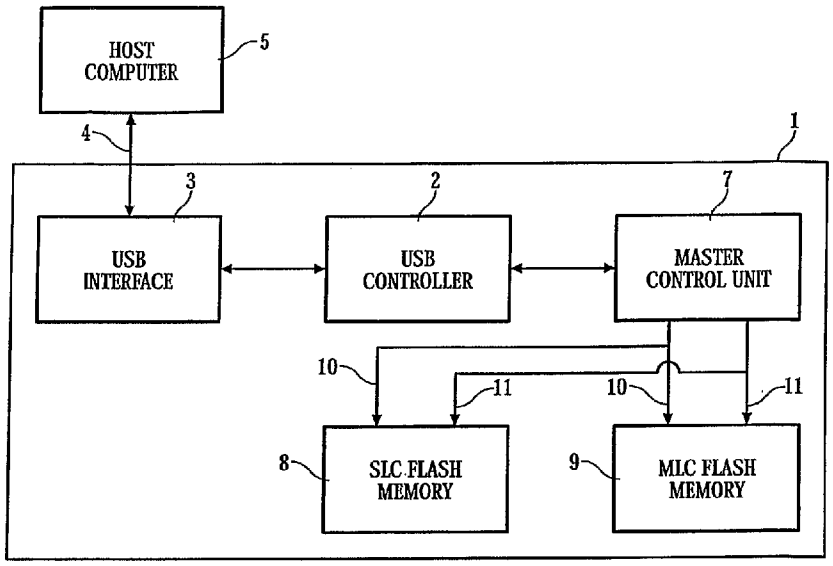
[Continued on next page]

(54) Title: PORTABLE DATA STORAGE USING SLC AND MLC FLASH MEMORY



(57) Abstract: A portable data storage device is disclosed that includes an interface (3) for enabling the portable data storage device to be used for data transfer with a host computer (5), and an interface controller (2) for controlling the interface (3). There is also a master controller (7) for controlling the writing of data to and reading of data from a non-volatile memory (8, 9). The non-volatile memory is at least one single level cell (SLC) flash memory (8) and at least one multiple level cell (MLC) flash memory (9). The at least one single level cell flash memory (8) and at least one multiple level cell flash memory (9) are able to operate simultaneously for improving the speed of operation over onl multiple level cell flash memory.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Portable Data Storage Using SLC and MLC Flash Memory

Reference to Related Patent

Reference is made to our earlier Singapore patent 87,504 dated 21 February 2000 for an invention entitled "A Portable Data Storage Device" (the "earlier patent") the contents of which are hereby incorporated by reference as if disclosed herein.

Field of the Invention

The present invention relates to portable data storage using single layer cell ("SLC") and multiple layer cell ("MLC") flash memory and refers particularly, though not exclusively, to data storage with the simultaneous use of SLC and MLC flash memories to improve the speed of operation.

Background to the Invention

Recently there has been much interest in providing data storage devices containing flash memory and which can be connected to a serial bus of a computer. Such devices are used for data storage, data transfer, media players such as, for example, MP3 players, and so forth. The structure and operation of such a portable storage device may be as shown in the earlier patent. Tradition flash memory is the SLC flash memory. The newer, MLC flash memory has a read and write speed that is much slower than SLC flash memory. Many devices are now including MLC flash memory but the operation of such devices is slower than if only SLC memory was used.

Summary of the Invention

In accordance with a first preferred aspect there is provided a portable data storage device comprising an interface for enabling the portable data storage device to be used for data transfer with a host computer, and an interface controller for controlling the interface. A master controller is provided for controlling the writing of data to and reading data from a non-volatile memory. The non-volatile memory comprises at least one single layer cell flash memory and at least one multiple layer cell flash memory. The at least one single layer cell flash memory and

at least one multiple layer cell flash memory are able to operate simultaneously for improving the speed of operation over only MLC flash memory.

According to a second preferred aspect there is provided a method of processing data on a portable data storage device, the portable data storage device comprising a master controller for controlling a memory, the memory comprising at least one single layer cell flash memory and at least one multiple layer cell flash memory. The method includes using the master controller to control the writing of data to and reading data from a non-volatile memory such that the at least one single layer cell flash memory and at least one multiple layer cell flash memory have data written to and read from them simultaneously.

The may also be at least one data bus operatively connected to the master controller and the at least one single layer cell flash memory and at least one multiple layer cell flash memory for writing data to and reading data from the at least one single layer cell flash memory and at least one multiple layer cell flash memory.

The at least one data bus may be a common data bus for both the at least one single layer cell flash memory and at least one multiple layer cell flash memory. Alternatively, it may be a first data bus operatively connected to the at least one single layer cell flash memory and a second bus operatively connected to the at least one multiple layer cell flash memory. The first data bus may be one of: an upper data bus and a lower data bus, the second data bus being the other of the upper data bus and the lower data bus.

In the first case, the master controller may be for writing data to and reading from the at least one single layer cell flash memory and the at least one multiple layer cell flash memory alternately, the data being in the form of blocks; data being written to and read from the at least one single layer cell flash memory in blocks or pages at a speed that is a multiplication factor higher than those of the at least one multiple layer cell flash memory.

In the second case the master controller may be for writing data to and reading data from the at least one single layer cell flash memory and the at least one multiple layer cell flash memory simultaneously, the data being in a form selected from the group consisting of: blocks, and page. The data may be written to and read from the at least one single layer cell flash memory at a speed a multiplication factor higher than that of the at least one multiple layer cell flash memory.

The multiplication factor may be in the range 5 to 10. Each block of data for the at least one single layer cell flash memory may be 64 pages; and each block of data for the at least one multiple layer cell flash memory may be 128 pages; each page being 2048 bytes.

Brief Description of the Drawings

In order that the invention may be fully understood and readily put into practical effect, there shall now be described by way of non-limitative example only preferred embodiments of the invention, the description being with reference to the accompanying illustrative drawings.

In the drawings:

Figure 1 is a block diagram illustrating the structure of a first embodiment;

Figure 2 is a flow chart for the operation of the first embodiment;

Figure 3 is a block diagram illustrating the structure of a second embodiment; and

Figure 4 is a flow chart for the operation of the second embodiment.

Detailed Description of the Preferred Embodiments

In Figure 1, the portable storage device is within a housing 1. It includes a USB controller 2 which controls a USB interface 3 which connects directly to the serial bus 4 via a USB socket (not shown) of a host computer 5. Data transferred to the USB interface 3 from the host computer 5 passes through the USB controller 2 to a master control unit 7. Data packets are normally of a size that is a multiple of 512 bytes.

The master control unit 7 passes the data packets via a data bus 11 (normally an 8-bit bus) that is common to single layer cell ("SLC") flash memory 8 and multiple layer cell ("MLC") flash memory 9. Command symbols are passed over one or more lines 10 that may be common to the SLC memory 8 and MLC memory 9, as shown. The command symbols passed over lines 10 will normally be ENABLE, ALE, WRITE and READ signals to control both SLC flash memory 8 and MLC flash memory 9.

The ENABLE signal is not sent to both of the memories 8, 9 simultaneously, especially when master control unit 7 is to write data to memory 8, 9, as it enables only one of the memories 8, 9. Enabling is by sending an ENABLE signal to the relevant memory 8 or 9. An ALE signal and WRITE signal are then sent to the respective enabled memory 8 or 9. Master control unit 7 then writes the address data and the data to be stored to the enabled memory 8 or 9 via bus 11.

Only the one of the memories 8 or 9 which is enabled stores the data in the location indicated by address data.

Similarly, when the master control unit 7 is to read data, it enables only one of the memories 8, 9 by using lines 10 to send an ENABLE signal, the ALE signal and READ signal, and the address data using the bus 11.

As the SLC flash memory 8 and MLC flash memory 9 share the same data bus 11, each of the memories 8, 9 has an identical address mapping table which stores the physical address and logical address of the data.

As shown in Figure 2, the master control unit 7 performs READ and WRITE operations on data block basis, and switches between SLC memory 8 and MLC memory 9 by use of control signals via the control signal line 10. For example, during a WRITE operation, the master control unit 7 sends an ENABLE signal to SLC memory 8 over line 10 and then sends a block

of data to the SLC memory 8 over bus 11. The master control unit 7 then sends an ENABLE signal to MLC memory 9 over line 10 then sends a block of data to the MLC memory 9 over bus 11. This process will be repeated until the WRITE operation is finished. The address mapping table for the SLC memory 8 and MLC memory 9 will be updated during each WRITE operation.

Substantially the same procedure will be followed during a READ operation when the master control unit 7 sends an ENABLE signal to each of the memories 8, 9 in turn and in response receives a page of data from the respective memory 8, 9. But the address mapping table will not be updated during a READ operation.

A page of data consists of 2048 bytes. A block of data in SLC memory 8 consists of 64 pages and a block of data in MLC memory 9 consists of 128 pages.

Also, SLC memory 8 has a faster writing (and reading) speed than MLC memory 9 – normally five to ten times faster. Therefore, the master control unit 7 transmits data to the memories 8, 9 depending on the writing speed of the relevant memory 8, 9. For example, if the SLC memory 8 is five times faster than MLC memory 9, in each data transmission the master control unit 7 transmits five times more data to the SLC memory 8 than to the MLC memory 9. In consequence, both memories are able to operate simultaneously even though they are receiving data sequentially. This is due to the different WRITE (and READ) speeds. In this way the amount of data written to each of the memories 8, 9 at each stage of the WRITE cycle is the maximum data it can process in the same time as the other of the memories 8, 9. In that way the WRITE operation is performed at maximum speed, and with minimal delay. It is similar for READ operations.

Figures 3 and 4 show a second embodiment. Common elements with the embodiment of Figures 1and 2 have the same reference numerals.

Here, the SLC memory 8 and MLC memory 9 are connected via first data bus 12 and a second data bus 13 respectively. The first and second data busses may be an upper and lower data bus respectively, or vice versa. The busses 12, 13 are separate with there being a bus for each of the memories 8, 9. Both busses 12, 13 may be 8-bit data busses. ENABLE and ALE signals are able to be sent to SLC memory 8 and MLC memory 9 simultaneously. WRITE signals are also sent to both memories 8, 9 via the respective upper bus 12 or lower bus 13. The address data and data stored to the SLC memory 8 is sent via the upper bus 12, whereas the address data and data stored to the MLC memory 9 is sent via lower bus 13.

Master control unit 7 may use 16-bit data lines to control both the SLC memory 8 and the MLC memory 9, with an upper 8-bit data line being connected to upper data bus 12, and a lower 8-bit data line being connected to lower data bus 13. During a WRITE operation, the master control unit 7 will simultaneously ENABLE the SLC memory 8 and the MLC memory 9 and send data to both memories 8, 9 simultaneously on a page or block basis. As the SLC memory 8 write speed is faster than that of the MLC memory 9 the SLC memory will write more pages or blocks than the MLC memory 9 in order to obtain an average write speed between both types of memory. Again, the data is written to the memories 8, 9 at optimum speed such that the WRITE time is minimized.

The READ operation is similar to that described above in relation to Figures 1 and 2. The main difference is that during the READ operation on SLC memory 8, the upper bus 12 data will be read from the master control unit 7; and during the READ operation on MLC memory 9, the lower bus 13 data will be read from master control unit. During a READ operation, the master control unit 7 will simultaneously ENABLE the SLC memory 8 and the MLC memory 9 and received data from both memories 8, 9 simultaneously on a page or block basis. As the SLC memory 8 read speed is faster than that of the MLC memory 9 the SLC memory will read more pages or blocks than the MLC memory 9 in order to obtain a read speed between both types of flash. Again, the data is read by the memories 8, 9 at optimum speed such that the READ time is minimized.

By simultaneously it is meant effectively simultaneously. There may be small time differences due to processing delays but these are to be encompassed within the meaning of simultaneously.

Whilst there has been described in the foregoing description preferred embodiments of the present invention, it will be understood by those skilled in the technology concerned that many variations or modifications in details of design, construction and operation without departing from the present invention as defined in the following claims.

The Claims

1. A portable data storage device comprising:

(a) an interface for enabling the portable data storage device to be used for data transfer with a host computer;

(b) an interface controller for controlling the interface;

(c) a master controller for controlling the writing of data to and reading data from a non-volatile memory;

(d) the non-volatile memory comprising at least one single layer cell flash memory and at least one multiple layer cell flash memory;

(e) the at least one single layer cell flash memory and at least one multiple layer cell flash memory being able to operate simultaneously for improving the speed of operation over only multiple layer flash memory.

2. A portable data storage device as claimed in claim 1 further comprising at least one data bus operatively connected to the master controller and the at least one single layer cell flash memory and at least one multiple layer cell flash memory for writing data to and reading data from the at least one single layer cell flash memory and at least one multiple layer cell flash memory.

3. A portable data storage device as claimed in claim 2, wherein the at least one data bus comprises a common data bus for both the at least one single layer cell flash memory and at least one multiple layer cell flash memory.

4. A portable data storage device as claimed in claim 2, wherein the at least one data bus comprises a first data bus operatively connected to the at least one single layer cell flash memory and a second bus operatively connected to the at least one multiple layer cell flash memory.

5. A portable data storage device as claimed in claim 3, wherein the master controller is for writing data to and reading data from the at least one single layer cell flash memory and the at least one multiple layer cell flash memory alternately; data being written to and read from the at least one single layer cell flash memory at a speed a multiplication factor higher than those of the at least one multiple layer cell flash memory; the data being in the form selected from the group consisting of: blocks, and page.

6. A portable data storage device as claimed in claim 5, wherein the multiplication factor is in the range 5 to 10.

7. A portable data storage device as claimed in claim 5, wherein each block of data for the at least one single layer cell flash memory is 64 pages; and each block of data for the at least one multiple layer cell flash memory is 128 pages.

8. A portable data storage device as claimed in claim 4, wherein the master controller is for writing data to and reading data from the at least one single layer cell flash memory and the at least one multiple layer cell flash memory simultaneously, the data being in a form selected from the group consisting of: blocks, and page.

9. A portable data storage device as claimed in claim 8, wherein the data being written to and read from the at least one single layer cell flash memory is at a speed a multiplication factor higher than that of the at least one multiple layer cell flash memory.

10. A portable data storage device as claimed in claim 9, wherein the multiplication factor is in the range 5 to 10.

11. A portable data storage device as claimed in claim 8, wherein each block of data for the at least one single layer cell flash memory is 64 pages; and each block of data for the at least one multiple layer cell flash memory is 128 pages; each page being 2048 bytes.

12. A portable data storage device as claimed in claim 4, where the first data bus is one of: an upper data bus and a lower data bus, and the second data bus is the other of the upper data bus and the lower data bus.

13. A method of processing data on a portable data storage device, the portable data storage device comprising a master controller for controlling a memory, the memory comprising at least one single layer cell flash memory and at least one multiple layer cell flash memory, the method comprising:
using the master controller to control the writing of data to and reading data from a non-volatile memory such that the at least one single layer cell flash memory and at least one multiple layer cell flash memory have data written to and read from them simultaneously.

14. A method as claimed in claim 13 further comprising writing data to and reading data from the at least one single layer cell flash memory and at least one multiple layer cell flash memory over at least one data bus operatively connected to the master controller and the at least one single layer cell flash memory and at least one multiple layer cell flash memory.

15. A method as claimed in claim 14, wherein the at least one data bus comprises a common data bus for both the at least one single layer cell flash memory and at least one multiple layer cell flash memory.

16. A method as claimed in claim 14, wherein the at least one data bus comprises a first data bus operatively connected to the at least one single layer cell flash memory and a second data bus operatively connected to the at least one multiple layer cell flash memory.

17. A method as claimed in claim 16, wherein the first data bus is one of: an upper data bus and a lower data bus, and the second data bus is the other of the upper data bus and the lower data bus.

18. A method as claimed in claim 15, wherein the master controller writes data to and reads data from the at least one single layer cell flash memory the and at least one multiple layer cell flash memory alternately; data being written to and read from the at least one single layer cell flash memory at a speed a multiplication factor higher than those of the at least one multiple layer cell flash memory; the data being in a form selected from the group consisting of: blocks, and page.

19. A method as claimed in claim 18, wherein the multiplication factor is in the range 5 to 10.

20. A method as claimed in claim 19, wherein each block of data for the at least one single layer cell flash memory is 64 pages; and each block of data for the at least one multiple layer cell flash memory is 128 pages.

21. A method as claimed in claim 16, wherein the master controller writes data to and reads data from the at least one single layer cell flash memory and the at least one multiple layer cell flash memory simultaneously, the data being in a form selected from the group consisting of: blocks, and page.

22. A method as claimed in claim 21, wherein the data is written to and read from the at least one single layer cell flash memory at a speed a multiplication factor higher than that of the at least one multiple layer cell flash memory.

23. A method as claimed in claim 22, wherein the multiplication factor is in the range 5 to 10.

24. A method as claimed in claim 21, wherein each block of data for the at least one single layer cell flash memory is 64 pages; and each block of data for the at least one multiple layer cell flash memory is 128 pages; each page being 2048 bytes

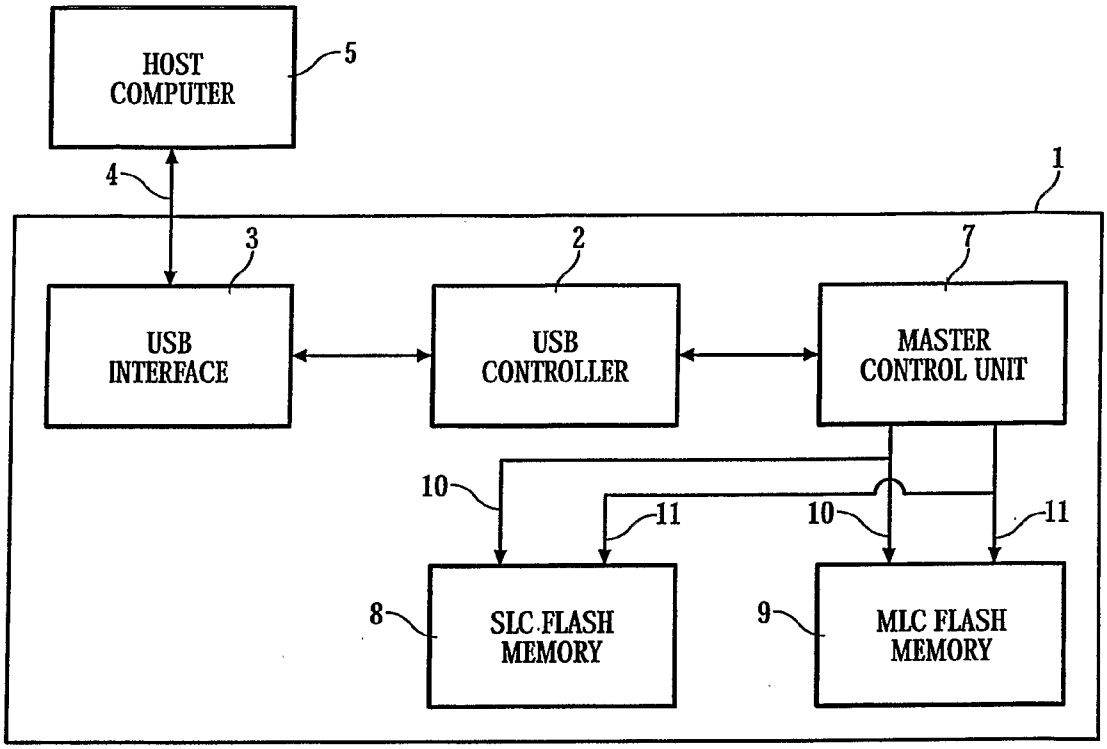
HOST COMPUTER
5
4
1
3
2
7
USB INTERFACE
USB CONTROLLER
MASTER CONTROL UNIT
10
11
10
11
8
SLC FLASH MEMORY
9
MLC FLASH MEMORY

FIG. 1

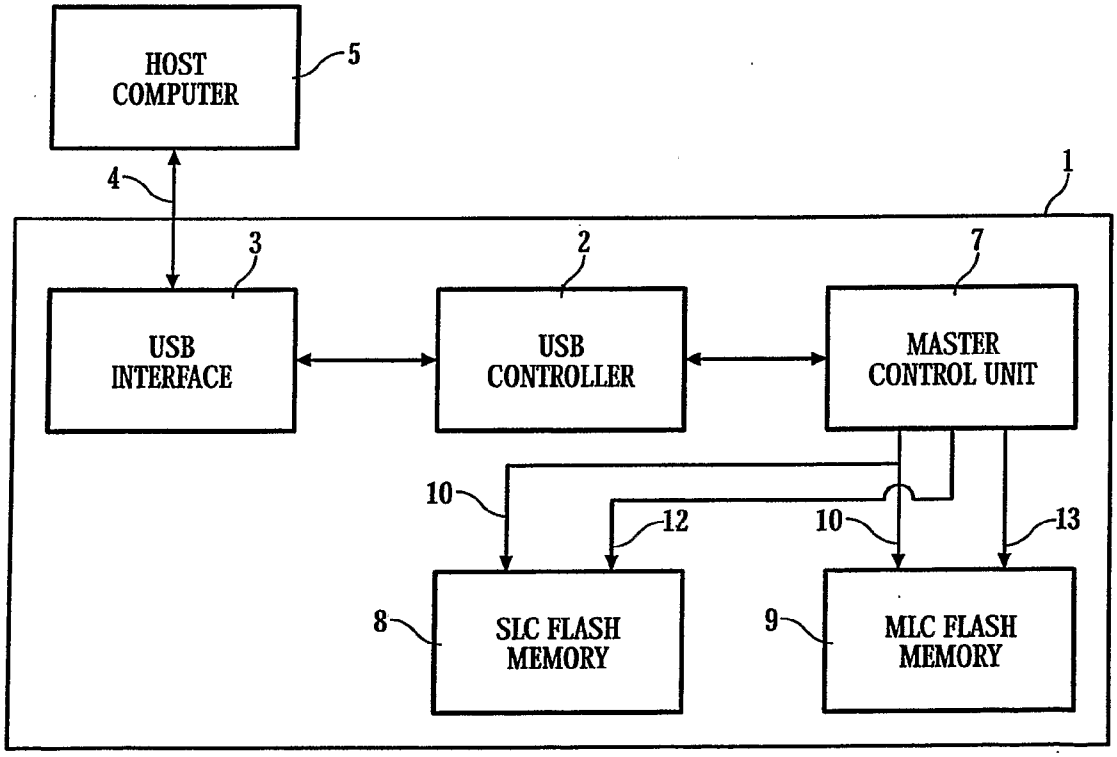
HOST COMPUTER
5
4
1
3
2
7
USB INTERFACE
USB CONTROLLER
MASTER CONTROL UNIT
10
12
10
13
8
SLC FLASH MEMORY
9
MLC FLASH MEMORY

FIG. 3

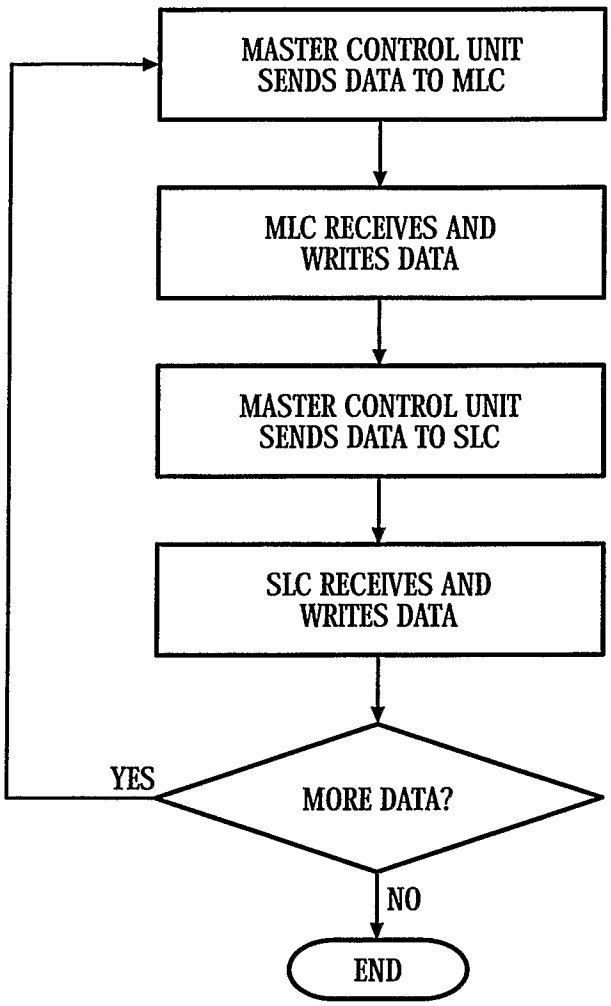
MASTER CONTROL UNIT SENDS DATA TO MLC
MLC RECEIVES AND WRITES DATA
MASTER CONTROL UNIT SENDS DATA TO SLC
SLC RECEIVES AND WRITES DATA
MORE DATA?
YES
NO
END

FIG. 2

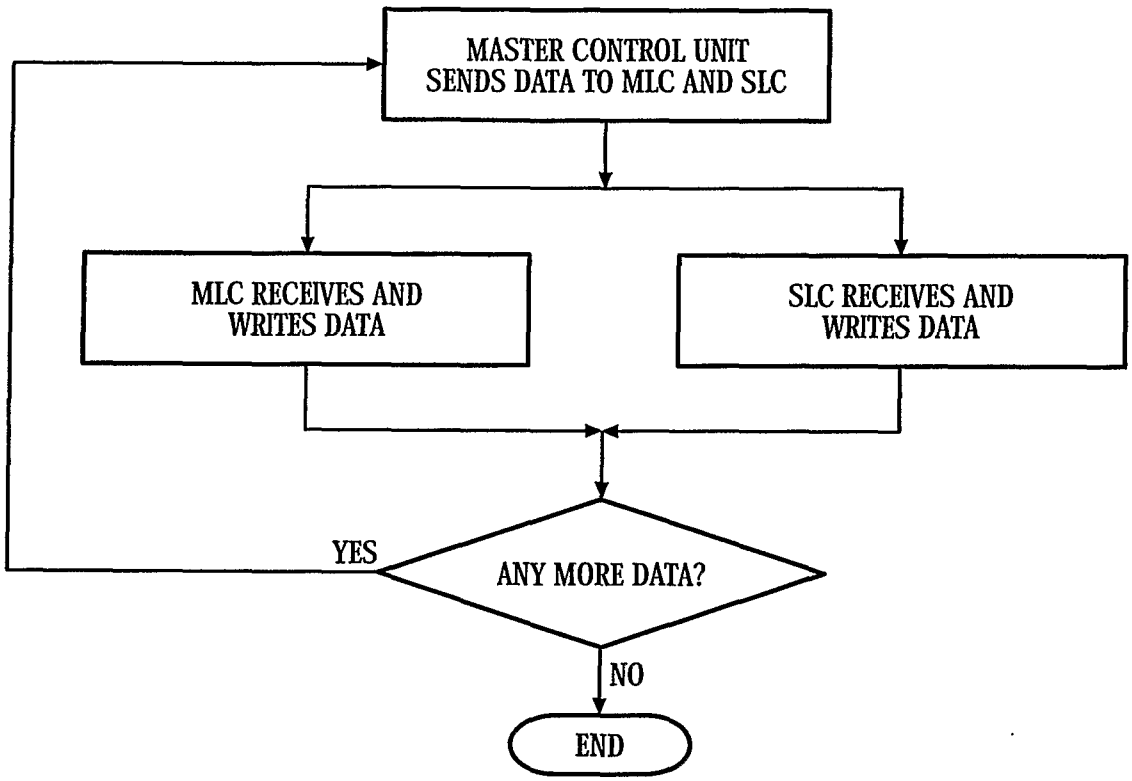
MASTER CONTROL UNIT
SENDS DATA TO MLC AND SLC
MLC RECEIVES AND
WRITES DATA
SLC RECEIVES AND
WRITES DATA
YES
ANY MORE DATA?
NO
END

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2005/000328

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: G11C 16/00, 7/00, G06F 12/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI, PCT, USPTO, IEEE, Google Scholar (slc, single level, single bit, mlc, multi level, multi bit, flash, nonvolatile, etc.)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/0112692 A1 (GONZALEZ et al), 19 June 2003 the whole document	1-24
A	US 5,671,388 A (HASBUN), 23 September 1997 the whole document	1-24
A	US 6,728,133 B2 (SHIMIZU), 27 April 2004 the whole document	1-24
A	US 5,966,326 A (PARK et al), 12 October 1999 the whole document	1-24

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

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Date of the actual completion of the international search
10 November 2005

Date of mailing of the international search report
16 NOV 2005

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,930,167 A (LEE et al), 27 July 1999 the whole document	1-24
A	US 5,541,886 A (HASBUN), 30 July 1996 the whole document	1-24

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2005/000328

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	2003112692	AU	2002366487	CN	1620700	US	6807106
		WO	03052764				
US	5671388	NONE					
US	6728133	JP	2003022687	US	2003007384		
US	5966326	JP	10106279				
US	5930167	NONE					
US	5541886	NONE					

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX