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F. J. HACKL

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BYPASSING OF PROCESSOR SEQUENCE CONTROLS FOR DIAGNOSTIC TESTS

Filed Dec. 23, 1964

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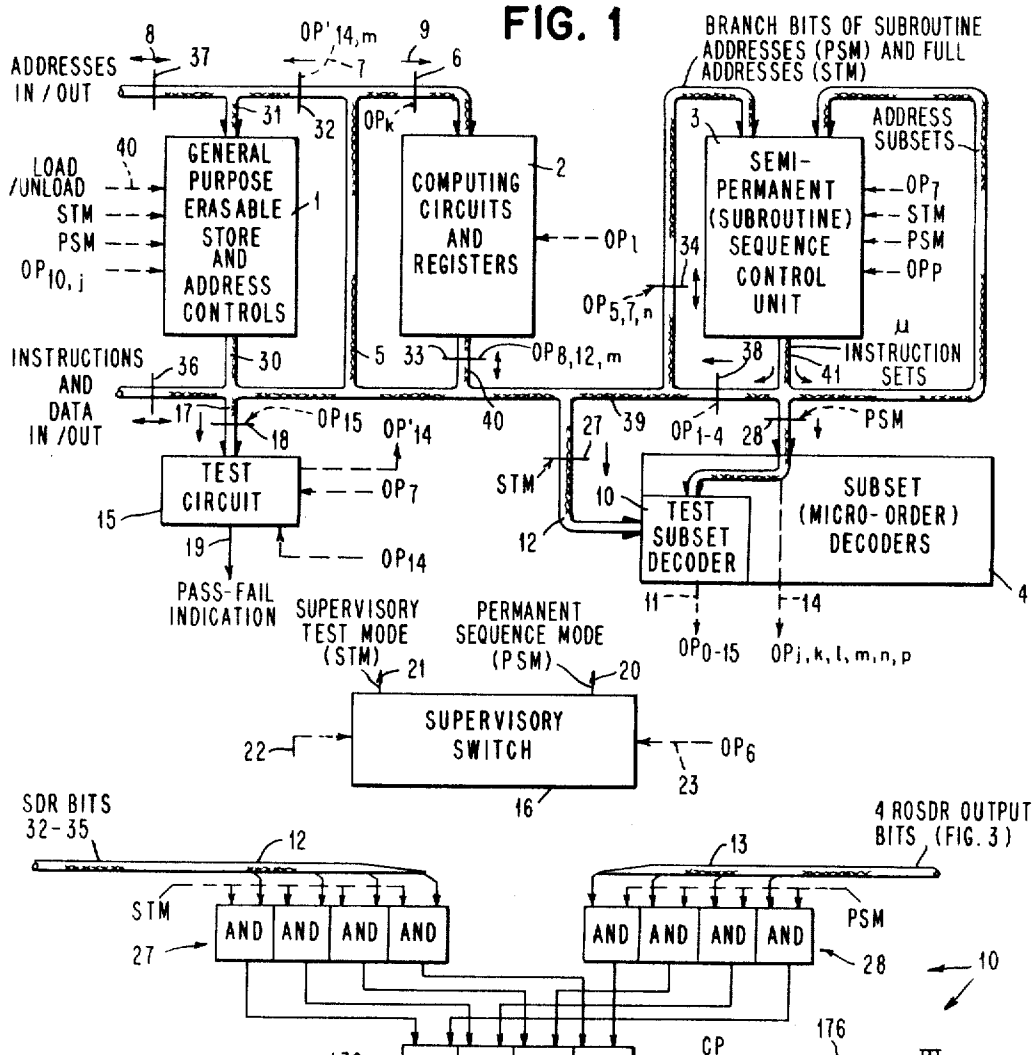
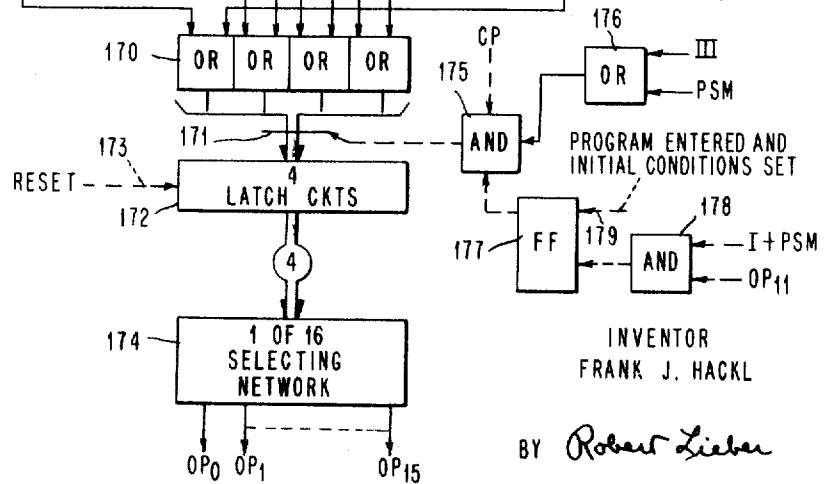


**FIG. 4**



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FIG. 5

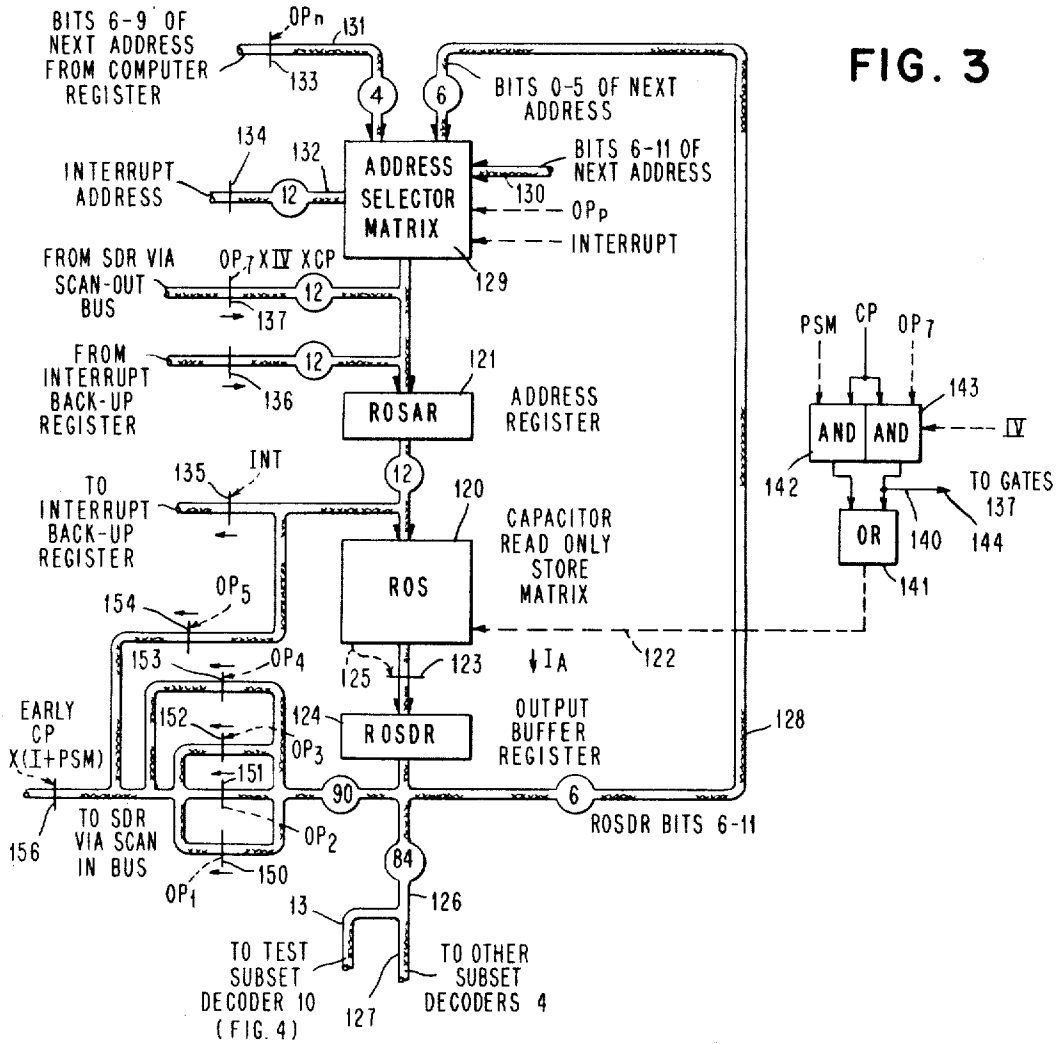
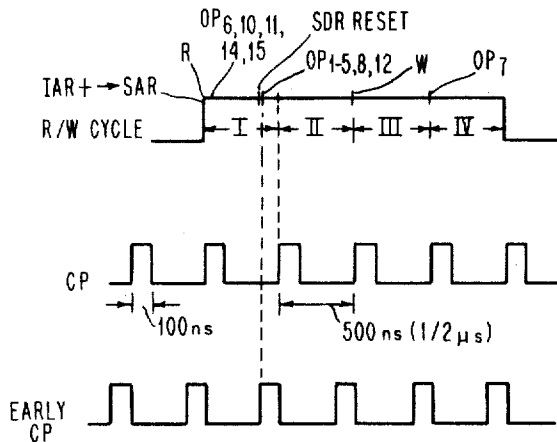


**FIG. 6**



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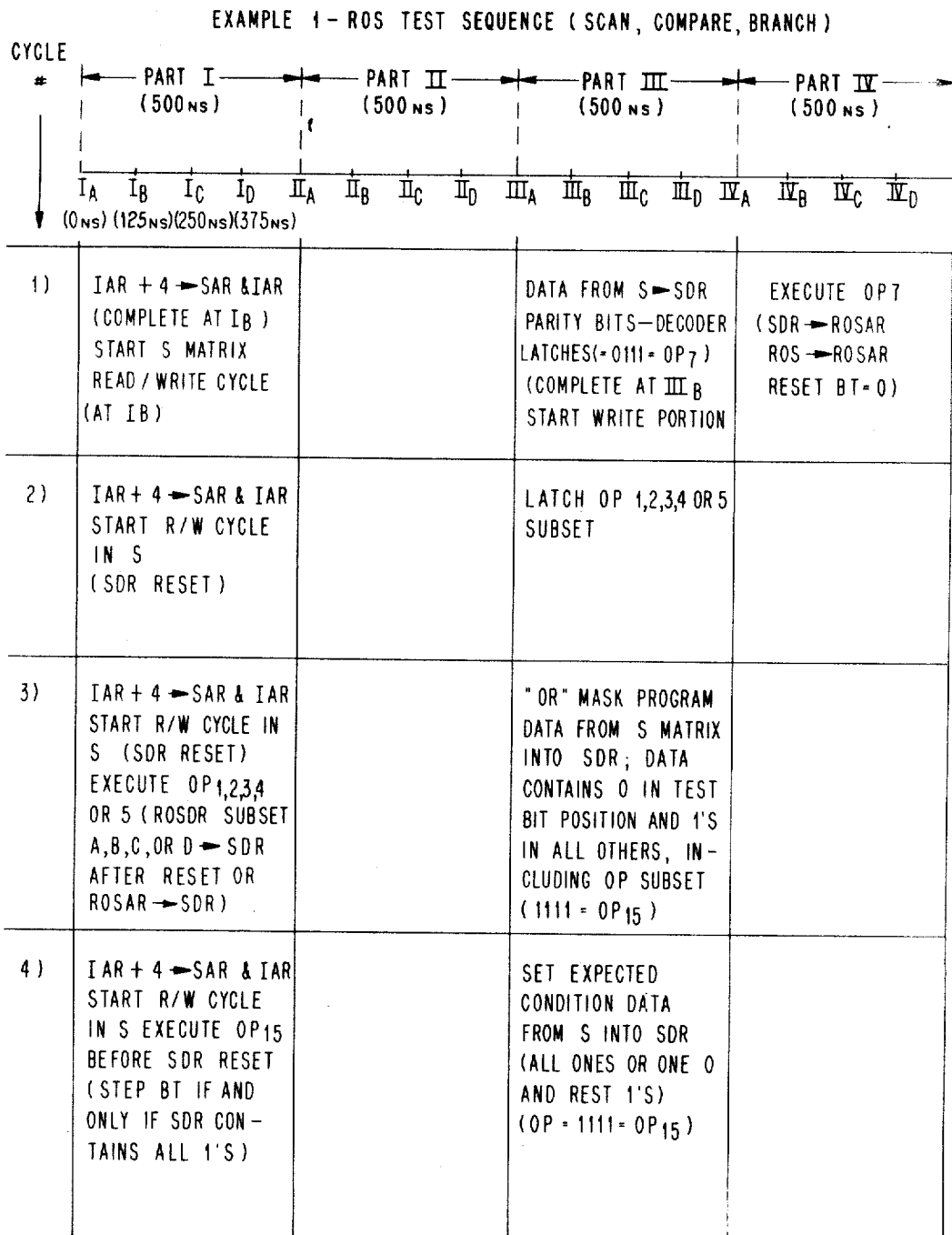
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FIG. 7A



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FIG. 7B

|    |                                                                                                                                                                                                                                                                                                                                                                                                            |  |                                                                                                                                                                                             |                                                           |
|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|
| 5) | IAR+4 → SAR & IAR<br>START R/W CYCLE IN<br>S (SDR RESET)<br>EXECUTE OP <sub>15</sub> BEFORE<br>SDR RESET                                                                                                                                                                                                                                                                                                   |  | S → SDR<br>OP <sub>14</sub> (1110) →<br>DECODER LATCHES                                                                                                                                     |                                                           |
| 6) | IAR+4 → SAR & IAR<br>START R/W CYCLE IN<br>S (SDR RESET)<br>EXECUTE OP <sub>14</sub><br>(SDR BITS 12-31 TO<br>IAR IF AND ONLY IF<br>BT=0; BLOCK GATE 88)                                                                                                                                                                                                                                                   |  | OP <sub>0</sub> (= 0000 = NO OP)<br>TO SDR AND<br>DECODER                                                                                                                                   |                                                           |
| 7) | IAR+4 → SAR & IAR<br>START R/W IN S<br>(SDR RESET)<br>OP = NO OP                                                                                                                                                                                                                                                                                                                                           |  | OP <sub>6</sub> , 7, 10, OR 11<br>LATCHED IN SDR<br>AND DECODER. ALL<br>BUT OP <sub>10</sub> ARE CON-<br>DITIONAL BRANCH DATA<br>OP <sub>10</sub> RESULTS FROM FA-<br>ILURE TO BRANCH CYC 6 | IF OP <sub>7</sub> : SDR → ROSAR<br>ROS → ROSDR<br>BT = 0 |
| 8) | IF OP <sub>10</sub> STOP BY<br>INHIBITING SAR GATING<br>(SDR BITS 0-11 AND<br>24-31 SPECIFY "BAD"<br>ROS WORD AND SCAN-<br>NED-IN BIT RESPECTIV-<br>ELY)<br>IF OP <sub>7</sub> ,<br>CONTINUE WITH<br>CYCLES 2-7<br>OF NEXT BIT<br>TEST SEQUENCE<br>IF OP <sub>6</sub> RETURN TO<br>PSM STATE<br>IF OP <sub>11</sub> INITIATE FLT<br>PROGRAM LOAD PRO-<br>CEDURE FOR LOADING<br>NEXT TEST SEGMENT<br>INTO S |  |                                                                                                                                                                                             |                                                           |

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# FIG. 8

## EXAMPLE 2-S TEST SEQUENCE

| CYCLE<br>↓ | PART I                                                                                                                 | PART II | PART III                                                                                                                                                                                                                                                                                                                                                                    | PART IV                                                                                                   |
|------------|------------------------------------------------------------------------------------------------------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|
| 1          | IAR + 4 → SAR & IAR<br>(RESET SDR)<br>START S R/W CYCLE                                                                |         | OP <sub>7</sub> FROM S TO SDR<br>AND DECODER                                                                                                                                                                                                                                                                                                                                | EXECUTE OP <sub>7</sub><br><div> <div>SDR → ROSAR</div> <div>ROS → ROSAR</div> <div>RESET BT</div> </div> |
| 2          | IAR + 4 → SAR & IAR<br>(RESET SDR)<br>START S CYCLE                                                                    |         | CODE OF BRANCH OP <sub>14</sub><br>FROM S TO SDR AND<br>DECODER DATA FROM<br>FIRST DIAGONAL AD-<br>DRESS LOCATION IN S<br>TO SDR; BITS 12-31<br>OF THIS DATA SPECIFY<br>NEXT DIAGONAL ADDR.<br>LOCATION OF NEXT<br>WORD ALL DATA WORDS<br>IN NON-DIAGONAL<br>LOCATIONS CONTAIN<br>OP <sub>0</sub> OR OP <sub>10</sub> AND<br>ALL DIAGONAL WORDS<br>CONTAIN OP <sub>14</sub> |                                                                                                           |
| 3          | IAR + 4 → SAR & IAR<br>(RESET SDR); START S<br>CYCLE; CONDITIONALLY<br>EXECUTE OP <sub>14</sub> (SDR<br>→ IAR IF BT=0) |         | LATCH OP <sub>0</sub> (NO OP)                                                                                                                                                                                                                                                                                                                                               |                                                                                                           |
| 4          | IAR + 4 → SAR & IAR<br>RESET SDR<br>START S CYCLE                                                                      |         | LATCH NEXT DIAG-<br>ONAL DATA WORD IF<br>OP <sub>14</sub> BRANCH WAS COR-<br>RECTLY COMPLETED.<br>OTHERWISE LATCH<br>OP <sub>10</sub> FROM NON-DIAG-<br>ONAL LOCATION                                                                                                                                                                                                       |                                                                                                           |
| 1          | IF OP <sub>14</sub> LATCHED EX-<br>ECUTE 3 ON SDR →<br>IAR ADDRESS; CYCLE.<br>IF OP <sub>10</sub> STOP                 |         |                                                                                                                                                                                                                                                                                                                                                                             |                                                                                                           |

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# FIG. 9

## EXAMPLE 3 - BT TEST SEQUENCE

| CYCLE<br>#<br>↓ | I                                                                                             | II | III                                                                      | VI                                            |
|-----------------|-----------------------------------------------------------------------------------------------|----|--------------------------------------------------------------------------|-----------------------------------------------|
| 1)              | IAR+4 → SAR & IAR<br>SDR RESET<br>CYCLE S                                                     |    | S → SDR<br>(OP7 → DECODER)                                               | SDR → ROSAR<br>ROS → ROSDR<br>BT = 0          |
| 2)              | IAR+4 → SAR & IAR<br>SDR RESET<br>CYCLE S                                                     |    | S → SDR (DATA=ALL 1'S)<br>OP15 → DECODER                                 |                                               |
| 3)              | IAR+4 → SAR & IAR<br>SDR RESET & CYCLES<br>EXECUTE OP 15<br>(STEP BT IF SDR =<br>ALL 1'S)     |    | S → SDR<br>OP14 → DECODER                                                |                                               |
| 4)              | IAR+4 → SAR & IAR<br>SDR RESET, S CYCLED<br>EXECUTE OP 14<br>(BRANCH ON BT=0<br>BY SDR → IAR) |    | S → SDR<br>OP0 → DECODER                                                 |                                               |
| 5)              | IAR+4 → SAR & IAR<br>SDR RESET<br>CYCLE S                                                     |    | S → SDR<br>OP10 → DECODER<br>(IF BT = 0)<br>OP7 → DECODER<br>(IF BT = 1) | IF OP7 SDR → ROSAR<br>ROS → ROSDR<br>RESET BT |
| 6)              | IF OP10 STOP; IF OP7,<br>IAR+4 → SAR & IAR,<br>SDR RESET, CYCLE S                             |    | S → SDR (ALL 1'S)<br>OP15 → DECODER                                      |                                               |
| 7)              | IAR+4 → SAR & IAR,<br>SDR RESET, CYCLE S,<br>EXECUTE OP15 (STEP<br>BT IF SDR = ALL 1'S)       |    | S → SDR (ALL 1'S)<br>OP15 → DECODER                                      |                                               |
| 8)              | IAR+4 → SAR & IAR,<br>SDR RESET, CYCLE S                                                      |    | S → SDR; OP15 →<br>DECODER                                               |                                               |
| 9)              | IAR+4 → SAR & IAR;<br>SDR RESET, CYCLE S;<br>BRANCH ON OP14                                   |    | S → SDR; OP0 →<br>DECODER                                                |                                               |
| 10)             | IAR+4 → SAR & IAR<br>SDR RESET CYCLE S;                                                       |    | S → SDR; OP10 OR OP7<br>→ DECODER                                        | IF OP7 SDR → ROSDR<br>ROS → ROSAR<br>RESET BT |
| 11)             | IF OP10 STOP; IF OP7=0<br>STEP 2 OF NEXT TEST                                                 |    |                                                                          |                                               |

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FIG. 10

| OP | SUBSET CODE | TYPE OF OPERATION | FUNCTION                                                                                                |
|----|-------------|-------------------|---------------------------------------------------------------------------------------------------------|
| 0  | 0000        | —                 | NO OP                                                                                                   |
| 1  | 0001        | SCAN-IN           | ROSDR SUBSET A (BITS 0-31) → SDR                                                                        |
| 2  | 0010        | SCAN-IN           | ROSDR SUBSET B (BITS 31-55) → SDR                                                                       |
| 3  | 0011        | SCAN-IN           | ROSDR SUBSET C (BITS 56-87) → SDR                                                                       |
| 4  | 0100        | SCAN-IN           | ROSDR SUBSET D (BITS 88-89) → SDR                                                                       |
| 5  | 0101        | SCAN-IN           | ROSAR → SDR                                                                                             |
| 6  | 0110        | TERMINAL BRANCH   | RESET SUPV SWITCH TO PSM STATE                                                                          |
| 7  | 0111        | SCAN-OUT          | RESET BT=0 SDR (BITS 19-30) → ROSAR; ROS → ROSDR                                                        |
| 8  | 1000        | SCAN-IN           | DISPLAY SWITCHES → SDR                                                                                  |
| 9  | 1001        | —                 | SPARE                                                                                                   |
| 10 | 1010        | TERMINAL BRANCH   | STOP WORD SPECIFIED BY SDR BITS 0-11 (ROS BIT SPECIFIED BY SDR BITS 24-31) (INHIBIT START OF MEM CYCLE) |
| 11 | 1011        | TERMINAL BRANCH   | INITIATE FLT PROGRAM LOAD PROCEDURE                                                                     |
| 12 | 1100        | SCAN-IN           | ERROR REGISTER (PARITY) → SDR                                                                           |
| 13 | 1101        | —                 | SPARE                                                                                                   |
| 14 | 1110        | TERMINAL BRANCH   | SDR (BITS 17-31) → IAR PROVIDING BT=0                                                                   |
| 15 | 1111        | COMPARE           | SWITCH BT PROVIDING SDR-ALL I'S                                                                         |

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18 Claims. (Cl. 340—172.5)

### ABSTRACT OF THE DISCLOSURE

Means are disclosed for by-passing the main source of internal gating and sequence selecting control signals of a data processor system or the like to permit diagnostic testing; particularly testing of the by-passed source. When operating in by-passed mode the system is cycled at a reduced rate determined by a separate timing source (ring counter). The information needed to control the system in this mode is introduced to the by-pass juncture from an erasable main program store which cycles at the reduced rate defined by the separate timing source.

This invention relates to a data processor test system distinguished by the presence therein of means permitting interchangeable utilization of a general purpose erasable store and a special purpose permanent, or semi-permanent, control store as microprogram sequence control elements in the control of certain testing operations.

Because of the complexity of modern data processing systems, it is desirable to incorporate in each system the facility to perform tests under automatic program control to locate malfunctioning circuit components, and thereby simplify the tasks of maintenance personnel. The problem, however, is to provide such a facility without adding materially to the cost of the data processing equipment. The problem is further magnified in a system having permanently or semi-permanently organized microprogram sequence controls because failures in certain parts of the latter can only be diagnosed by duplicate parts which perform the same function, such duplication on a permanent basis being considered inefficient and economically unfeasible.

An object of this invention, therefore, is to provide an integral self-testing facility for a data processing system which is distinctively economical and efficient in construction, and can test all parts of a malfunctioning data processing system.

Another object is to provide a test facility in a data processing system which can interchangeably utilize a general purpose erasable store and a special purpose control store to control certain basic testing operations.

System diagnostic tests generally involve extensive repetition of operations which may be broadly characterized as: scan operations, compare operations, branch operations, and terminal or exit operations. In a scan operation information is scanned in to the elements to be tested, the system is allowed to perform operations involving actions of the test elements for a predetermined number of elemental cycles, and then signals representative of the state or states of the test elements are scanned in to a comparison device. The latter compares the scanned in signal to a stored reference signal representative of the expected scanned in condition for correctly functioning elements, and produces a branch signal which conditions the selection of the next testing operation. With such branching a new test sequence may be initiated, or the tests may be concluded in a terminal action, such as a dead stop halting all system activity, or a reversion to ordinary processing control; for example, in those instances

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in which a test indicates that a failure is the result of an intermittent condition which has ceased to exist.

Another object of this invention is to provide a test system capable of interchangeably utilizing a general purpose erasable store and a special purpose permanent control store as sequence control elements to control a complete set of scanning, comparing, branching and terminal operations sufficient to conduct a complete series of automatically programmed tests on parts of a data processing system both internal and external to the sequence control elements of the system.

Another object is to provide a test circuit device particularly effective for use in a test system as disclosed herein which is of particularly economical construction.

A feature of this invention resides in the provision of a relatively small complement of testing and control circuitry, for use interchangeably in association with a general purpose erasable store and a special purpose permanent or semi-permanent control store to control execution of a complete series of tests including tests of both the erasable and permanent stores, and of the testing circuitry.

A subsidiary feature resides in the provision of a testing circuit arrangement of particularly simple, economical and efficient organization, for use in tests controlled by either the general purpose erasable store or the permanent control store. This circuit comprises a simple AND circuit (all 1's tester) and a one stage counter (binary trigger) which can be repeatedly sequenced to test out a group of binary circuit elements one element at a time under the direction of program information stored in the erasable store, whereby circuits for selecting the individual elements of the group need not be provided. A particularly nice aspect of this is that all 1's checking AND circuit or an equivalent thereof is usually provided in connection with the initial manually controlled testing of a newly constructed erasable store.

With this testing circuit it is possible to combine a group of signal bits to be individually tested with the bits of a variable program mask word containing a zero bit in a test bit position and one bit in all other positions whereby the presence or absence of an all 1's condition in the combination corresponds to the presence or absence of a one bit in the test bit position of the signal group, and can be used as a bit test condition to step the one stage counter. It is possible to alternatively step the counter in accordance with the presence or absence of all 1's in a reference word of program information representative of the expected condition of the combination of the signal group being tested with the program mask word previously mentioned, whereby if the test bit conditions in the actual and expected conditions are identical the counter is stepped twice or not at all and remains in an initial reset or zero condition representative of a passed test, whereas if the two responses are different the counter is stepped only once and remains in an odd or one state indicative of a failure.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment and examples of test applications thereof, as illustrated in the accompanying drawings, wherein:

FIG. 1 represents a generalized schematic block diagram for explaining the general features of the invention;

FIG. 2 is a schematic drawing showing the erasable store and the connections thereto for the subject testing application;

FIG. 3 is a schematic of the semi-permanent control store for which the erasable store can be interchangeably employed in the subject testing application and further illustrating scan connections for testing said control store;

FIG. 4 is a schematic block diagram illustrating details of the test subset control signal decoding circuit shown in the preceding figures;

FIG. 5 is a schematic block diagram illustrating details of the test circuit shown in FIGS. 1-3;

FIG. 6 is a timing diagram for explaining the relative sequence of operations of the erasable store shown in FIG. 1 with reference to the timing of the semi-permanent sequence controls also shown in the latter figure;

FIG. 7 is a tabular description in two sections, 7A and 7B, of an exemplary sequence of operations performed by the erasable store in connection with the testing of the semi-permanent sequence controls;

FIG. 8 is a tabular description of another exemplary sequence of operations of the erasable store in connection with the testing of the erasable store itself;

FIG. 9 is a tabular description of a third exemplary sequence of operations of the erasable store and the bit testing circuit which is used to check the said bit testing circuit; and

FIG. 10 is a tabular description of the basic test subset code group which can be decoded by the test subset decoding circuit of FIG. 4 to control the respective functions indicated in the table.

### GENERAL DESCRIPTION

Referring to FIG. 1 a data processing system to which the present invention is applicable includes a general purpose erasable store and its address controls 1, computing circuits and register 2, and a permanent or semi-permanent sequence control unit 3. Programs held in the store 1 are executed by the computing circuits and registers 2 under the direction of signals provided by the sequence control unit 3 through a series of decoding networks or circuits indicated at 4. The sequence controls are of the type known as micro-program, or subroutine, sequence controls, which are adapted to sequentially examine general program instructions held in the store 1, and to control the execution of a corresponding sequence of basic, or micro-operations. The subset decoding networks 4 operate upon subsets of each microinstruction signal set to produce micro-operation control signals which act directly to control the sub-systems 1 and 2, and the transfer of information between these two sub-systems. In the drawing plural bit information flow paths are indicated by double solid lines, as shown for example at 5, plural gates for controlling the flow of information through each flow path are indicated by a single stroke perpendicular to and intersecting the double solid line which represents the path, as indicated for example at 6, and lines carrying control information signals for controlling the information transfer gates are indicated by broken lines such as that shown at 7. The direction of passage of signals through the gates is indicated by arrows adjacent the gate stroke symbol, a two-headed arrow such as 8 denoting a bi-directional flow, and a single-headed arrow such as 9 denoting a unidirectional flow in the direction of the arrow head.

One of the subset decoding networks within the unit 4 which is of particular interest in the testing application hereof is indicated at 10. Its output, shown schematically as a single broken line 11, actually comprises sixteen separate and distinct micro-operation control lines denoted jointly by the symbol OP and individually by numerical subscript characters 0-15. The subset decoder 10 is supplied with four bit binary signal combinations from one of two groups of input lines 12 or 13 and translates these into control signals on exclusives ones of the sixteen lines 11. Similarly, the other decoders of the group of decoders 4 translate control signals to individual lines in respective groups of output control lines indicated collectively at 14. Each output line group is denoted by the symbol OP and an individual subscript  $j, k, l, m, n$ , or  $p$ .

Also of particular interest in connection with the present invention, the system is provided with a test circuit 15 and a supervisory switch 16. The test circuit 15 is effective

to accept as input 36 bit parallel signal sets via an information flow path 17 in which there are gates 18 controlled by one of the output lines  $OP_{15}$  of the decoder 10, and to provide at its output 19 a pass-fail signal indicative of the test status of a variable one of the 36 bits traversing the path 17. A particularly economical and effective arrangement for providing these indications is described below.

The supervisory switch 16 can be conditioned to one of two states denoted Permanent Sequence Mode (abbreviated PSM) or Supervisory Test Mode (abbreviated STM). When it is in the PSM state switch 16 provides a control signal only on PSM control line 20 and in the STM state it provides a signal only on STM control line 21. The switch is conditioned to the STM state by signals supplied through automatic or manual means indicated by line 22, the details of which are not particularly relevant to the present invention, and it is restored to the PSM state by signals on the control line 23 which connects to line  $OP_8$  of the group of output lines 11 of the test subset decoder 10.

The decoder 10 is conditioned by control information in an exclusive one of the two four-line connections, 12 or 13, depending upon whether the supervisory test switch 15 is respectively in the STM or PSM state, as may be inferred from the illustrated control inputs to gates 27 and 28 in the paths of the said respective connections. Signals in the path 12 are supplied from four output bit positions of the general purpose erasable store 1 and signals in the path 13 are supplied from four output bit positions of the sequence controls 3.

It is noteworthy although not essential, that in the present embodiment the path 12 connects to a parity channel of the bus 30. Thus maximum use is made of the information capacity of the bus 30. This, however, creates a program loading problem, since the stored bits comprising the codes for producing  $OP_0$  to  $OP_{15}$  may not be in the correct parity relation to the other bits in the associated word in store 1, and yet it is desirable to maintain a parity check on each program word as it is written into storage. For example, it is necessary to provide mask words in storage as previously mentioned containing a variably positioned 0 bit and 1's in all other bit positions. The four parity bits for such a word would therefore ordinarily vary according to the position of the 0 bit. To produce a predetermined constant bit in each parity position of such a test word, while loading the word with appropriate parity checks, a programming expedient is employed whereby two different words are sequentially loaded into the same storage location, one word being combined with the other in the store, in an internal logical-OR operation, to produce the cancellation of parity with validly checked inputs.

The following specific example will suffice. A group of bits to be loaded into storage is  $A=1011111(1)$ , the 1 in parenthesis occupying a parity bit position. Assume that the actual parity of 1011111 is 0 (i.e. assume odd parity is represented by a 0). Then we first load  $B=1011111(0)$  into storage thereby maintaining correct input parity and follow this up by non-destructively "Or-ing"  $C=10100000(1)$  which also has correct input parity, with B in an internal logical OR operation by non-destructively regenerating B while writing C into storage. The unchecked internal logical OR combination of B and C (written  $B+C$ ) is 1011111(1), which is the group A as required. The means by which the internal logical OR operation is carried out is described below.

In ordinary operation, the supervisory switch 15 is in the PSM condition whereby decoder input gates 28 are enabled and decoder input gates 27 are disabled. In this mode of operation information flows into and out of the general purpose store 1, via the path 30, relative to particular address locations within the store determined by address information supplied via the path 31 or incremented address information supplied by counting controls within the store 1, as described below with reference to FIG. 2. Information leaving the store 1 in the PSM

mode flows through one or more of the sets of gates 32, 6, 34, 18 and 36, and information entering the store 1 passes through one or more of the sets of gates 32, 33, 34, 36 and 38. Information passing through gates 6 and 33 into computing circuits 2 is operated upon by the said 5 computing circuits and passed in the opposite direction through the gates 33 to the main data bus 30 or the main address bus 31, as and when required. The gates 36 and 37 on the other hand represent channel connections to external input/output devices, such as tape storage units, printing stations, and the like, which are external sources and sinks for processed information. The load/unload controls for controlling the flow of such information into and out of the store 1 are indicated generally at 40.

In STM mode operations, information can flow through one or more of the connecting paths 12, 17, 31, 39, and 40. Paths 12, 17 and 31 carry information from the output of store 1 to decoder 10, test circuit 14 and the address controls of the store 1. Path 39 carries scan-in test information, from either the address controls or the output field 41 of the sequence controls 3, to the store 1, and scan-out test information from the store 1 to the address controls of 3. Path 40 carries scan-in test information from registers 2 to store 1. Thus test conditions can be established in and read out of the sub systems 2 and 3 under the control of decoder 11, the output of which controls the gates in paths 39 and 40. Operations of test circuit 15 can be interleaved with such scanning operations to provide PASS-FAIL test indications via output 17 and address branching control signals via the line designated OP'14, the latter controlling the gate 32 leading to the address controls via the input path 31 of the store 1.

#### ERASABLE STORE AND PROGRAM LOAD AND TEST CONNECTIONS THERETO

Reference is had to FIG. 2 for a more detailed comprehension of the organization of the store 1 and the connections made thereto during the initial loading of Fault Location Test (abbreviated FLT) programs and during execution of such programs under STM mode control. The store 1 comprises a magnetic core storage matrix 60 (abbreviated S) addressed in accordance with information supplied by a storage address register 61 (abbreviated SAR). Information leaving and entering S is buffered in a storage data register (abbreviated SDR) which has an input path connection 63 to the sense amplifiers of S and an output path connection 64 to the write driver amplifiers of S.

The matrix S includes internal timing controls and connections not shown which control the various phases of the handling of information, between SDR and the storage address locations in S, in predetermined read/write (abbreviated R/W) cycles or predetermined write cycles (abbreviated W), in response to energization of control line 66 or 67, respectively. In an R/W cycle the first half of the cycle is devoted to the delivery of information from the addressed location in S to SDR. During this portion of the cycle the internal timing circuits of S deliver a reset signal to SDR via control lines 68 and 69 in preparation for the entry of the sensed information into SDR. Following this reset the timing circuits deliver control signals to SDR input gates 70, via control lines not shown, to strobe the sensed output of S into SDR. During the later or write half of an R/W cycle the internal timing controls of S act to gate the output of SDR through connecting lines 64 and write drivers (not shown) into the addressed location. With certain exceptions the information written into SDR in the second half of an R&W cycle is identical to the information sensed during the first half-cycle (i.e., the information in the addressed location is non-destructively sensed).

In a Write cycle induced by a signal on control line 67, the SDR input strobing signals to gates 70 are usually suppressed during the first half of the cycle, so that

in effect no reading takes place in S during that first half, while information is entered into SDR via the gates 36A, and IN-BUS connection 72. During the second half of the cycle information is written from SDR into S via the connecting lines 64 in place of the information previously stored in the addressed location. Thus, a W cycle is similar to an R/W cycle except that the information transferred from SDR to S in the second half cycle is generally unrelated to the previously stored information.

As mentioned above, the strobing signals to gates 70 are usually suppressed in W cycles. One exception to this occurs during the loading of parity-checked FLT program information in which the parity bits must be altered by an internal logical OR operation. In such operations the information is entered combinatorially in two W cycles, the first of which is an ordinary W cycle with gates 70 idle. In the second W cycle the strobing of gates 70 in the first half of this cycle is not suppressed and therefore information read into SDR from S is "OR'd" with parity checked information accepted from IN-BUS 72, whereby the desired word with incorrect parity is written into S during the second half of this cycle.

A part of the internal cycle timing controls of S is shown at 75. This part is a 4-state counting circuit having relatively exclusive outputs on four lines indicated at 76 which subdivide each cycle into four distinct equal parts, or sections. Two of these sections coincide with the sensing half of a storage cycle, and the other two sections coincide with the writing or regenerating half of a cycle. In STM mode of operation, gates 77 are energized to produce control signals on the lines identified by the Roman numbers I, II, III and IV, the functions of which are discussed below.

In addition to the IN-BUS connection 72, SDR has an IN-BUS (input) connection 80 to a SCAN-IN bus 81 via gates 82 and an OUT-BUS (output) connection to external output devices via gates 36B. Other output connections of SDR extend to test circuit 15 via gates 18, to test subset decoder 10 via gates 27, to a SCAN-OUT bus 83 via gates 84, to ADDRESS bus 85 via gates 32 and the OUT-BUS and to computing circuits 2 via gates 6.

The gates 32 couple address information to either the SAR register 61 via gates 86 or to an instruction address register 87 (also denoted IAR) via gates 88. The information in IAR is ordinarily used during program execution to control the addressing of program instructions. The output of IAR communicates selectively with the inputs of SAR and IAR via an increment adding circuit 89, and gates 90, 86, and 88. It is noted that information is stored in S in word units of 36 bits, four of which may be parity bits bearing a predetermined relationship to corresponding byte (1 byte=8 bits) subsets of the other thirty two bits. Addresses in SAR are usually 20 bits in length and denote the initial boundaries in S of full word (36 bit) and half word (18 bit) groups of cells. Each access to S results in retrieval and regeneration or initial recording of information commencing at either a full or half word boundary. The storage capacity of SDR, and the parallel signal handling capacity of the IN-BUS and OUT-BUS connections thereto, is 36 bits.

The circuit 89 can be selectively actuated to add a byte address count of 0, 2, or 4 to the output of IAR to thereby increment the instruction address by a corresponding number of 0, 1/2 or 1 word boundary units. Of the incrementing controls associated with the increment adder 89, only the one for incrementing the instruction count by four byte units, or one word address, is shown since that is the only one of interest in connection with STM mode sequency. The gates which control this four unit incrementing action are indicated at 96. These gates are controlled by outputs 97 of an OR

circuit 98 which combines the relatively exclusive outputs of two AND circuits 99 and 100. AND circuit 99 is effective during the first part (I) of an STM R/W cycle to transfer basic clock pulses CP, synchronous with the clock pulses delivered to input line 101 of cycle counter 75, to OR circuit 98, providing that the control line designated  $OP_{10}$  is inactive ( $\overline{OP}_{10}$ ). AND circuit 100 is effective in PSM mode sequencing to transfer the clock pulses (CP) to OR circuit 98 providing that a signal is present on the control line designated  $OP_j$ .

In PSM operation, data addresses are supplied to SAR via external gate connection 37A and gates 86 or via gates 86, 32 and 33. Instruction address information is supplied to SAR from IAR via gates 90 and 86, with appropriate increments added to the instruction address via the gates 96 or other gates not shown. Instruction addresses are supplied to IAR via the incrementing path 90, 88, or via the computer register path 32, 33, or via a direct connection from the output 30 of the SDR register 62 and the gates 32 and 88.

In STM mode sequencing, storage addresses are supplied to SAR only through the gating path 90, 86 and instruction addresses are supplied to IAR through either the incrementing path 90, 88 or the branch address input path 30, 32, 88 from SDR.

In either the STM or PSM mode of sequencing, the outputs  $OP_0$  to  $OP_{15}$  of the test subset decoder 10 control a unique set of micro-operations listed in the table of FIG. 10 which are discussed below.

#### SEQUENCE CONTROLS AND CONNECTIONS THERETO FOR TESTING

Referring to FIG. 3 the sequence controls of the subject data processing system comprise a control store including capacitor read only store (also denoted ROS) matrix 120 which is addressed in accordance with 12-bit words of address information contained in a read only store address register 121 (also denoted ROSAR). ROS reacts to signals furnished on its control input 122 to transfer 90 bit output signals in parallel through gates 123 into its output buffer register 124 (denoted ROSDR for Read Only Store Data Register).

The particular embodiment herein comprises a matrix of crossed pairs of row input drive wires and column output sense wires, at the crosspoints of which the row pairs are variably coupled to the column pairs by pairs of capacitive couplings which represent binary complements of each other whereby different binary patterns of column output control signals are obtained by energization of different row drive wires. A typical store of this type is disclosed for example in the IBM Technical Disclosure Bulletin, vol. 5, No. 8, pp. 47-48, by C. E. Owen et al., in the article entitled, "Read Only Memory." ROS contains 90 pairs of sense wires and 2,816 pairs of row lines for producing 2,816 distinct 90-bit control fields, otherwise known as microinstructions.

Upon excitation of ROS by a signal on the connection 122, a 90-bit signal is presented to the gates 123. The latter are energized at an appropriate instant of time by strobe signals furnished by an internal source (not shown) via the control coupling link 125. Eighty-four of the 90 bits of each output of ROSDR are applied through the connection 126 to the subset decoders 4. These branch into the test subset decoder path 13 and the other decoder input paths 127. Six of the ROSDR output bits are applied via the path connection 128 to an input of the address selection matrix 129 which, in PSM operations, cyclically selects the next address input to ROSAR. These bits can be combined with six other bits supplied through the path connection 130 or the path connection 131 to form a twelve-bit address, or all twelve bits of the address can be supplied through path connection 132. For one particular condition on the connecting lines 127 the decoders 4 are effective to provide a signal  $OP_p$  which

translates six address bits on connecting lines 130 together with six bits on connecting lines 128 through the matrix 129 into ROSAR. Of the six bits on line 130 in such operations, four are microinstruction bits contained in the field 127 and two are variably derived branch control bits. When the decoders 4 select line  $OP_n$ , the gates 133 are energized to transfer four program instruction bits from a computer register within the block 2 of FIG. 1 via connecting lines 131 together with the bits on lines 128 to produce ten of the twelve next address bits, the last two bits being 0's in this type of transfer. When an interrupt condition occurs, gates 134 are energized to supply an entire 12-bit address on lines 132 which is carried through the selector matrix 129 directly into ROSAR. Thus, the selection of a next control address can be conditioned in one of three ways to produce the required microprogram sequencing.

Upon occurrence of an interrupt condition, the previous address contents of ROSAR are transferred by gates 135 to a backup register (not shown) within the computing unit 2 (FIG. 1), and upon termination of the appropriate interrupt microprogram sequence, the same information is transferred back to ROSAR, from the backup register, via the gates 136.

ROSAR can receive a twelve-bit address word from one other source—namely, the SDR register coupled to the erasable matrix S of FIG. 2—via the gates 137. When this path is energized, all other address signal paths are suppressed.

Actuation of the matrix ROS is determined by signals produced by the logic circuit indicated generally at 140, including the OR circuit 141, and the two AND circuits 142 and 143 which produce relatively exclusive outputs. AND circuit 142 is operated periodically in PSM operation by clock pulses CP which transfer through the OR circuit 141 to cyclically actuate the ROS matrix at intervals of one-half microsecond. AND circuit 143 can be selectively actuated in the fourth section (IV) of a two microsecond cycle by an  $OP_7$  signal from the test subset decoder 10 of FIG. 1. Thus, in STM mode sequencing, ROS operates only when  $OP_7$  is selected by the SDR information on lines 12 (FIGS. 1 and 2). As indicated by the output branch 144 from the output of AND circuit 143, gates 137 are energized by each output from AND circuit 143 to pass a 12-bit address signal into ROSAR from the register SDR, via the SCAN-OUT bus, whereby ROS is operated to transfer a 90-bit signal into ROSDR from an ROS address specified by SDR information.

In a matrix such as 120 with extensive extraneous capacitive coupling between the drive and sense lines, it is necessary to time or strobe the output signal (i.e. via the gates 123 and strobing connection 125) with a high degree of precision so as to sample or capture the sensed information at its peak. For each individual word position in the matrix, this is not particularly difficult to accomplish. However, the 2,816 word outputs of the matrix may occur at relatively different phases of a control cycle with reference to the rise time of the pulses CP which initiate the excitation of the matrix drive lines, due to inductive and capacitive differences in the various coupling paths. Thus it is necessary to compromise the position of the strobing signal so that it occurs at a relatively optimum point for all output words and over a given range of supply voltage variation. For this reason it is necessary to precisely adjust the timing of the internal strobing signal of ROS when the matrix is initially assembled, when the timing adjustment varies with use of the equipment in the field, and when a modification to the matrix is made in the field. Concerning the latter it should be noted that the ROS matrix is of semi-permanent modular construction and includes a number of sub-matrix cards or boards which are assembled into a complete matrix on a plug-in basis. In making a field substitution of one board or set of boards for another board or set of boards, a completely new set of extraneous cou-

pling and marginal voltage operating conditions is introduced into the matrix system which requires extensive readjustment of the strobe timing.

In any event, adjustment of the strobe timing requires the use of a control external to the ROS system itself for selecting the address to be examined in any particular cycle, since the address selector matrix 129 is at least partially dependent upon information in the current output field produced by ROSDR, and since the latter is or may be of uncertain character prior to adjustment of the strobe timing. It will be shown below that with the connections controlled by gates 137 and certain other connections more fully described below, the general purpose erasable store 1 (FIG. 1) can be used interchangeably with the ROS system 3 to control the subset decoder, or micro-operation selector, 10 to produce a sequence of scan, compare and address branching micro-operations for effectively testing any and all elements of the ROS system including the strobe timing adjustment.

Five scan-in connecting paths controlled by respective gates 150-154 provide subset scan-in connections from the ROS system to the SDR register of FIG. 2, for testing the entire ROS system. Gates 150 to 154 are respectively controlled by test subset decoder outputs  $OP_1$  to  $OP_5$ . Scan-in connections 150-153 connect ROSDR to SDR in groups of at most 31 bits. Scan-in connection 154 connects the 12 bit output of ROSAR to SDR. For convenience the timing controls of all of these scan-in connections are shown by a single set of gates 156. Although the logic for this is not shown in the figure, the gates 156 are operated by the combination of one of the early clock pulses CP shown in FIG. 6 together with a control signal I or PSM.

FIG. 6 illustrates the time relationships between the early and late CP clock pulses and the section I-IV of an R/W cycle. As shown in FIG. 6 an R/W cycle of the matrix S begins and terminates with the start of a CP pulse. The R half of the cycle coincides with sections I and II and the W half of the cycle coincides with sections III and IV. With the exception of  $OP_7$  all of the actions produced by the outputs of subset decoder 10 in STM sequencing take place in section 1 of an R/W cycle. Notice that there is an early clock pulse coinciding with the terminal part of each section and an ordinary clock pulse coinciding with the initial part of each section. The actions controlled by  $OP_1$  to  $OP_5$ ,  $OP_8$ , and  $OP_{12}$ , which are the scan-in operations for transferring test information to SDR, all occur during the period coinciding with the early clock pulse in section I, and all other operations are executed during the period coinciding with the ordinary clock pulse in section I. The SDR reset occurs prior to the early clock pulse in section I.

#### TEST SUBSET DECODER

With reference to FIG. 4, decoder 10 includes four AND circuits 27 having respective input connections to four positions, 32-35, of the 36 positions, 0-35, of SDR. Positions 32-35 are parity bit positions during ordinary PSM operation. Another set of four AND circuits 28 is coupled to respective ones of four lines 13 controlled by outputs of ROSDR. Circuits 27 and 28 are subject to relatively exclusive control by the STM and PSM lines respectively coupled thereto.

Outputs of circuits 27 and 28 are combined in pairs by four OR circuits 170. The outputs of the latter are conditionally sampled and held by a combination of gates 171 and latching flip-flop circuits 172, the latter having a reset input 173 whereby its output can be set to the binary combination of conditions 0000 for selecting  $OP_0$ .

The 4-bit output of latch circuits 172 selects a corresponding one of the 16 control lines  $OP_0$  to  $OP_{15}$  via a 1 of 16 selecting network 174, details of which are not shown since such networks are now considered old in the art. The sampling action of gates 171 is controlled by the combination of a clock pulse CP and control signal III

or PSM, acting through AND-circuit 175 and OR-circuit 176. An additional control line is connected to AND-circuit 175 to permit manual or other control to be exercised over sequencing whereby a test program may be loaded into S and IAR set to an initial test address when the PSM controls are known to be functioning incorrectly. If the PSM controls are operating well enough to load a program into S although perhaps not well enough to continue operation under marginal supply voltage conditions, it is a relatively simple matter to switch to PSM mode ( $OP_8$ , FIG. 10) for program loading. But if this can not be done, an arrangement such as that provided by flip-flop 177 and AND-circuit 178 can be used to block AND-circuit 175 in response to the combination of  $OP_{11}$  and I or PSM, to hold the latch output at  $OP_{11}$ . This blocks gates 77 (FIG. 2) thereby preventing R/W cycling of 5 via OR-circuit 98. When the flip-flop is reset the latches 172 are reset to select  $OP_0$  and STM cycling resumes with operation of matrix S and latches 172.

During FLT program loading other controls not shown condition SAR and IAR to cycle S in W cycles via the write controls 67 (FIG. 2), to load an FLT program segment into S, after which IAR is conditioned to store the address of the first FLT test word, and a signal is given via 179 to reset flip-flop 177 to the active state and via 173 to reset the latch circuits.

#### TEST CIRCUIT

Test circuit 15, as shown in FIG. 5 includes a 36 input AND circuit 200 the inputs of which connect to the 36 output positions of SDR and the output of which is energized only for an all ones input condition. The output of circuit 200 is applied to another AND circuit 201, which can be conditioned to produce an output pulse by the combination of an all ones output from 200, a clock pulse CP, an operation control condition  $OP_{15}$ , and an output from OR circuit 202. OR circuit 202 delivers an enabling output continuously in PSM mode and during the I section of each STM cycle.

A pulse output from 201 switches a binary trigger 203 (BT) to its complementary state. Two such pulses therefore leave BT in the state it was in prior to the first of the two pulses. BT is reset to an initial reference state ( $BT=0$ ) by the combination of CP,  $OP_7$ , and PSM or I, acting through OR-circuit 202 and AND circuit 204. The output of BT is applied to an AND circuit 205 which reacts to the combination of  $BT=0$ , CP,  $OP_{14}$  and PSM or I, to produce the signal  $OP'_{14}$  which controls the transfer of a branch address from SDR to IAR via gates 32 (FIG. 2), whereby a branch test sequence can be initiated starting from a new address in S.

#### Example 1.—ROS tests

The coordinated operation of the apparatus thus far described can be more fully understood by referring to the tabular descriptions of application thereof given in FIGS. 7-10 together with the following explanations thereof. The first example of operation given in FIGS. 7A and 7B relates to the testing of the ROS control store, including the strobe timing as previously mentioned, by means of the relatively independent STM controls including the matrix S and the test subset decoder 10, test circuit 15, and the SCAN-OUT and SCAN-IN bus connections shown in FIGS. 2 and 3.

At the top of FIG. 7A a time scale is provided which indicates the relative timing of sections I-IV of an STM cycle. As indicated, these sections each have durations of 500 nanoseconds (abbreviated ns) or one half microsecond. For convenience the start of each 125 nanosecond quarter of an STM section is denoted by a letter subscript; the first quarter for example starting at  $I_A$ , the second at  $I_B$ , and so forth.

Prior to initiating a test sequence, a test program segment is entered into S as previously described and IAR is set to an address which is four less than the address of

the first test word. In the first test cycle, the IAR address incremented by four is circulated to SAR and IAR, and S is actuated to commence an R/W cycle. In the R part of each such cycle, SDR is reset and the test word stored at the address specified by SAR is strobed into SDR. SDR is reset at approximately  $I_D$  and the sensed information in the matrix S is strobed into SDR at approximately  $III_A$ . This first test word contains as its control segment (bits 32-35) the code combination 0111 for selecting  $OP_7$ . Hence, this code is latched during section III in the circuits 172 (FIG. 4) while the regenerate or W half of the R/W cycle is taking place.

During section IV and the initial part of section I, the operations controlled by  $OP_7$  are executed. Twelve SDR bits are transferred to ROSAR via the OUT-BUS and SCAN-OUT BUS (FIG. 2) and gates 137 (FIG. 3) and ROS is operated for one cycle via the control connection 122 (FIG. 3) to strobe a 90-bit word into ROSDR. The correctness of this word can be tested by the other test words of the sequence being described. At the beginning of section I of the next cycle, BT (FIG. 5) is reset to 0.

In the second STM cycle, the output of OR circuit 98 (FIG. 2) again initiates the transfer IAR plus 4 to IAR and SAR, and another R/W cycle relative to the next word address in S is commenced. Bits 32-35 of the second test word strobed into SDR are latched during section III of this cycle. These bits constitute a code for selecting one of the five SCAN-IN control operation lines  $OP_1$  to  $OP_5$ . The selected OP is executed after the SDR reset in section I of the next R/W cycle for reasons which are explained below. In section I of the third STM cycle the contents of IAR, incremented by four, are transferred to SAR and IAR, an R/W cycle is commenced, and SDR is reset. Then (see FIG. 6) a selected one of the control operations  $OP_1$  to  $OP_5$  is executed by a selective transfer of information to SDR from either ROSAR or ROSDR.

Referring to FIG. 10,  $OP_1$  transfers ROSDR bits 0-30 to SDR,  $OP_2$  transfers ROSDR bits 31-55 to SDR,  $OP_3$  transfers ROSDR bits 56-87 to SDR, and  $OP_4$  transfers ROSDR bits 88 and 89 to SDR.  $OP_5$  transfers the 12 address bits in ROSAR to SDR. Each such transfer is carried out with reference to pre-assigned bit positions in SDR, excluding the control bit positions 32-35. Since the scanned information is placed in SDR after the SDR reset, the third test word strobed into SDR during section III will be superimposed over (i.e., "OR'd" with) the scanned information. This third word is a mask word determined by programming which consists of one zero bit in a selected one of the SDR positions 0-31 and one bits in all of the other 35 positions. Thus, the OR'd combination of the mask word and the scanned information will consist of either one zero and thirty-five ones or all ones, depending upon the condition of one particularly placed bit in the scanned information.

Since the scanned information is excluded from stages 32-35 of SDR these stages will contain four ones, which constitutes the code for selecting  $OP_{15}$ .  $OP_{15}$  is executed (BT complemented if SDR contains all ones) at the beginning of section I of the next (fourth) cycle prior to the SDR reset. During this same section I a new R/W cycle is commenced with the transfer of IAR plus 4 to SAR and IAR. The fourth test word is a reference word determined by programming consisting of all ones, or one zero and thirty-five ones, corresponding to the expected condition of the OR'd mask and scanned information combination. Thus,  $OP_{15}$  is again latched during section III of this fourth cycle and is executed at the beginning of the next (fifth) cycle (FIG. 7B). If the reference and "OR'd" words are the same in both cycles of execution of  $OP_{15}$  they will produce the same effect (i.e. BT will either remain unenergized through both cycles or it will be stepped twice). On the other hand, if the reference and "OR'd" words are different BT will be complemented in one cycle and unenergized in the other cycle. Since BT

is reset to the state  $BT=0$  between cycles 1 and 2, it follows that the state of BT after the fifth cycle will be either 0 or 1 depending upon whether the reference and "OR'd" words are the same or different. Since these words can only differ in a selected bit position determined by programming, it also follows that the state of BT will be determined exclusively by the scanned information in that bit position. It is therefore significant and constitutes a feature of this invention that the state of BT can be made to correspond to a single bit in a group of scanned bits, without any physical selecting circuits having been employed to designate that bit or distinguish it from the others.

In the fifth cycle, the operations IAR+4 to SAR and IAR, cycle S, and reset SDR, are executed. During section III of this cycle the fifth test word is latched in SDR. The control bits in this word, which constitute the code 1110 for selecting  $OP_{14}$ , are latched in the decoder latches 172 of FIG. 4. Referring to FIG. 5 it is seen that during section I of the next (sixth) cycle, if BT is 0, due to having been stepped either twice or not at all,  $OP_{14}$  will act through AND circuit 205 to transfer a clock pulse to control line  $OP'_{14}$  to initiate a transfer of bits 12-31 of SDR to IAR.  $OP'_{14}$  also acts to block gate 88 (FIG. 2) and enable gate 32 (FIG. 2), whereby the transfer IAR+4 to IAR is suppressed, and in its place the SDR to IAR transfer is made in coincidence with the IAR+4 to SAR transfer. For reasons which are not relevant to the present discussion it was considered technically unfeasible to attempt to complete an SDR to SAR transfer in one cycle. Hence, a waiting or idle operation ( $OP_0$ ) is introduced by programming in cycle 6.

As has been noted the branch address transfer of  $OP_{14}$  is conditioned upon  $BT=0$ . Accordingly the address contained in IAR at the end of cycle 6 if  $BT=0$  will be the branch address transferred from SDR, or four more than the address in the previous cycle if  $BT=1$ . Accordingly, since  $BT=0$  represents a pass condition and  $BT=1$  represents a fail condition, the test word programmed into these two addresses will initiate different operations. The branch address information supplied to IAR from SDR is programmed to four units less than the actual address of the branch test word to be produced during the seventh cycle, so that when it is incremented by four in the seventh cycle, the correct address will be represented.

In the seventh cycle a number of options are given to the programmer. If the test indicates a failure ( $BT=1$ ), the addressed location in S may be provided with a word having the control bits for selecting STOP operation  $OP_{10}$ . Referring to FIGS. 2, 7B and 10,  $OP_{10}$  inhibits the initiation of the next R/W cycle of S by inhibiting AND circuit 99 (FIG. 2), whereby the conditions latched during the previous cycle persist. Bits 0-11 and 24-31 of this word are programmed to indicate the ROS word and bit addresses at the point of failure.

If  $BT=0$  (PASS) in cycle 7 the next word in S specifies selection of  $OP_7$ ,  $OP_8$ , or  $OP_{11}$  according to the stage of testing which has been reached. If all tests in one program load have been executed  $OP_{11}$  is specified to initiate entry of the next program load in S. If all tests in a complete series have been executed  $OP_8$  is specified to revert the controls to PSM mode of operation. In all other instances  $OP_7$  is specified.

It might be said that  $OP_7$  is not required to test a ROS bit which is not the first bit of a ROS word. But this is true only when the previous test concludes with  $BT=0$ . If it concludes with  $OP_{10}$  (STOP) due to  $BT=1$  (FAIL), before the next bit can be tested BT must be reset. Thus in S the test control information would be stored in a sequence as follows:  $OP_7$ ,  $OP_1$ , 2, 3, 4, or 5,  $OP_{15}$ ,  $OP_{15}$ ,  $OP_{14}$ ,  $OP_0$ ,  $OP_7$  (next bit test), and so forth.

A test of one 90-bit ROS DR word involves storage of at least  $7 \times 90 = 630$  test words in S. Since the capacity of S may be only 16,000 words, one FLT program load could not test more than 25 ROSDR words. It is note

worthy however that a single FLT program pass through a 16,000 word S matrix at 2 microseconds per cycle requires only .032 second, and it has been observed that in the worst situation a complete battery of tests can be executed upon the ROS system in less than five minutes, which compares quite favorably with the time ordinarily required for a human technician to execute equivalent tests.

As shown in cycle 8 in FIG. 7B, if the last test of a series has been completed successfully, the last word of this test can select OP<sub>6</sub> to return control of the system to the ROS system by resetting the supervisory switch to PSM mode. If the last test sequence is merely the last sequence of an FLT load, the last test word can select OP<sub>11</sub> to initiate the start of a new FLT program load procedure as previously discussed.

#### Example 2.—S test sequence

The example just given is illustrative of the sequence of STM operations required to test the ROS system. A sequence can also be performed in STM mode for checking the condition of the S matrix and its peripheral equipment without any hardware additional to that previously described. Referring to FIG. 8 the sequence begins with an initial set of four test cycles and continues on a conditional basis with follow-up sets of two test words as follows. The first cycle of the first set of tests is the same as the first cycle in FIG. 7A with OP<sub>7</sub> latched in the decoder latches. The important action in this cycle is the resetting of BT (FIG. 5), all other actions being superfluous.

In the second cycle the code for selecting control operation OP<sub>14</sub> is latched and the information stored in bit positions 12–31 of SDR constitutes a branch address.

The matrix S is a three-dimensional X, Y, Z matrix having a square plane configuration in the X, Y dimension with the 36-bit words extending parallel to the Z direction. By programming it is arranged that the ostensible address of the second test word addressed in S defines the location of the first word position along the main diagonal of the X, Y plane. It is further arranged by programming that each word along the main diagonal contains the address of the next consecutive word along the same diagonal in bit positions 12–31 thereof, and the code for selecting OP<sub>14</sub> in bit positions 32–35, while each word not on the main diagonal except for the word adjacent the main diagonal word, contains the code for selecting OP<sub>10</sub> (STOP). The word adjacent the main diagonal word specifies OP<sub>0</sub> (NO OP).

Thus, OP<sub>14</sub> will be selected in part III of the second cycle only if a word, in particular the first word along the main X, Y diagonal, is correctly addressed and correctly strobed into SDR. If anything other than this occurs OP<sub>0</sub> or OP<sub>10</sub> would be selected in part III, and the test would terminate in one of the next two cycles. If OP<sub>14</sub> is selected a waiting operation is performed in the third cycle such as that previously explained with reference to the sixth cycle in FIG. 7B, to allow time for the SDR to SAR branch address transfer conditioned on the state of BT. In the next or fourth cycle, assuming that OP<sub>14</sub> was selected and that a branch address was transferred to IAR during the previous cycle the information strobed into SDR should ostensibly be that located along the next word position of the main X, Y diagonal of S whereby the fourth cycle would conclude with conditions the same as at the conclusion of the second cycle except that the second main diagonal address would be tested instead of the first, and the next step in the test would be a repetition of the action indicated in the third cycle. On the other hand, if, due to a failure, OP<sub>10</sub> is latched during the fourth cycle, all operation will be halted. Thus, the test continues with repetition of the action called for in cycles 3 and 4 or it concludes upon failure.

Significant information can be gleaned from each failure. For example, inability to address any diagonal location will be indicative of an addressing failure, while inability

to address one particular address location could be indicative of a strobe timing failure due to noise in the sense lines of S, or the like. Failure to successfully address any address location in S might also be due to failure of the input parity checking circuitry associated with the program loading channel.

#### Example 3.—BT test sequence

A third example of an application for the test arrangement disclosed herein is shown in FIG. 9, and concerns the testing of the binary trigger circuit BT and its associated logic as shown in FIG. 5. The first six cycles of the test sequence shown in FIG. 9 are designed to test whether BT can be reset to the condition  $BT=0$  via its reset input control line (the output of AND circuit 204 FIG. 5) and whether it can be complemented from this state to the state  $BT=1$  by an action of the AND circuits 200 and 201 of FIG. 5 and the connections thereto. In cycle 1 BT is ostensibly set to the state  $BT=0$ , by selection of control line OP<sub>7</sub> due to appropriate programming of the first test word of information in S. In the second cycle, BT is ostensibly complemented by providing an all 1's test word in the second test address position of S which if appropriately handled would energize the AND circuit 200 shown in FIG. 5 and also select OP<sub>15</sub> to energize AND circuit 201 in the same figure. During the third cycle, the third test word strobed into SDR will contain control information for selecting OP<sub>14</sub> so that in the fourth and fifth cycles a branch address selection operation takes place according to the condition of BT. If  $BT=0$ , which means that it has failed to step even though ostensibly it should have stepped to the state  $BT=1$ , the branch address specified in SDR will be transferred to IAR to produce a control code for selecting OP<sub>10</sub>, terminating the test with a failure indication. On the other hand, if the test should successfully indicate that  $BT=1$  (note that this is the opposite of the test criterion used in the ROS tests of FIGS. 7A and 7B) the test continues with a series 6–10 designed to test whether BT can be first reset to the state  $BT=0$  and then complemented twice to produce the state  $BT=0$  again after first passing through the state  $BT=1$ . In cycle 6, OP<sub>7</sub>, selected in the previous cycle, resets BT to the state  $BT=0$  and the addressed location in S provides an all 1's word, for energizing AND circuit 200 and for selecting OP<sub>15</sub> to ostensibly complement BT. In cycle 7 the word addressed in S is again an all 1's word and again BT is ostensibly complemented to restore it to the state  $BT=0$ . In cycle 8, OP<sub>14</sub> is selected and in cycles 9 and 10 an address branch procedure is executed in accordance with the condition of BT. In this branch, if  $BT=0$  OP<sub>14</sub> is effective to transfer a branch address from SDR to IAR and the information at the branch address initiates cycle 1 of a new series of tests. If BT is not equal to 0 the current series will terminate with selection of OP<sub>10</sub>.

#### SUMMARY

The foregoing examples have shown how a general purpose erasable store not normally used for direct micro-operation control purposes can be connected into a circuit which makes use of a small portion of the special purpose permanent micro-operation controls of a data processing system to provide an efficient and economical check on the bulk of the micro-operation sequence controls of the system as well as a rapid check on the operability of the erasable store itself and of the shared control circuits. Upon successful conclusion of the entire series of tests it may be assumed that both the erasable and permanent controls are correctly operating, so that if a failure condition persists, further tests may be conducted under the direct control of the permanent micro-operation sequence controls relative to all other parts of the data processing system, including computing circuits and peripheral devices, until the fault is located.

It has been shown that the described arrangement is particularly economical in the sense that it can test parallel groups of signals one bit at a time without special circuit hardware for distinguishing or selecting the individual bits, the selecting function being performed by the use of programmed binary mask words each containing a selectively placed zero bit in an otherwise all ones field.

While the invention has been shown and described in connection with one particular embodiment thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. In a data processing system including a first internal source of microprogram sequence control signals operating at a first characteristic cyclic rate and a second internal source of program command and intelligence signals cycling at a second characteristic cyclic rate different from said first rate, an internal test sub-system comprising: 15  
comparator means:

means for supplying to said comparator means test signals derived from components within said data processing system;

means coupled to said second source for supplying reference signals for comparison to said test signals; and  
means operable in alternate modes of operation thereof to control the operation of said comparator means and signal supplying means by means of control signals obtained alternately from said first and second sources at said respective first and second cyclic rates. 20

2. In a data processor system including a general purpose erasable store having address selecting, address sequencing and sensing controls, an integral test system for testing parts of said data processor system comprising: 35

a plurality of gate-controlled test connections between said store and said parts of said data processor system;

a testing circuit connected to one of said test connections; 40

means for selectively controlling said testing circuit, said test connections, and the selecting, sequencing and sensing controls of said store to provide a coordinated sequence of basic test operations relative to parts of said data processor system; 45

means for selectively connecting the output of said store to said selectively controlling means to control the individual operations of the latter means in accordance with information held in said store; and 50

means controlled by said testing circuit in cooperation with said selectively controlling and selectively connecting means to control the address selecting controls of said store to initiate a variable branch in a coordinated test sequence. 55

3. In a data processor test system having an erasable store and plural line connections for conveying information signals in parallel sets between said store and other parts of said system, a signal testing circuit for testing individual signals of a set without special circuits for distinguishing or selecting the lines carrying said individual signals comprising: 60

means responsive to a particular set of signal conditions to produce a test indication;

means for selectively translating sets of signals obtained from said erasable store to said test indication producing means for obtaining a test indication if said particular set of conditions is present in a translated set; and 65

means for selectively superimposing a first set of signals carried on one of said plural-line connections on a second set obtained from said store to cause said translating means to translate the logical OR combinations of the signals of said first and second sets to said test indication producing means. 70

4. In a data processor test system having a store and plural line connections for conveying information signals in parallel sets between said store and other parts of said system, a signal testing circuit for testing individual signals of a set without special circuits for distinguishing or selecting the lines carrying said individual signals comprising: 5

means responsive to a particular set of signal conditions to produce a test indication;

means for selectively translating sets of signals obtained from said store to said test indication producing means for obtaining a test indication if said particular set of conditions is present in a translated set; and 10

means for selectively superimposing a set of first signals carried on one of said plural-line connections on a set of second signals being translated from said store to supply the logical OR combinations of the first and second signals as a set to said test indication producing means. 15

5. In a data processor test system having an erasable store and plural line connections for conveying information signals in parallel sets between said store and other parts of said system, a signal testing circuit for testing individual signals of a set without special circuits for distinguishing or selecting the lines carrying said individual signals comprising: 25

means responsive to a particular combination of signals in a set to produce a test indication;

means for selectively translating sets of signals from said erasable store to said test indication producing means for obtaining a test indication if said particular combination of signals is present; 30

means for selectively superimposing a set of test signals carried on one of said test indication plural-line connections on a set being translated from said store to said test indication producing means to form the logical OR combinations of the individual signals of said test and stored sets at the input of said test indication producing means; and 35

means for operating said selective superimposing means during alternate operations of said selective translating means relative to said test indication producing means to supply mixed test and store and unmixed store signals to said test indication producing means to produce consecutive test indications only when said mixed and unmixed signals are identically equal to said particular combination of signals. 40

6. In a data processor test system having an erasable store and plural line connections for conveying information signals in parallel sets between said store and other parts of said system, a signal testing circuit for testing individual signals of a set without special circuits for distinguishing or selecting the lines carrying said individual signals comprising: 45

means responsive to a particular combination of signals in a set to produce a test indication;

means for selectively translating sets of stored signals from said erasable store to said test indication producing means for obtaining a test indication if said particular combination of signals is present; 50

means for selectively superimposing a set of test signals carried on one of said plural-line connections on a set being translated from said store to said test indication producing means to apply the logical OR combinations of said test and stored sets to said test indication producing means; 55

means for operating said selective superimposing means during alternate operations of said selective translating means relative to said test indication producing means to induce said test indication producing means to produce consecutive test indications only when its consecutive stored and combined test and stored inputs are identically equal to said particular combination of signals; and 60

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means coupled to said test indication producing means and operable conditionally in response to control signals held in said store for counting the test indications produced in pairs of consecutive operations of said selective translating means.

7. A testing circuit according to claim 6 wherein said counting means includes:

a single stage binary counter;  
means for conditioning said counter to a predetermined one of its two stable states prior to a pair of operations of said selective translating means;  
means for conditionally applying the output of said test indication producing means to said counter; and  
means for controlling said conditionally applying means with information supplied from said store.

8. A testing circuit according to claim 6 wherein said test indication producing means comprises:  
an AND circuit coupled to said translating means; and  
means for controlling the transfer of a signal from said AND circuit to produce a test indication.

9. In a data processor system including a general purpose erasable store having address selecting, address sequencing and data sensing controls, an integral test system for testing parts of said data processor system comprising:

a plurality of plural-line test connections between said store and said parts of said data processor system;  
a testing circuit connected to one of said test connections;  
a control store;

means for alternatively and selectively controlling said testing circuit and said test connections and a selected one of said erasable and control stores in accordance with control information supplied by the said selected one of said erasable and control stores to provide coordinated sequences of basic test operations relative to parts of said data processor system; and  
means operable by said testing circuit acting in cooperation with said controlling means to initiate a branch selection of one of a plurality of basic operations at a predetermined phase of each said coordinated sequence.

10. In a data processing system, having an information store and a buffer register communicating directly with said store in reading cycles of predetermined duration, program controllable circuit testing means comprising:

means conditionally operable during one read/write cycle of said store to superimpose signals supplied from circuits external to said store on a word read from within said store at said buffer register to form a modified word of information in said register, the digits of which modified word are the logical OR combinations of correspondingly ordered digit elements of said external signals and said word read from within;

means operable in response to a predetermined combination of digits in said buffer register to produce a distinctive test signal indication during said cycle; and  
means coupled to said test signal indication producing means for conditionally counting the number of said test signal indications produced during a predetermined sequence of read/write cycles of said store.

11. In a data processor system including an erasable data store, a relatively permanent control store and control selector circuits responsive to sets of input signals to select individual micro-operation control lines, a test system comprising:

means adapted to interchangeably couple said data and control stores to at least one of said selector circuits to permit either store to alternatively control test micro-operations; and

means cooperative with the first-named means to control said erasable store when the latter is coupled to said selector circuits to produce a variable sequence of micro-operations.

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12. In a data processor as defined in claim 11 cooperative erasable store control means comprising:

a source of timing impulses;  
means for coupling said impulses to said erasable store to automatically cycle address controls of said erasable store through a series of address locations therein to non-destructively transfer micro-operation control information to said coupled selector circuits; and  
means responsive to an output of said coupled selector circuits to selectively vary the address sequence of said automatic cycling means.

13. In a data processing system including a general purpose erasable store, a special purpose control store, and micro-operation control selector circuits, a test system comprising:

means for alternatively coupling said general and special purpose stores to at least one of said selector circuits for controlling test micro-operations in accordance with information supplied by the coupled store;

a main signal bus for handling plural signals in parallel between said general purpose store and other parts of said data processing system including the address controls and output of said special purpose control store;

a test circuit controlled by at least one of said micro-operation selector circuits;

means controlled by at least one of said test micro-operation selector circuits for translating stored signals from said general purpose store to said test circuit in plural signal sets;

other means controlled by at least one of said test micro-operation selector circuits for selectively superimposing plural signal sets from said other parts of said data processing system on said stored signals translated to said test circuit; and

means for automatically sequencing operations of said general purpose store independently of the condition of said special purpose store.

14. In a data processing system including a general purpose erasable store and a special purpose semi-permanent control store, a test system comprising:

a main signal connection for conveying binary signals in plural-bit sets between said erasable store and other parts of said data processing system including the address controls and output of said control store;

test micro-operation selector means including latching means for retaining a plural-bit binary code signal, a test selector network responsive to the output of said latching means for selecting one of a plurality of test control lines in accordance with the said code signal, and means for alternatively coupling outputs of said general and special purpose stores to said latching means for interchangeably controlling test micro-operations in accordance with intelligence stored respectively in said general and special purpose stores;

a supervisory switch circuit for alternatively establishing first and second modes of control operation;

means coupling said switch circuit to said alternative coupling means for conditioning the latter to couple alternately to said special and general purpose stores in said first and second modes respectively;

means coupled to said test selector network and switch circuit and effective in said second mode to sequence an automatic series of operations of said erasable store to reproduce plural-bit test words stored in an ordered sequence within said erasable store at the output of said erasable store;

a test circuit controlled by said test micro-operation selector means for testing plural-bit sets of binary signals one bit at a time including a plural input AND circuit coupled to the output of said erasable store, a one-stage counting circuit having a reset input for establishing it in a predetermined one of its two

states, and means controlled by said selector means for selectively operating said counting circuit to count an impulse providing said AND circuit is operated and to selectively reset itself;

said erasable store main signal connection including means controlled by said test micro-operation selector means for selectively conveying the logical OR combinations of signal sets stored in said erasable store, and externally produced signal sets carried on said main signal connection, to said test circuit; and means controlled by said test micro-operation selector means and the output of said one-stage counting circuit of said test circuit to selectively condition the address controls of said erasable store to vary the sequence of selection of test words within said erasable store.

**15.** Testing apparatus comprising:

first means for storing a plurality of plural place binary mask words in each of which all but one variably determined digit place have identical binary values and in which said one place has an arbitrary binary value;

second means for providing plural place binary test words for examination;

third means for generating a binary valued logical function of the bits of a binary word;

fourth means for alternately supplying to said third means single words selected from said first means and composite words formed by combining mask words selected from said first means with test words produced by said second means;

and fifth means responsive to consecutive outputs of said third means for producing a pass/fail test indication representative of the presence or absence of error in a selected bit place of each test word provided by said second means.

**16.** The system improvement defined in claim **15** wherein said program information source is an erasable main store of program command and data words each having a first predetermined number of bits and wherein each output of said control store includes a group of bits of a

second predetermined number different from said first number.

**17.** In a data handling system having a control store and translational logic for translating the output of the control store into micro-instructional control signals used to control said control store and said system, the improvement for controlling said system and control store at a reduced cyclic rate from a source other than said control store, for diagnostic purposes, comprising:

a source within said system of program information signals used by said system, said source having a slower rate of signal output than said control store; switch means interposed between said program information source, said control store and a section of said translational logic for alternately coupling to said section of logic, in different modes of operation thereof, signals provided by said control store and other signals provided by said program information source; and

timing means associated with said switch means for controlling the cycling of said system and sub-system at different cyclic rates synchronous with the rates of operation of said program information source and control store when said switch is connected to said program information source and control store respectively.

**18.** The improvement as in claim **17** wherein said program command and data words include a parity character and wherein said switch is adapted when coupled to said main store to transfer as control intelligence to said translational logic only the bit orders of the parity characters in the words emitted from said main store.

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