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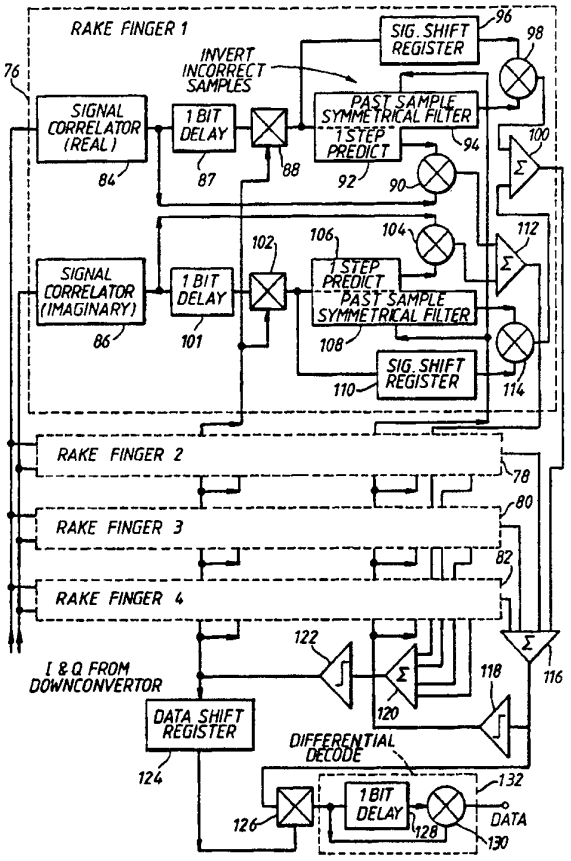
(54) **Title:** DUAL-PASS RAKE RECEIVER FOR A DIGITAL RADIO LINK BETWEEN A FIXED AND A MOBILE RADIO UNIT

(57) **Abstract**

The apparatus comprises a plurality of Rake fingers each arranged to generate a data output signal and a feed back signal. Each Rake finger includes a Wiener-like filter for an I and Q channel, and processing means for determining the nature of the feed back signal to be applied to each Rake finger to modify the input signal. Each Wiener filter has an associated past sample symmetrical filter, and an output from each Wiener filter is processed by said processing means, and an output from said past sample symmetrical filter is used to generate said output data signal.



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# DUAL-PASS RAKE RECEIVER FOR A DIGITAL RADIO LINK BETWEEN A FIXED AND A MOBILE RADIO UNIT

The present invention relates to apparatus for use in equipment providing a digital radio link between a fixed and a mobile radio unit.

Equipment for providing such a radio link is described in UK Application No 9304901.3. This application describes the use of Wiener-like filters for providing good estimates of the amplitudes of the In-phase I, and Quadrature phase Q, components of, for example, a spread spectrum pilot signal.

A known form of Wiener filter for use in a spread spectrum binary phase shift keying (BPSK) radio receiver, using a pilot signal, is shown in Figure 1.

The RF input signal is passed through a filter 2, the output of which is applied to an input of half linear multipliers 4, 6. A local oscillator 8 feeds a 0/90° phase shifter 10 which applies the local oscillator signal to a second input of the half linear multiplier 4 and a 90° phase signal to the second input of the half linear multiplier 6. The output signal from each of the half linear multipliers 4 and 6 is applied to a number of Rake fingers 10, 12, 14, 16. Each Rake finger comprises a pilot correlator 18, the output of which is connected to a Wiener-like filter 20, and a signal correlator 24, the output of which is connected to a delay circuit 26. The correlators 18, 24 each receive the output signal from the half linear multiplier 6. The output of the Wiener-like

filter 20 and the delay circuit 26 are multiplied together by a multiplier 22, the output of which is applied to a first input of an adder circuit 28. Each Rake finger also includes a pilot correlator 30, the output of which is connected to a Wiener-like filter 32. A signal correlator 36 has an output connected to delay circuit 38. The pilot correlator 30 and the signal correlator 36 receives the output signal from the half linear multiplier 4. The output signals from the Wiener filter 32 and the delay circuit 38 are multiplied by a multiplier 34, the output of which is applied to a second input of the adder circuit 28. The output signal generated by the adder circuit 28 is applied to a further adder circuit 40 which combines all the output signals from the other Rake fingers 12, 14, 16. The multipliers 22, 34 are four quadrant multipliers having several bit precision on their inputs. All the circuitry shown in Rake finger 1 is repeated in the other Rake fingers. The only difference between the different Rake fingers is that the correlators are fed with pseudo random sequences timed to correlate against signals received over different paths. The architecture shown in Figure 1 implements fully coherent maximum ratio combining over the different Rake fingers. Multiplication with the Wiener filter outputs not only compensates the phase of the signal but also weights the amplitude of each Rake component according to its signal strength prior to addition.

It will be appreciated that the circuit described above is only suitable for use with pilot signals.

With reference to Figure 2, another form of Wiener-like filter arrangement is shown which may be used in the demodulation of DBPSK (dual binary phase shift keying). When demodulating DBPSK with no pilot reference, it is still possible to obtain and exploit a carrier reference by means of decision directed carrier extraction. Here, the samples fed into the Wiener-like filter are modified according to the data decisions to provide a reference. In Figure 2 a plurality of Rake fingers are shown 42, 44, 46, 48. Each Rake finger comprises a signal correlator 50 which handles the in-phase signal and a further signal correlator 52 which handles the Quadrature phase signal. The output signal from the correlator 50 is applied to a half linear multiplier 54 by way of a 1-bit delay circuit 53. The output of the half linear multiplier 54 is applied to an input of a Wiener-like filter 56. The output of the Wiener-like filter 56 is applied to a multiplier 58. The output of the correlator 50 is also applied to a further input of the multiplier 58, the output of which is applied to a first input of an adder circuit 60.

The output signal from the signal correlator 52 is applied to a half linear multiplier 62 by way of a 1-bit delay circuit 61. The output of the half linear multiplier 62 is applied to an input of a further Wiener-like filter 64. The output of the Wiener-like filter 64 is applied to an input of a multiplier 66. The output signal from the correlator 52 is also applied to a further input of the multiplier 66, the output of which is applied to a second input of the adder circuit 60. The output of the adder circuit 60 together with the output signals from the other Rake fingers 44, 46, 48 are

applied to an adder circuit 68 which generates a combined sum of all the input signals for application to a decision circuit 70. The decision circuit 70 merely identifies whether the signal is high or low and the output of the decision circuit 70 is fed back by way of a latch circuit 71, to a second input of the respective half linear multipliers 54, 62 in the Rake finger 1, 42 and similarly to the half linear multipliers in the other Rake fingers to modify the signal applied to the respective Wiener-like filters 56, 64 in the Rake finger 1, 42 and similarly in the other Rake fingers. The output of the decision circuit 70 is applied to an input of a differential decode circuit 72 which is arranged to output data on the output line 74.

The circuit shown in Figure 2 uses hard decisions which are taken using the sum over all the Rake fingers to remove the modulation from the received signal. The most up to date available decision is the previous one so in order to remove the modulation this must be applied to the previous sample, leading to a one sample delay. This delay is removed from the derived channel estimate by using a Wiener-like filter operating as a one step predictor. Inevitably this will mean that the variance in the channel estimate will be greater than in systems incorporating a pilot which can apply symmetrical filtering.

An object of the present invention is to provide apparatus for use in equipment for providing a digital radio link between a fixed and mobile radio unit which uses a Wiener-like filter arrangement having an improved performance over the prior art arrangements.

According to the present invention there is provided apparatus for use in equipment providing a digital radio link between a fixed and a mobile radio unit, said apparatus comprising a plurality of circuit means each being arranged to generate a data output signal and a feedback signal, said circuit means including a Wiener-like filter for an In-phase channel and a Quadrature phase channel and arranged to receive an In-phase and Quadrature phase input signal respectively, processing means for determining the nature of said feedback signal to be applied to each circuit means to modify the input signal, characterised in that each Wiener filter has an associated past sample symmetrical filter, and an output from each Wiener filter is processed by said processing means, and an output from the said past sample symmetrical filter is used to generate said output data signal.

An embodiment of the present invention will now be described with reference to the accompanying drawings, in which:

FIGURE 3 shows a block diagram of a double pass decision directed demodulator in accordance with the present invention;

FIGURE 4 shows a block diagram of a dual role Wiener-like filter for use in the arrangement shown in Figure 3;

FIGURES 5 shows a simplified variation of the block diagram of the demodulator shown in Figure 3;

FIGURE 6 shows a variation of the Wiener-like filter shown in Figure 4 for use with the demodulator shown in Figure 5;

FIGURES 7 and 8 show a variation of the demodulator and Wiener-type filter shown respectively in Figures 5 and 6;

FIGURES 9 and 10 show a block diagram of a further embodiment of the present invention suitable for handling multiple phase differential phase shift keying (MDPSK), and,

FIGURE 11 shows a variation of the block diagrams shown in Figures 9 and 10.

Referring to Figure 3, a demodulator is shown having a plurality of Rake fingers 76, 78, 80, 82. Each Rake finger includes a signal correlator 84 which handles the In-phase signals and a signal correlator 86 which handles Quadrature phase signals. The correlator 84 is connected to an input of a 1-bit delay circuit 87 and to an input of a multiplier 90. The output of the 1-bit delay circuit 87 is connected to an input of a half linear multiplier 88, the output of which is connected to a one step predictor filter 92, a past sample symmetrical filter 94 and to a signal shift register 96. The output of the one step predictor filter 92 is connected to a further input of the multiplier 90. The output of the past sample symmetrical filter 94 is connected to an input of a multiplier 98, and the output of the signal shift register 96 is connected to a further input of the multiplier 98. The output of the multiplier 98 is connected to an input of an adder circuit 100.

The signal correlator 86 has an output connected to an input of a 1-bit delay circuit 101 and to an input of a multiplier 104. The output of the 1-bit delay circuit 101 is connected to an input of the half linear multiplier 102, the output of which is connected to an input of a one step predictor filter 106, an input of a past sample symmetrical filter 108, and to an input of a signal shift register 110. The output of the one step predictor filter 106 is

connected to a further input of the multiplier 104. The output of the multiplier 104 is connected to an input of an adder circuit 112, which receives at a second input the output of the multiplier circuit 90. The output of the past sample symmetrical filter 108 is connected to an input of a multiplier circuit 114, and the output of the signal shift register 110 is connected to a further input of the multiplier circuit 114. The output of the multiplier circuit 114 is connected to a further input of the adder circuit 100. Each Rake finger includes the above mentioned circuitry, and the output signals from the respective adder circuits 100 are summed by an adder circuit 116. The output of the adder circuit 116 is connected to a limiter 118 the output of which is connected to a further input of each past sample symmetrical filter 94, 108 in each Rake finger to invert the incorrect samples. The output of the adder 116 is also connected to an input of a half linear multiplier 126. As mentioned previously, each Rake finger has an adder circuit 112, the output of which is connected to the input of an adder circuit 120 which has its output connected to a limiter devices 122. The output of the limiter devices 122 is connected to a further input of each half linear multiplier 88, 102 in each Rake finger and is also connected to an input of a data shift register 124. The output of the data shift register 124 is connected to a further input of the half linear multiplier 126. The output of the half linear multiplier 126 is connected to an input of a 1-bit delay circuit 128, and to an input of a multiplier 130. An output of the 1-bit delay circuit is connected to a further input of the multiplier

130. The 1-bit delay circuit 128 and multiplier circuit 130 define a differential decode circuit 132.

The operation of the arrangement shown in Figure 3 will now be described.

The arrangement shown in Figure 3 improves the performance of the prior art arrangements of Figures 1 and 2, by combining the beneficial effects of each of those arrangements. This is achieved by taking a second pass to demodulate the data. Essentially the procedure is as follows, tentative decisions are taken on the basis of the one step predictor filter as used in the architecture shown in Figure 2. Simultaneously, these tentative decisions are used to feed a symmetrical past sample filter 94, 108 which will produce its channel estimate corresponding to the current sample at a later time. When this new sample, which should be more accurate, becomes available, it can be used to validate or contradict the previous tentative decision. Any modification to the decision is applied not only to the output but also to the second half of the contents of the longer Wiener filter.

As mentioned above, the arrangement shown in Figure 3 combines the features of Figure 1 and Figure 2, which use respectively known pilot and decision directed operations respectively. In Figure 3, the block designated 76, Rake finger 1, shows the real and the imaginary circuits drawn as mirror images. The elements closest together implement the decision directed operations of the prior art circuit shown in Figure 2, whilst the elements furthest apart implement pilot reference detection operations of Figure 1. The one step predictor and the past

sample symmetrical filter 92, 94 and 106, 108 respectively are shown combined into one block because as will be explained later significant savings in complexity can be achieved by performing the two filtering operations together.

The principles of operation are as follows. The one step predictor filter 92, 106 provides channel estimates which are used to phase align and amplitude weight the signals on each of the Rake fingers 76 to 82. These output signals from the one step predictors are combined by the adder circuit 112, after passing through the respective multipliers 90, 104 and hard (tentative) decisions are taken. The data which is fed into the one step predictor filters and the past sample symmetrical filters are corrected in sense by the decisions. For any given place in a received sequence, sometime later, the past sample symmetrical filter will produce a new, usually more accurate, channel estimate. This new channel estimate is used to phase align and weight the correspondingly delayed received signal sample. The delay in the received single sample is caused by the respective signal shift register 96, 110. The output signal from the multipliers 98 and 114 are combined by the adder circuit 100 to create new decisions. Note however, that each delayed signal sample has already been compensated by the tentative decisions.

This means that the new decisions represents the difference between the tentative decisions and the final decisions. If the output of the limiter device 122 is positive, then the original decision is validated otherwise it should be inverted. The output signal from the limiter device 122 is applied to the inputs of the

combiner circuits 88, 102 and to the shift register 124. The output from the shift register is combined with the output from the adder circuit 116 in the half linear multiplier 126, and applied to the differential decode circuit 132. Now the new decisions can also be used to correct the contents of the shift register contained in the past sample symmetrical filters. This is achieved by the feedback path from the second limiter device 118 to the Wiener filter block marked "Invert Incorrect Sample".

An implementation of a one step predictor filter and a past sample symmetrical filter will now be described with reference to Figure 4 which shows a dual role Wiener-like filter.

The Wiener-like filter comprises a shift register 136 which receives an input signal from the respective half linear multiplier 88, 102, Figure 3. An integrate and dump circuit 142 also receives the input signal. The final stage of the shift register 136 is connected to a half linear multiplier 138 which receives the Invert Incorrect Samples signal as shown in Figure 3. The output of the half linear multiplier 138 is connected to a shift register 140 and to an input of a second integrate and dump circuit 146. The final stage of the shift register 140 is connected to the second input of the integrate and dump circuit 146. The integrate and dump circuit 142 has its second input connected to one of the stages of shift register 136. The output of the integrate dump circuit 142 is connected to an input of a shift register 144, and the output of the integrate dump circuit 146 is connected to the input of a shift register 148.

The block designated 150 represents a one step predictor and comprises three multiplying circuits 152, 154, 156, each having an input connected to a respective stage of the shift register 144, and each multiplying circuit having a second input for receiving a weighted coefficient as shown. The output from each multiplying circuit is connected to an input of an adder circuit 158 which also has an input connected to the output of the second integrate and dump circuit 142. The output of the adder circuit 158 represents the output of the one step predictor which is connected to its associating multiplying circuit in Figure 3.

The symmetrical past sample filter includes adder circuits 160, 162, 164, 166. The output of the second integrate and dump circuit 146 is connected to an input of the adder circuit 160, and the second input of the adder circuit 160 is connected to the final stage of the shift register 144. The adder circuits 162 and 164 each have a pair of input lines, one of which is connected to a respective different stage of the shift register 144, and their second input is connected to a respective different stage of the shift register 148. The adder circuit 160 has an input connected to the last stage of the shift register 148 and its other input is connected to the output of the integrate and dump circuit 142. The output of the adder circuits 162, 164, 166 is connected to an input of a respective multiplying circuit 168, 170, 172. The multiplying circuits 168, 170, 172 have a further input for receiving a weighted coefficient as shown. The outputs from the multiplying circuits are connected to an input of a further adder circuit 174 which also receives the output from the adder circuit

160. The output of the adder circuit 174 represents the output of the symmetrical past sample filter which is connected to the respective multiplier in Figure 3.

The block designated 150 may be replicated, for example, three times with different coefficients according to the required filter speed.

Referring to Figure 5, this Figure shows a simplified variation of the circuit shown in Figure 3. It will be appreciated that like circuit blocks have been designated with the same numerical reference and their function is the same as that described with reference to Figure 3.

It will be seen from Figure 5 that each past sample symmetrical filter 94, 108 has an extra input to which the output from the signal correlator 84 and 86 is connected respectively. Furthermore, the signal shift registers 96, 110 also receive the output from the signal correlators 84, 86 respectively instead of being connected to receive the output from the half linear multipliers 88, 102 respectively. With the circuit connected as shown, the second half of the modulation is removed by the signal fed from the limiter device 118, and the additional input to each past sample symmetrical filter constitutes the second half of the input signal.

In Figure 5, there is no need for the data shift register 124 and the half linear multiplier 126 as shown in Figure 3. The output of the adder circuit 116 is connected directly to the input of the 1-bit delay circuit 128 of the differential decode circuit 132. It will be appreciated that the operation of Figure 5 is

essentially as described with reference to Figure 3. It should be noticed that the first half of the signal input is that which is generated from the output of the half linear multipliers 88 and 102.

The modifications to Figure 3, as discussed with reference to Figure 5, cause modification to be necessary to the dual role Wiener-like filter shown in Figure 4. It will be appreciated that the dual role Wiener-like filter shown in Figure 6 operates essentially in the same way as that described with reference to Figure 4, and therefore like circuit elements have been designated with like numerical references to that of Figure 4. It will be appreciated by reference to Figure 6 that the shift register 136 receives the second half input signals, and the first half input signals are fed directly to a further shift register 175, which has a final output stage connected to an input of the integrate and dump circuit 142. The further input of the integrate and dump circuit 142 receives the first half input signals directly.

Another variation of the circuitry shown in Figures 5 and 6 are shown in Figure 7 and 8. It will be appreciated that the circuits operate in similar manner and like elements have been given like designations. It will be seen by comparing Figure 6 with Figure 8 that with respect to the second half input there is no need for the shift register 136 and the half linear multiplier 138, which was used to remove the second half of the modulation. With reference to Figure 8, the second half input is fed directly to the shift register 140 and to the integrate and dump circuit 146. In order to achieve this economy of circuitry, the block diagram

shown in Figure 7 now includes a further 1-bit delay circuit 97 and a further combiner circuit 99 with respect to the In-phase channel and a further 1-bit delay circuit 111 and a half linear multiplier 113 in respect to the Quadrature-phase channel. In each case the 1-bit delay circuit 97, 111 receives the output from the shift registers 96 and 110 respectively, and the output from the 1-bit delay circuit is combined with the signal fed from the limiting circuit 118 by the half linear multiplier 99, 113 respectively. The outputs from the half linear multipliers 99, 113 are applied to the past sample symmetrical filter 94, 108 respectively, as the second half input as shown in Figure 8.

Referring to Figure 9, a block diagram is shown of a further embodiment of the present invention suitable for handling multiple phase differential phase shift keying (MDPSK).

A number of Rake fingers are shown designated 180, 182, 183 and 184 and it will be appreciated that each Rake finger includes the circuitry shown as described with reference to Rake finger 180. Each Rake finger includes a signal correlator 186 which receives an In-phase signal I from a down converter at an input thereof. The output of the signal correlator 186 is connected to an input of a 1-bit delay circuit 188, an input of a signal shift register 190, and to an input of a multiplier 192. An output of the signal shift register 190 is connected to an input of a multiplier 194 and an output of the 1-bit delay circuit 188 is connected to a first input of a complex linear multiplying circuit 196. A second signal correlator 198 receives a Quadrature phase signal from the down converter at an input thereof, and the

output of the signal correlator 198 is connected to an input of a 1-bit delay circuit 200, an input of a multiplier 202, and to an input of a signal shift register 204. An output of the signal shift register 204 is connected to an input of a multiplier 206. An output of the 1-bit delay circuit 200 is connected to a second input of the complex linear multiplying circuit 196. The complex linear multiplying circuit 196 has a first output connected to a past sample symmetrical filter 208 and to a one step predictor filter 210. An output from the past sample symmetrical filter 208 is connected to a further input of the multiplying circuit 194. An output of the one step predictor filter 210 is connected to a further input of the multiplying circuit 192. A second output from the complex linear multiplying circuit 196 is connected to an input of a further past sample symmetrical filter 212, and to an input to a one step predictor filter 214. An output of the past sample symmetrical filter 212 is connected to a further input of the multiplying circuit 206, and an output of the one step predictor filter 214 is connected to a further input of the multiplying circuit 202. The outputs from the multiplying circuits 194, 206 are respectively applied to an input of an adder circuit 216, 218. It will be appreciated that these adder circuits receive the outputs from the other Rake fingers 182, 183, 184. The outputs from the multiplying circuits 192, 202 are connected respectively to further adder circuits 220, 222, and it will be appreciated that the adder circuits 220, 222 receive the respective outputs from the other Rake finger circuits 182, 183, 184. The outputs of the adder circuits 216, 218 are connected to

respective inputs of a differential decode circuit 224 which generates data on an output lead 226. The outputs of the adder circuits 216, 218 may also be connected to respective inputs of a normalised amplitude and threshold nearest phase in alphabet circuit 228, the outputs from which are connected to respective inputs of a complex conjugate circuit 230. The outputs from the adder circuits 220, 222 are respectively connected to an input of a further normalise amplitude and nearest threshold phase in alphabet circuit 232, the outputs of which are connected to a respective input of a further complex conjugate circuit 234 and to inputs of a respective delay circuit 236, 238. The outputs from the complex conjugate circuit 234 are connected to a respective input of the complex linear multiplying circuit in each Rake finger such as circuit 196 in Rake finger 1. The outputs from the delay circuits 236, 238 are connected to a respective input of a further complex linear multiplying circuit 240, which also receives the outputs from the complex conjugate circuit 230. The complex linear multiplying circuit 240 has two output lines which may be connected to the complex linear multiplying circuits such as 196 in each Rake finger instead of those signals which may be generated from the complex conjugate circuit 234. When this latter connection is used, the complex linear multiplying circuit 196 has two output lines each connected to an input designated I Comp In on the past sample symmetrical filter 208 and to an input designated Q Comp In on the past sample symmetrical filter 212. The output designated I Comp Out from the past sample symmetrical filter 208 is connected to an input of the complex

linear multiplying circuit 196, and similarly the output designated Q Comp Out from the past sample symmetrical filter 212 is connected to a further input of the complex linear multiplying circuit 196.

The operation of the circuit described with reference to Figures 9 and 10 will now be described.

Figure 9 described the new implementation of the invention designed to handle multiple phase differential phase shift keying (MPDSK). Because MPDSK modulates information into the I and the Q channels separately, a full complex demodulation function is required. The first operation in the channel estimation path is to, as before, remove the effect of the data, and then to remove the modulation from the received signal. Because the modulation is now complex this has to be done by a complex linear multiplier circuit 196. This circuit receives inputs from the first past demodulator as will be described later. The outputs of the complex linear multiplier circuit 196 feed, as before, into the paired past sample symmetrical filter 208, 212 and the one step predictor filter 210, 214 and phase and amplitude weighting and compensation are applied as before in respect of the first and second past outputs. The previous outputs pass from the multipliers 192, 202 and are summed across the other Rake fingers in the adder circuits 220, 222. At this stage we have a complex signal which is phase compensated and has been optimally combined across the Rake components. For the purposes of stripping off the modulation from the received signal, a form of decision is required on these outputs. The output from

the adder circuits 220, 222 are fed into a circuit 232 which normalises the amplitude of the complex signal and thresholds it to the nearest phase in the signal alphabet, so for eight phase DPSK, for example, the thresholding would be to the nearest of the 8, $\pi$ / 4 phases. Having performed this function, the outputs are passed to a circuit 234 which performs the complex conjugate of this output, thus reversing the associated phase. This inverts the Q channel whilst passing through. The signal is then passed up to complex linear multiplier 196 for removal of the modulation. On the second pass the outputs from the multiplier circuits 194, 206 are again summed across the Rake fingers in the adder circuits 216, 218 and for the normal purposes of demodulation the output signals are fed to a differential decode circuit 224 which performs differential decoding. This operation consists of complex multiplication of the current complex sample with the complex conjugate of the previous complex sample, thus if the current complex sample is denoted Zn and previous complex sample is denoted Zn-1, the output will be Zn x Z*n-1. The demodulation then can be performed through suitable thresholding or if a form of error control coding has been applied then this complex signal may then be applied directly to the decoder.

A further attribute of the invention as described earlier, is the ability to perform the second pass compensation of data to the contents of the second half of the past sample symmetrical filter, this operation is not essential to the working of the invention but will improve performance. If required then the blocks shown within the dotted outline 242 are used. The outputs of the adder

circuits 216, 218 feed into the circuit 228 which performs the same function as previously described, thus providing a phaser which has the correct decision applied to it. Now because this signal bears the modulation and it is desirable to compensate the signal that has had the modulation stripped, there is a need to remove the original stripping of the modulation from the original signal. The original stripping signal was derived from the outputs of circuit 232, and is this held over by delay circuits 236, 238. The difference between the data on the two outputs is computed in the complex linear multiplier circuit 240. The outputs of the complex multiplier circuit 240, labelled Mid-Filter Compensating Lines can then be applied to compensate the phase of the signals within the centre point of the past sample symmetrical filters through the respective outputs and inputs I Comp Out, I Comp In, Q Comp Out, Q Comp In. For clarity these operations are shown separately in Figure 6. Here, it is shown how the outputs I Comp Out and Q Comp Out are fed to a complex linear multiplier for processing by the outputs from the mid-filter compensating lines before being returned back into the filters through the I Comp In line and the Q Comp In lines respectively.

Referring to Figure 11, a variation of the block diagram shown in Figure 9 is depicted. Again, like elements have been given the same designation and function in the same manner as described with reference to Figure 9. It will be seen that the variation mainly concerns the box identified as 242. The complex linear multiplying circuit 230 is no longer used to generate signals on the mid filter compensating lines, but receives as before the

output signals from the complex conjugate circuit 230. The complex linear multiplying circuit receives signals from respective 1-bit delay circuits 236 and 238, whose inputs are connected to the outputs of the signal shift register 190 in the I-signal channel, and to signal shift register 204 in the Q-signal channel respectively. Complex linear multiplying circuit 230 generates two output signal designated e, f which are applied to the respective inputs of the past sample symmetrical filters 208, 212.

It will be appreciated by those skilled in the art that various modifications are possible without departing from the spirit and scope of the present invention. For example in Figure 4, the implementation of the combined past sample symmetrical filter and the one step predictor filter could still be as shown in Figure 4, except that the multiplier circuit 138 would be removed from this figure and the input would become I Comp Out and its output would become I Comp In or Q Comp Out and Q Comp In for the other filter.

# CLAIMS

1. Apparatus for use in equipment providing a digital radio link between a fixed and a mobile radio unit, said apparatus comprising a plurality of circuit means each being arranged to generate a data output signal and a feedback signal, said circuit means including a Wiener-like filter for an in-phase channel and a Quadrature phase channel and arranged to receive an in-phase and Quadrature phase input signal respectively, processing means for determining the nature of said feedback signal to be applied to each circuit means to modify the input signal, characterised in that each Wiener filter has an associated past sample symmetrical filter, and an output from each Wiener filter is processed by said processing means, and an output from the said past sample symmetrical filter is used to generate said output data signal.

2. Apparatus as claimed in claim 1, wherein each channel further includes a signal correlator for receiving the input signal having an output connected to a first multiplying means, the output of which is connected to the Wiener filter and past sample symmetrical filter, second multiplying means for multiplying the output from the Wiener filter with the output from the signal correlator, an output of said second multiplying means is connected to a first adder circuit having a second input which receives an output from a second multiplying circuit associated with the other channel, said first adder circuit providing an output

signal which is fed back as an input to said first multiplying means.

3. Apparatus as claimed in claim 2, wherein the output of said past sample symmetrical filter is connected to an input of third multiplying means, said third multiplying means having a second input connected to an output of a signal shift register, said signal shift register being arranged to receive the output signal from said first multiplying means, and said third multiplying means providing an output connected to a second adder circuit which at a second input receives an output from a third multiplying means associated with the other channel and is arranged to generate a data output signal of the circuit means.

4. Apparatus as claimed in claim 3, wherein the shift register has its input connected to the output of the signal correlator instead of to the output of the combiner means, and said past sample symmetrical filter is connected to receive at a further input, the output signal from the signal correlator.

5. Apparatus as claimed in claims 1, 2 or 3, wherein the data output signals from each circuit means are applied to a third adder circuit, the output of which is connected to a limiter circuit, an output of said limiter circuit is connected to an input of the symmetrical past sample filter.

6. Apparatus as claimed in claim 5, wherein the processing means comprises a fourth adder circuit connected to a limiter circuit, the output of which is connected to each first multiplying means and to an input of a data shift register which has an output connected to a fourth multiplying means having a further input connected to the output of the third adder circuit, an output of said fourth multiplying means is connected to a differential decode circuit arranged to generate the data output signal.

7. Apparatus as claimed in claim 5, wherein the processing means comprises a fourth adder circuit connected to a limiter circuit, the output of which is only connected to the first multiplying means, and the output of the third adder means is connected to the input of the differential decode circuit.

8. Apparatus as claimed in any preceding claim, wherein the Wiener-like filter and the past sample symmetrical filter comprises a first shift register, arranged to receive an input signal, said first shift register having its output stage connected to first multiplying means which has a second input for receiving a signal indicative of sample inversion, said first multiplying means having an output connected to an input of a second shift register and connected to an input of a first integrate and dump circuit, said first integrate and dump circuit having a second input connected to the last stage of said second shift register, a second integrate and dump circuit which has a first input arranged to receive the input signal, a second input thereof connected to a

further stage of said first shift register, said second integrate and dump circuit having an output connected to an input of a third shift register, having a plurality of stages connected to a one step predictor filter, said first integrate and dump circuit having an output connected to an input of a fourth shift register and to an input of a first adder circuit, said fourth shift register having a plurality of stages connected to an input of second, third and fourth adder circuits respectively, said second, third and fourth adder circuits being connected at a further input thereof to said stages of said third shift register and to the output of said second integrate and dump circuit respectively, said second, third and fourth adder circuits have their outputs connected to a first input of a respective second multiplying means each of which receive at a second input thereof a weighted coefficient signal, and said adder circuit which is connected to the output of said first integrate and dump circuit has an output connected directly to a further adder circuit which is arranged to receive the output from second said multiplying means, said further adder circuit being arranged to generate the output signal of the symmetrical past sample filter.

9. Apparatus as claimed in claim 8, wherein the first multiplying means at said second input receives a signal indicative of modulation removal, said first shift register is arranged to receive half of said input signal, said second integrate and dump circuit is connected to receive the other half of said input signal at a first input thereof, and, a fifth shift register has a

final stage connected to a second input of the second integrate and dump circuit, said fifth shift register being arranged to receive said other half of said input signal at a first stage thereof.

10. Apparatus as claimed in claims 3 and 5, wherein the signal shift register has its input connected to the output of the signal correlator and not to the first multiplying means, and the output of said shift register is also connected to an input of a delay device, the output of which is connected to further multiplying means which at a second input thereof is connected to receive the output from the third adder circuit by way of said limiter circuit, an output from said further multiplying means being connected to provide the input to the past sample symmetrical filter.

11. Apparatus as claimed in claims 9 and 10, wherein said first shift register and said first multiplying means are not used and said half of said input signal is applied directly to said second shift register and to said first integrate and dump circuit.

12. Apparatus as claimed in claim 1, wherein each channel further includes a signal correlator, for receiving the input signal, having an output connected to a first complex linear multiplying circuit having an output line connected to a Wiener filter and past sample symmetrical filter associated with each channel, respectively first multiplying means associated with each channel arranged to multiply the output from the past sample symmetrical filter with the output from the signal correlator, and

having an output connected to a first adder circuit which is arranged to receive output signals from the first circuit means associated with the said plurality of circuit means, each first adder circuit having an output connected to an input of a differential decode circuit which is arranged to provide a data output signal, second multiplying means associated with each channel, for receiving an output from the Wiener filter and an output from the signal correlator, said second circuit means having an output connected to an input of a second adder circuit, said second adder circuit being connected to an output of said second multiplying means associated with the plurality of circuit means, said second adder circuits having an output connected to first normalising means, said first normalising means having its outputs connected to a first complex conjugate means, the outputs of which are connected to two further inputs of the complex linear multiplying circuit.

13. Apparatus as claimed in claim 12, wherein second normalising means is provided, and arranged to receive the signals applied to said differential decode circuit, said second normalising means having its outputs connected to a second complex conjugate means, said second complex conjugate means having its outputs connected to inputs of a second complex linear multiplying circuit, the outputs of which are connected to said first complex linear multiplying circuit instead of the outputs from said first complex conjugate means, and wherein the outputs from said first complex linear multiplying means are respectively

connected to further inputs of the past sample symmetrical filter in each channel, and each past sample symmetrical filter has a further output connected to further inputs of the first complex linear multiplying circuit.

14. Apparatus as claimed in claim 12, wherein second normalising means is provided, and arranged to receive the signals applied to the differential decode circuit, said second normalising means having its outputs connected to a second complex conjugate means, said second complex conjugate means having its outputs connected to input of a second complex linear multiplying means, said second complex linear multiplying means at two further inputs thereof, receive the output signals from the signal shift registers associated with each channel, by way of a respective delay device, and the outputs from said second complex linear multiplying means are connected to a respective one of said past sample symmetrical filters.

15. Apparatus as claimed in any preceding claim, wherein the modulation is differential phase shift keying.

16. Apparatus as claimed in claims 1 to 14, wherein the modulation is differential binary phase shift keying.

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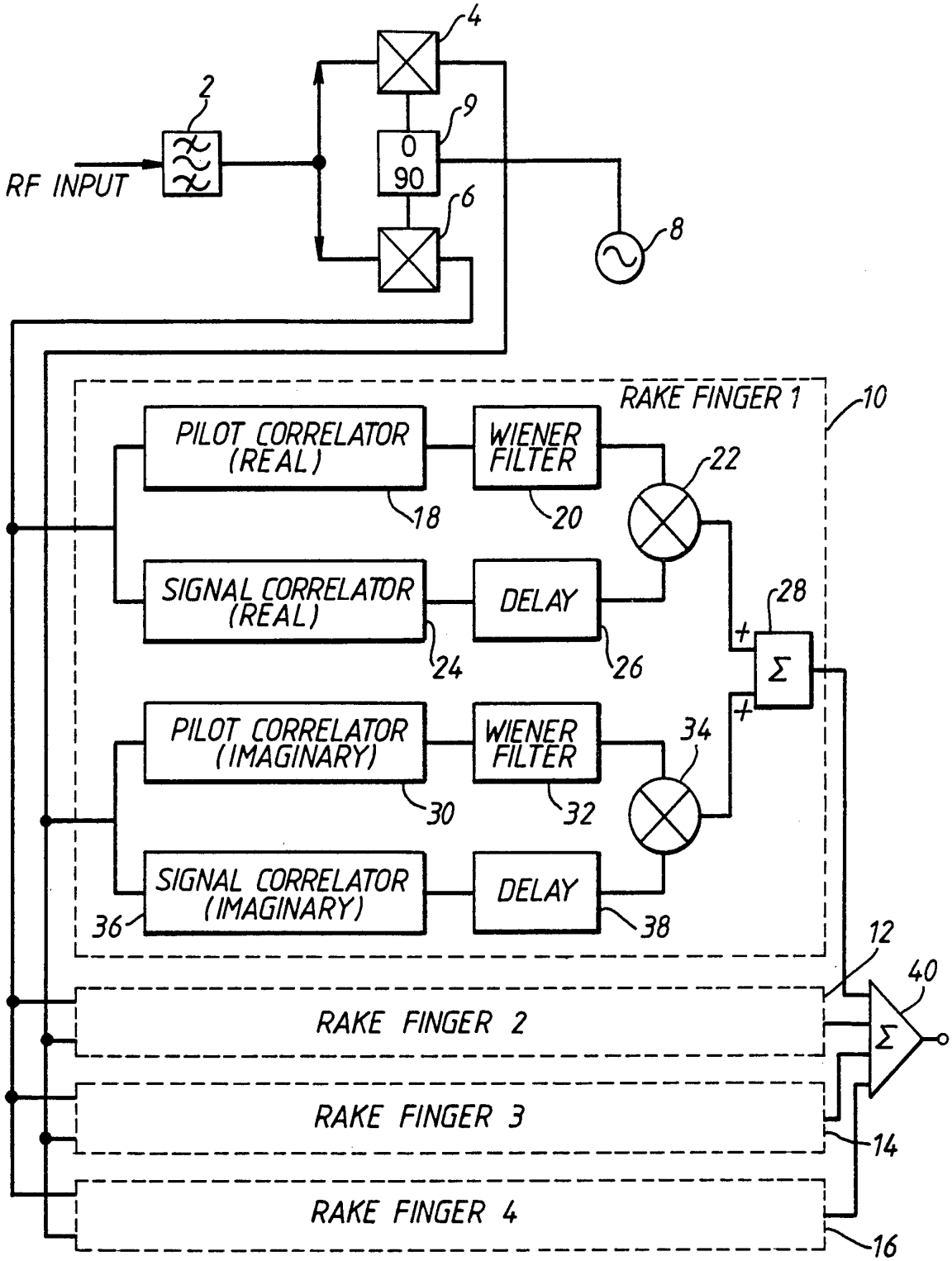
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4
9
0
90
6
8
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10
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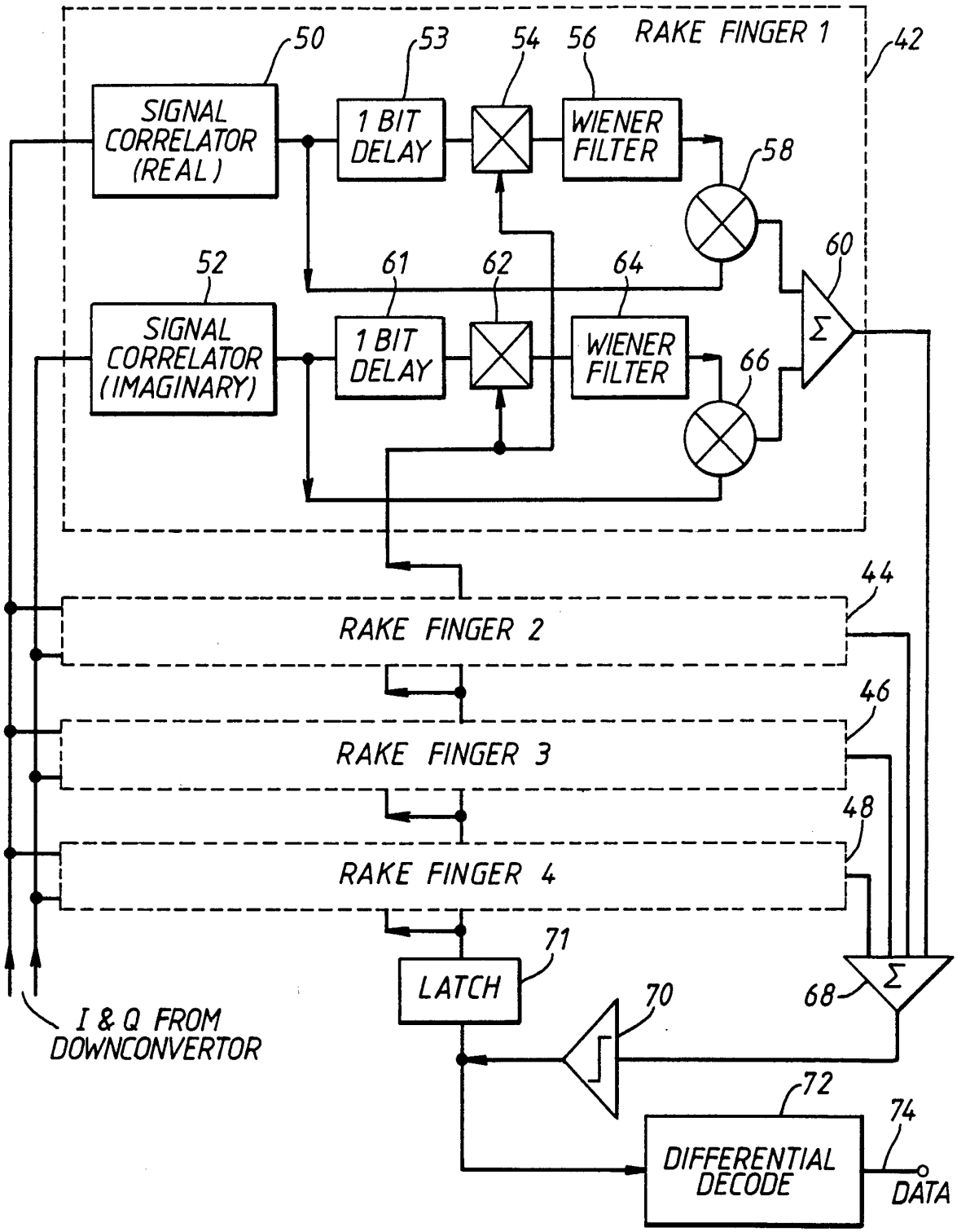
WIENER FILTER
18
20
22
SIGNAL CORRELATOR (REAL)
DELAY
24
26
28
Σ
PILOT CORRELATOR (IMAGINARY)
WIENER FILTER
30
32
34
SIGNAL CORRELATOR (IMAGINARY)
DELAY
36
38
12
40
RAKE FINGER 2
RAKE FINGER 3
14
RAKE FINGER 4
16

Fig. 1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WIENER FILTER
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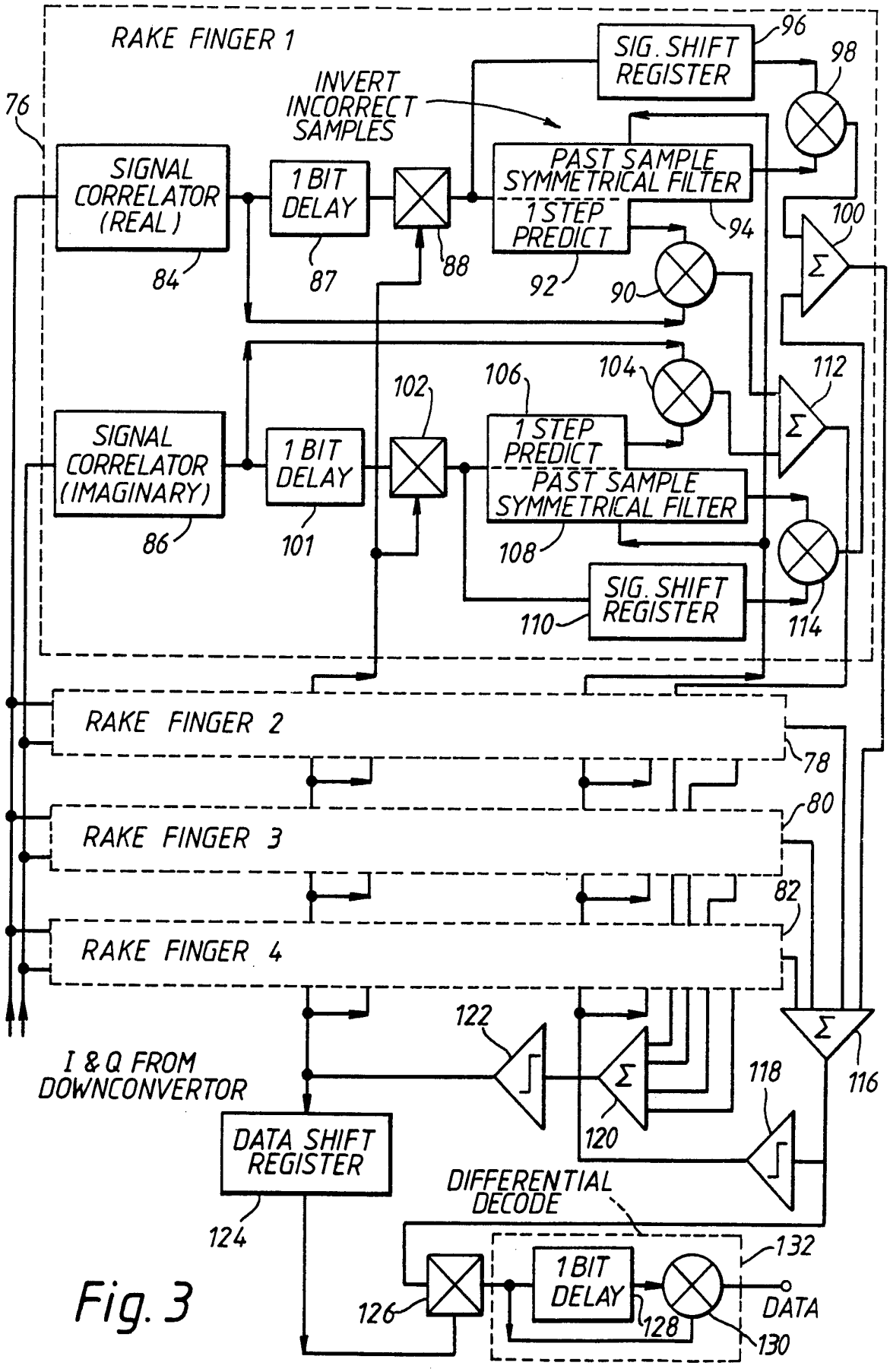
61
62
64
SIGNAL CORRELATOR (IMAGINARY)
1 BIT DELAY
WIENER FILTER
66
Σ
44
RAKE FINGER 2
46
RAKE FINGER 3
48
RAKE FINGER 4
71
LATCH
70
68
Σ
I & Q FROM DOWNCONVERTOR
72
74
DIFFERENTIAL DECODE
DATA

Fig. 2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SIG. SHIFT REGISTER
96
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SIGNAL CORRELATOR (REAL)
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1 STEP PREDICT
94
100
84
87
88
92
90
102
106
104
112
SIGNAL CORRELATOR (IMAGINARY)
1 BIT DELAY
1 STEP PREDICT
PAST SAMPLE SYMMETRICAL FILTER
86
101
108
SIG. SHIFT REGISTER
110
114
RAKE FINGER 2
78
RAKE FINGER 3
80
82
RAKE FINGER 4
122
118
116
I & Q FROM DOWNCONVERTOR
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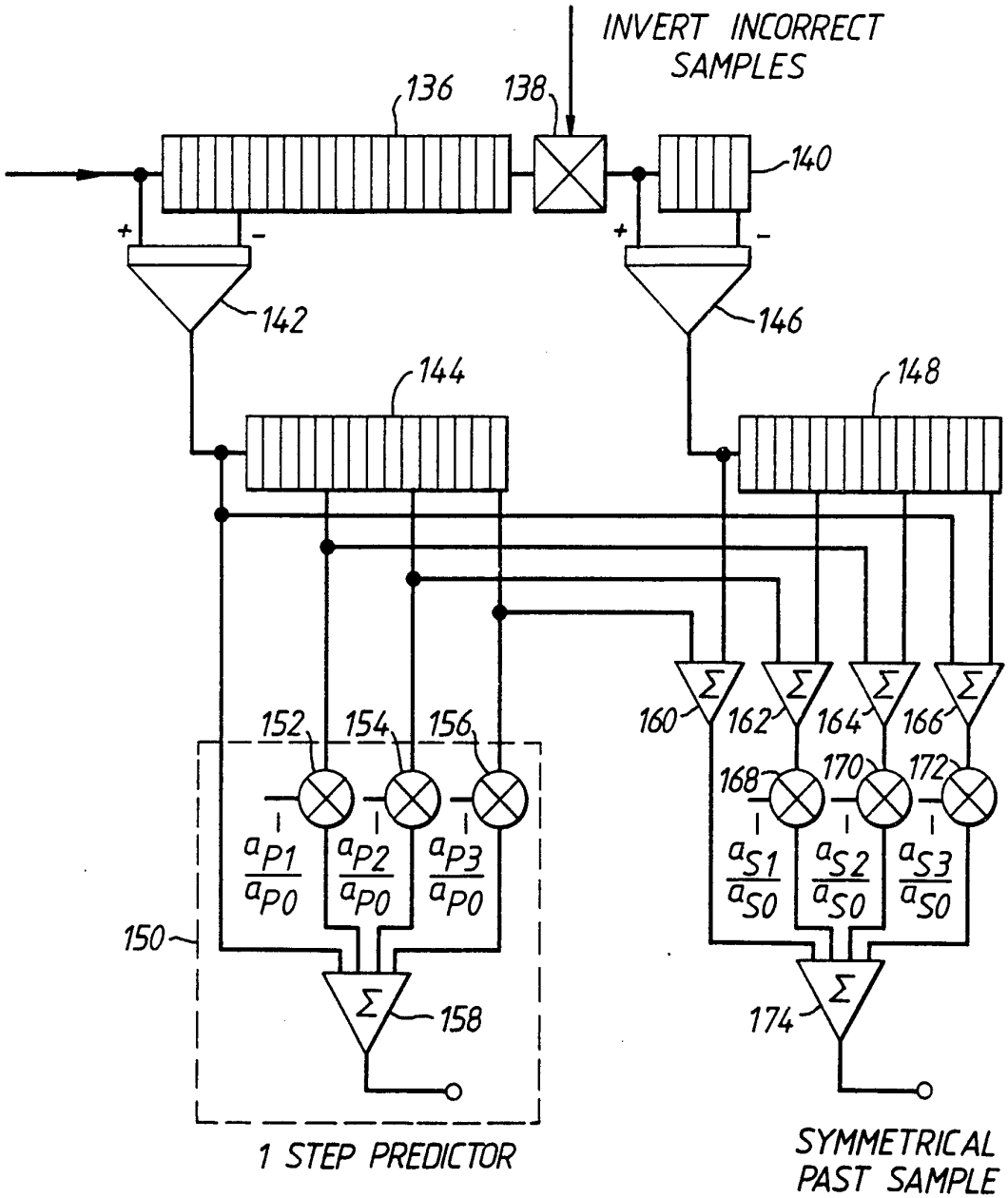
DATA SHIFT REGISTER
DIFFERENTIAL DECODE
124
132
1 BIT DELAY
126
128
DATA
130

Fig. 3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146
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166
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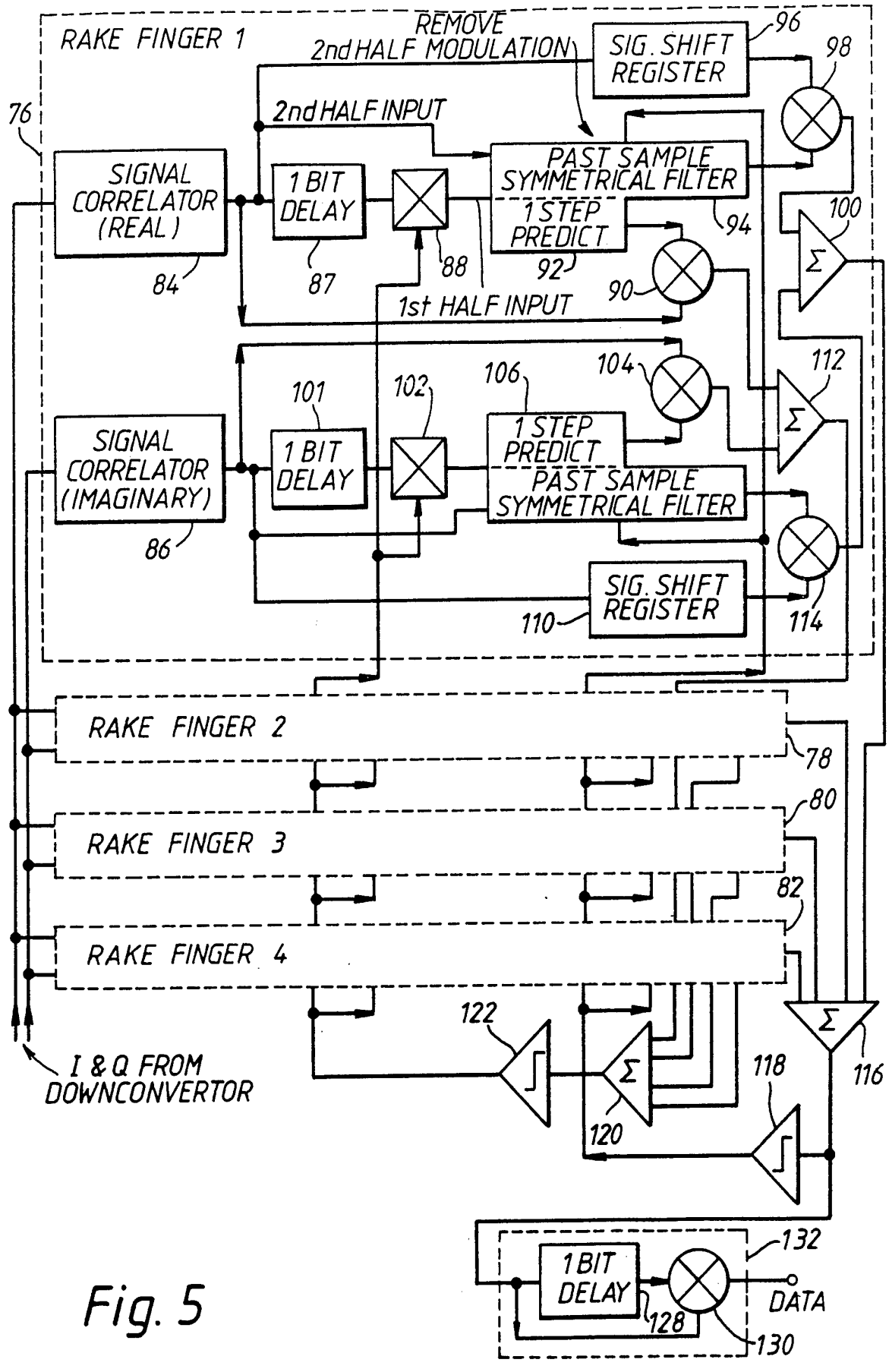
170
172
150
158
174
1 STEP PREDICTOR
SYMMETRICAL PAST SAMPLE

Fig.4


RAKE FINGER 1
REMOVE 2nd HALF MODULATION
SIG. SHIFT REGISTER
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98
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2nd HALF INPUT
SIGNAL CORRELATOR (REAL)
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1 BIT DELAY
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88
PAST SAMPLE SYMMETRICAL FILTER
1 STEP PREDICT
92
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90
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1st HALF INPUT
104
106
112
101
102
SIGNAL CORRELATOR (IMAGINARY)
86
1 BIT DELAY
1 STEP PREDICT
PAST SAMPLE SYMMETRICAL FILTER
SIG. SHIFT REGISTER
110
114
RAKE FINGER 2
78
80
RAKE FINGER 3
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RAKE FINGER 4
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116
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I & Q FROM DOWNCONVERTOR
132
1 BIT DELAY
DATA
128
130

Fig. 5

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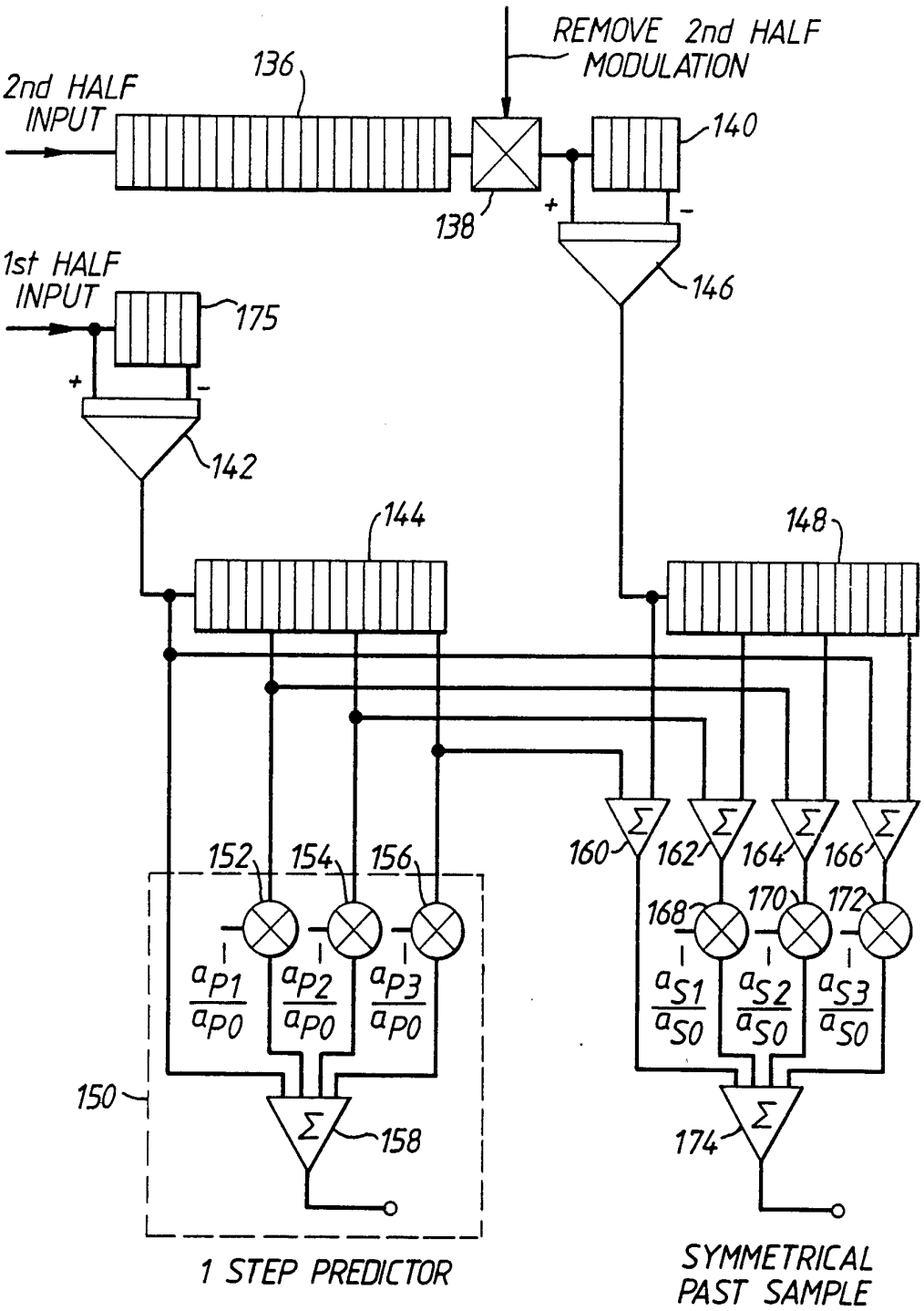
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166
168
170
172
$a_{P1}/a_{P0}$
$a_{P2}/a_{P0}$
$a_{P3}/a_{P0}$
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$a_{S2}/a_{S0}$
$a_{S3}/a_{S0}$
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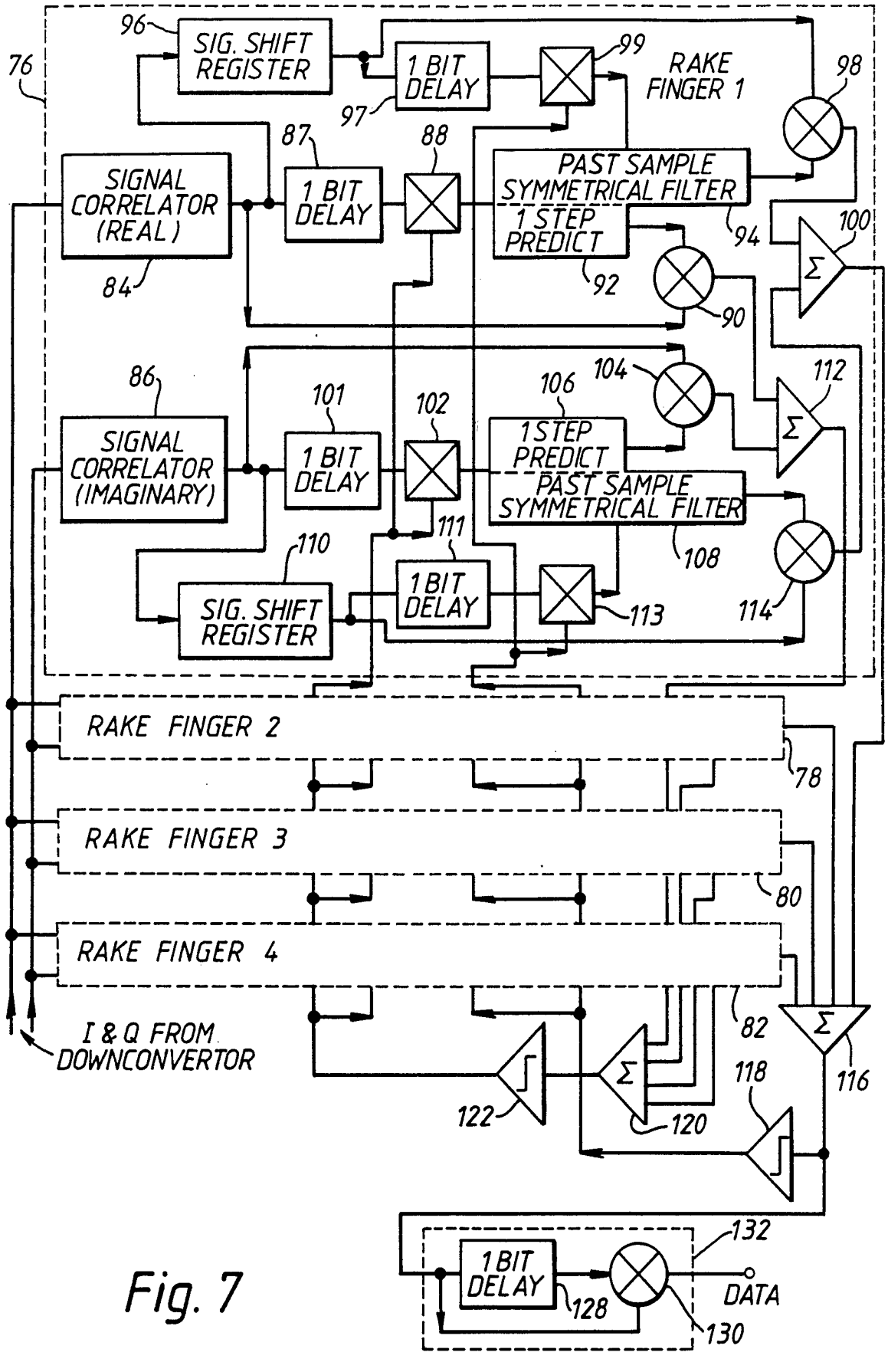
174
1 STEP PREDICTOR
SYMMETRICAL PAST SAMPLE

Fig.6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SIG. SHIFT REGISTER
1 BIT DELAY
97
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RAKE FINGER 1
98
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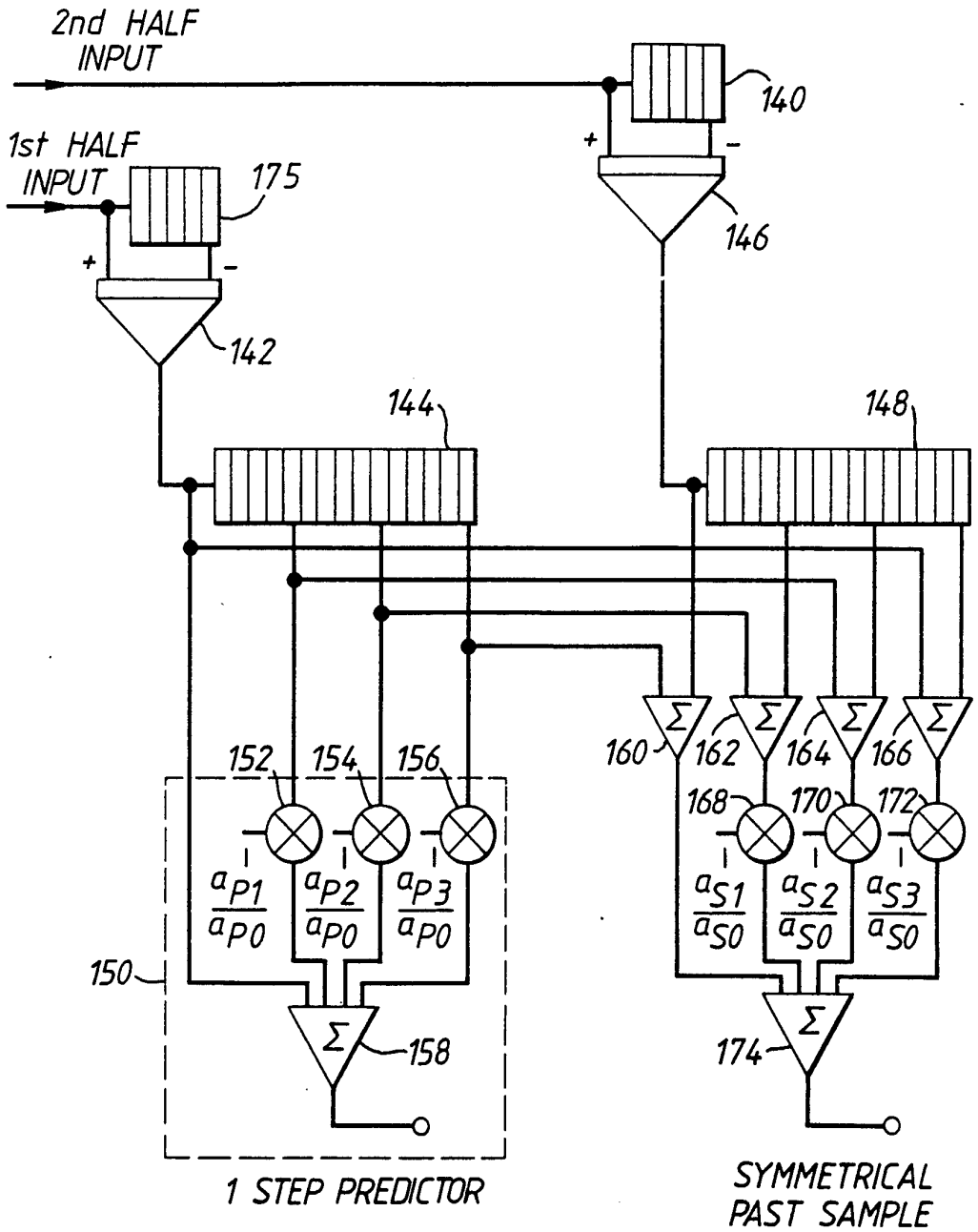
87
88
SIGNAL CORRELATOR (REAL)
1 BIT DELAY
PAST SAMPLE SYMMETRICAL FILTER
1 STEP PREDICT
94
100
84
92
90
86
101
102
104
106
112
SIGNAL CORRELATOR (IMAGINARY)
1 BIT DELAY
1 STEP PREDICT
PAST SAMPLE SYMMETRICAL FILTER
108
110
111
SIG. SHIFT REGISTER
1 BIT DELAY
113
114
RAKE FINGER 2
78
RAKE FINGER 3
80
RAKE FINGER 4
82
I & Q FROM DOWNCONVERTOR
116
118
122
120
132
1 BIT DELAY
128
DATA
130

Fig. 7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1st HALF INPUT
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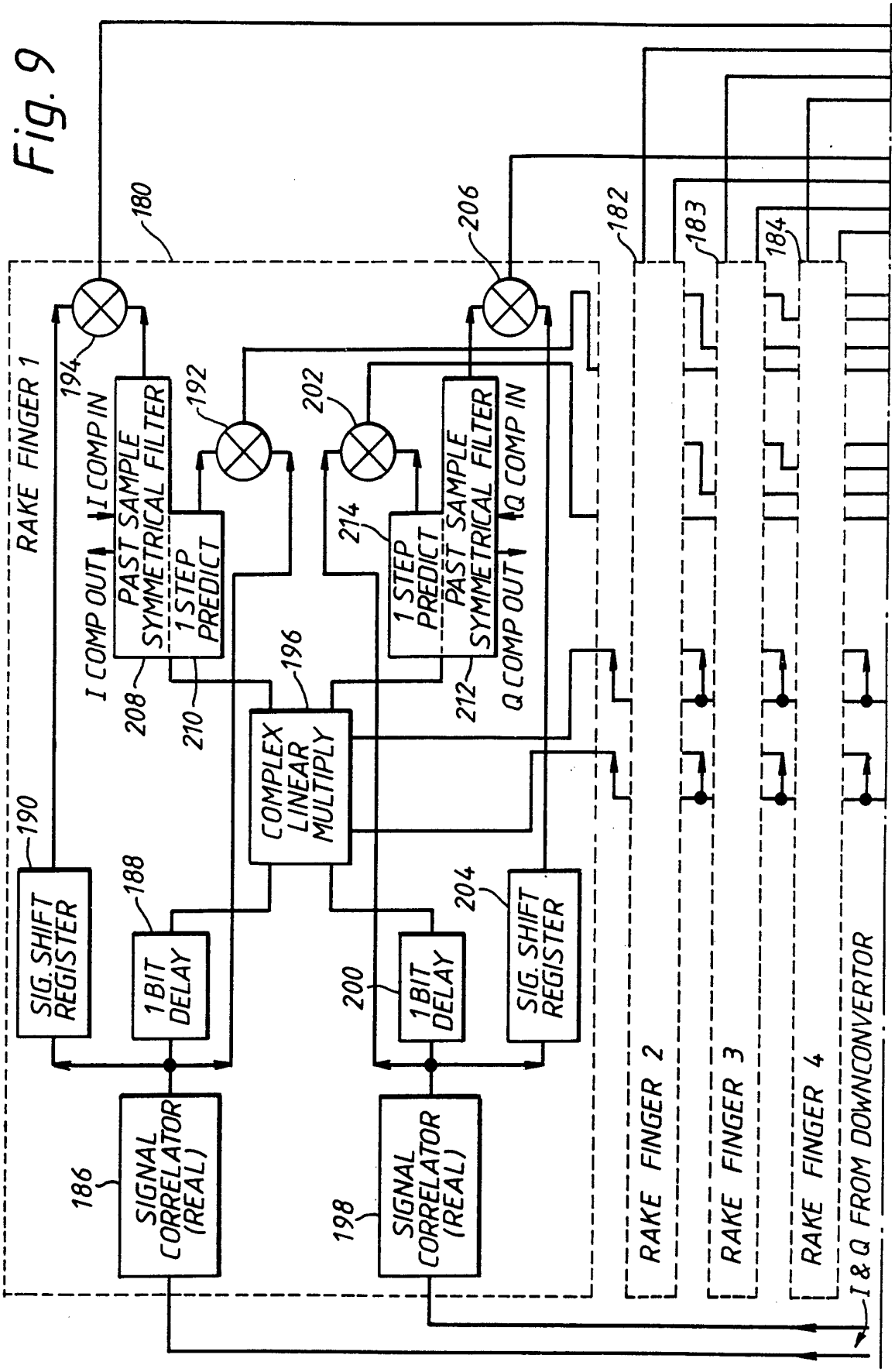
174
1 STEP PREDICTOR
SYMMETRICAL PAST SAMPLE

Fig.8

Fig. 9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I COMP IN
I COMP OUT
PAST SAMPLE SYMMETRICAL FILTER
1 STEP PREDICT
Q COMP IN
Q COMP OUT
COMPLEX LINEAR MULTIPLY
SIG. SHIFT REGISTER
1 BIT DELAY
SIGNAL CORRELATOR (REAL)
RAKE FINGER 2
RAKE FINGER 3
RAKE FINGER 4
I & Q FROM DOWNCONVERTOR
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208
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212
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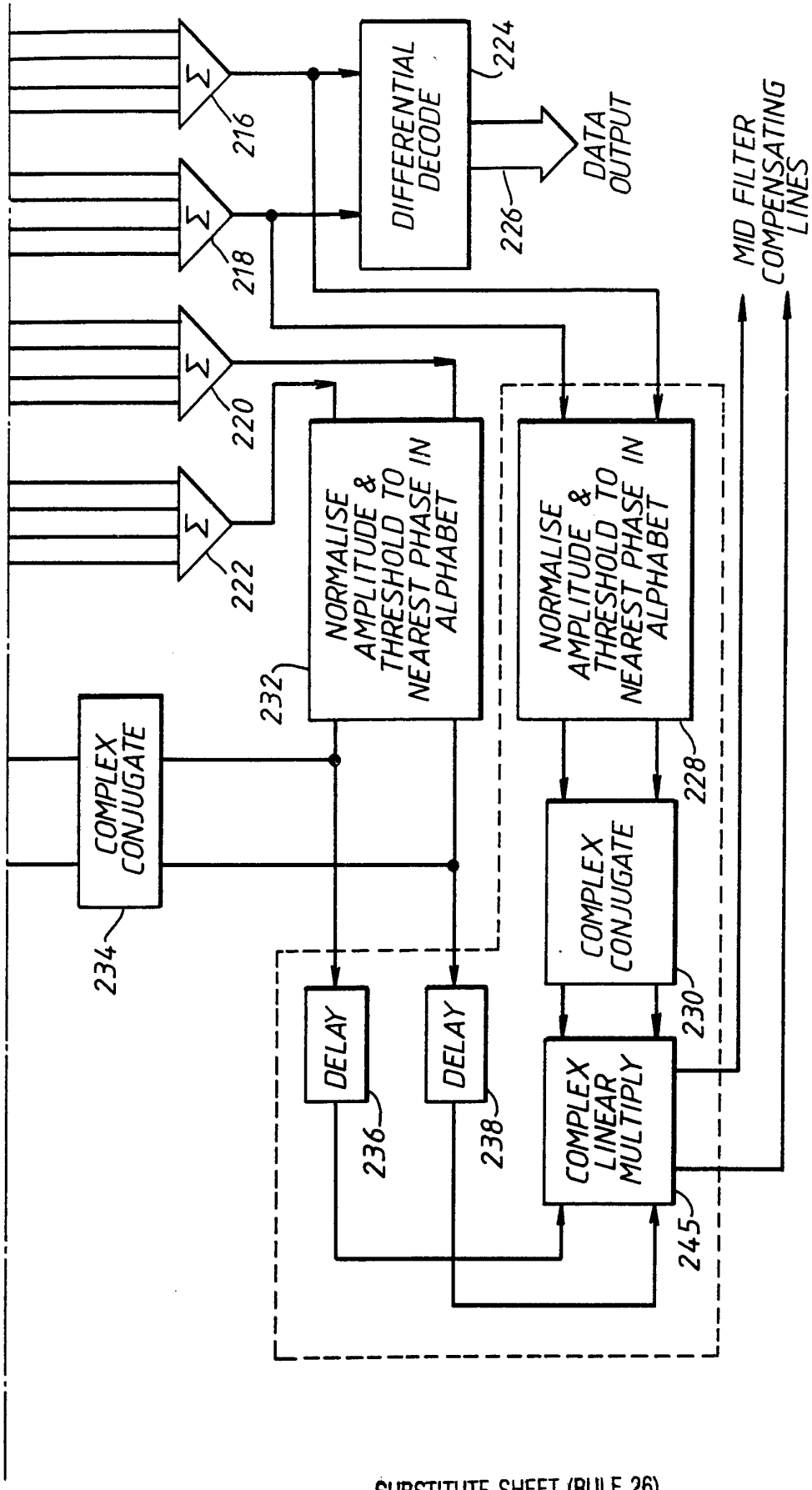
Σ
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DATA OUTPUT
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MID FILTER COMPENSATING LINES
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NORMALISE AMPLITUDE & THRESHOLD TO NEAREST PHASE IN ALPHABET
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DELAY
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COMPLEX LINEAR MULTIPLY
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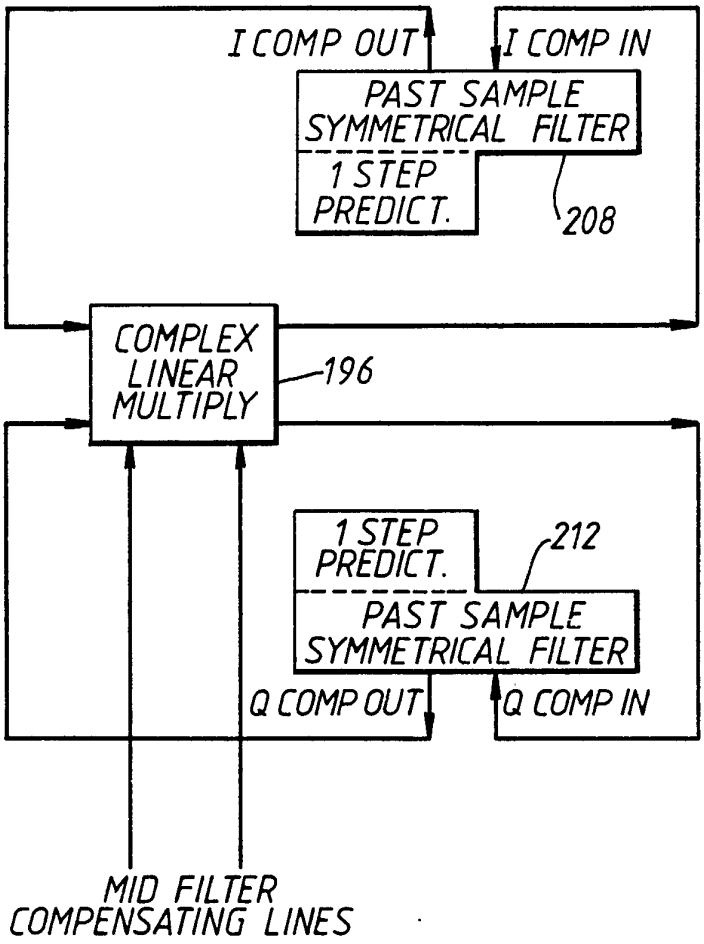
Fig. 9 cont.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1 STEP PREDICT.
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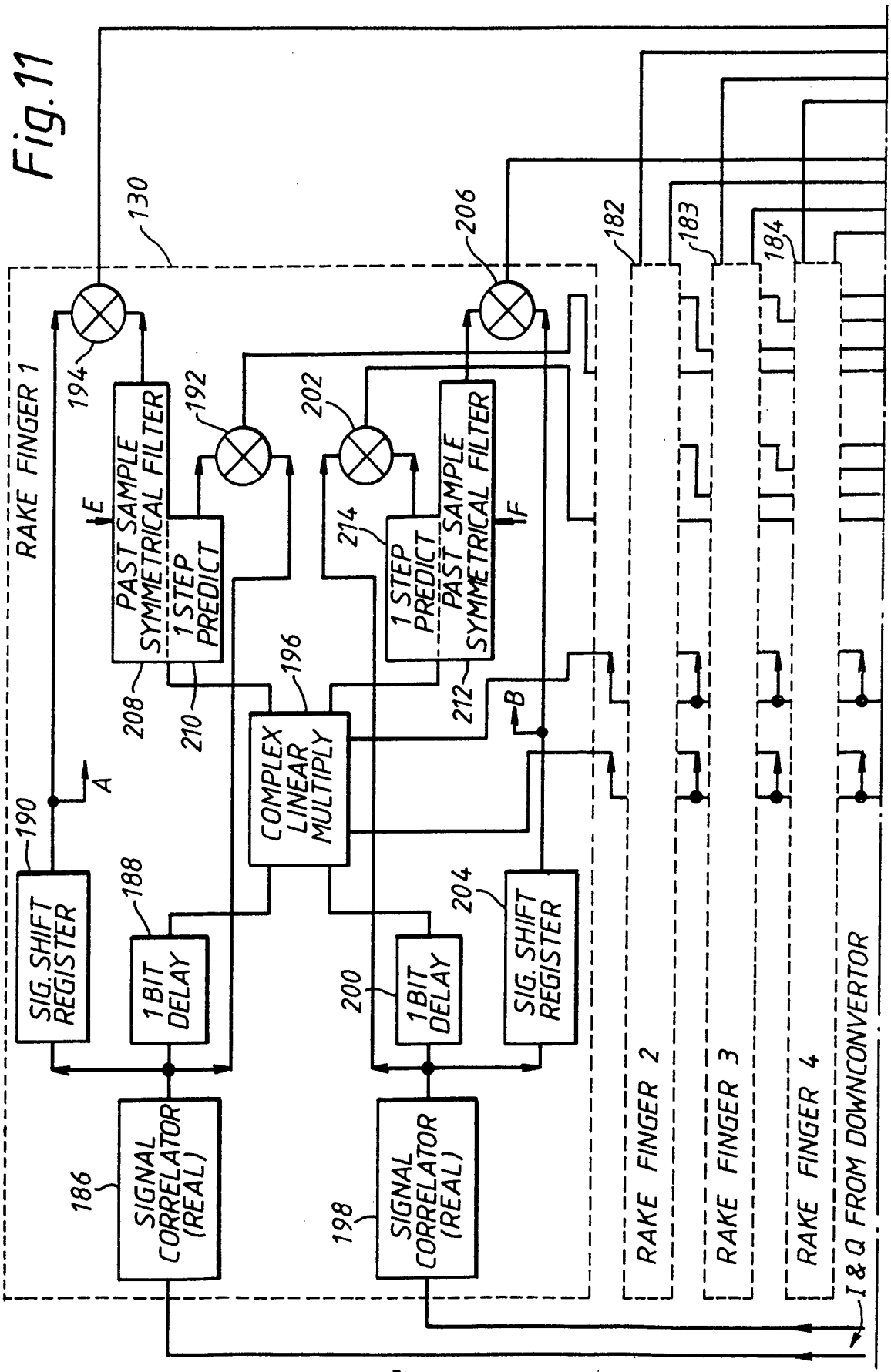
Q COMP OUT
Q COMP IN
MID FILTER COMPENSATING LINES

Fig. 10

Fig.11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SIGNAL CORRELATOR (REAL)
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RAKE FINGER 3
RAKE FINGER 4
I & Q FROM DOWNCONVERTOR

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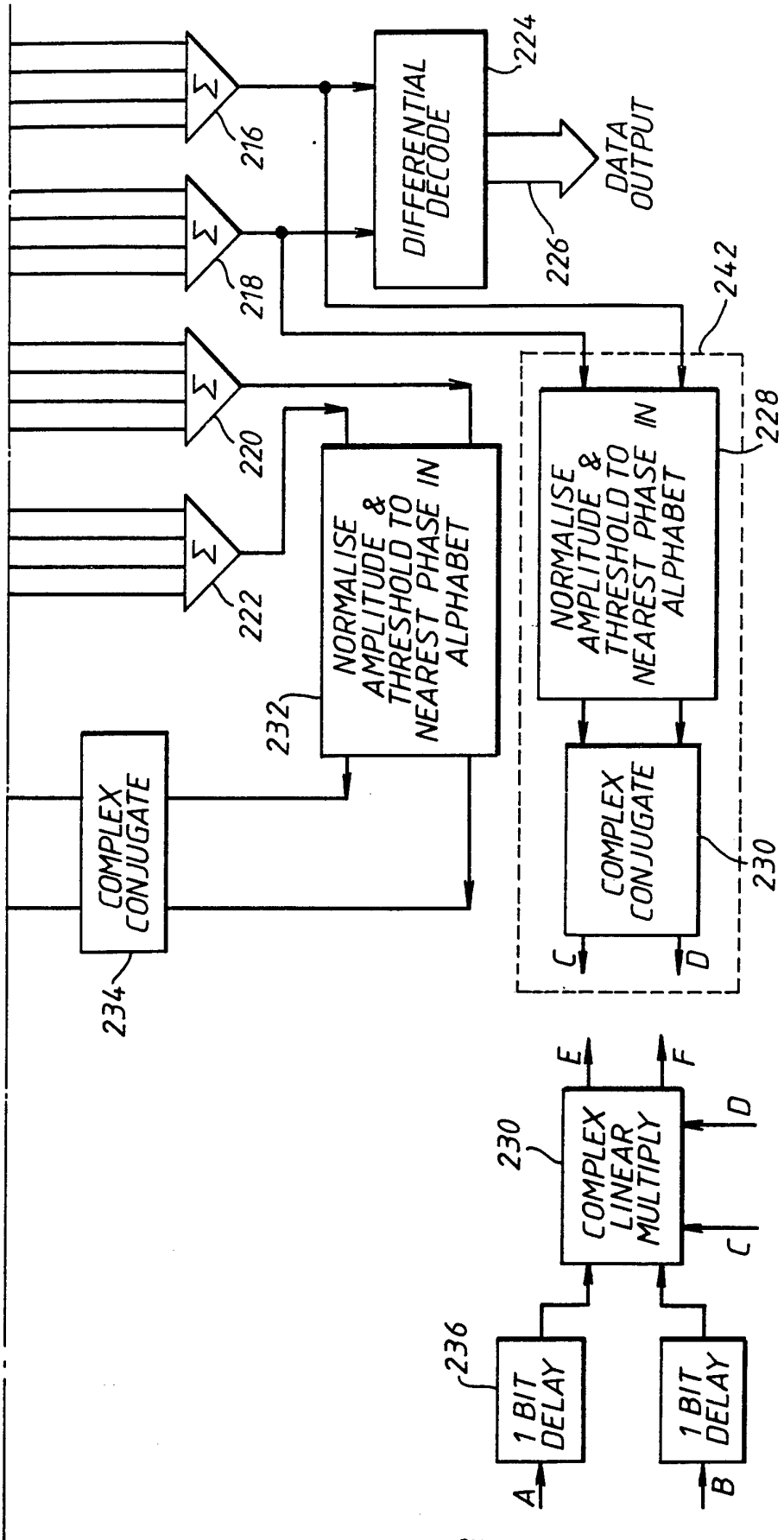


Fig. 11 cont.

# INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/GB 94/00580

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H04B7/005 H04B7/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | WO,A,92 08298 (BRITISH TELECOMMUNICATIONS PUBLIC LIMITED COMPANY) 14 May 1992<br>see abstract<br>see page 3, paragraph 3 - page 4, paragraph 2<br>see page 14, paragraph 4 - page 19, paragraph 1<br>see page 24, paragraph 2<br>see page 25, line 8 - line 15<br>see claims 1-6,9; figures 2,9<br>---<br>-/-- | 1 |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 24 June 1994 | 08.07.94 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. ( + 31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: ( + 31-70) 340-3016 | Gries, T |

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | IEE PROCEEDINGS I. COMMUNICATIONS, SPEECH AND VISION., vol.138, no.6, December 1991, STEVENAGE GB pages 566 - 576, XP274181 W.T. WEBB / R. STEELE: 'Equaliser techniques for QAM transmissions over dispersive mobile radio channels.' see abstract see page 571, left column, paragraph 3 - page 573, left column, paragraph 5; figure 9 --- | 1 |
| A | MILCOM 88. 1988 IEEE Military Communications Conference, San Diego, US, 23.-26.10.1988, vol. 1, pages 89-95, IEEE, New York, US; P.A. BELLO: 'Performance of some RAKE modems over the non-disturbed wide band HF channel.' see page 90, right column, paragraph 2 -paragraph 5; figures 2,3 ----- | 1 |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter onal Application No
PCT/GB 94/00580

| Patent document cited in search report | Publication date | Patent family member(s) | | Publication date |
|---|---|---|---|---|
| WO-A-9208298 | 14-05-92 | AU-A- | 8751091 | 26-05-92 |
| | | CA-A- | 2095025 | 01-05-92 |
| | | EP-A- | 0555289 | 18-08-93 |
| | | JP-T- | 6504414 | 19-05-94 |