

[54] **APPARATUS AND METHOD FOR SELECTIVELY ALTERABLE VOICING IN AN ELECTRICAL INSTRUMENT**

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[51] Int. Cl. **G10h 1/00**

[58] Field of Search **84/1.01, 1.03, 1.19, 84/1.29, 1.26**

[56] **References Cited**

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3,610,799	10/1971	Watson	84/1.26 X
3,646,241	2/1972	Ott	84/1.03

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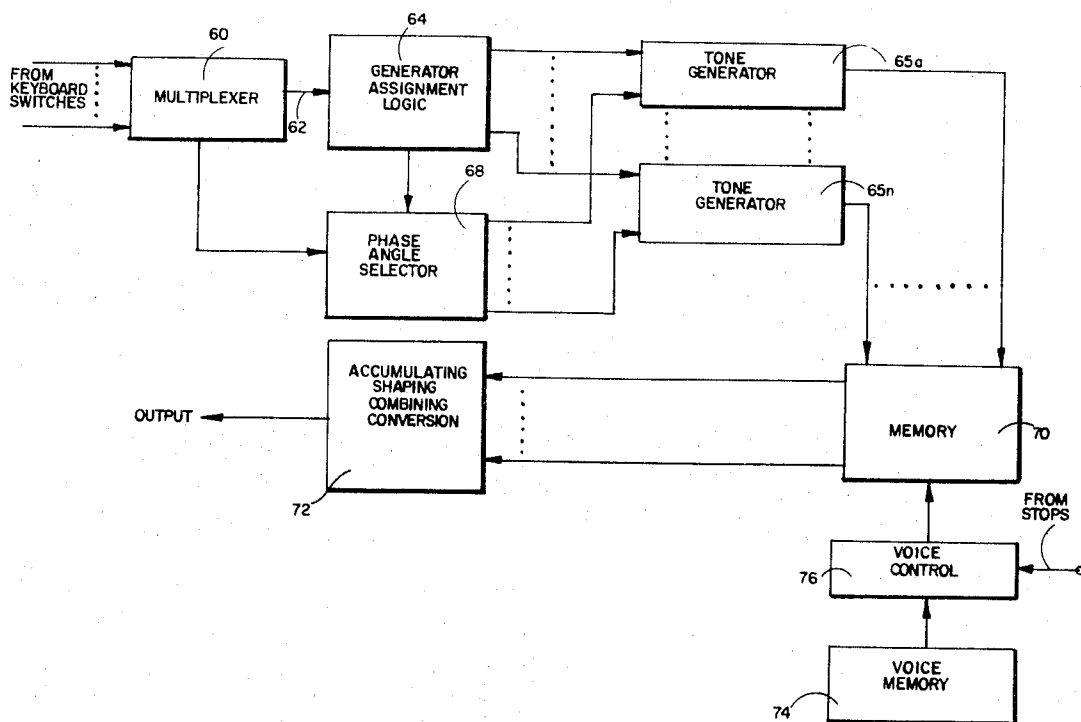
Attorney—L. Lee Humphries, H. Fredrick Hamann et al.

[57]

ABSTRACT

A number of different voices of an electrical organ are stored in specification memories as groups of amplitude samples of respective voices of the instrument. Under control of selectively actuated stops, groups of amplitude samples of chosen voices are extracted from the specification memories, combined, and stored in an alterable or registration memory. The latter is addressed for read out at a rate selected according to the frequency of the note to be generated. The various voices are combinable in different groups and chosen combinations are selectively stored in any one of several registration memories of which there may be one for each division of an organ and which may feed two or more separate audio channels. Selective scaling of one or more of the voices read from the specification memories will increase the number of voice combinations available. Loading of a newly selected voice combination into the registration memory may occur continuously during read out of the registration memory, or only upon actuation of a stop. Although loading of a new voice combination into the registration memory in one embodiment takes place during the read out of the registration memory, the loading may take place at less than musical frequency and at rates slower than registration memory read out rates.

24 Claims, 4 Drawing Figures



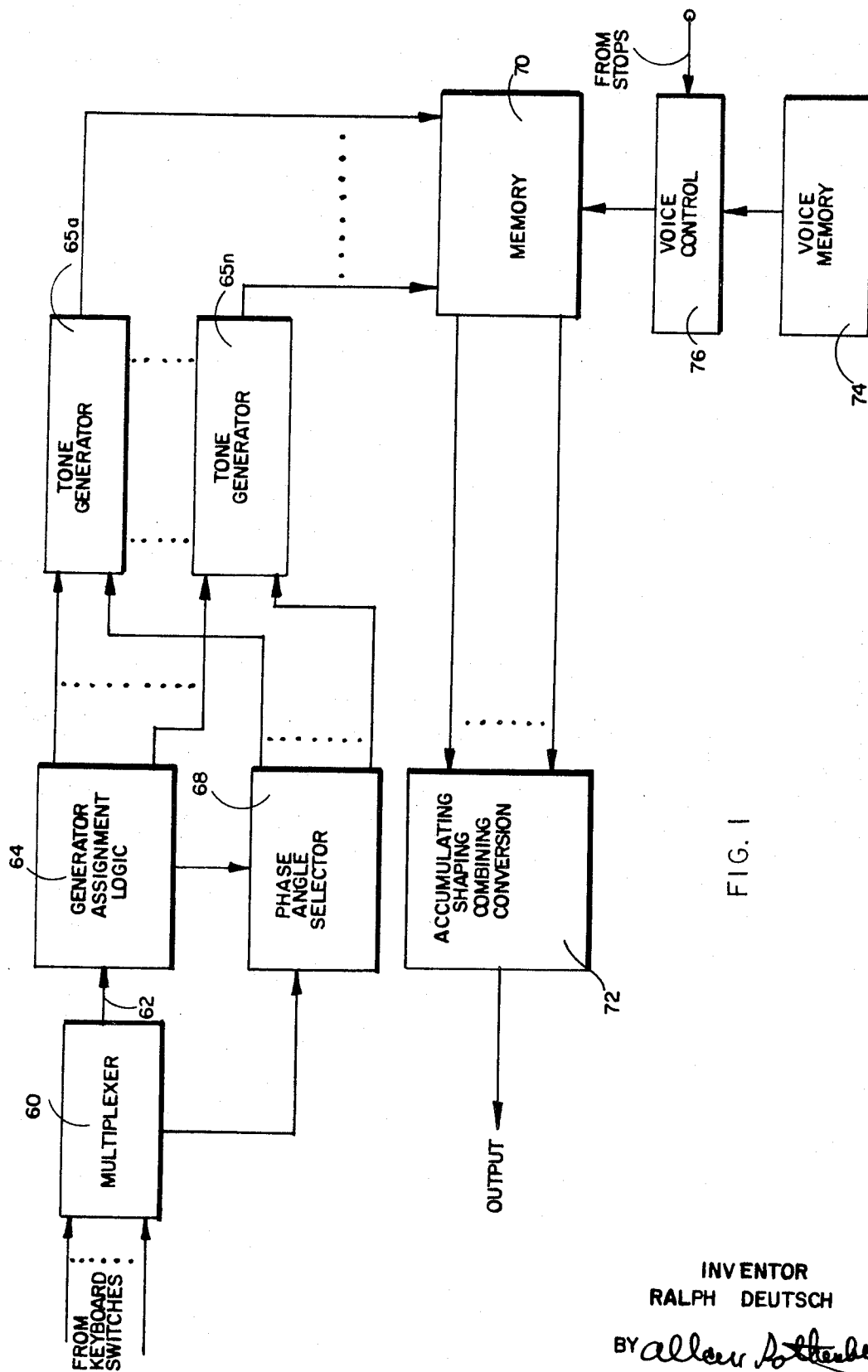


FIG. 1

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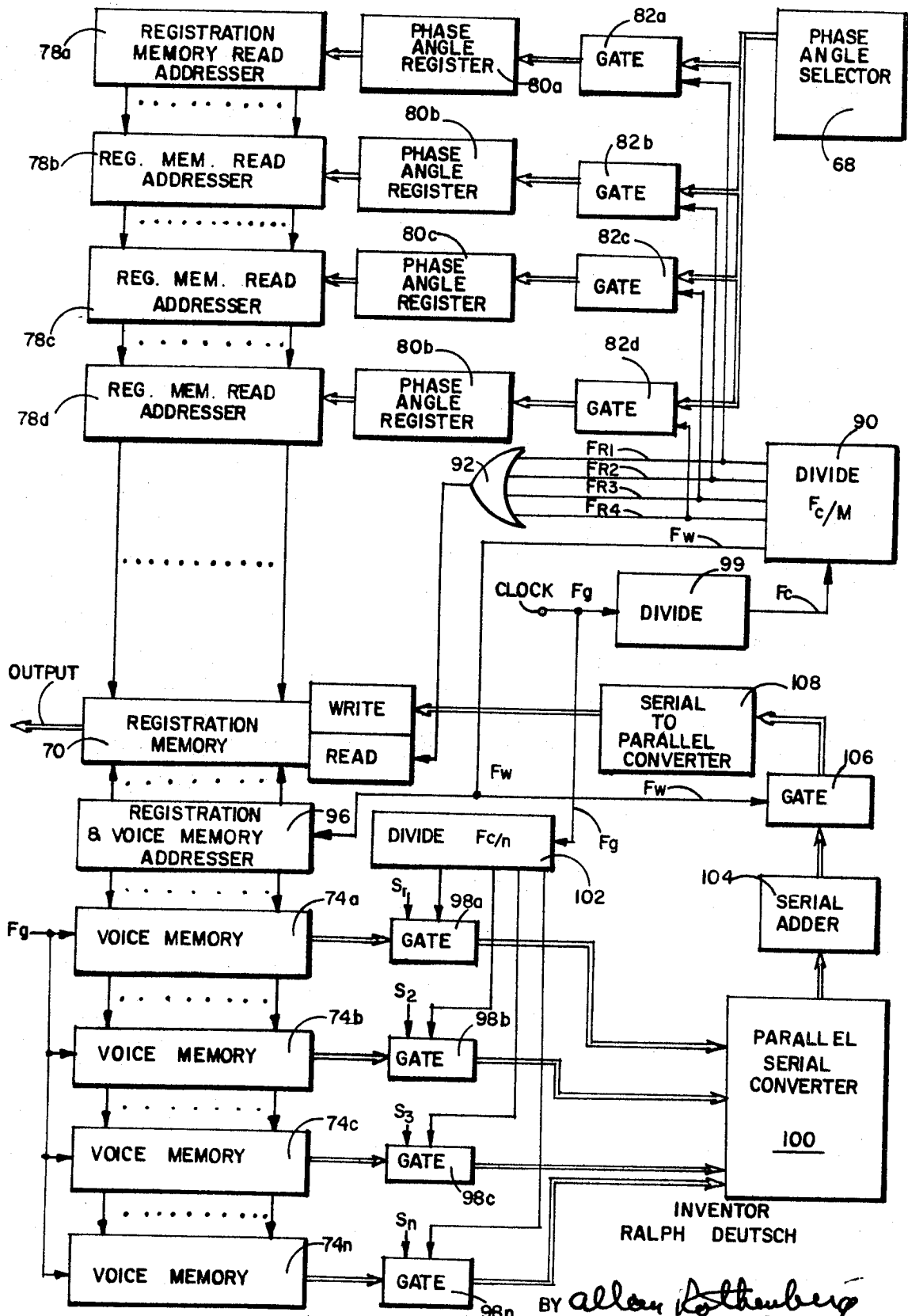


FIG. 2

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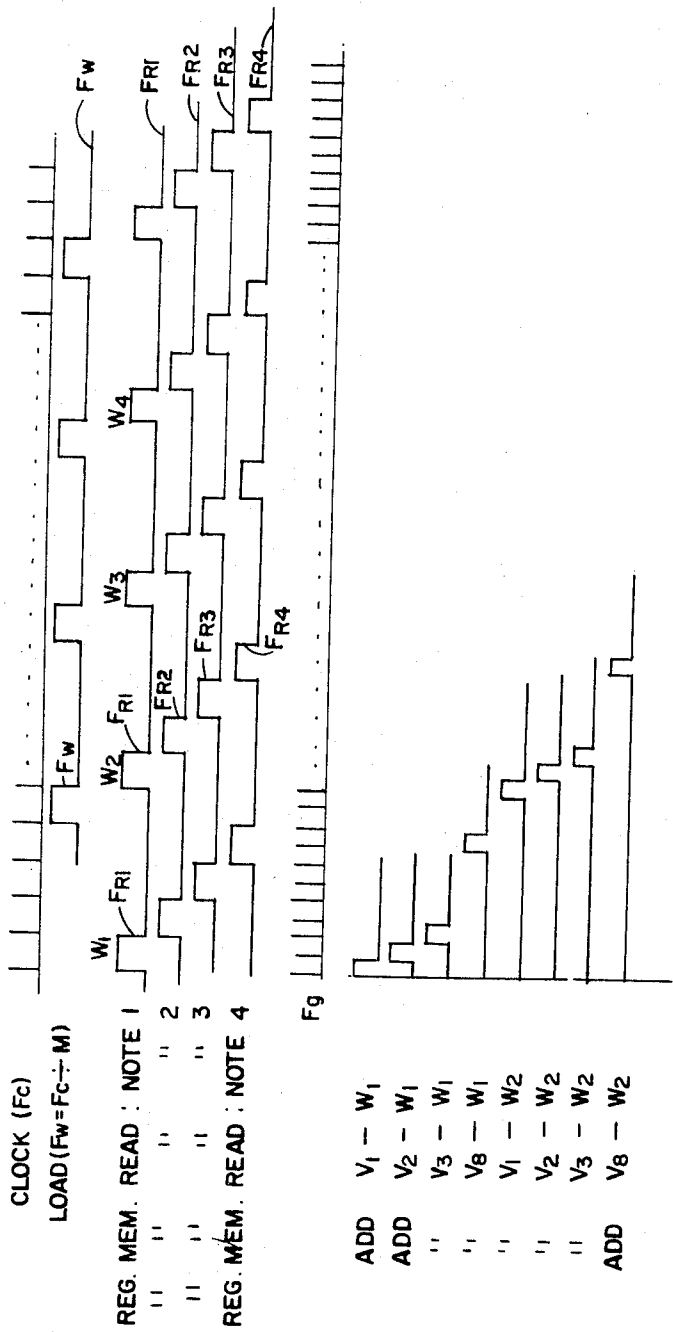


FIG. 3

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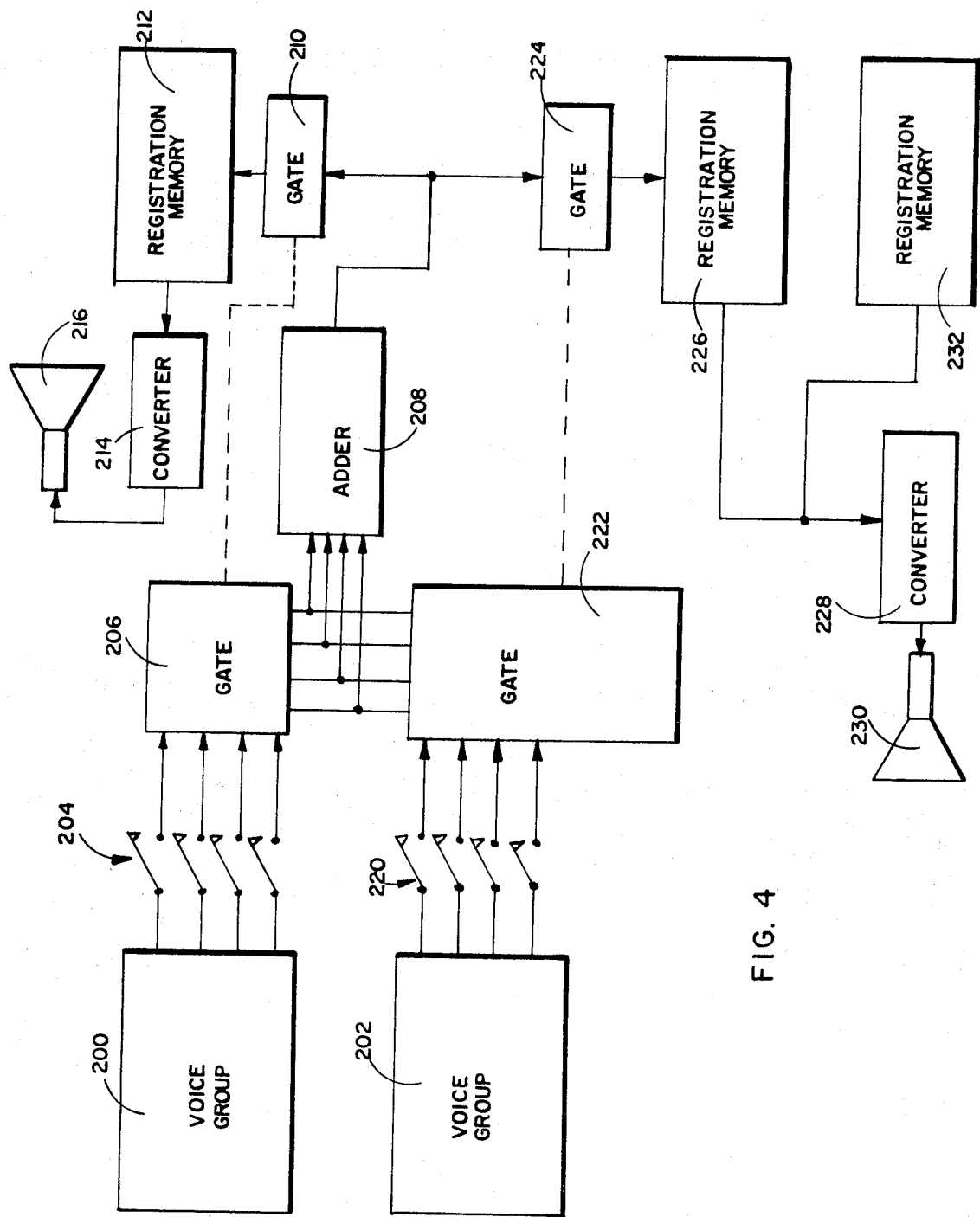


FIG. 4

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APPARATUS AND METHOD FOR SELECTIVELY ALTERABLE VOICING IN AN ELECTRICAL INSTRUMENT

BACKGROUND OF THE INVENTION:

1. Field of the Invention: The present invention relates to memory systems for electronic musical instruments, and more particularly concerns methods and apparatus for storing, selectively combining and reading combinations of a large number of different musical voices.

2. Description of Prior Art

Various types of electrical musical instruments, and in particular keyboard instruments such as the organ, are capable of producing, in addition to the usual musical frequencies, a number of different voices of varying tonal quality or timbre. Such voices include those in the categories of flutes, various non-flutes, such as reeds, diapason and strings, different groups of voices being available in several divisions including swell, great, and pedals. A number of such voices are commonly listed as an instrument "specifications" which may include 40 or more different voices. The instrument is provided with tabs or stops that may be selectively actuated individually or in combinations so as to cause the various notes, played at frequencies selected by the keyboard, to embody a selected voice or combinations of voices. Several types of special effects may also be included in the instrument voicing capabilities. U. S. Pat. No. 3,515,792 for Digital Organ issued to Ralph Deutsch, and assigned to the assignee of the present invention, discloses a digital electronic organ in which a particular wave shape or several wave shapes are stored in a memory as digital amplitude samples or digital words. These amplitude samples are repetitively read from one or more of the memories, then combined, shaped, converted to analog form and thence employed to produce an audio signal.

It will be readily apparent that the number of different voice combinations in an arrangement such as employed in the Deutsch patent is limited by the cost and complexity of required combining or adding circuitry. This is so because of the fact that the number of additions required to obtain selected combinations of two or more of the different stored voices increases with an increase in the number of stored voices. Thus with the Deutsch system of combining voices, it may be impractical, at least for economic reasons, to make available even a major portion of the possible combinations of voices.

Still another major problem related to the combining of voices in the above-identified Deutsch patent derives from the fact that in the scheme of this patent the various voices must be combined in real time at the frequency of the rate of read out from the memories. This is the desired musical frequency. In such a system each voice, or each wave form is stored as a number of amplitude sample representations or words which may be some 30 to 40 in number. Accordingly for a voice that is delineated by 32 words, each wave form is extracted from the memory by reading all 32 words, one at a time. Successive wave forms are provided by repetitively reading groups of words, at a group repetition rate that defines the musical frequency of the selected note. At higher frequencies the time limitation on combination of voices is severe. Each digital word or amplitude sample of a combination selective from as many

as 40 voices must be added at frequencies up to 64 kilohertz. A frequency of 64 kilohertz for a combination of voices would be required when reading out a note having a frequency of 2,000 Hertz that is defined by 32 digital words or stored sampled amplitudes. The problem of such combinations is at best difficult where parallel addition is employed, requiring complex and rapid acting circuitry, but approaches economic and practical nonfeasibility where the addition is serial.

A system which eliminates some of the problems of the above-identified Deutsch patent is shown in my co-pending application for Alterable Voice for Digital Organ, Ser. No. 152,122, filed on June 11, 1971. The disclosure of this application is incorporated herein by this reference as though fully set forth. In this patent application there is disclosed a system that not only combines different voices extracted from a specification or voice memory, but which also employs a selectively alterable memory. The latter is alterable by punched cards, for example. The alterable memory is employed as an additional memory of which the output is combined with outputs of the voices stored in permanent memory. Although this arrangement of my co-pending application increases the number of voices available, it suffers from the same limitation of my prior patent in that the number of available combinations (once the alterable memory has been loaded with a given voice) is still seriously limited by the adding circuitry. The arrangement of my co-pending application also suffers from the time limitation imposed by combining different voices at musical frequencies.

Various types of punched card control systems for achieving so-called "registration", or combination of voices, are shown in the U.S. Patent to R. A. Clauson, U.S. Pat. No. 3,213,179, and the U.S. Patent to Campbell, Jr. et al., U.S. Pat. No. 3,172,939. Although these systems facilitate selection of various combinations of stops, they do not modify the instrument tone generation system, nor improve the voice storage of the instrument. In fact, these patents are concerned not with storage, but merely with improved stop actuation by punched cards, or the like.

U. S. Pat. No. 2,989,885, to Pearson, describes an electronic musical instrument in which a number of wave form generators are commutated, or sampled, and then subjected individually to wave form shapers, filters, and the like. However, no combination of large numbers of selected voices is shown in this patent.

Accordingly, it is an object of the present invention to provide improved methods and apparatus for selecting one of a number of different combinations of stored voices of a musical instrument.

SUMMARY OF THE INVENTION

In carrying out principles of the present invention in accordance with a preferred embodiment thereof, groups of representations delineating one or more complex wave shapes of one or more voices are read from selected ones of a plurality of specification or voice memories. Selected groups of representations are combined in accordance with selectively actuated stops and then stored in a registration memory at rates that are independent of registration memory read out rate of successive combined representations. Groups of combined representations are read from the registration memory at a rate related to the frequency of the selected tone whereby the tone is comprised of the com-

bination of voices selected by the actuated stops. The read out, combination and temporary storage of the specification memories need not occur at musical frequencies. The arrangement is such that a large number of specification memories may be selectively combined according to selected actuation of stops or groups of stops, employing but a relatively few combining or adding circuits so that the large number of combinations desired is no longer limited by requiring similarly large quantities of circuitry.

In one arrangement wherein a registration memory is sequentially addressed by each of a number of tone generators or addressing circuits, all of the voice memories are read out, combined and loaded into the registration memory during the time between successive advancing of one registration memory addresser. Thus serial addition or combination of amplitude samples from the several voices is possible.

BRIEF DESCRIPTION OF THE DRAWINGS:

FIG. 1 shows the general arrangement of an embodiment of this invention,

FIG. 2 illustrates details of the memory arrangement of the embodiment of FIG. 1,

FIG. 3 is a synchrograph showing certain timing relations of the embodiment of FIG. 2,

FIG. 4 is a block diagram illustrating application of the invention to an instrument having several groups of voice memories and a number of registration memories.

DETAILED DESCRIPTION

One of the significant advantages of the present invention, is the loading of the registration memory at rates independent of and selectively lower than registration memory read out rates (musical frequencies). Although this may be achieved by employing parallel adders, such a mechanization would be limited by the practicability and economics of large numbers of adders that are required for the many possible combinations of voices. The arrangement illustrated in FIG. 1 not only achieves improved timing of registration memory loading, but does so with the use of a serial adder that allows large numbers of voice combinations without excessive circuitry. The alterable memory arrangement employing serial combination of selected voice memories and loading of a registration memory at other than musical frequencies may be employed with a variety of electrical musical instrument systems that store representations of amplitude samples of a complex wave form and with many different memory addressing schemes. In order to better illustrate principles of these features of the present invention, there is shown in FIG. 1 an electrical musical instrument having a memory system in which the musical frequency of read out is controlled by a selected phase angle number as more particularly described in the U. S. Pat. No. 3,610,799 to George A. Watson for Multiplexing System For Selection of Notes and Voices in an Electrical Musical Instrument, and U. S. Pat. No. 3,639,913 to George A. Watson for Method and Apparatus for Addressing a Memory at Selectively Controlled Rates, both assigned to the assignee of the present invention.

Briefly, the digital organs that are described in detail in the Watson patents and generally illustrated in part in FIG. 1 hereof, embody a multiplexer 60 that provides a series of output signals on a line 62, each signal

occurring in a unique specifically allocated time slot of each multiplexer cycle. As the operator actuates a given key or pedal or some combination of keys or pedals of the instrument, the arrangement scans each key and pedal during each multiplexer cycle and produces a pulse or no-pulse at a particular time slot allocated to a given key, depending on whether such key or pedal has been actuated. The multiplexed signal on line 62 is fed to a generator assignment logic circuit 64 which feeds the pulses representing actuated keys or pedals to tone generating circuits 65a-65n. Although in an actual system there may be as many as 12 such tone generating circuits, or tone generators, the use of more than one such tone generator is not required either for operation or understanding of the present invention. However, where several of such tone generators are employed, each will be identical to the other, and in such case, the function of the generator assignment logic is to direct a signal from the multiplexer that represents actuation of a given key to one of the tone generators that is not already engaged in receiving a signal and producing a tone therefrom.

A phase angle number selector 68, which may be common to all of a number of tone generators when several of these are employed, selects (either from storage or repetitive calculation) a number from a set of distinct and different numbers that vary according to the 12th root of 2. As is well known, a semi-tone or half tone in the musical scale of equal temperament is a frequency ratio between any two tones whose frequency ratio is the 12th root of 2. Therefore, the several numbers of the set calculated by or stored in selector 68 identify phase angles of frequencies of the individual notes of the scale of notes to be played. These phase angle numbers identify rate of read out of stored amplitude sample representations of the complex wave form for the respective note frequencies in the entire range of frequencies of the musical scale of the particular instrument. Details of such calculation and/or storage, together with circuitry therefor are set forth in the above-identified Watson patent.

A number from the phase angle selector is gated into a phase angle register which feeds the numbers stored therein to a memory read address register, and upon each clock pulse received from a sampling clock, augments the number stored in the read address register by the number in the phase angle register. As the memory read address register is augmented, its count advances and thereby advances the address location of the working memory 70 that is accessed for read out. The sampled amplitude representations stored in the memory 70 as digital words are fed to output circuitry 72 for further processing and conversion to a musical tone, as more particularly described in the above identified Watson patents. Thus, it will be seen that the arrangement selects a phase angle number according to identity of an actuated key, gates the selected number into a phase angle register and then proceeds to cause a memory read address register to be repetitively augmented by the number stored in the phase angle register at a rate determined by a sampling clock.

In accordance with principles of the present invention the individual voices of the instrument are not stored, at least initially, in the memory 70, but are stored in a number of voice memories 74 that may be of the read-only type and of a desired number. One or some combination of these voice memories are selected and com-

bined by a voice control circuit 76 that responds to stops as in the previously described embodiment.

Further details of an exemplary arrangement of voice memories and voice control circuits for loading into the working

Registration memory 70 (FIG. 2) is a read-write memory of conventional type. It is addressed by a registration memory read addresser 78a. The addresser 78a contains a number that is repetitively augmented by a number stored in phase angle register 80a. The number stored in phase angle register 80a is repetitively gated into the register and thus repetitively added to the number in addresser 78a via a gate 82a from the phase angle selector 68 and at a sampling clock rate determined by a sampling clock signal F_{r1} .

The arrangement is such that the addresser does not necessarily address and read a different location of memory 70 at each of its counts. Rather the addresser will read a different address of the memory only when it counts to particular counts that are separated from each other by selected amounts. As an heuristic example, consider a decimal analogy in which the memory contains ten locations and accordingly ten words. The addresser may be arranged to count consecutively from one through one hundred and is connected to address a different memory location only at each tenth count although it may read out from any particular address at which it is positioned upon each and every count. Accordingly, when the addresser reaches its count of ten, a first word W_1 will be read from the memory. The second word W_2 is read when the addresser reaches the count 20 and so on, to read the tenth and last word upon reaching the count of 100, whereupon the addresser starts counting anew. In the described example the particular word of the last addressed memory location is read from the memory at each time the addresser steps, regardless of whether such a step will cause a change in address or will step the addresser to a specific new memory location. The amount by which the memory address advances upon each sampling clock pulse F_{r1} is determined by the number in the phase angle register. For the highest frequency of read out, such number is equal to the difference between memory address register counts at successive memory address locations so that a new memory address for location is accessed upon each clock pulse. For lower frequencies, several additions of the phase angle register number to the number in the memory addresser are required to change from one address to the next. Nevertheless the word at the last addressed memory location is read out at each sampling clock pulse, whereby for all but the highest frequency each word in the memory may be read out several times in succession.

Circuitry including a memory addresser, and a phase angle register, comprises a tone generator. There may be as many as 12 tone generators, each comprising a separate memory address system and each capable of individually and independently addressing the same memory 70. In the exemplary arrangement illustrated in FIG. 2 there are four such tone generators comprising registration memory addressers 78a, 78b, 78c, and 78d, phase angle registers 80a, 80b, 80c and 80d, and gates 82a, 82b, 82c, and 82d, all of the latter receiving a selected phase angle number from selector 68, the numbers being fed from selector 68 in synchronism with the operation of the gates 82a through 82d.

A sample clock signal F_c is provided to control the rate of augmenting of the registration memory read addresser 78a in a cyclic sequence with the other registration memory read addressers. Accordingly the train of pulses at repetition rate F_c is divided in a divider 90 by the number M which, in this example, is one greater than the number of tone generators employed. Divider 90 may be a shift register which sequentially provides output pulses at the rate $F_{c/M}$, as indicated on lines F_{r1} , F_{r2} , F_{r3} , F_{r4} , and F_w . Lines F_{r1} through F_{r4} are respectively fed to sequentially enable gates 82a - 82d and also fed through an OR gate 92 to enable read out of the read-write registration memory 70 each time that a selected one of the addressers 78 is augmented.

The relative timing of the registration memory read address circuitry is illustrated in FIG. 3 wherein the first line shows the sample clock pulses F_c . The second line illustrates the load or write pulses F_w which occur at the frequency F_c/M . The third line in FIG. 3 illustrates the read pulses applied from registration memory read addresser 78a. In this illustration each successive read pulse is assumed to access a successively different memory location and successive memory word, such as W_1 , W_2 , W_3 , etc. This condition of course, exists only when the highest frequency read out occurs. At lower frequencies each word will be read out several times in succession. Regardless of the frequency, addresser 78a will achieve read out, whether from one address or successive addresses, at the rate F_{r1} . Similarly read out via the addressers 78b - 78d occurs as indicated at the rates F_{r2} , F_{r3} , and F_{r4} . The fifth pulse F_w is employed for loading of the registration memory (writing into the registration memory) and occurs when no read out from the registration memory takes place.

Although an exemplary number of tone generators, including the four illustrated registration memory read addressers, is shown in FIG. 2, only one such registration memory read addresser is required for practice of the present invention. The fact that the same registration memory may be shared by a number of tone generators may be advantageously employed, but is not necessary either for understanding or practice of this invention. Accordingly, we may omit from the ensuing discussion the 4th, 5th and 6th lines of FIG. 3 (identified as "Reg. Mem. Read: Note 2", "Reg. Mem. Read: Note 3", or "Reg. Mem. Read: Note 4", respectively) and also the tone generators comprising elements 78b - 78d, 80b - 80d, and 82b - 82d. Thus there is a read out from the registration memory 70 in the described example at every fifth sample clock pulse. In accordance with a significant feature of the present invention, the time interval between successive occurrences of a read out pulse F_{r1} is employed to scan all of a group of voice or specification memories, combine amplitude sample representations read from selected ones of the voice memories and load the combined voice representations into the registration memory under control of the load signal F_w .

Thus, as illustrated in FIG. 2, a number of voice memories, which may be read-only memories indicated at 74a - 74n, are all addressed simultaneously by a registration and voice memory addresser 96. The latter also addresses the read-write registration memory 70 but only or writing or loading into this memory. The read out rate of the voice memories and the loading or writing rate of the registration memory are both under the control of the load signal F_w which accordingly

steps the addresser 96 at the clock rate F_c/M . Although the voice memory addressing and registration memory write addressing both advance at the rate F_w , the read out of all voice memories occurs in unison at the rate F_θ . This is achieved by feeding a voice read signal F_θ to actuate read out of each of the voice memories.

The voice read signal is a pulse train having a greater repetition rate than the rate of the sample clock signal F_c . The relation between the two is such that all voices may be sequentially combined between successive load pulses F_w . In the exemplary embodiment disclosed herein there are eight voice memories, each of which is available for combination, one after the other, at successive ones of the voice read pulses F_θ . Accordingly there are eight voice read pulses for each load pulse. This relation is conveniently achieved by dividing the pulse train F_θ in a divider 99 to obtain the pulse train F_c .

The various timing signals and pulse trains may all be derived from a master clock, divided down as described above. This is a matter of convenience only since the rate of addressing of the registration memory for read out is independent of the rate of write addressing thereof except for synchronization from the master clock. The rate at which read out steps from one registration memory location to another (as distinguished from the registration memory read out rate) is controlled by the selected note frequency (via the selected phase angle number) and thus is independent, except for synchronization, of system clock rate.

Although all voice memories are read out in unison at the rate F_θ , they are time multiplexed by means of a set of gates 98a - 98n so that representations from each of the voice memories may be passed in sequence to a parallel to serial converter 100.

Control of the multiplexing cycle of voice memory gating is provided by the outputs of a shift register or divide circuit 102 that divides voice read pulses F_θ by the number n of voice memories. Thus upon each occurrence of a pulse F_θ a different successive one of the gates 98a - 98n is enabled so that the words read from the same location of all voice memories at each pulse F_θ are sequentially converted to serial form. It may be noted here that in the described arrangement each word or amplitude sample representation is stored in a given memory location as an eight bit digital word of seven bits plus sign.

Gates 98a - 98n are also selectively enabled by signals S_1 through S_n respectively representing actuation of different ones of different combinations of the several stops. Accordingly only representations from those voices selected by operation of a particular stop or stops are fed to the parallel to serial converter 100. The output of the latter is fed to a serial adder 104 which sequentially adds the representations from selected voices, one by one. After all voices have been scanned, the output of the serial adder, which comprises the total of corresponding representations of all voices selected by stops $S_1 - S_n$, is gated by the load pulse F_w through a gate 106 to a serial to parallel converter 108 which loads the combined signals of selected voices into the registration memory 70.

Timing of the above operation is illustrated in the lower eight lines of FIG. 3. Shift register 102 divides the voice read pulse train by the number of voice memories so that at one pulse F_θ , word one (W_1) of the first voice (V_1) memory 74a is gated into the converter 100 via

gate 98a. At the next pulse F_θ the first word (W_1) of the second voice (V_2) memory, 74b is gated into the converter by gate 98b, and so on until the n^{th} voice (V_n) memory 74n has its first word gated into the converter via gate 98a.

Pulses from divide circuit 102 may be inhibited during the load time F_w since the voice memory address register is stepped and no voice read out is desired at this time.

After the combination of the first word from selected voices is loaded into the registration memory, the voice read out multiplexing cycle again commences reading the second word (W_2) of the first voice (V_1), the second word (W_2) of the second voice (V_2), and so on, at each voice gate pulse F_θ , until the second word of all the voices have been read and combined in the serial adder. Thereupon the next load signal F_w gates the combination of the second word of the selected voices, advances the address for both voice memory and loading of the registration memory and enables the loading of this combination of second words into the next address of the registration memory.

This sequential operation of feeding words from the several selected voice memories is illustrated in the last eight lines of the graph of FIG. 3 which respectively shows the sequential gating of the first word W_1 of each of four of the exemplary eight voices V_1, V_2, V_3 , and V_8 , during a first interval between load pulses F_w , followed by the load interval F_w and then a second voice multiplexer cycle in which the second word of each of the voices V_1, V_2, V_3 , through V_8 are sequentially gated for serial combination to be loaded into the next address location of the registration memory. Although the exemplary embodiment shown in FIG. 2 shows simultaneous read out of all voices and successive gating of selected voices, it will be readily appreciated that an equivalent function may be achieved by successively gating (under control of stop switches $S_1 - S_n$) read out from the voice memories and feeding all such read outs directly to the converter 100. Various elements employed in the mechanization of the present invention are standard, well known components. Thus, the text "Computer Handbook" by Huskey and Korn, First Edition (1962) McGraw-Hill, discloses on pages 15-9 and 15-10 details of serial binary adders that may be employed in the arrangement of FIG. 2. Pages 16-14 of this Huskey and Korn text disclose exemplary arrangements that may be employed in the present invention for translation of information from serial to parallel representation and vice versa.

In the illustrated arrangement timing is selected such that the interval between reading under control of the pulses F_{r1} , for example, is employed for read out, combination and loading of the voices into the registration memory. In an instrument employing a number of tone generators, which are multiplexed so that each may successively address the same working memory (as described in the Watson U.S. Pats. Nos. 3,610,799 and 3,639,913), there is necessarily an interval between successive addressing of the memory by any one tone generator. The arrangement of FIG. 3 shows timing of an exemplary embodiment employing four tone generators successively addressing the memory at pulse times F_{r1}, F_{r2}, F_{r3} , and F_{r4} , respectively, with a fifth pulse time in a single cycle F_w employed solely for loading into the registration memory. In a system where twelve tone generators are employed, it is extremely

unlikely that all twelve will be simultaneously assigned since seldom, if ever, are twelve notes played together. Accordingly, the twelfth time slot of the cycle of tone generators (analogous to the fifth time slot F_w in the five interval cycle of FIG. 3) is employed for loading of the registration memory. If deemed necessary or desirable, where a time slot of one of the tone generators is employed for loading, the load operation may be automatically inhibited in those rare instances when all twelve tone generators are employed. Such inhibition of the loading of the registration memory has no adverse affect upon operation of the system in a large majority of instances because loading of the selected combination of voices merely repeats the same loading operation unless and until a change in one of the stops is effected. Thus, the probability of a stop change being implemented while twelve different notes are being played is negligibly small in a manually controlled instrument.

In the arrangement illustrated in FIG. 3, it will be noted that the read addressing of the registration memory is independent of the addressing of either the voice memories for reading or the registration memory for loading, although the loading occurs at a time when no read out of the registration memory takes place. Therefore, should only a single tone generator be employed to read from the registration memory, it will be readily appreciated that the rate of read out from the registration memory and also the rate of advance from one read out address location to the next, may be considerably higher than that illustrated in FIG. 3 in view of the fact that no time need be allowed for the multiplexing or time sharing of the one registration memory for access by plural tone generators. In such a situation, a registration memory read out rate for high frequency notes, (when the rate of stepping from one address to the next may approach the read out rate) may be higher than the loading rate (the rate of stepping from one writing address to the next during a write operation into the registration memory).

For the timing shown in FIG. 3, illustrative of read out of the highest musical frequency, the read out advances from one address location to the next at the rate of F_{r1} and loading also advances from one memory location to the next at the same rate (as controlled by F_w). At all other frequencies the read out rate of advancing from one address location to the next occurs at slower rates. Although read out is still at the rate of F_{r1} , such read out is repeated at each address location. Nevertheless, the advancing from one memory address location to the next for registration memory loading, remains the same at all frequencies (although more time is available at lower frequencies for voice combining). Therefore at lower frequencies, loading takes place faster than read out. If a relatively slower pace of loading (and voice combining is desired) the load pulses F_w and voice read pulses may be caused to occur at a still lower repetition rate as by dividing these pulse trains or inhibiting selected pulses of these trains.

It is a significant advantage of the present invention to enable a highly flexible selection of write address and read address rates of the registration memory. These rates are independent of each other and will be chosen according to requirements of a given system. For example, writing successive words into the registration memory may occur once for each read out of two or more words from this memory (even at the highest

musical frequency). In such a situation, several complete groups of amplitude sample representations will be read from the registration memory before its contents have been completely updated according to the latest selection of voices. Nevertheless, the effect of partial updating occurs only upon a few cycles of the note or notes being played, and then only when a stop change is made during the playing of a note.

A conventional organ may have a number of divisions such as pedal, swell, and great, and each of these divisions may have a number of different voices or groups of voices unique to the respective division. Further, different voice groups may be played through plural audio channels and different numbers of registration memories. In general, an instrument embodying the present invention will have at least one registration memory for each division (for each manual and pedal). Further, any voice may be directed to any registration memory. The overall arrangement of aspects of such a system is illustrated in block form in FIG. 4 wherein a first group of voice memories 200 may comprise, for example, 16 non-flute voices for swell, and a second group of 16 flute voices 202 for great. Different voices, or combination of voices of the non-flutes 200 are selected by operation of stops collectively indicated at 204 and fed through gating circuitry 206 to a voice combiner 208. The selected combination of voices from combiner 208 is fed via a gate 210 to a first registration memory 212 from whence the combined voices may be read as previously described, shaped and converted for audio presentation in circuitry generally indicated at 214, for presentation to a loud speaker 216.

The second group of voices, the flute voices in the memories 202 are selected by stops collectively indicated at 220 and passed through gating circuitry 222 to a voice combiner 208 from whence the combination selected voices is passed via gating circuitry 224 to a second registration memory 226 from which selected flute voices may be fed to shaping and conversion circuitry 228 to drive a separate audio channel or loud speaker 230.

A third registration memory 232 may have a selected combination of pedal voices, for example, loaded into its various memory locations from a third group of pedal voices (not shown) in the manner heretofore described. The memory 232 may conveniently have its output combined with the output of memory 226 so that both pedals and flutes for example, may employ the same audio channel. Gating circuitry 206 and 210 are operated in unison, and gates 222 and 224 are likewise operated in unison, the two pairs of gates being alternatively operated so that the combiner 208 will combine either voices selected from voice group 202 for loading into memory 212 or will combine voices from the group 202 for loading into the memory 226. It will be readily appreciated that the overall arrangement of voice groups and registration memories as shown in FIG. 4 is merely exemplary of many different combinations of voice group memories and registration memories that are possible and facilitated by means of the present invention. Several embodiments of the invention have been described in connection with various types of note selection and stop selection systems. It will be readily appreciated that the described principles of selectively combining voices for loading into a registration memory substantially independent of the read out from said registration memory may be imple-

mented in still other arrangements and with still other modes of note and stop selections. One such embodiment of the present invention that employs multiplexing of keyboard switches, tone generators and also employs multiplexed stops for reading selected combinations of voices into a registration memory is shown in the above-mentioned Watson U.S. Pat. No. 3,610,799.

The described arrangement has a number of advantages including the fact that there is possible a much lower rate of combining of the selected voices since the combining and loading of the registration memory need not occur at the readout rate from the registration memory. A further advantage which derives from the provision of more time for the combination of voices is the fact that serial combination of the representations of amplitude samples of different voices may be employed, thus, considerably decreasing the amount and expense of required circuitry.

As indicated, readout and combination of voice memories may be timed so as to achieve loading of successive locations of the registration memory at rates that are less than the rates at which the same locations are addressed for readout. Thus, the memory read address may be implemented to step from one memory location to the next at a rate that is greater than that at which the addressor steps from one memory location to the next for loading of the registration memory. This relation of a higher readout compared to writing rate for the registration memory may put the least burden on the voice memory readout and combining circuit. However, such a relation is not necessary since the registration memory may be loaded at the same rate as readout as long as writing and reading do not occur together.

Although the invention described herein is applied to digital organ systems, it will be readily appreciated that may be a core memory of the type described in pages 180 et seq., Chapter 7 of "Fundamentals of Electronic Computers Digital and Analog" by Matthew Mandel. Various types of microelectronic integrated circuit read/write memories are also available and are preferred where other circuitry is mechanized by microelectronic techniques.

Loading of combined information into the registration memory, as previously described, may proceed at a slower rate than does read out from the registration memory. For example, the combining of voices and loading of the registration memory may take place at the rate of 15.5 kHz instead of the 62 kHz rate of registration read out of a high frequency note.

It will be noted that in the arrangements of the present invention, once a stop combination has been selected, loading of the registration memory may repetitiously continue. That is, the same selected voice combination may be repetitively read into the registration memory unless the stops are changed during the playing of a particular note. However, if a stop is changed while playing, there will occur only a very abrupt transient in the form of a nearly inaudible click in the audio output of the instrument. Generally, such a transient will be acceptable. However, especially in the playing of classical music, the stop change is seldom made during play.

A stop change sensor may be employed to provide a single or a pair of registration memory load cycles which are initiated upon sensed change of a stop position. In such an arrangement, memory load would also

be initiated upon turn on of the instrument, since the stops may be changed at a time when the instrument is not supplied with power.

There have been described various methods and apparatus for selectively combining different voices of a musical instrument at rates not dependent upon musical frequency, which enable implementation in many different modes with larger number of voices and voice combinations, and less circuitry.

The foregoing detailed description is to be clearly understood as given by way of illustration and example only, the spirit and scope of this invention being limited solely by the appended claims.

I claim:

1. An alterable memory system for an electrical musical instrument comprising
 - a registration memory,
 - a plurality of voice memories, each containing a group of amplitude sample representations of a complex wave form of an instrument voice,
 - means for combining amplitude sample representations read from a selected combination of one or more of said voice memories,
 - means for writing said combined amplitude sample representations into said registration memory, and
 - means for reading said combined representations from said registration memory at a group repetition rate related to the frequency of a tone to be generated by said instrument.
2. The apparatus of claim 1 wherein said combined representations are read from said registration memory at a rate that is independent of the rate at which said combined representations are written into said registration memory.
3. The apparatus of claim 1 wherein at least some of said voice memories are read only memories.
4. The apparatus of claim 1 wherein said means for writing combined representations into said registration memory loads successive address locations thereof at intervals between readout from different address locations thereof.
5. The apparatus of claim 1 wherein said means for reading representations for said voice memories comprise means for reading such representations one by one, and means for combining corresponding representations of selected voice memories and writing such combined representations one by one into said registration memory during intervals between read out of successive combined representations from said registration memory.
6. The apparatus of claim 1 wherein said means for combining and writing representations from said voice memories and writing such combined representations comprises means for accomplishing such combining and writing into a single address location of said registration memory during a period in which more than one read out from said registration memory occurs.
7. The apparatus of claim 1 wherein said means for combining representations from said voice memories and writing said combined representations comprises means for combining and writing one complete group of representations into said registration memory during the time that a complete group of combined representations is read from said registration memory more than once.
8. The system of claim 1 wherein said means for combining groups of amplitude sample representations read

from said voice memories comprises an adder, and means for transferring to said adder representations from respective ones of said voice memories in sequence.

9. The system of claim 1 including a second registration memory, said voice memories including first and second sets, said means for writing comprising means for writing into said first-mentioned registration memory combined representations read from memories of said first set, and means for writing into said second registration memory combined representations read from memories of said second set, said means for reading from said registration memories comprising means for separately reading from either or both at group repetition rates related to frequencies of tones to be generated by said instrument.

10. The method of generating a musical tone which tone comprises the combination of a selected one or more of a number of musical voices each of which is separately stored in a voice memory as a group of amplitude sample representations of a complex wave form of a respective voice, said method comprising the steps of

reading amplitude sample representations from at least selected ones of said voice memories, combining corresponding representations read from different ones of said voice memories in accordance with a desired voice combination of a tone to be generated, said combining being at a first rate, temporarily storing said combined amplitude sample representations, and reading said temporarily stored combined amplitude sample representations at a second rate related to the frequency of the tone to be generated by the instrument.

11. The method of claim 10 wherein said second rate is less than said combining rate.

12. The method of claim 10 wherein said second rate is greater than the rate of storing said combined representations.

13. The method of claim 10 wherein at least one of said steps of reading said voice memories, combining representations read from said voice memories, and temporarily storing such combined representations is initiated when a different voice or combination of voices is chosen.

14. The method of claim 13 wherein said one step that is initiated when a different voice or combination of voices is chosen is terminated after a number of complete cycles of temporary storage of combined representations.

15. The method of claim 14 for use in an electrical musical instrument wherein said one step is also initiated when power is applied to said instrument.

16. An electrical musical instrument comprising first storage means for storing sampled amplitude representations of a musical voice, means for reading said stored sampled amplitude representations from said first storage means, means for modifying the sampled amplitude representations read from said first storage means, second storage means, means for reading repetitive groups of sampled amplitude representations from said second storage means at a group repetition rate corresponding to a selected frequency of a musical tone, and

means for writing said modified sampled amplitude representations into said second storage means at a rate that is independent of said group repetition reading rate.

17. The instrument of claim 16 wherein said means for modifying said sampled amplitude representations read from said first storage means comprises means for combining with said representations of said first storage means a group of sampled amplitude representations delineating a second musical voice.

18. The method of combining voices of a multiple voice electrical instrument comprising the steps of generating representations of a plurality of voices, selectively combining representations of at least two of said voices, storing said combined representations in a storage device, repetitively reading out of said storage device groups of combined representations stored therein, said reading out being repeated at a group repetition rate that is manually selectable according to the frequency of a tone to be generated including said combined voices, and producing an output signal from said repetitive groups of representations.

19. The method of claim 18 wherein said representations comprise amplitude samples collectively delineating a complex wave shape.

20. The method of claim 18 wherein the rate of storing representations in said storage device is independent of the rate of read out therefrom.

21. An alterable memory system for a musical instrument comprising a read-write registration memory having a plurality of address locations for respectively storing representations of amplitude samples of a complex wave form,

read out means including means for advancing from one address location of said memory to the next at a rate related to a selected musical frequency, whereby groups of said amplitude representations are repetitively read from said memory at a group repetition rate related to said musical frequency, a plurality of voice memories, each storing representations of amplitude samples of a musical voice, and

means for combining representations from selected voices and loading such combined representations into successive address locations of said registration memory, said last-mentioned means including means for advancing said loading of combined representations from one address location to the next in said registration memory at a rate that is independent of said first-mentioned rate of read out advancing from one location to the next.

22. The system of claim 21 wherein said rate of advancing from one address location to the next for loading into said registration memory is less than said rate of advancing from one address location to the next for read out therefrom, whereby selected ones of said voices may be combined at rates less than musical frequencies.

23. The system of claim 21 wherein said rate of advancing from one address location to the next for loading into said registration memory is substantially equal to said rate of advancing from one memory location to the next for read out from said registration memory.

24. The system of claim 21 wherein said rate of advancing from one address location to the next for loading into said registration memory is greater than said rate of advancing from one address location to the next for read out therefrom.

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