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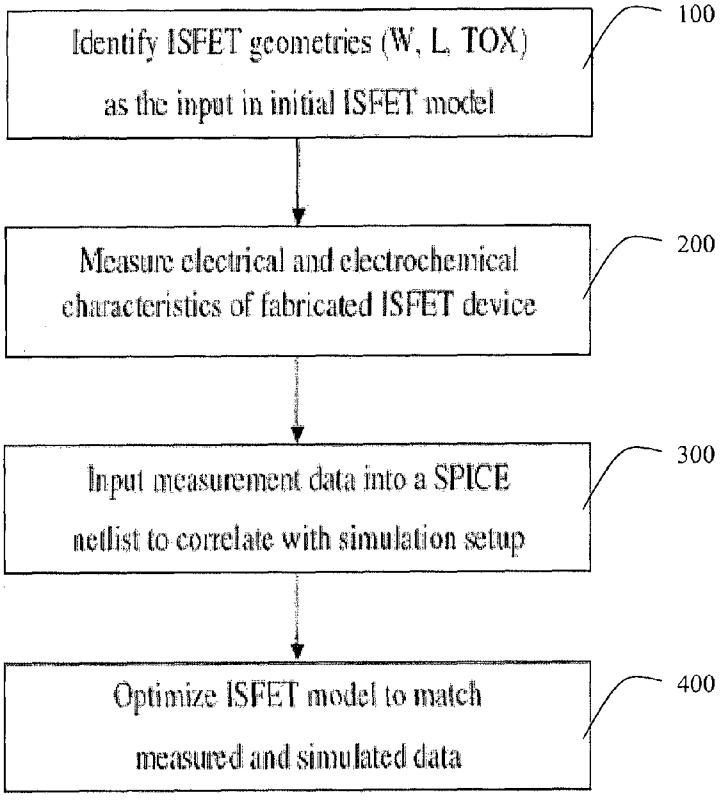
(54) Title: A METHOD OF GENERATING SPICE-COMPATIBLE ISFET MODEL



(57) Abstract: The present invention relates to a method to generate a compact SPICE model based on the available sub-circuit model descriptions. The method comprisingcomprising: identifying ISFET device geometries for width, length and gate oxide thickness as inputs in initial ISFET modeling (100); and measuring electrical and electrochemical characteristics of the fabricated ISFET device (200); characterized in that transferringthe electrical and electrochemical characteristics measurement data into SPICE netlist and correlating with simulation setup (300); and optimizing the ISFET model parameters using optimizer in SPICE simulator (400).

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— *as to the identity of the inventor (Rule 4.17(i))*

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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Description

Title of Invention: A METHOD OF GENERATING SPICE-COMPATIBLE ISFET MODEL

[1] **FIELD OF INVENTION**

[2] The present invention relates to a method of generating user-friendly ISFET model for simulation of semiconductor integrated circuit. It is particularly suitable to accurately characterize the electrical and electrochemical behaviors of the ISFET device.

[3] **BACKGROUND OF THE INVENTION**

[4] There is no user-friendly extraction flow available for Ion-Sensitive Field Effect Transistor (ISFET) model. This fact leads to the difficulties of modeling and integrating ISFET devices into complete circuit architecture for several critical purposes such as design optimization and yield prediction. Circuit level design integration and simulation are vital to meet the increasing demand of robust sensor products. Some researchers tend to use any available commercial model parameters from provided commercial datasheet or any research papers which is not extracted from the actual fabricated wafer, resulting to the wrong analysis and lengthen the product development cycle. The difficulty of developing this model is mainly due to the complicated integration between standard electrical and non-standard electrochemical characteristics of the ISFET device. There are some efforts done to characterize ISFET device in order to ensure that the ISFET device could be simulated and integrated with other silicon-based devices and produce highly value-added sensor products.

[5] Unfortunately, most of the reports are focusing on the system level device modeling such as using VHDL or Verilog-A platforms. This requires huge efforts in understanding the program source code and compiling the whole program for the sake of proper ISFET model extraction. There are also reports on ISFET model development based on the well-known SPICE (Simulation Program with Integrated Circuit Emphasis) simulator but the model still contains several parameters which are not SPICE-compatible and more towards the behavioral modeling. Besides that the said behavioral model also do not provides any tool or method for the critical model extraction purpose.

[6] Integrated circuit designers usually use circuit simulator to test the circuit design. In most cases, a simulation test is done to verify the design functionalities prior to the actual wafer fabrication stage. Besides that, the designers use the simulation analysis for further design optimization as well as predicting the design yield with the availability of accurate device model. ISFET is one of the available devices in semiconductor industry. A part from its important role in the development of highly integrated sensor products, the device is actually suffers the lack of support in device modelling department. This drawback has leads to difficulties in integrating such device into the complete circuit architecture. There are prior arts have been developed

for ISFET model but they typically used either system level or hybrid model platforms which resulting to the complicated model extraction flow, as shown in **Figure 1**. Considering the fact that the current ISFET models are developed based on certain platforms, so it is only suitable for certain simulator and cannot be easily ported into other simulators. These constrains have actually put further dilemma to the ISFET device engineer and circuit designer in finding the correct solution during the design integration stage. Therefore, there is need to develop a user-friendly ISFET model to be easily used and understand by both device engineer and circuit designer.

[7] **SUMMARY OF THE INVENTION**

[8] According to an aspect of the present invention, the present invention provides a method of generating SPICE-compatible ISFET model using built-in optimizer function, wherein the methods comprising: identifying ISFET device geometries for width, length and gate oxide thickness as inputs in initial ISFET modeling (100); and measuring electrical and electrochemical characteristics of the fabricated ISFET device (200); characterized in that transferring the electrical and electrochemical characteristics measurement data into SPICE netlist and correlating with simulation setup (300); and optimizing the ISFET model parameters using optimizer in SPICE simulator (400).

[9] The above provision is advantageous as it provides a method to generate a compact SPICE model based on the available sub-circuit model descriptions. SPICE is the de-facto standard which has revolutionized the semiconductor industry and is easily ported to other non-SPICE circuit simulators such as Spectre and Eldo. The constrain of integration between electrical and electrochemical characteristics is handled by extracting standard MOSFET model parameters for standard electrical part first follows by the sub-circuit modeling to take care on the electrochemical part. It serves as a generic description of the ISFET devices in different kind of supported commercial and educational simulators as it use SPICE-compatible format. The present invention requires the electrical measurement from actual fabricated ISFET device. The measurement results are transferred into the circuit simulator netlist for the extraction of related model parameters. In the initial stage, the uses of default model parameters would not show good agreement between measured and simulated data. Built-in optimizer function in SPICE circuit simulator is utilized in the present invention for the curve fitting between measured and simulated.

[10] **BRIEF DESCRIPTION OF THE DRAWINGS**

[11] **Figure 1** illustrates the flow chart of the prior art of the present invention.

[12] **Figure 2** illustrates the method of generating SPICE-compatible ISFET model of the present invention.

[13] **Figure 3** illustrates details of ISFET measurement flow from electrical to electrochemical characteristics.

[14] **Figure 4**illustrates the optimization process to ensure the good fitting between

measured and simulated curves.

[15] **Figure 5** illustrates an example of optimization steps with SPICE model parameters and measurement and simulation setup.

[16] **Figure 6**illustrates the example of SPICE simulation file for model extraction process.

[17] **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

[18] Generally, the present invention relates to amethod of generating SPICE-compatible ISFET model using built-in optimizer function, wherein the methods comprising: identifying ISFET device geometries for width, length and gate oxide thickness as inputs in initial ISFET modeling (100); and measuring electrical and electrochemical characteristics of the fabricated ISFET device (200); characterized in that transferring the electrical and electrochemical characteristics measurement data into SPICE netlist and correlating with simulation setup (300); and optimizing the ISFET model parameters using optimizer in SPICE simulator (400).

[19] With reference to **Figure 2**, a wafer with fabricated ISFET structures is required in the first stage of the extraction flow. The geometrical parameters such as length (L), width (W) and gate oxide thickness (TOX) need to be identified first for the suitable selection of level in device modeling (100). Bigger ISFET structure could be modeled with SPICE model level 1, 2 or 3 while smaller ISFET structure need to use SPICE model level 13 (i.e. BSIM1). The next step is the actual device measurement using parameter analyzer (200).The step of measuring electrical and electrochemical characteristics (200) further comprising: measuring I-V curves at reference, lower and upper pH values (201); and exporting the measurement data into text file with certain format to agree with simulation setup (203).

[20] The electrical and electrochemical measurements are then transferred to the SPICE netlist (300) which contains the MOS model parameters and related sub-circuit description of the ISFET electrochemical component.The step of transferring the electrical and electrochemical characteristics measurement data into SPICE netlist (300) further comprising: setting the optimization setup for number of iterations, calculation of error between measured and simulated data and optimization acceptance criteria (301); connecting and sweeping the ISFET terminals for I-V curves simulation (303); and determining the correct setup with respect to the measurement data (305).

[21] The model parameters are extracted and optimized using built-in optimizer (400) available in the SPICE simulator to fit the measured and simulated curves.The step of optimizing the ISFET model parameters (400) further comprising: setting the initial ISFET model with default model parameters (401); adding the initial ISFET model into the SPICE netlist in accordance with the obtained measurement data (403); identifying the SPICE model parameters for each optimization steps (405); setting the optimization range for the minimum and maximum values based on the provided typical value (407);

[22] simulating the SPICE netlist and optimization process is done based on the provided ISFET model parameters and optimization range (409); comparing the measured and simulated curves for a good fitting (411); adjusting the optimization range if the fitting is not good, in order to improve the fitting quality and continuing with the optimization (413); and continuing the optimization process if the fitting is good until it completes all the steps (415). The step of setting the initial ISFET model further comprising (401): selecting BSIM1 model with related ISFET sub-circuit model parameters (401a) and the typical model parameters comprising typical values for vfb0, phi0, k1, k2, eta0, x3e, muz, mus, u00, u1, x3u1, x3ms, x2e, x2m, x2ms, x2u0, x2u1, n0, nb0, nd0, Nsil and Nnit.The optimization process continues until the error between measured and simulated data are less than root-mean-square (RMS) error is less than 10%.

[23] The details of ISFET measurement flow from electrical to electrochemical characteristics are shown in **Figure 3**. Electrical characteristics are referring to the I-V curves measurements at typical or reference pH value while electrochemical characteristics are referring to the I-V curves measurement at pH smaller and bigger than the reference value. **Figure 4** illustrates the optimization process to ensure the good fitting between measured and simulated curves. The optimization process loops through all the optimization steps, so as to consider one optimization step at a time. **Figure 5** is a table illustrating an example of optimization steps with SPICE model parameters and measurement and simulation setup. **Figure 6** illustrates the example of SPICE simulation file for model extraction process.

[24] Although the invention has been described with reference to particular embodiment, it is to be understood that the embodiment is merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiment that other arrangements may be devised without departing from the scope of the present invention as defined by the appended claims.

Claims

[Claim 1] A method of generating SPICE-compatible ISFET model comprising:
identifyingISFET device geometries for width, length and gate oxide thickness as inputs in initial ISFET modeling (100); and
measuringelectrical and electrochemical characteristics of the fabricated ISFET device (200);
characterizedin that
transferringthe electrical and electrochemical characteristics measurement data into SPICE netlist and correlating with simulation setup (300); and
optimizingthe ISFET model parameters using optimizer in SPICE simulator (400).

[Claim 2] A method of generating SPICE-compatible ISFET model as claimed in Claim 1, wherein the step of measuring electrical and electrochemical characteristics (200) further comprising:
measuringI-V curves at reference, lower and upper pH values (201); and
exportingthe measurement data into text file with certain format to agree with simulation setup (203).

[Claim 3] A method of generating SPICE-compatible ISFET model as claimed in Claim 1, wherein the step of transferring the electrical and electrochemical characteristics measurement data into SPICE netlist (300) further comprising:
settingthe optimization setup for number of iterations, calculation of error between measured and simulated data and optimization acceptance criteria (301);
connectingand sweeping the ISFET terminals for I-V curves simulation (303); and
determiningthe correct setup with respect to the measurement data (305).

[Claim 4] A method of generating SPICE-compatible ISFET model as claimed in Claim 1, wherein the step of optimizing the ISFET model parameters (400) further comprising:
settingthe initial ISFET model with default model parameters (401);
addingthe initial ISFET model into the SPICE netlist in accordance with the obtained measurement data (403);
identifyingthe SPICE model parameters for each optimization steps (405);
settingthe optimization range for the minimum and maximum values based on the provided typical value (407);

simulatingthe SPICE netlist and optimization process is done based on the provided ISFET model parameters and optimization range (409);
comparingthe measured and simulated curves for a good fitting (411);
adjustingthe optimization range if the fitting is not good, in order to improve the fitting quality and continuing with the optimization (413); and
continuingthe optimization process if the fitting is good until it completes all the steps (415).

[Claim 5] A method of generating SPICE-compatible ISFET model as claimed in Claim 4, wherein the step of setting the initial ISFET model further comprising (401):
selectingBSIM1 model with related ISFET sub-circuit model parameters (401a).

[Claim 6] A method of generating SPICE compatible ISFET model as claimed in Claim 4, wherein the step of continuing the optimization process (415) covers all steps right from threshold voltage, drain current, sub-threshold swing parameters, to surface site density parameters.

[Claim 7] A method of generating SPICE-compatible ISFET model as claimed in Claim 5, wherein the typical model parameters comprising typical values for vfb0, phi0, k1, k2, eta0, x3e, muz, mus, u00, u1, x3u1, x3ms, x2e, x2m, x2ms, x2u0, x2u1, n0, nb0, nd0, Nsil and Nnit.

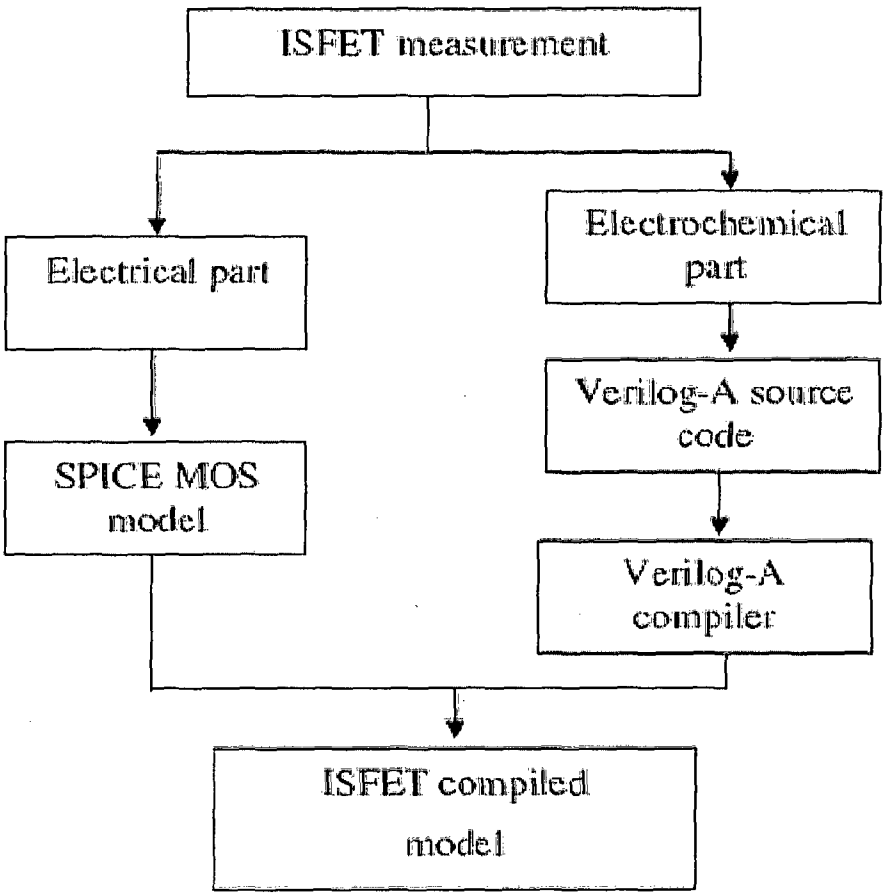
ISFET measurement
Electrical part
Electrochemical part
SPICE MOS model
Verilog-A source code
Verilog-A compiler
ISFET compiled model

Figure 1

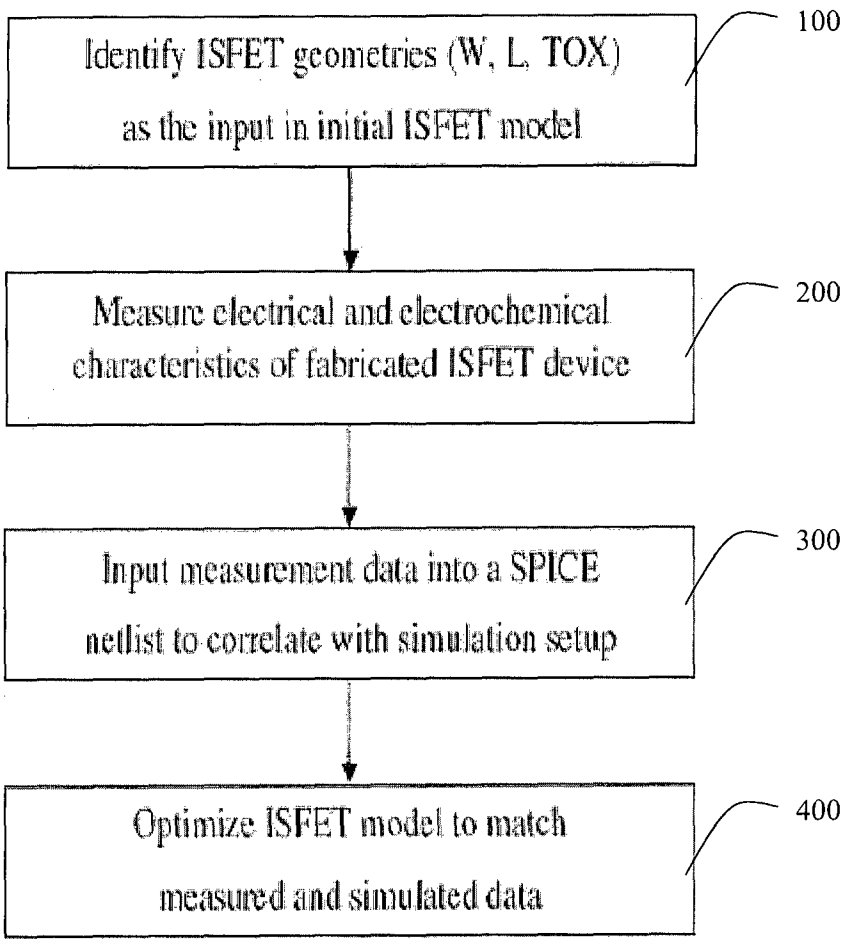
Identify ISFET geometries (W, L, TOX) as the input in initial ISFET model
100
Measure electrical and electrochemical characteristics of fabricated ISFET device
200
Input measurement data into a SPICE netlist to correlate with simulation setup
300
Optimize ISFET model to match measured and simulated data
400

Figure 2

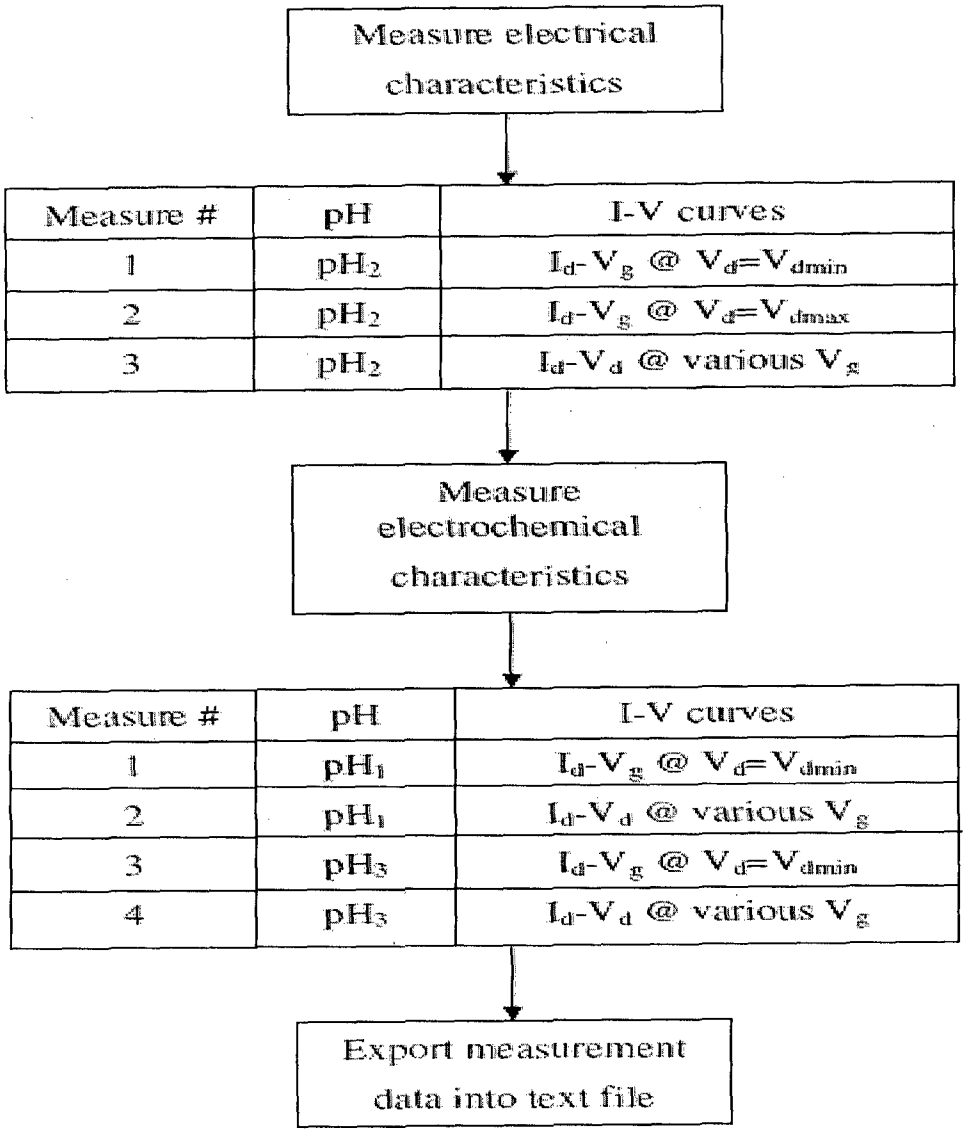
Measure electrical characteristics
Measure # | pH | I-V curves
1 | pH2 | Id-Vg @ Vd=Vdmin
2 | pH2 | Id-Vg @ Vd=Vdmax
3 | pH2 | Id-Vd @ various Vg
Measure electrochemical characteristics
Measure # | pH | I-V curves
1 | pH1 | Id-Vg @ Vd=Vdmin
2 | pH1 | Id-Vd @ various Vg
3 | pH3 | Id-Vg @ Vd=Vdmin
4 | pH3 | Id-Vd @ various Vg
Export measurement data into text file

Figure 3

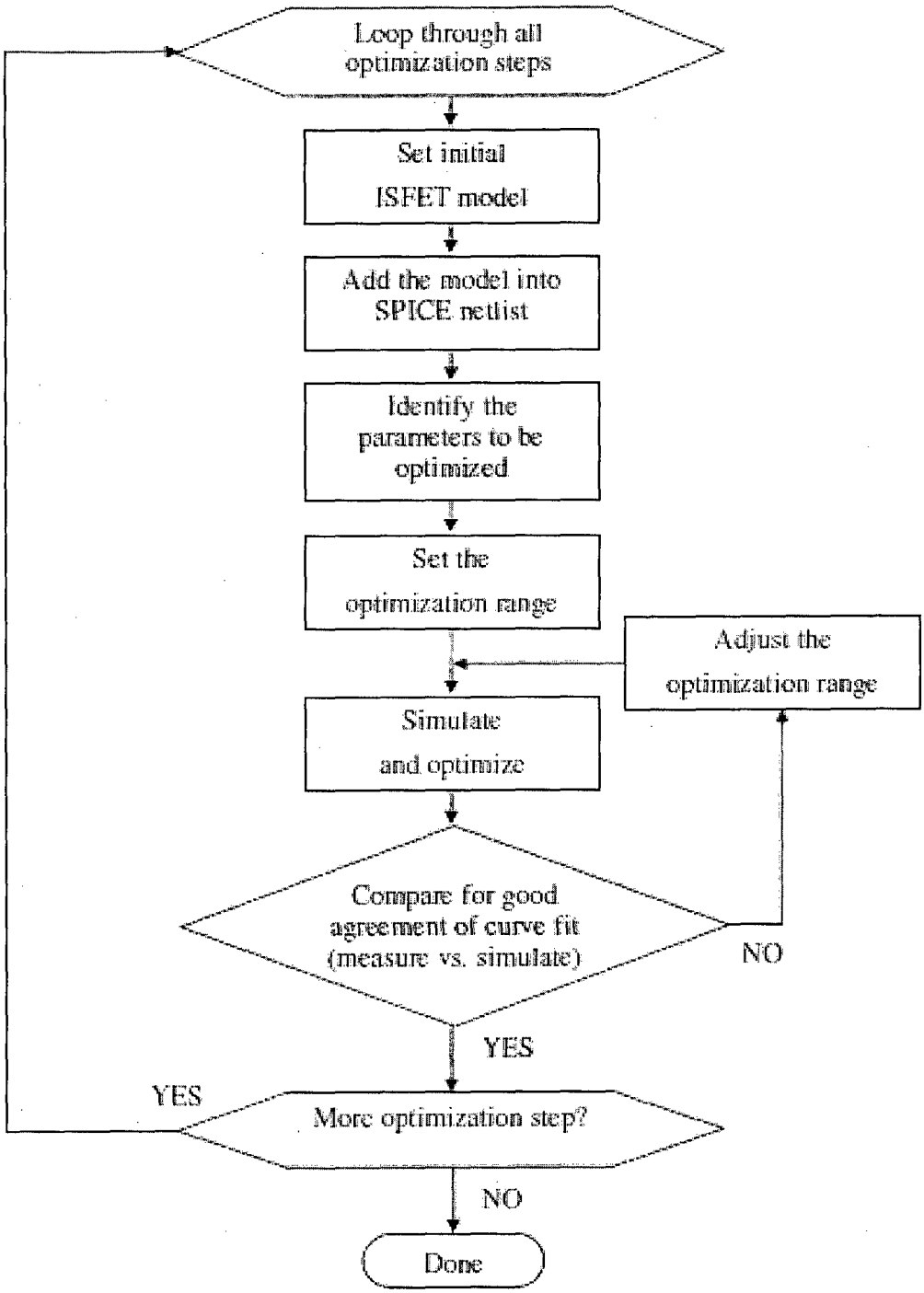
Loop through all optimization steps
Set initial ISFET model
Add the model into SPICE netlist
Identify the parameters to be optimized
Set the optimization range
Adjust the optimization range
Simulate and optimize
Compare for good agreement of curve fit (measure vs. simulate)
NO
YES
YES
More optimization step?
NO
Done

Figure 4

Step #	ISFET model extraction	SPICE model parameters	Measurement & simulation setup
1	1st threshold voltage parameters	vfb0, phi0, k1, k2	I_d-V_g @ V_d=V_{dmin} & pH=pH_2
2	2nd threshold voltage parameters	eta0, x3e	
3	1st drain current parameters	muz, mus, u00, u1, x3u1, x3ms	I_d-V_d @ various V_g & pH=pH_2
4	2nd drain current parameters	x2e, x2m, x2ms, x2u0, x2u1	
5	Subthreshold swing parameters	n0, nb0, nd0	I_d-V_g @ V_d=V_{dmax} & pH=pH_2
6	Surface site density parameters	Nsil, Nnit	I_d-V_d @ various V_g & pH=pH_1, pH_2 & pH_3

Figure 5

```
*****  ISFET model extraction – step 3  *****
.model optmod opt itropt=30
.inc "isfet.mod"

** Id-Vd curves for ISFET @ pH=pH2 & different Vg **
XIS  D   REFEL  S     B    PHIN     ISFET

Vbias  REFEL     0      Vbias
VpH    PHIN      0      DC      pH2
Vd     108       0      Vid
Vid    108       D      DC      0

.dc  DATA=drain  optimize=opt1    results=comp1     model=optmod
.meas  dc   comp1   err1   par(IVid)   I(Vid)   minval=1e-04   ignor=1e-05

.param  Vid=0     Vbias=0     VpH=0      IVid=0
.DATA   drain          Vid     Vbias   VpH     IVid
                       Vid1    Vbias1  VpH2    IVid1
                       Vid2    Vbias1  VpH2    IVid2
                       Vid3    Vbias1  VpH2    IVid3
                       Vid4    Vbias1  VpH2    IVid4
                       Vid1    Vbias1  VpH2    IVid1
                       .....   .....   .....   .....
                       .....   .....   .....   .....
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Figure 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2013/000192

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F17/50
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MARTINOIA S ET AL: "A behavioral macromodel of the ISFET in SPICE", SENSORS AND ACTUATORS B: CHEMICAL: INTERNATIONAL JOURNAL DEVOTED TO RESEARCH AND DEVELOPMENT OF PHYSICAL AND CHEMICAL TRANSDUCERS, ELSEVIER S.A, CH, vol. 62, no. 3, 1 March 2000 (2000-03-01), pages 182-189, XP004194214, ISSN: 0925-4005, DOI: 10.1016/S0925-4005(99)00377-9 page 182 - page 186 ----- -/--	1-7

[X] Further documents are listed in the continuation of Box C.

[ ] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 February 2014	06/03/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Alonso Nogueiro, L

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2013/000192

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MARTINOIA S ET AL: "Modeling ISFET microsensor and ISFET-based microsystems: a review", SENSORS AND ACTUATORS B: CHEMICAL: INTERNATIONAL JOURNAL DEVOTED TO RESEARCH AND DEVELOPMENT OF PHYSICAL AND CHEMICAL TRANSDUCERS, ELSEVIER S.A, CH, vol. 105, no. 1, 14 February 2005 (2005-02-14), pages 14-27, XP027810274, ISSN: 0925-4005 [retrieved on 2005-02-14] page 14 - page 25	1-7
A	"BSIM3v3.2.2 Manual. CHAPTER 6: Parameter Extraction", , 1 January 1999 (1999-01-01), pages 6-1, XP055104580, Retrieved from the Internet: URL:http://www.ee.ucr.edu/~rlake/EE135/SPICE/BerkeleySpice/BSIMv323/chp6.pdf [retrieved on 2014-02-26] the whole document	1-7
A	ANKELE B ET AL: "Enhanced MOS parameter extraction and SPICE modelling for mixed analogue and digital circuit simulation", MICROELECTRONIC TEST STRUCTURES, 1989. ICMTS 1989. PROCEEDINGS OF THE 1989 INTERNATIONAL CONFERENCE ON EDINBURGH, UK 13-14 MARCH 1989, NEW YORK, NY, USA,IEEE, US, 13 March 1989 (1989-03-13), pages 73-78, XP010043014, DOI: 10.1109/ICMTS.1989.39285 ISBN: 978-0-87942-714-6 the whole document	1-7
A	NAIMI S E ET AL: "Modeling of the pH-ISFET thermal drift", MICROELECTRONICS (ICM), 2009 INTERNATIONAL CONFERENCE ON, IEEE, PISCATAWAY, NJ, USA, 19 December 2009 (2009-12-19), pages 288-291, XP031631870, ISBN: 978-1-4244-5814-1 the whole document	1-7