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(54) **SEMICONDUCTOR DEVICE HAVING NANOSHEET TRANSISTOR AND METHODS OF FABRICATION THEREOF**

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(52) **U.S. Cl.**

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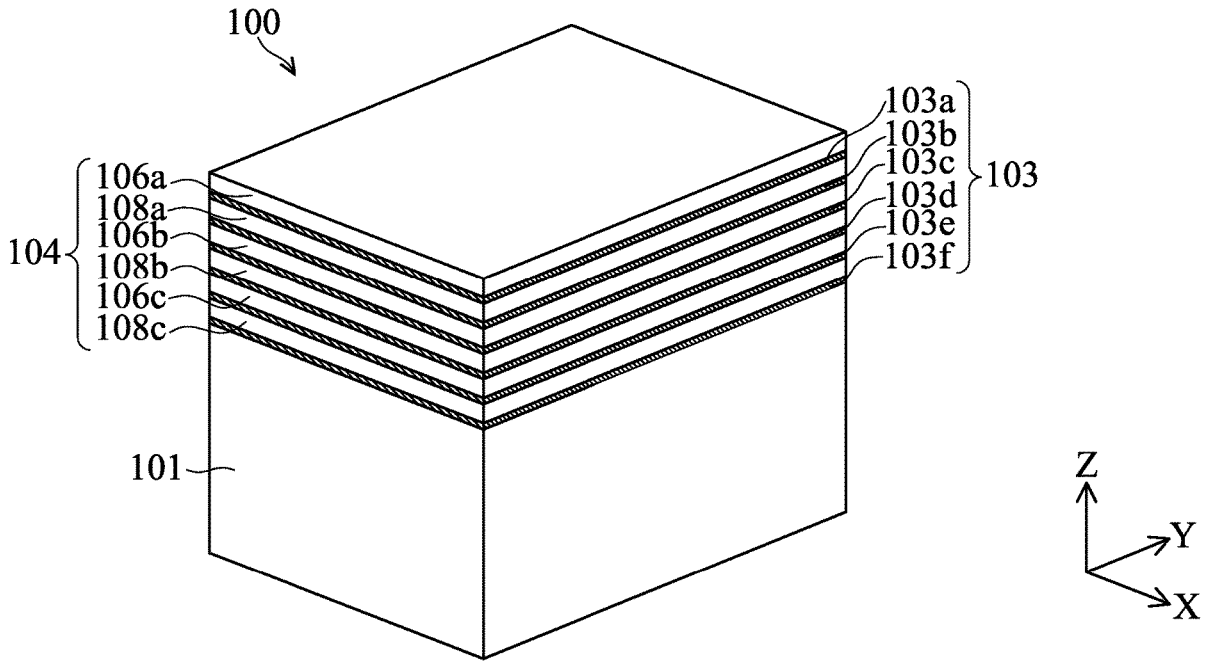
(57) **ABSTRACT**

Embodiments relate to a semiconductor device structure including a first channel layer having a first surface and a second surface, a second channel layer having a first surface and a second surface, and the first and second channel layers are formed of a first material. The structure also includes a first dopant suppression layer in contact with the second surface of the first channel layer, and a second dopant suppression layer parallel to the first dopant suppression layer. The second dopant suppression layer is in contact with the first surface of the second channel layer, and the first and second dopant suppression layers each comprises carbon or fluorine. The structure further includes a gate dielectric layer in contact with the first and second dopant suppression layers and the first surface of the first channel layer, and a gate electrode layer disposed on the gate dielectric layer.



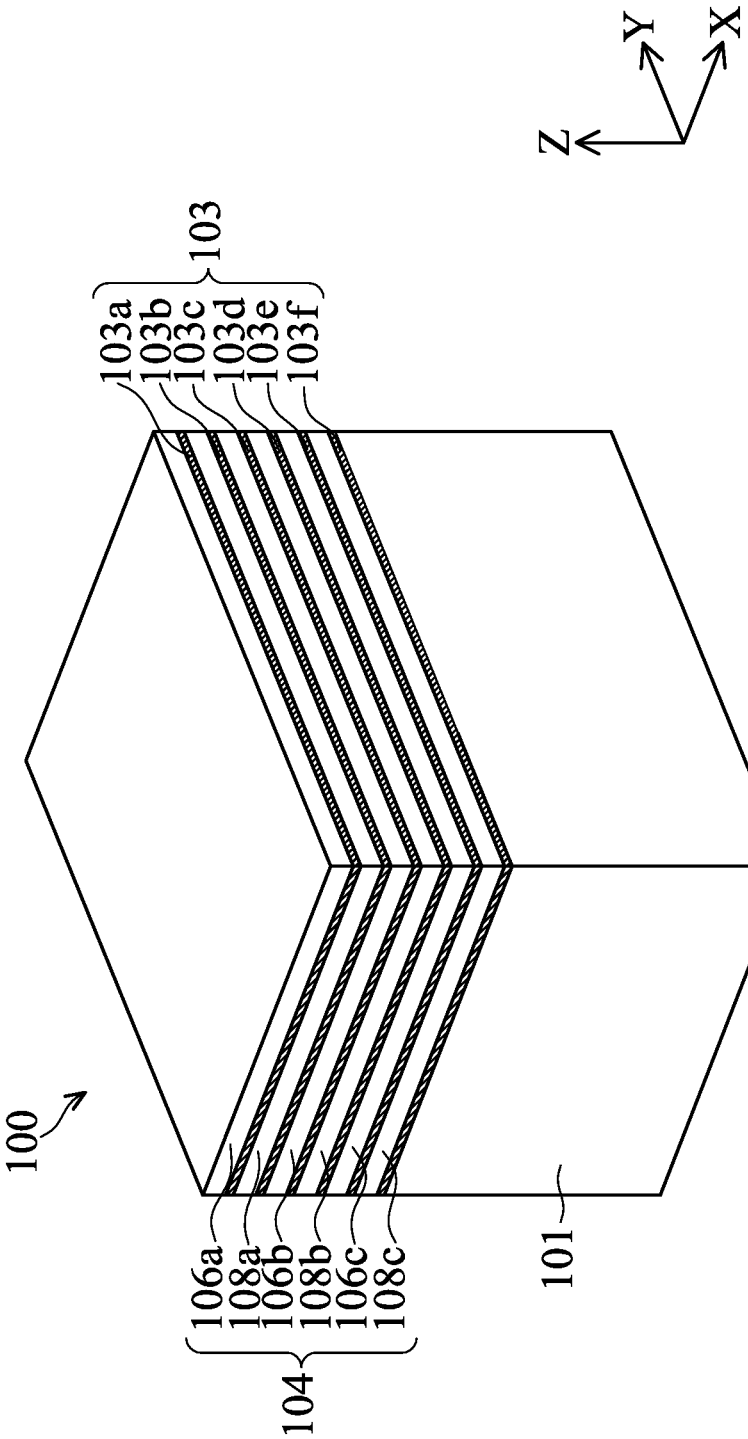

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FIG. 1

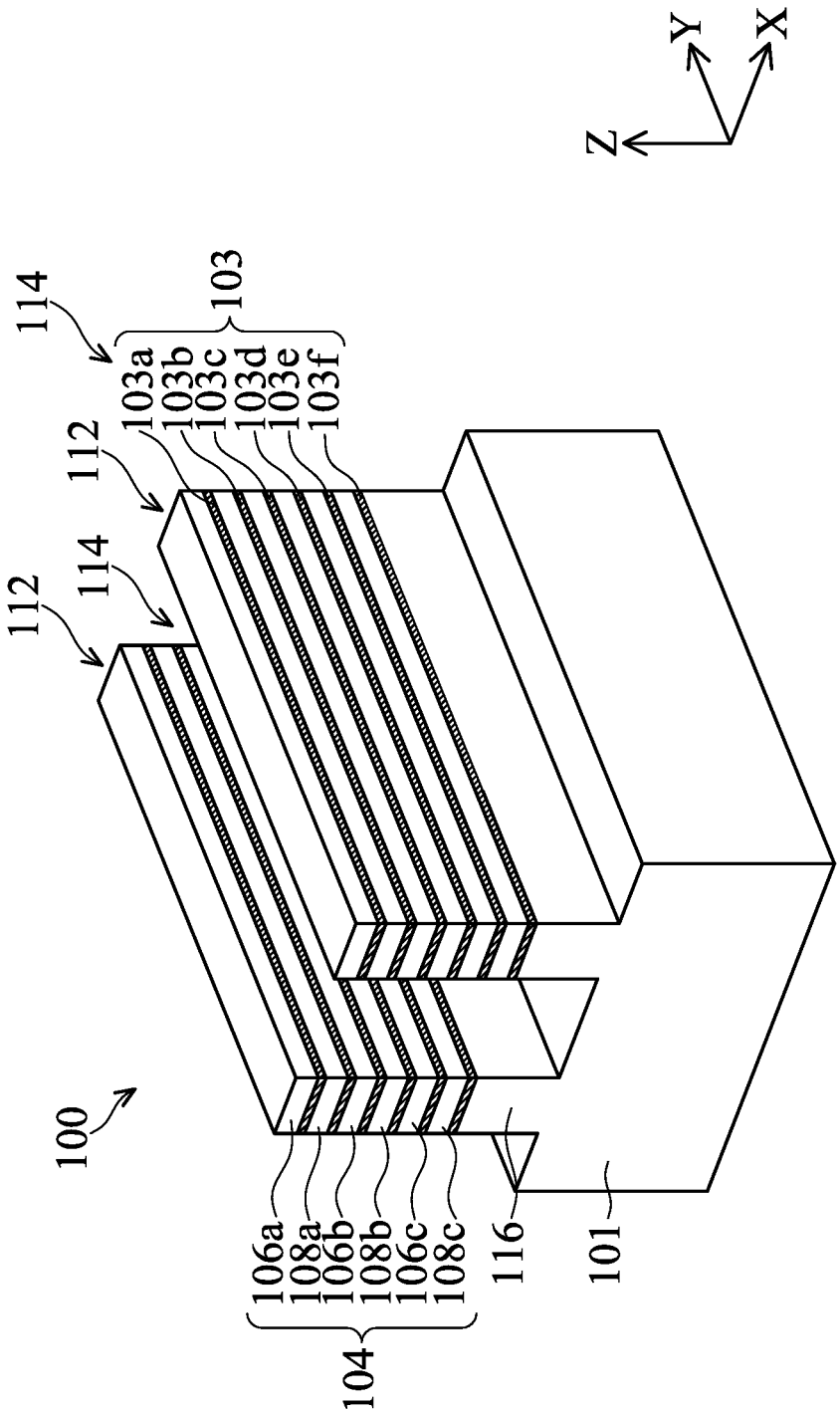
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FIG. 2

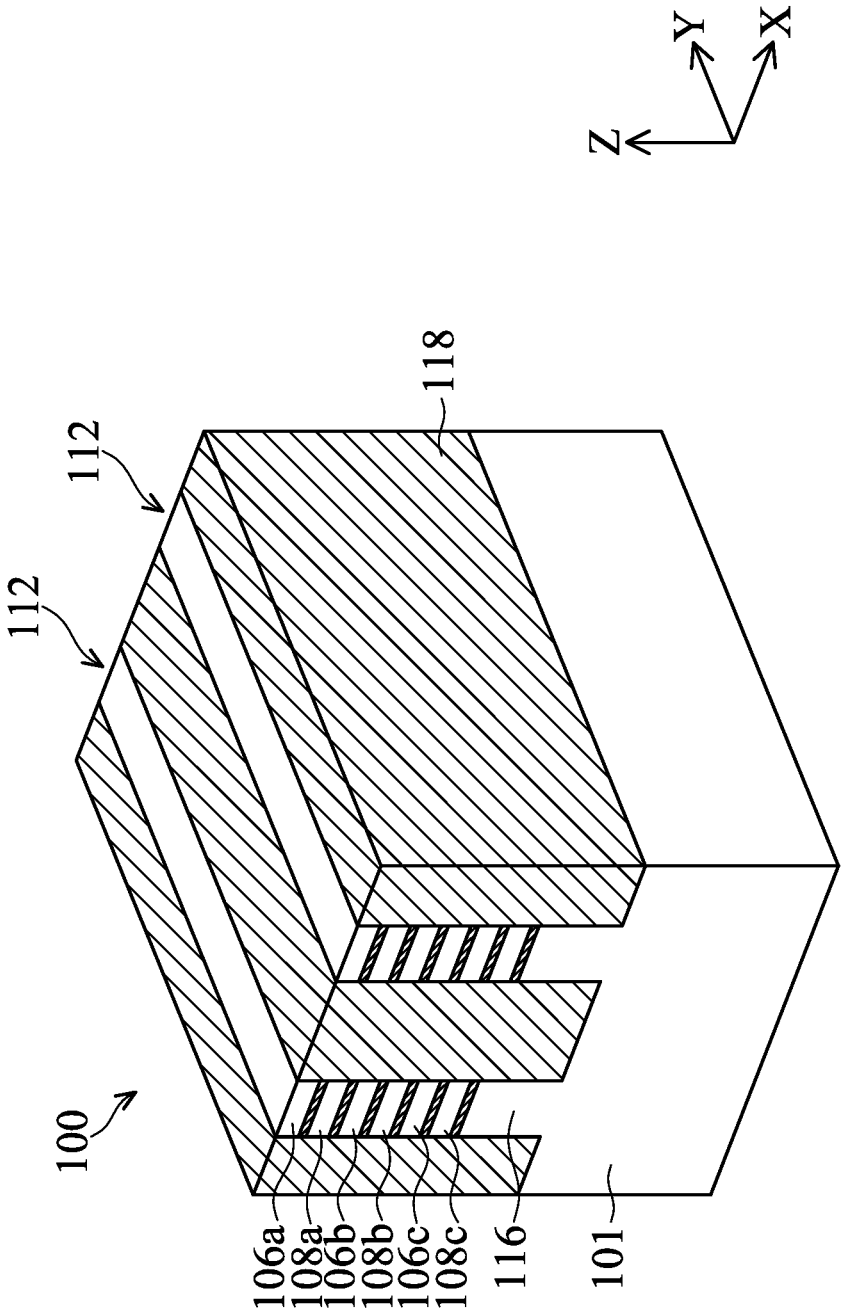

FIG. 3

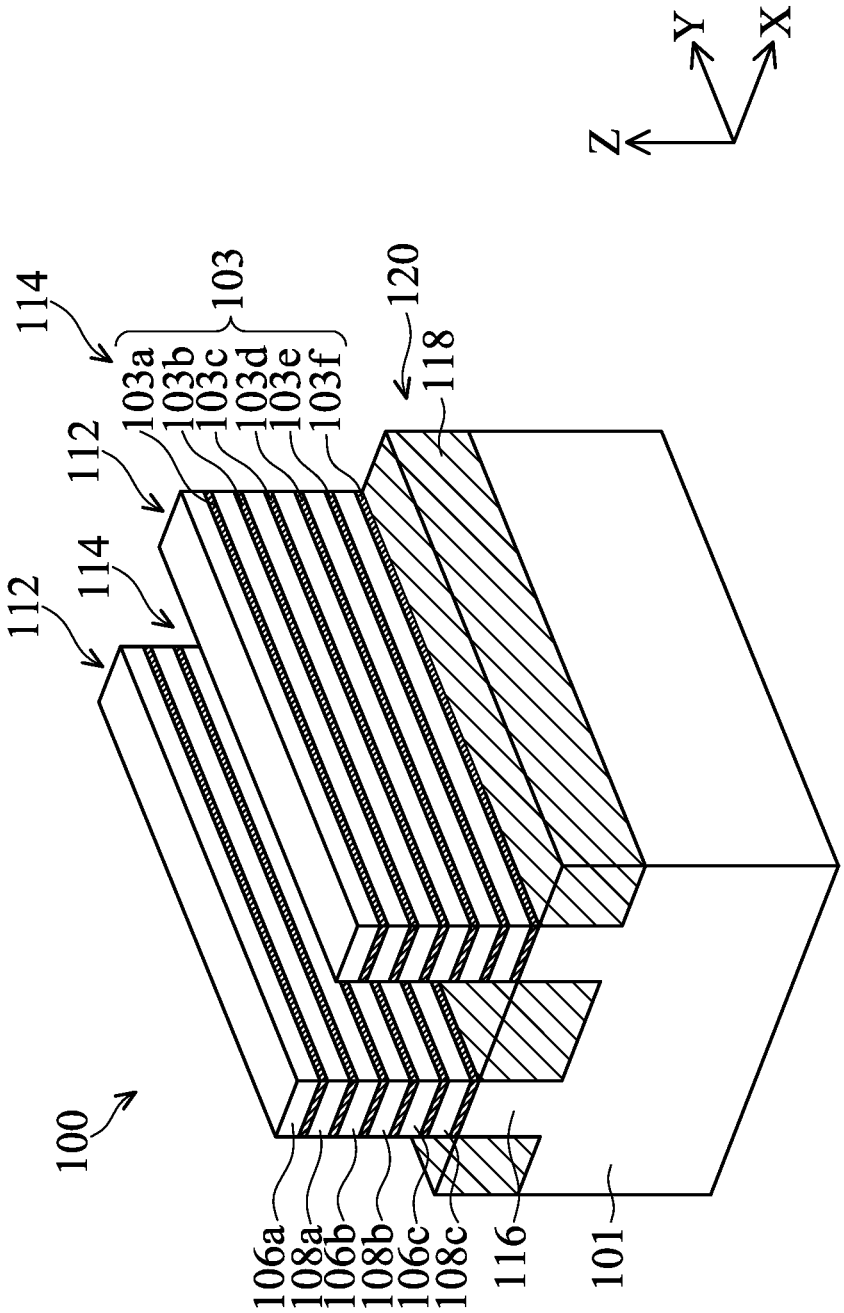
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FIG. 4

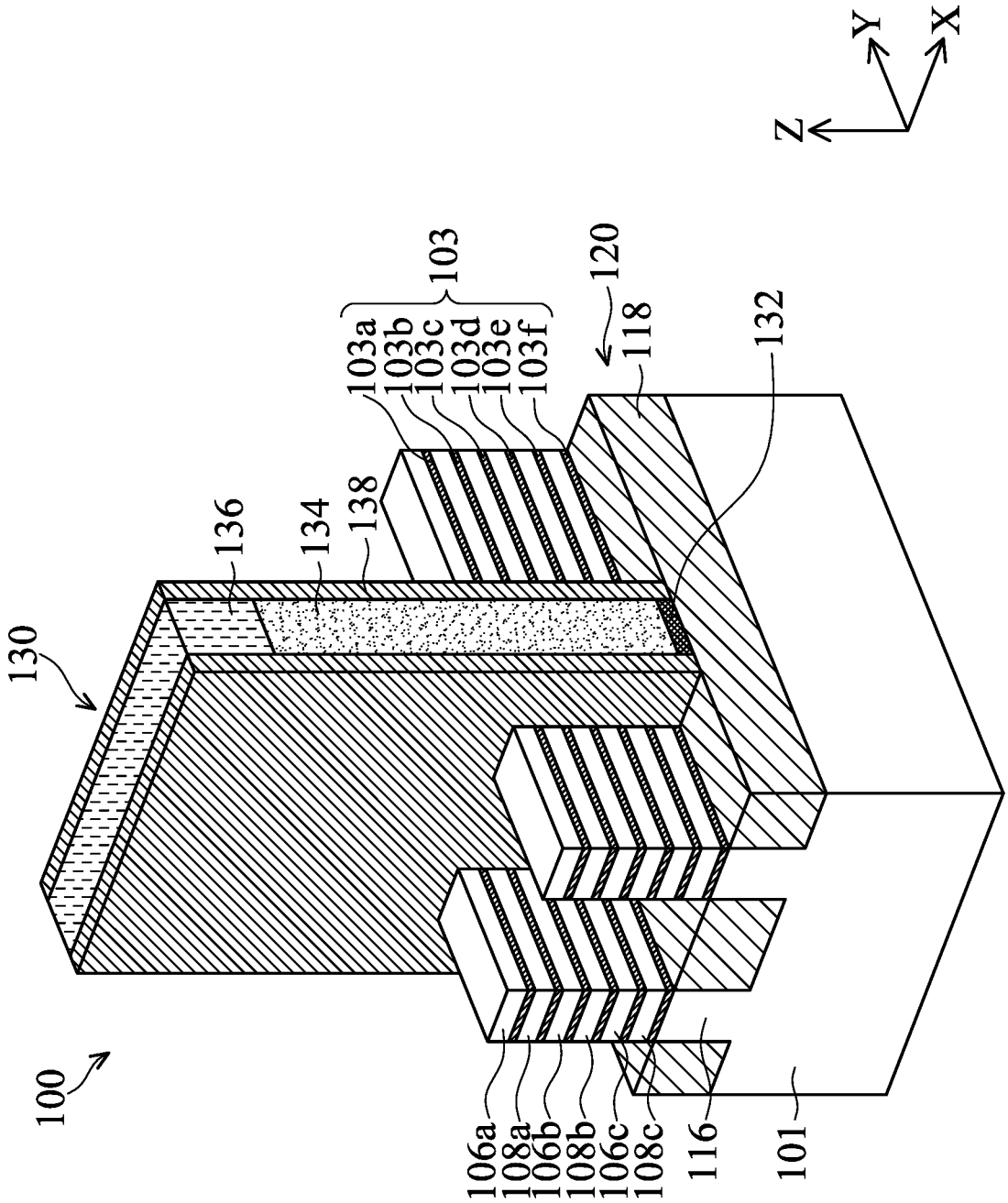
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FIG. 5

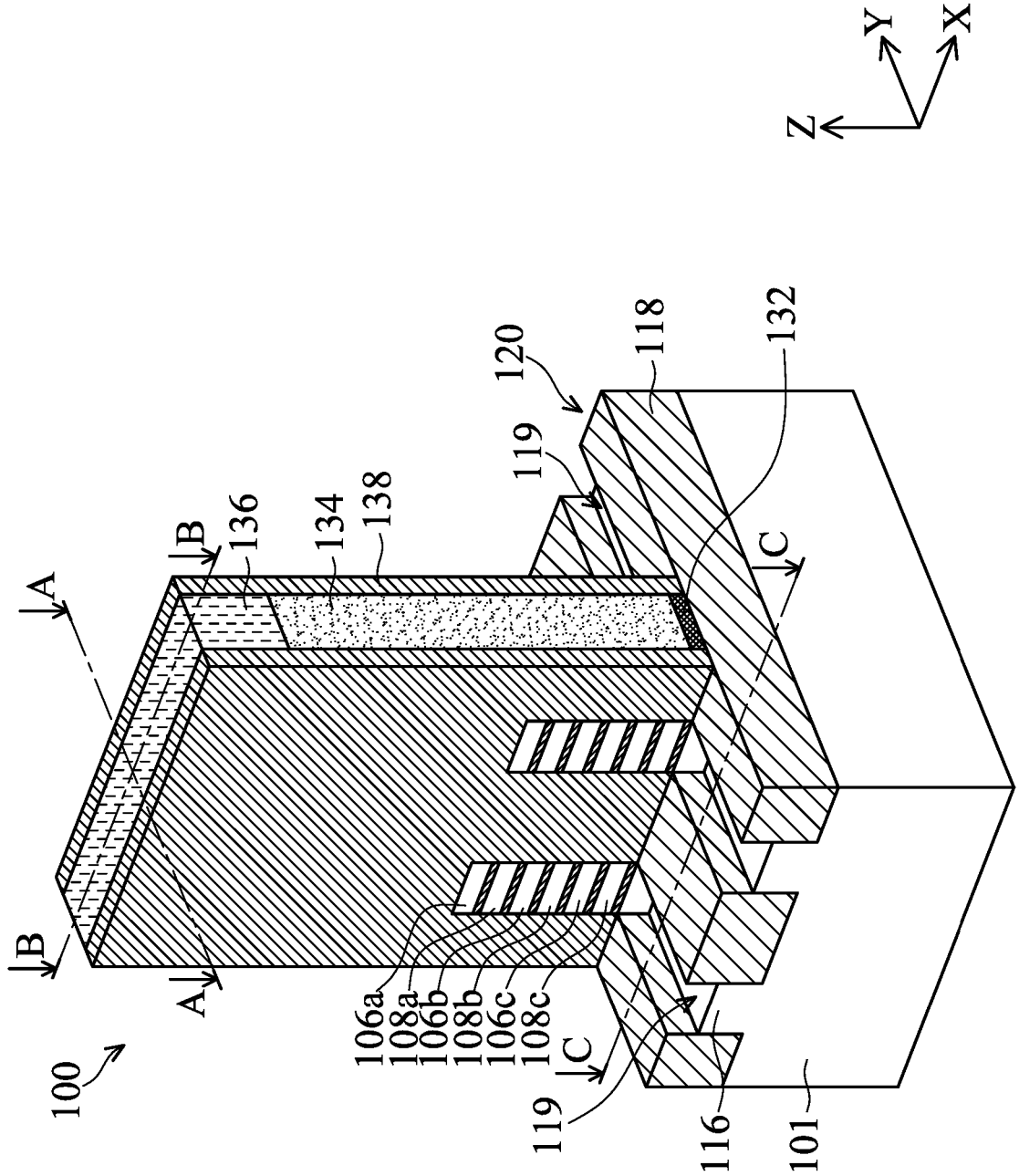
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FIG. 6

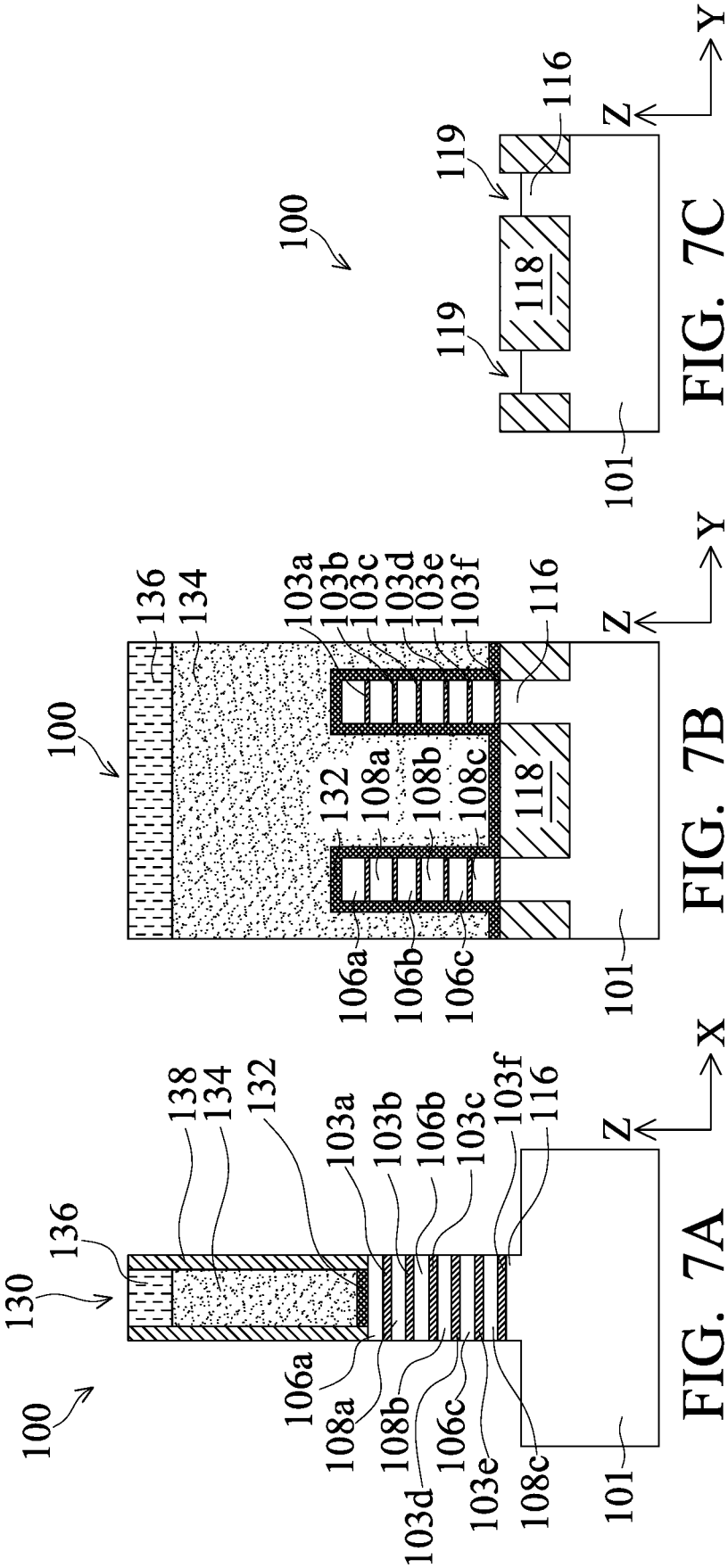

FIG. 7A

FIG. 7B

FIG. 7C

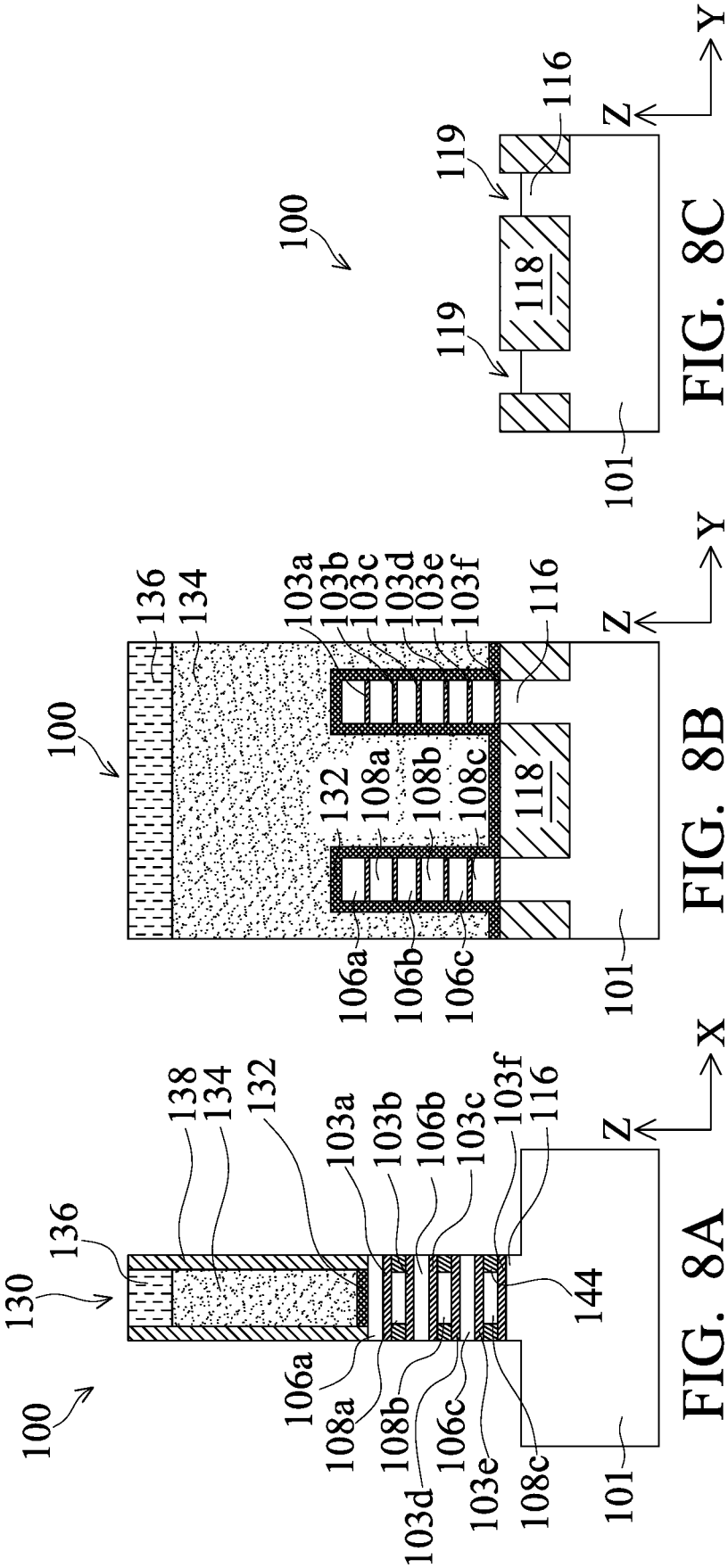

FIG. 8A

FIG. 8B

FIG. 8C

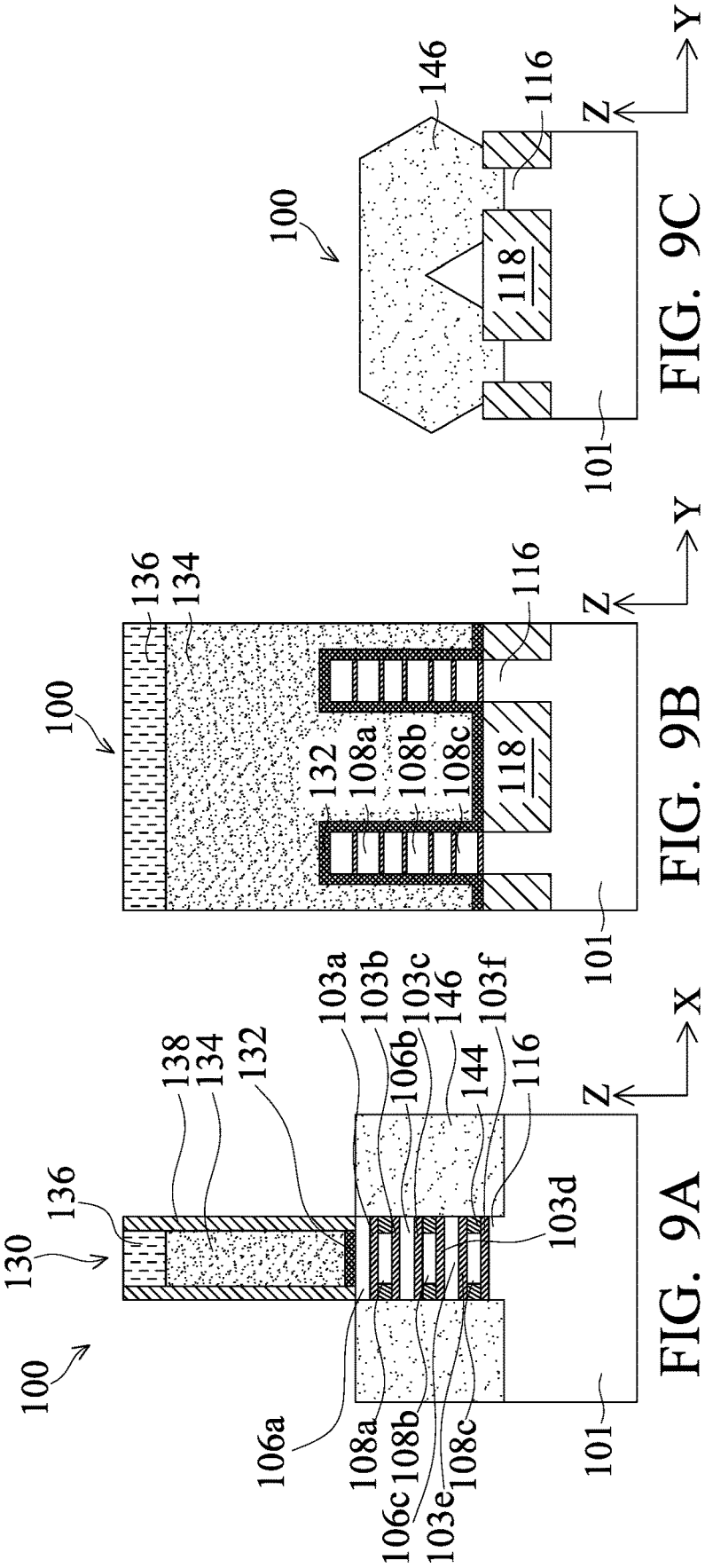

FIG. 9A

FIG. 9B

FIG. 9C

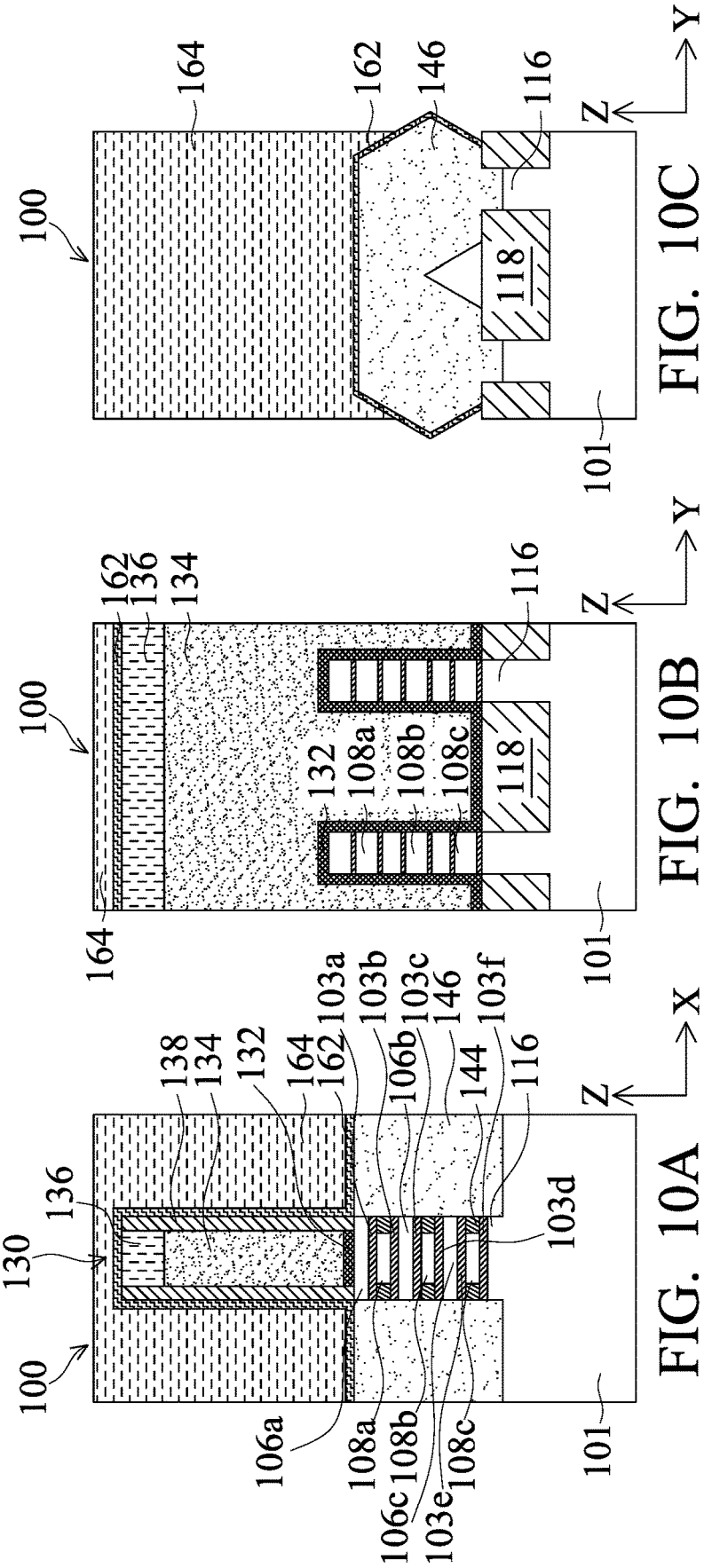

FIG. 10A

FIG. 10B

FIG. 10C

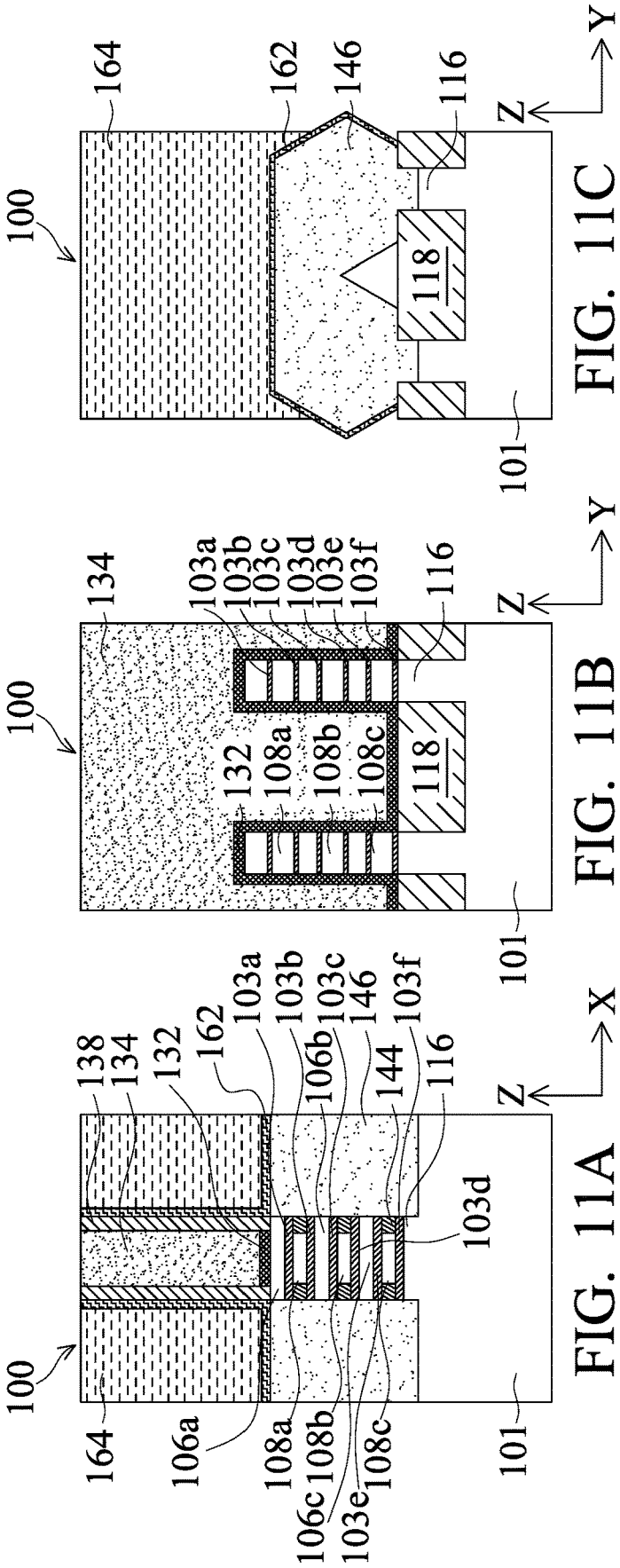

FIG. 11A

FIG. 11B

FIG. 11C

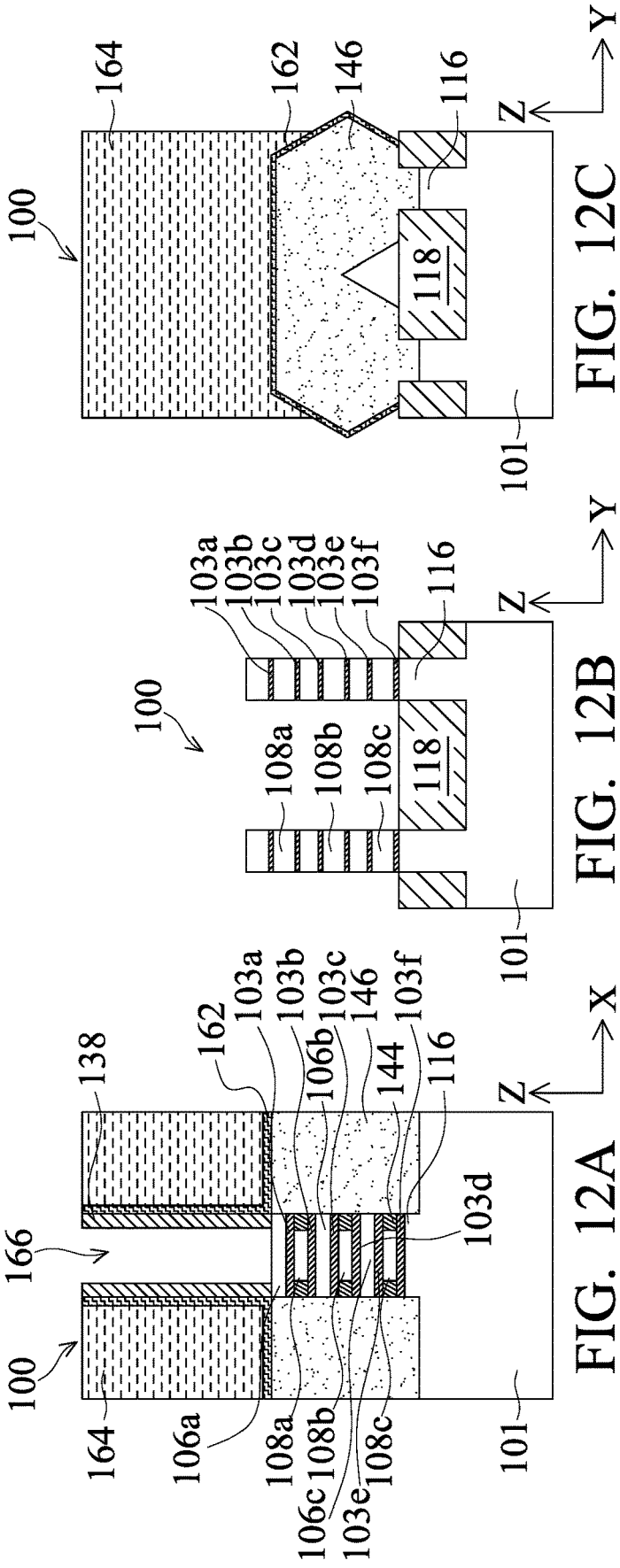

FIG. 12A

FIG. 12B

FIG. 12C

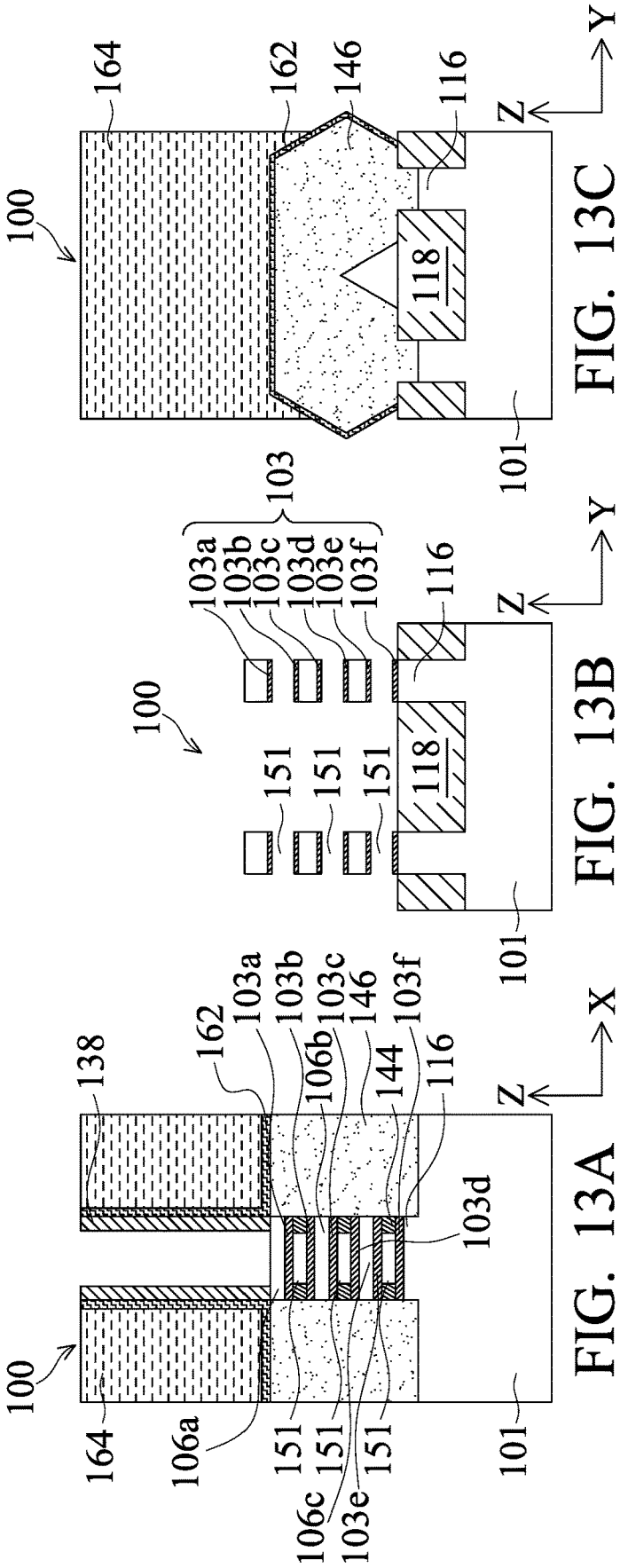

FIG. 13A

FIG. 13B

FIG. 13C

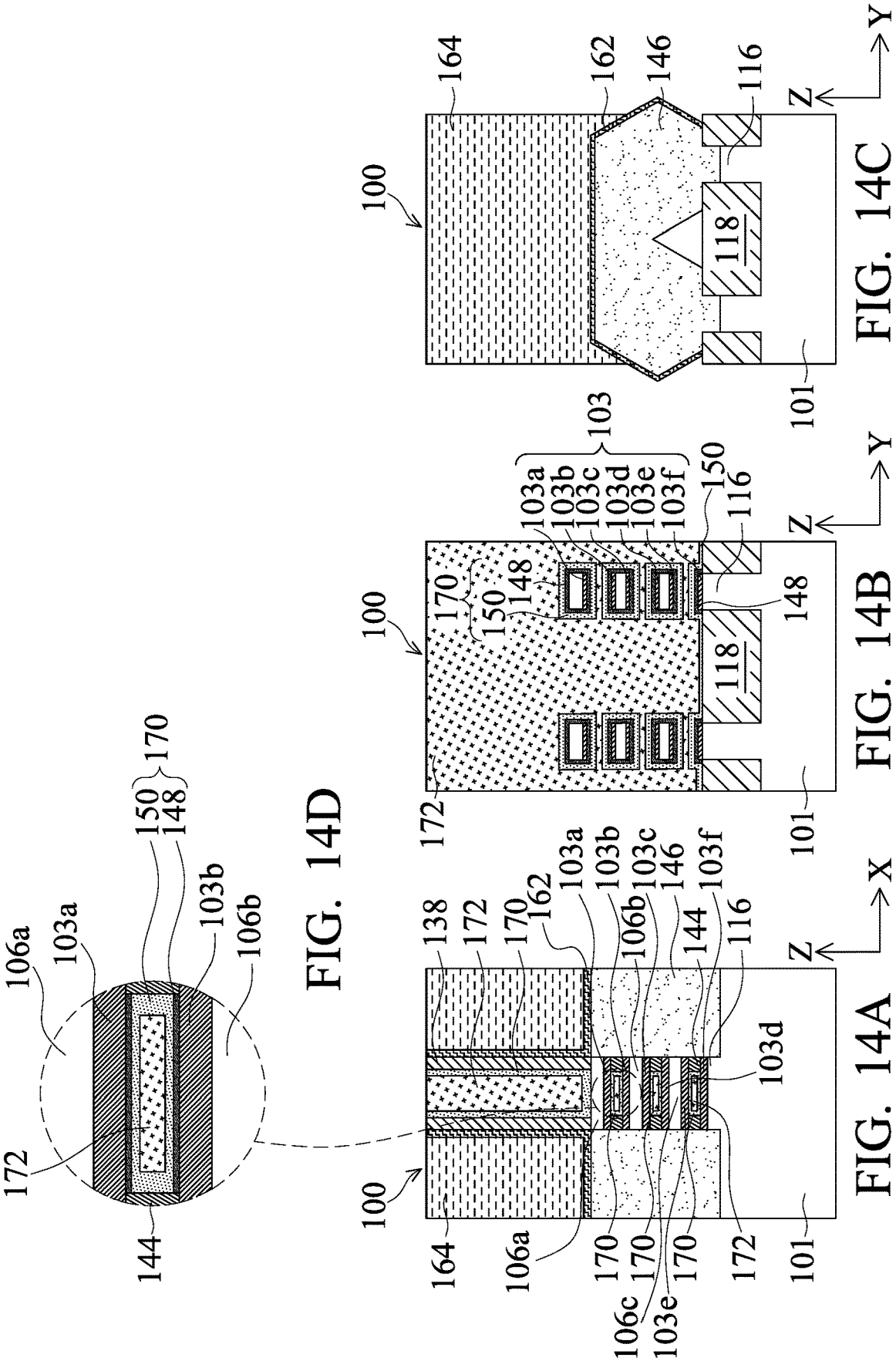
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FIG. 14C
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FIG. 14A
FIG. 14D

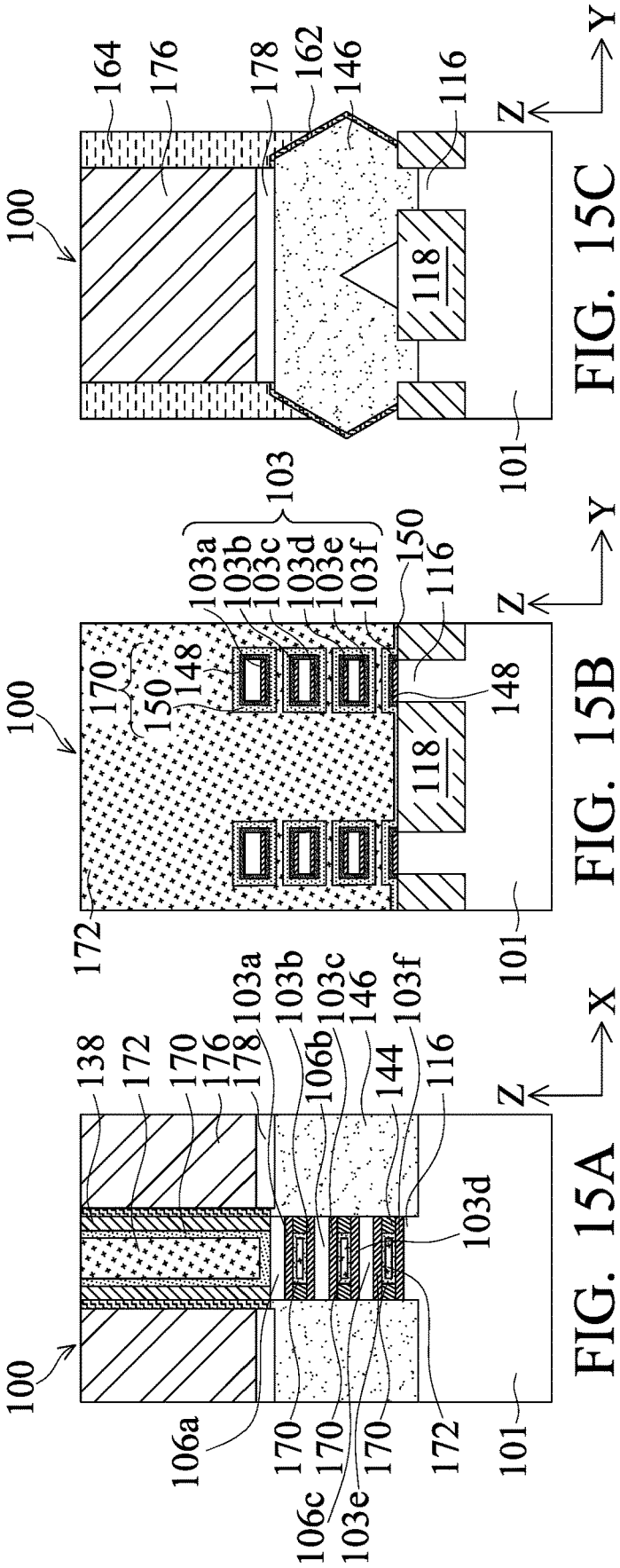

FIG. 15A

FIG. 15B

FIG. 15C

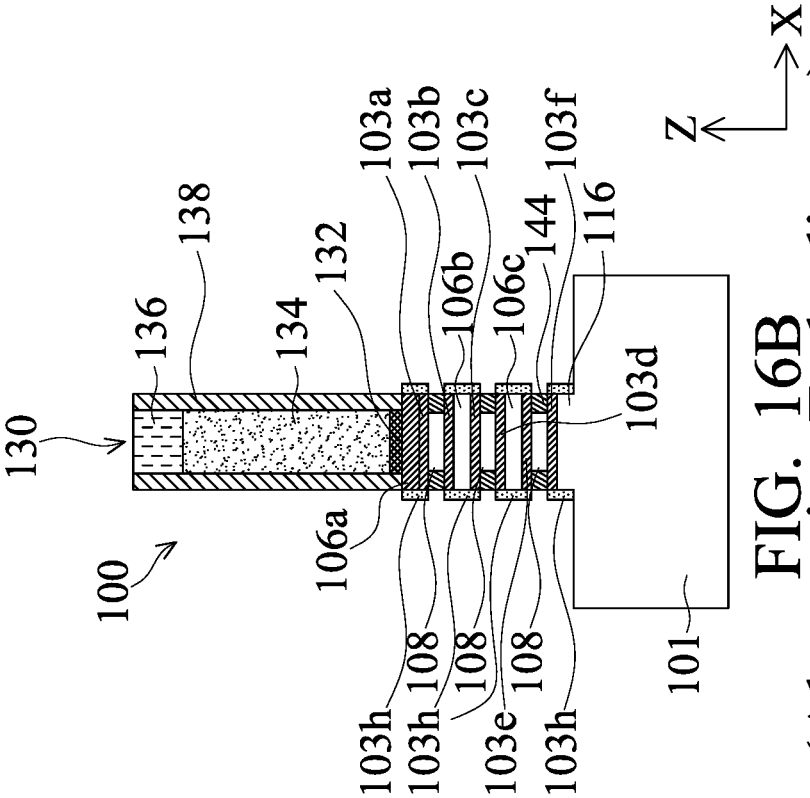

FIG. 16B
(Alternative Embodiment)

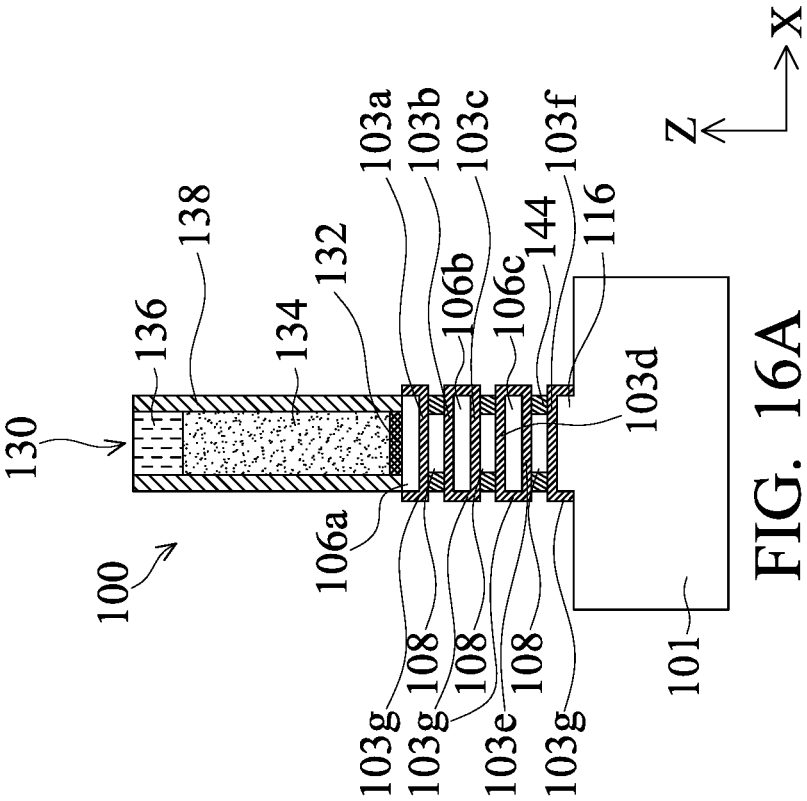

FIG. 16A

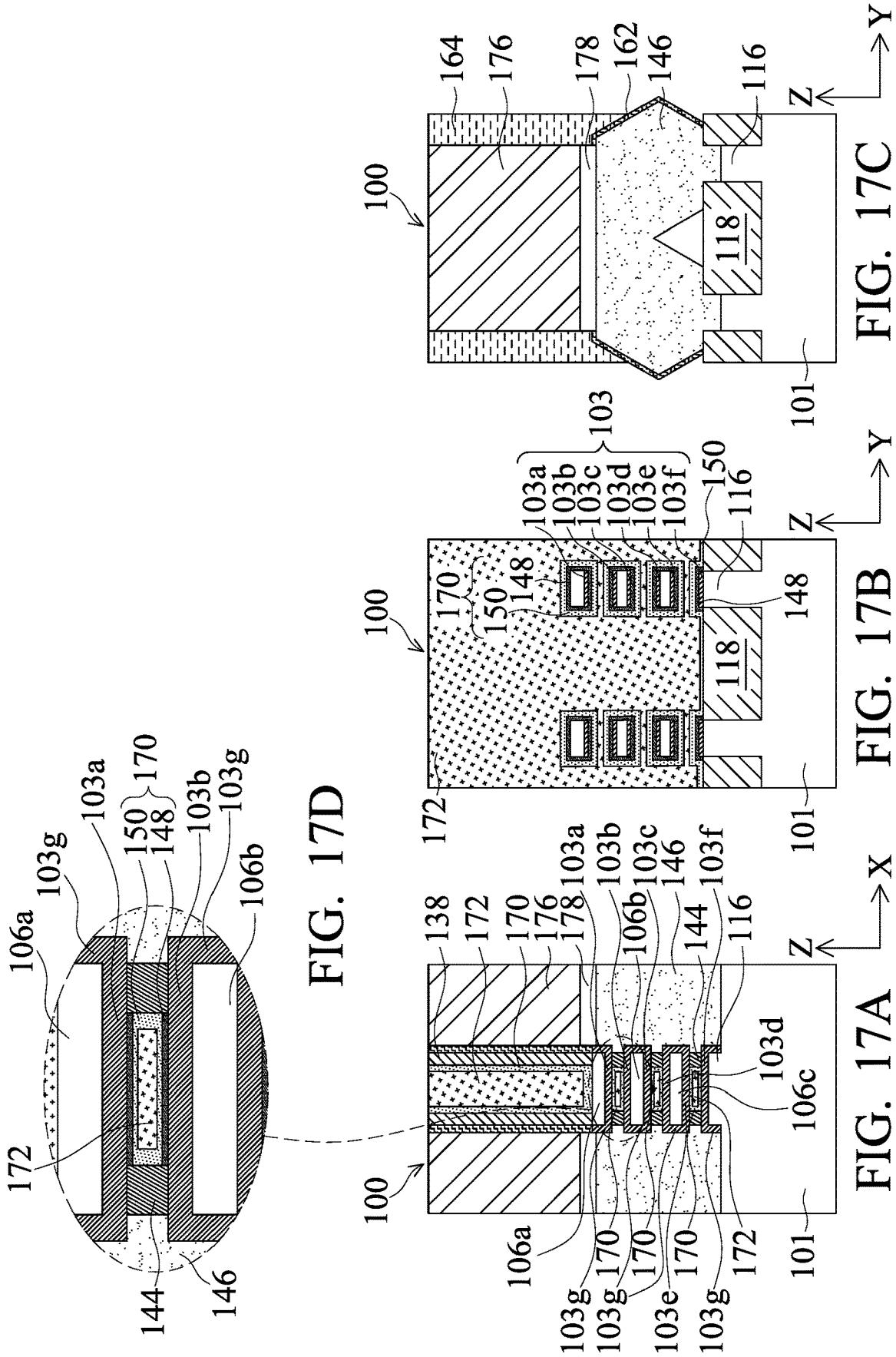
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FIG. 17C
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FIG. 17B
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FIG. 17D

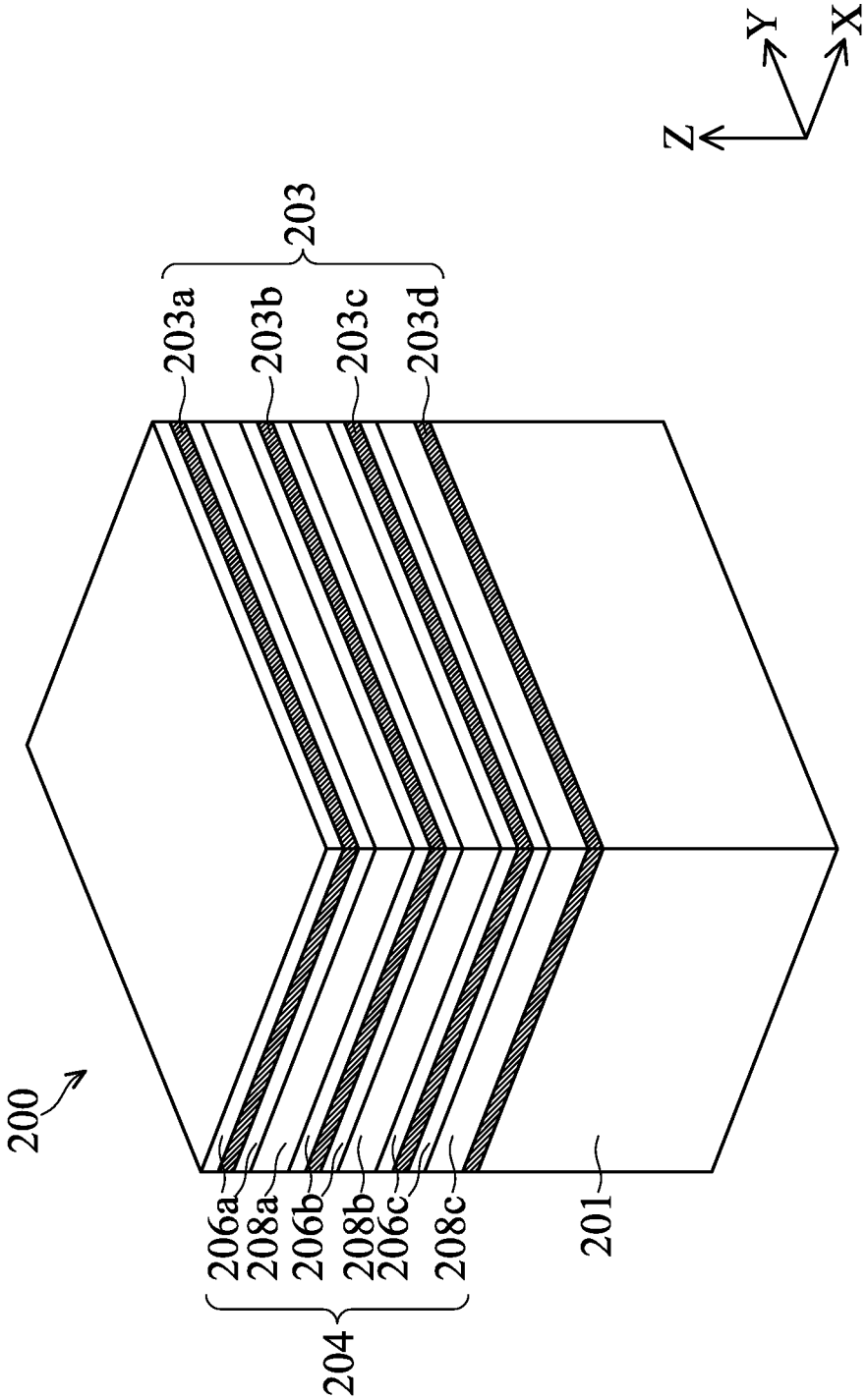

FIG. 18
(Alternative Embodiment)

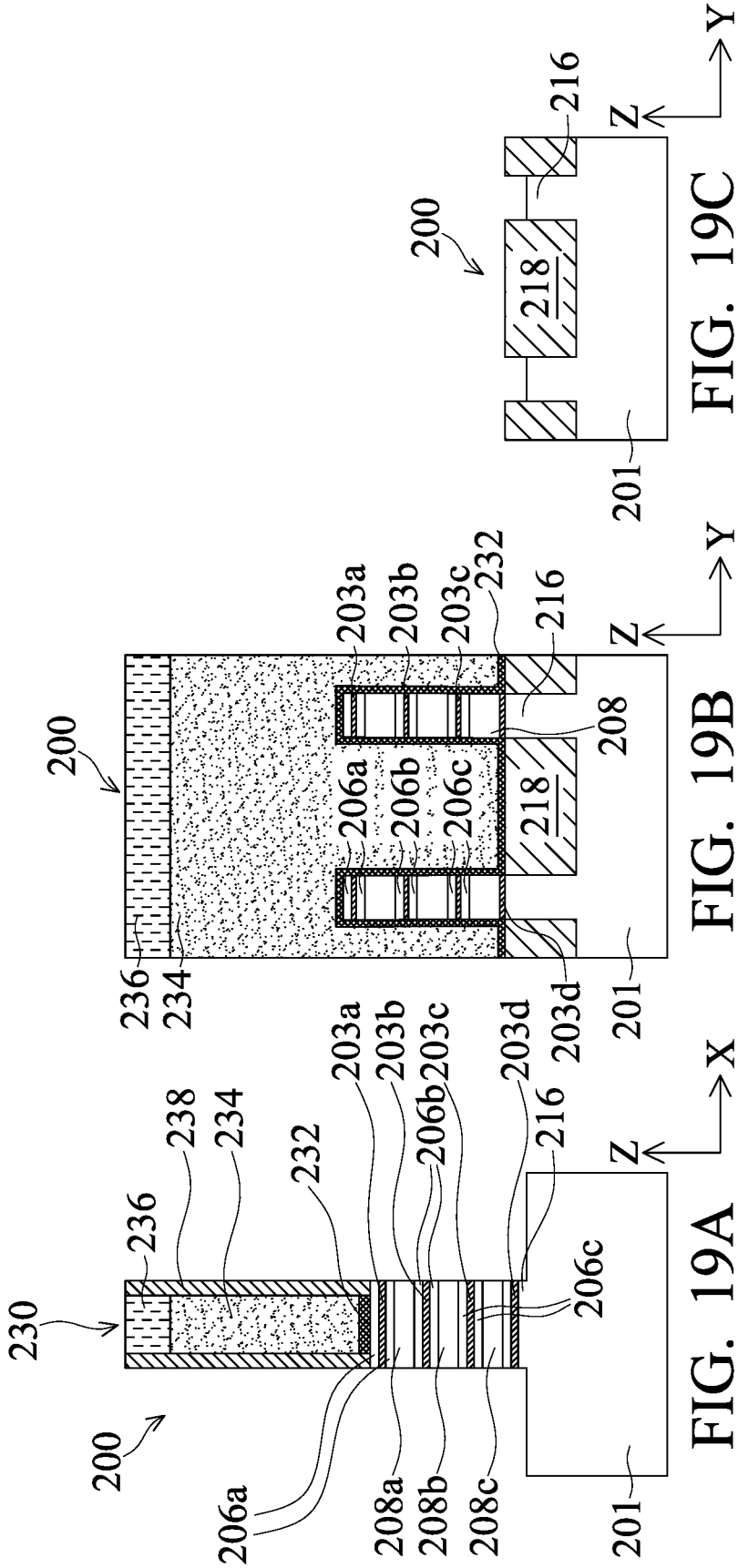

FIG. 19C

FIG. 19B

FIG. 19A

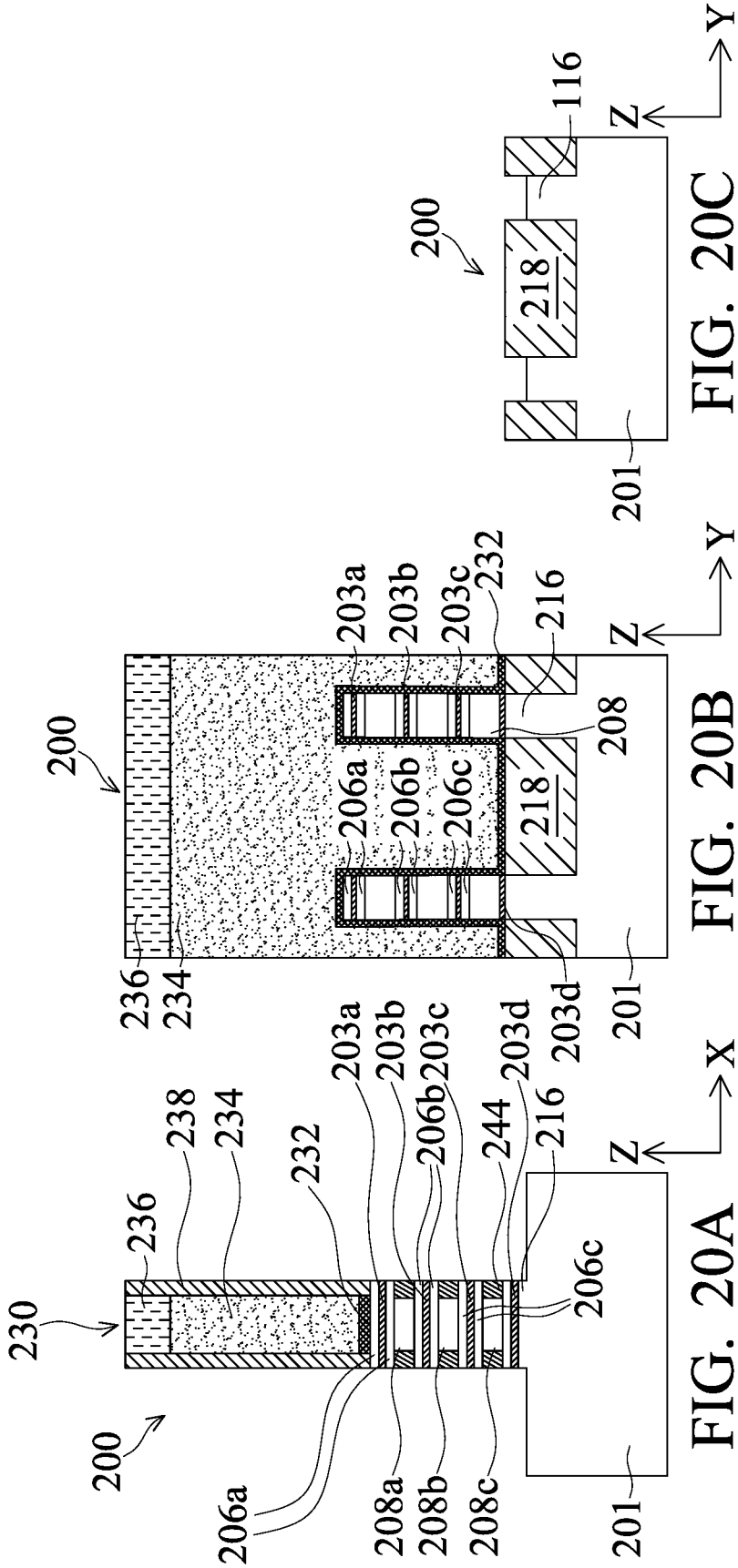

FIG. 20C

FIG. 20B

FIG. 20A

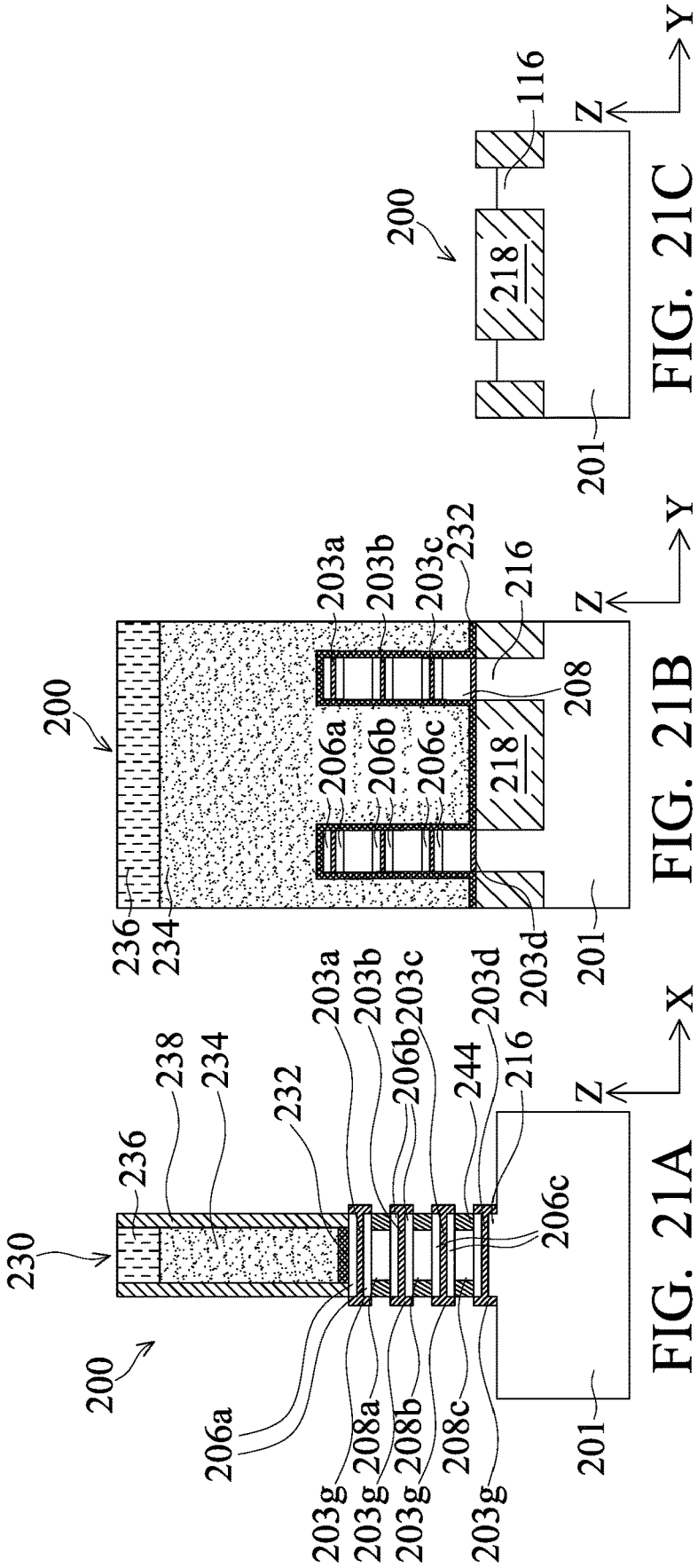

FIG. 21C

FIG. 21B

FIG. 21A

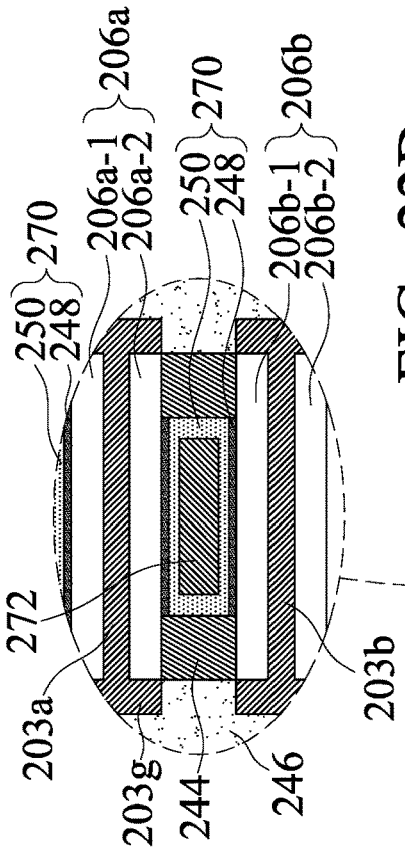

FIG. 22D

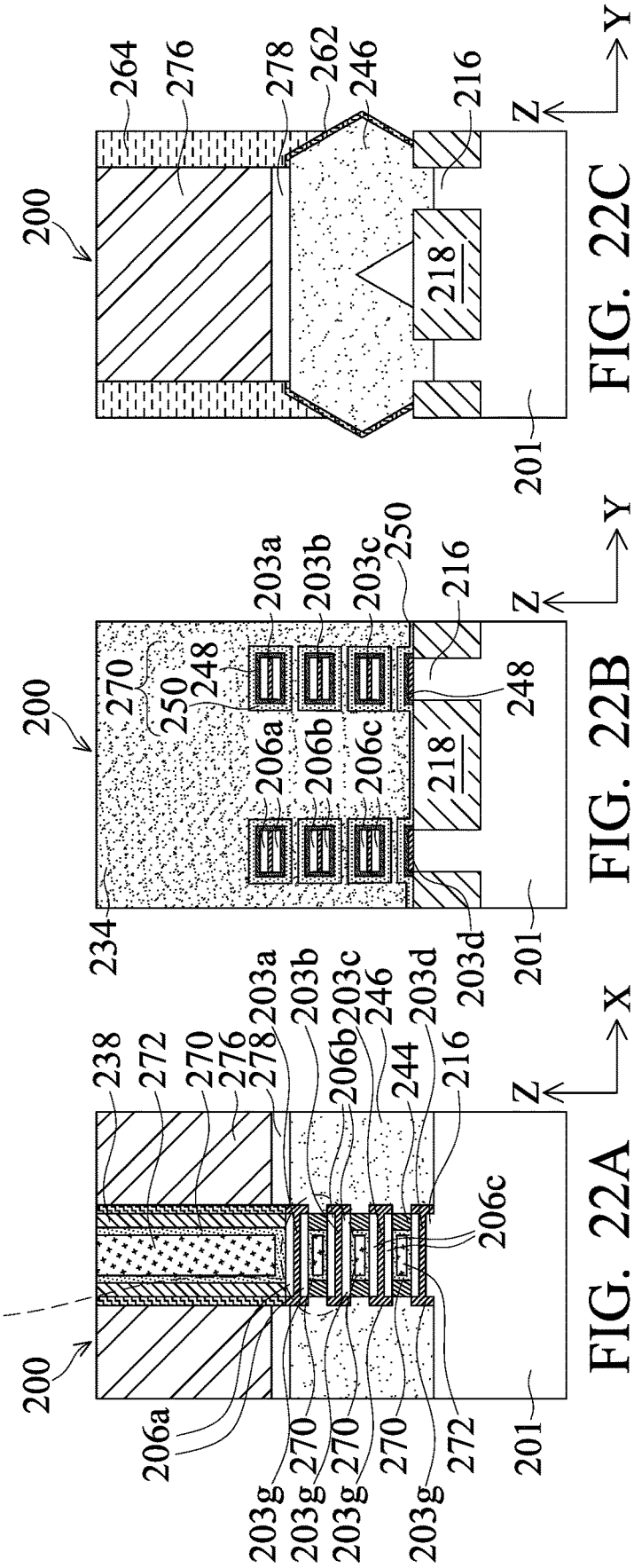

FIG. 22A

FIG. 22B

FIG. 22C

SEMICONDUCTOR DEVICE HAVING NANOSHEET TRANSISTOR AND METHODS OF FABRICATION THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional application of U.S. patent application Ser. No. 17/104,666 filed Nov. 25, 2020, which is incorporated by reference in its entirety.

BACKGROUND

[0002] The semiconductor integrated circuit (IC) industry has experienced exponential growth. Technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation. In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. This scaling down process generally provides benefits by increasing production efficiency and lowering associated costs. Such scaling down presents new challenge. For example, transistors using nanowire channels have been proposed to improve carrier mobility and drive current in a device. N-type or p-type dopants are often used in highly doped source and drain regions to help reduce parasitic resistance of the transistors. As device size reduces, such dopants may propagate and result in poor mobility due to impurity scattering.

[0003] Therefore, there is a need to improve processing and manufacturing ICs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0005] FIGS. **1**-**6** are perspective views of various stages of manufacturing a semiconductor device structure in accordance with some embodiments.

[0006] FIGS. **7**A, **7**B, **7**C to **14**A, **14**B, **14**C are cross-sectional side views of various stages of manufacturing the semiconductor device structure taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance with some embodiments.

[0007] FIG. **14**D shows an enlarged view of a portion of the semiconductor device structure shown in FIG. **14**A, in accordance with some embodiments.

[0008] FIGS. **15**A, **15**B, and **15**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance with some embodiments.

[0009] FIGS. **16**A and **16**B are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure taken along line A-A of FIG. **6** in accordance with some embodiments.

[0010] FIGS. **17**A, **17**B, **17**C are cross-sectional side views of the semiconductor device structure of FIG. **16**A after the processes discussed above with respect to **9**A-**9**C to **15**A-**15**C are performed on the semiconductor device structure; FIG. **17**D illustrates an enlarged view of a portion of the nanosheet channels according to some embodiments of the present disclosure.

[0011] FIG. **18** illustrates a perspective view of a semiconductor device structure in accordance with some alternative embodiments.

[0012] FIGS. **19**A, **19**B, **19**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure of FIG. **18** after the processes discussed above in FIGS. **2**-**6** are performed on the semiconductor device structure.

[0013] FIGS. **20**A, **20**B, and **20**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure taken along the first line (e.g., line A-A of FIG. **6**), the second line (e.g., line B-B of FIG. **6**), and the third line (e.g., line C-C of FIG. **6**), respectively, in accordance with some embodiments.

[0014] FIGS. **21**A, **21**B, and **21**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure taken along the first line (e.g., line A-A of FIG. **6**), the second line (e.g., line B-B of FIG. **6**), and the third line (e.g., line C-C of FIG. **6**), respectively, in accordance with some embodiments.

[0015] FIGS. **22**A-**22**C illustrate cross-sectional side views of the semiconductor device structure of FIG. **21**A after the processes discussed above with respect to **9**A-**9**C to **15**A-**15**C are performed on the semiconductor device structure.

[0016] FIG. **22**D is an enlarged view of a portion of the nanosheet channels of the semiconductor device structure according to some embodiments.

DETAILED DESCRIPTION

[0017] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0018] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "over," "on," "top," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated **90** degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0019] Embodiments of the present disclosure relate to gate all around (GAA) transistors, such as nanosheet FETs, which has a stack of semiconductor layers including first and second semiconductor layers alternatingly formed over a substrate. The first semiconductor layers form nanosheet channel(s) of the transistors. Portions of the second semiconductor layers are removed so that the first semiconductor layers in the nanosheet channels are wrapped around by a gate electrode for better gate control. According to embodiments of the present disclosure, exposed surfaces of the first semiconductor layers are covered by a dopant suppression layer to prevent dopant diffusion from source/drain regions into the nanosheet channels.

[0020] While the embodiments of this disclosure are discussed with respect to nanosheet channel FETs, implementations of some aspects of the present disclosure may be used in other processes and/or in other devices, such as planar FETs, Fin-FETs, Horizontal Gate All Around (HGAA) FETs, Vertical Gate All Around (VGAA) FETs, and other suitable devices. A person having ordinary skill in the art will readily understand other modifications that may be made are contemplated within the scope of this disclosure. In cases where gate all around (GAA) transistor structures are adapted, the GAA transistor structures may be patterned by any suitable method. For example, the structures may be patterned using one or more photolithography processes, including double-patterning or multi-patterning processes. Generally, double-patterning or multi-patterning processes combine photolithography and self-aligned processes, allowing patterns to be created that have, for example, pitches smaller than what is otherwise obtainable using a single, direct photolithography process. For example, in one embodiment, a sacrificial layer is formed over a substrate and patterned using a photolithography process. Spacers are formed alongside the patterned sacrificial layer using a self-aligned process. The sacrificial layer is then removed, and the remaining spacers may then be used to pattern the GAA structure.

[0021] FIGS. **1-22**D show exemplary processes for manufacturing a semiconductor device structure **100** according to embodiments of the present disclosure. It is understood that additional operations can be provided before, during, and after processes shown by FIGS. **1-22**D, and some of the operations described below can be replaced or eliminated, for additional embodiments of the method. The order of the operations/processes is not limiting and may be interchangeable.

[0022] FIGS. **1-6** are perspective views of various stages of manufacturing a semiconductor device structure **100** in accordance with some embodiments. As shown in FIG. **1**, a semiconductor device structure **100** includes a stack of layers **104** formed over a front side of a substrate **101**. The substrate **101** may be a semiconductor substrate. The substrate **101** may include a single crystalline semiconductor material such as, but not limited to silicon (Si), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), indium antimonide (InSb), gallium phosphide (GaP), gallium antimonide (GaSb), indium aluminum arsenide (InAlAs), indium gallium arsenide (InGaAs), gallium antimony phosphide (GaSbP), gallium arsenic antimonide (GaAsSb) and indium phosphide (InP). In some embodiments, the substrate **101** is a silicon-on-insulator (SOI) substrate having an insulating layer (not shown) disposed between two silicon layers for enhancement. In one aspect, the insulating layer is an oxygen-containing layer.

[0023] The substrate **101** may include various regions that have been doped with impurities (e.g., dopants having p-type or n-type conductivity). Depending on circuit design, the dopants may be, for example boron for an p-type field effect transistor (PFET) and phosphorus for a n-type field effect transistor (NFET).

[0024] The stack of layers **104** includes alternating semiconductor layers made of different materials to facilitate formation of nanosheet channels in a multi-gate device, such as nanosheet channel FETs. In some embodiments, the stack of layers **104** includes first semiconductor layers **106** (**106***a*-**106***c*) and second semiconductor layers **108** (**108***a*-**108***c*). In some embodiments, the stack of layers **104** includes alternating first and second semiconductor layers **106**, **108**. The first semiconductor layers **106** are aligned with the second semiconductor layers **108**. The first semiconductor layers **106** and the second semiconductor layers **108** are made of semiconductor materials having different etch selectivity and/or oxidation rates. For example, the first semiconductor layers **106** may be made of Si and the second semiconductor layers **108** may be made of SiGe. In some examples, the first semiconductor layers **106** may be made of SiGe and the second semiconductor layers **108** may be made of Si. In some cases, the SiGe in the first or second semiconductor layers **106**, **108** can have a germanium composition percentage between about 10% and about 50%. Alternatively, in some embodiments, either of the semiconductor layers **106**, **108** may be or include other materials such as Ge, SiC, GeAs, GaP, InP, InAs, InSb, GaAsP, AlinAs, AlGaAs, InGaAs, GaInP, GaInAsP, or any combinations thereof.

[0025] The first semiconductor layers **106** or portions thereof may form nanosheet channel(s) of the semiconductor device structure **100** in later fabrication stages. The term nanosheet is used herein to designate any material portion with nanoscale, or even microscale dimensions, and having an elongate shape, regardless of the cross-sectional shape of this portion. Thus, this term designates both circular and substantially circular cross-section elongate material portions, and beam or bar-shaped material portions including, for example, a cylindrical in shape or substantially rectangular cross-section. The nanosheet channel(s) of the semiconductor device structure **100** may be surrounded by a gate electrode. The semiconductor device structure **100** may include a nanosheet transistor. The nanosheet transistors may be referred to as nanowire transistors, gate-all-around (GAA) transistors, multi-bridge channel (MBC) transistors, or any transistors having the gate electrode surrounding the channels.

[0026] The stack of layers **104** also includes a plurality of dopant suppression layers **103** (**103***a-f*) formed over the front side of the substrate **101**. It has been observed that dopants such as phosphorus or arsenic may diffuse from subsequently formed source and drain (S/D) regions into the nanosheet channels (e.g., first semiconductor layers **106**) along the heterojunction (e.g., the interface of Si/SiGe layers). Diffusion of dopants into the nanosheet channels results in leakage current at or near the heterojunction, thereby degrading the performance of the semiconductor device structure **100**. The dopant suppression layers **103** (e.g., dopant suppression layers **103***b*, **103***c* as shown below in FIGS. **14**A, **14**B and **14**D) cover the major surfaces of the

first semiconductor layers **106** and thus block or minimize diffusion of dopants into the nanosheet channels from the (S/D) regions.

[0027] In some embodiments, one or more dopant suppression layers **103** are disposed between the first semiconductor layer **106** and the second semiconductor layer **108**. In the embodiment shown in FIG. **1**, the second semiconductor layer **108** is sandwiched between the dopant suppression layers **103**. In one exemplary aspect, for example, the dopant suppression layer **103***a* is in contact with the first semiconductor layer **106***a* and the second semiconductor layer **108***a*; the dopant suppression layer **103***b* is in contact with the second semiconductor layer **108***a* and the first semiconductor layer **106***b*; the dopant suppression layer **103***c* is in contact with the first semiconductor layer **106***b* and the second semiconductor layer **108***b*; the dopant suppression layer **103***d* is in contact with the second semiconductor layer **108***b* and the first semiconductor layer **106***c*, the dopant suppression layer **103***e* is in contact with the first semiconductor layer **106***c* and the second semiconductor layer **108***c*; and the dopant suppression layer **103***f* is in contact with the second semiconductor layer **108***c* and the substrate **101**.

[0028] In various embodiments, the dopant suppression layers **103** may be or include a silicon-containing layer or a carbon-containing layer. Exemplary materials may include, but are not limited to, silicon carbide, carbon doped silicon, silicon carbonitride (nitride-bonded silicon carbide or silicon carbide doped with nitrogen), or any suitable material that contains at least the elements silicon and carbon. Carbon doped silicon or the like is advantageous for minimizing dopant diffusion because carbon tends to trap silicon vacancies, which in turn reduces the silicon interstitial concentrations available for bonding with dopants (e.g., boron or phosphorous) in silicon-based materials. In addition, since the carbon doped silicon have greater lattice constant than that of the silicon-based first semiconductor layers **106**, the dopant suppression layers **103** can produce tensile strained nanosheet channels (e.g., n-channel FET), which in turn enhances electron mobility of the semiconductor structure device **100**.

[0029] In one embodiment, the dopant suppression layer **103** is silicon carbide. In another embodiment, the dopant suppression layer **103** is carbon doped silicon. In either case, the dopant suppression layers **103** may have a carbon atomic concentration (at. %) in a range between about 0.1 at. % and about 3 at. %. If the carbon concentration exceeds over 3 at. %, defects such as dislocations may occur at or near the interface between the dopant suppression layers **103** and the layers the dopant suppression layers **103** abutting against thereto (e.g., first and second semiconductor layers **106**, **108**) due to lattice mismatch. On the other hand, if the carbon concentration is less than 0.1 at. %, the dopant suppression layers **103** may not be sufficient to trap silicon vacancies and reduce the silicon interstitial concentrations available for bonding with dopants. As a result, the dopant suppression layers **103** may fail to block or minimize unwanted dopant diffusion coming from the source and drain regions.

[0030] In some embodiments, the dopant suppression layers **103** may be or include arsenic doped silicon carbide, arsenic doped silicon, or any suitable material containing at least the elements silicon and arsenic, which may contain one or more additional elements, such as carbon. In one embodiment, the dopant suppression layer **103** is arsenic doped silicon carbide. In another embodiment, the dopant suppression layer **103** is arsenic doped silicon. In either case, the dopant suppression layers **103** may be doped with arsenic at a level of about 1×10^{18} atoms per cubic centimeter (atoms/cm^3) or less.

[0031] In some embodiments, the dopant suppression layer **103** may be or include fluorine doped silicon. In one embodiment, the dopant suppression layer **103** is silicon fluoride or any suitable material containing at least the elements silicon and fluorine. In another embodiment, the dopant suppression layer **103** is fluorine-rich silicon. In such a case, the dopant suppression layers **103** may be doped with fluorine at a level of about $\mathbf{1x10^{18}}$ atoms per cubic centimeter (atoms/cm^3) or less.

[0032] The first and second semiconductor layers **106**, **108** are formed by any suitable deposition process, such as epitaxy. By way of example, epitaxial growth of the layers of the stack of layers **104** may be performed by a molecular beam epitaxy (MBE) process, a metalorganic chemical vapor deposition (MOCVD) process, and/or other suitable epitaxial growth processes. The dopant suppression layers **103** may be formed by chemical vapor deposition (CVD) process, physical vapor deposition (PVD), or any suitable deposition process.

[0033] Each first semiconductor layer **106** may have a thickness in a range between about 5 nm and about 30 nm. Each second semiconductor layer **108** may have a thickness that is equal, less, or greater than the thickness of the first semiconductor layer **106**. In some embodiments, each second semiconductor layer **108** has a thickness in a range between about 2 nm and about 50 nm. Each dopant suppression layer **103** may have a thickness of about 3 nm or less, for example about 0.1 nm to about 1.5 nm. While three first semiconductor layers **106** and three second semiconductor layers **108** are illustrated in FIG. **1**, any number of the first and second semiconductor layers **106**, **108** can be formed in the stack of layers **104**, and the number of layers depending on the predetermined number of channels for the semiconductor device structure **100**.

[0034] In FIG. **2**, fin structures **112** are formed from the stack of layers **104**. Each fin structure **112** has an upper portion including the semiconductor layers **106**, **108**, the dopant suppression layers **103**, and a well portion **116** formed from the substrate **101**. The fin structures **112** may be formed by patterning a hard mask layer (not shown) formed on the stack of layers **104** using multi-patterning operations including photo-lithography and etching processes. The etching process can include dry etching, wet etching, reactive ion etching (RIE), and/or other suitable processes. The photo-lithography process may include forming a photoresist layer (not shown) over the hard mask layer, exposing the photoresist layer to a pattern, performing post-exposure bake processes, and developing the photoresist layer to form a masking element including the photoresist layer. In some embodiments, patterning the photoresist layer to form the masking element may be performed using an electron beam (e-beam) lithography process. The etching process forms trenches **114** in unprotected regions through the hard mask layer, through the stack of layers **104**, and into the substrate **101**, thereby leaving the plurality of extending fin structures **112**. The trenches **114** extend along the X direction. The trenches **114** may be etched using a dry etch (e.g., RIE), a wet etch, and/or combination thereof.

[0035] In FIG. **3**, after the fin structures **112** are formed, an insulating material **118** is formed on the substrate **101**. The insulating material **118** fills the trenches **114** between neighboring fin structures **112** until the fin structures **112** are embedded in the insulating material **118**. Then, a planarization operation, such as a chemical mechanical polishing (CMP) method and/or an etch-back method, is performed such that the top of the fin structures **112** is exposed. The insulating material **118** may be made of silicon oxide, silicon nitride, silicon oxynitride (SiON), SiOCN, SiCN, fluorine-doped silicate glass (FSG), a low-K dielectric material, or any suitable dielectric material. The insulating material **118** may be formed by any suitable method, such as low-pressure chemical vapor deposition (LPCVD), plasma enhanced CVD (PECVD) or flowable CVD (FCVD).

[0036] In FIG. **4**, the insulating material **118** is recessed to form an isolation region **120**. The recess of the insulating material **118** exposes portions of the fin structures **112**, such as the stack of layers **104**. The recess of the insulating material **118** reveals the trenches **114** between the neighboring fin structures **112**. The isolation region **120** may be formed using a suitable process, such as a dry etching process, a wet etching process, or a combination thereof. A top surface of the insulating material **118** may be level with or below a surface of the dopant suppression layer **103***f* in contact with the well portion **116** formed from the substrate **101**.

[0037] In FIG. **5**, one or more sacrificial gate structures **130** (only one is shown) are formed over the semiconductor device structure **100**. The sacrificial gate structures **130** are formed over a portion of the fin structures **112**. Each sacrificial gate structure **130** may include a sacrificial gate dielectric layer **132**, a sacrificial gate electrode layer **134**, and a mask layer **136**. The sacrificial gate dielectric layer **132**, the sacrificial gate electrode layer **134**, and the mask layer **136** may be formed by sequentially depositing blanket layers of the sacrificial gate dielectric layer **132**, the sacrificial gate electrode layer **134**, and the mask layer **136**, and then patterning those layers into the sacrificial gate structures **130**. Gate spacers **138** are then formed on sidewalls of the sacrificial gate structures **130**. The gate spacers **138** may be formed by conformally depositing one or more layers for the gate spacers **138** and anisotropically etching the one or more layers, for example. While one sacrificial gate structure **130** is shown, two or more sacrificial gate structures **130** may be arranged along the X direction in some embodiments.

[0038] The sacrificial gate dielectric layer **132** may include one or more layers of dielectric material, such as a silicon oxide-based material. The sacrificial gate electrode layer **134** may include silicon such as polycrystalline silicon or amorphous silicon. The mask layer **136** may include more than one layer, such as an oxide layer and a nitride layer. The gate spacer **138** may be made of a dielectric material such as silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, SiCN, silicon oxycarbide, SiOCN, and/or combinations thereof.

[0039] The portions of the fin structures **112** that are covered by the sacrificial gate electrode layer **134** of the sacrificial gate structure **130** serve as channel regions for the semiconductor device structure **100**. The fin structures **112** that are partially exposed on opposite sides of the sacrificial gate structure **130** define source/drain (S/D) regions for the semiconductor device structure **100**. In some cases, some S/D regions may be shared between various transistors. For example, various one of the S/D regions may be connected together and implemented as multiple functional transistors. It should be understood that the source region and the drain region can be interchangeably used since the epitaxial features to be formed in these regions are substantially the same.

[0040] In FIG. **6**, the portions of the fin structures **112** in the S/D regions (e.g., regions on opposite sides of the sacrificial gate structure **130**) are recessed down below the top surface of the isolation region **120** (or the insulating material **118**), by removing portions of the fin structures **112** not covered by the sacrificial gate structure **130**. The recess of the portions of the fin structures **112** can be done by an etch process, either isotropic or anisotropic etch process, or further, may be selective with respect to one or more crystalline planes of the substrate **101**. The etch process may be a dry etch, such as a RIE, NBE, or the like, or a wet etch, such as using tetramethylammonium hydroxide (TMAH), ammonium hydroxide (NH_4OH), or any suitable etchant. Trenches **119** are formed in the S/D regions as the result of the recess of the portions of the fin structures **112**.

[0041] FIGS. **7**A, **7**B, and **7**C are cross-sectional side views of the semiconductor device structure **100** taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively.

[0042] FIGS. **8**A, **8**B, and **8**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance with some embodiments. As shown in FIG. **8**A, edge portions of each second semiconductor layer **108** of the stack of layers **104** are removed horizontally along the X direction. The removal of the edge portions of the second semiconductor layers **108** forms cavities. In some embodiments, the portions of the second semiconductor layers **108** are removed by a selective etch process. The selective etch process removes the second semiconductor layers **108** but not the mask layer **136**, the gate spacers **138**, the first semiconductor layers **106**, and the dopant suppression layers **103**. In cases where the second semiconductor layers **108** are made of SiGe and the first semiconductor layers **106** are made of silicon, the second semiconductor layer **108** can be selectively etched using a wet etchant such as, but not limited to, ammonium hydroxide (NH_4OH), tetramethylammonium hydroxide (TMAH), ethylenediamine pyrocatechol (EDP), or potassium hydroxide (KOH) solutions.

[0043] After removing edge portions of each second semiconductor layers **108**, a dielectric layer (or so-called inner spacer) is deposited in the cavities to form dielectric spacers **144**. The dielectric spacers **144** are in contact with portions of the dopant suppression layers **103**, as shown in FIG. **8**A. The dielectric spacers **144** may be made of a low-K dielectric material, such as SiON, SiCN, SiOC, SiOCN, or SiN. The dielectric spacers **144** may be formed by first forming a conformal dielectric layer using a conformal deposition process, such as ALD, followed by an anisotropic etching to remove portions of the conformal dielectric layer other than the dielectric spacers **144** formed in the cavities. The dielectric spacers **144** are protected by the first semiconductor layers **106** and the dopant suppression layers **103** during the anisotropic etching process. The remaining second semiconductor layers **108** are capped between the dielectric spacers **144** along the X direction.

[0044] FIGS. **9**A, **9**B, and **9**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance with some embodiments. As shown in FIGS. **9**A and **9**C, epitaxial S/D features **146** are formed in the source/drain (S/D) regions. The epitaxial S/D features **146** may be made of one or more layers of Si, SiP, SiC and SiCP for n-channel FETs or Si, SiGe, Ge for p-channel FETs. For p-channel FETs, p-type dopants, such as boron (B), aluminum (Al), or gallium (Ga), may also be included in the epitaxial S/D features **146**. For n-channel FETs, n-type dopants, such as phosphorus (P), arsenic (As) or antimony (Sb), may also be included in the epitaxial S/D features **146**. The epitaxial S/D features **146** may be formed by an epitaxial growth method using CVD, ALD or MBE.

[0045] In one example shown in FIG. **9**A, one of a pair of epitaxial S/D features **146** disposed on one side of the sacrificial gate structure **130** is designated as a source feature/terminal, and the other of the pair of epitaxial S/D features **146** disposed on the other side of the sacrificial gate structure **130** is designated as a drain feature/terminal. The source feature/terminal and the drain feature/terminal are connected by the channel layers (e.g., the first semiconductor layers **106**). The epitaxial S/D features **146** are in contact with the first semiconductor layer **106** and the dopant suppression layers **103** under the sacrificial gate structure **130**. In some cases, the epitaxial S/D features **146** may grow pass the topmost semiconductor channel, i.e., the first semiconductor layer **106** under the sacrificial gate structure **130**, to be in contact with the gate spacers **138**. The second semiconductor layer **108** under the sacrificial gate structure **130** are separated from the epitaxial S/D features **146** by the dielectric spacers **144**.

[0046] The epitaxial S/D features **146** may grow both vertically and horizontally to form facets, which may correspond to crystalline planes of the material used for the substrate **101**. In some cases, the epitaxial S/D features **146** of a fin structure may grow and merge with the epitaxial S/D features **146** of the neighboring fin structures, as one example shown in FIG. **9**C.

[0047] FIGS. **10**A, **10**B, and **10**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance with some embodiments. In FIGS. **10**A, **10**B, and **10**C, a contact etch stop layer (CESL) **162** is conformally formed on the exposed surfaces of the semiconductor device structure **100**. The CESL **162** covers the sidewalls of the sacrificial gate structure **130**, the insulating material **118**, the epitaxial S/D features **146**, and the exposed surface of the stack of layers **104**. The CESL **162** may include an oxygen-containing material or a nitrogen-containing material, such as silicon nitride, silicon carbon nitride, silicon oxynitride, carbon nitride, silicon oxide, silicon carbon oxide, or the like, or a combination thereof, and may be formed by CVD, PECVD, ALD, or any suitable deposition technique. Next, an interlayer dielectric (ILD) layer **164** is formed on the CESL **162** over the semiconductor device structure **100**. The materials for the ILD layer **164** may include compounds comprising Si, O, C, and/or H, such as silicon oxide, TEOS oxide, SiCOH and SiOC. Organic materials, such as polymers, may also be used for the ILD layer **164**. The ILD layer **164** may be deposited by a PECVD process or other suitable deposition technique. In some embodiments, after formation of the ILD layer **164**, the semiconductor device structure **100** may be subject to a thermal process to anneal the ILD layer **164**.

[0048] FIGS. **11**A, **11**B, and **11**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance with some embodiments. As shown in FIG. **11**A, after the ILD layer **164** is formed, a planarization operation, such as CMP, is performed on the semiconductor device structure **100** until the sacrificial gate electrode layer **134** is exposed.

[0049] FIGS. **12**A, **12**B, and **12**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance with some embodiments. As shown in FIGS. **12**A and **12**B, the sacrificial gate structure **130** is removed. The ILD layer **164** protects the epitaxial S/D features **146** during the removal of the sacrificial gate structure **130**. The sacrificial gate structure **130** can be removed using plasma dry etching and/or wet etching. For example, in cases where the sacrificial gate electrode layer **134** is polysilicon and the ILD layer **164** is silicon oxide, a wet etchant such as a tetramethylammonium hydroxide (TMAH) solution can be used to selectively remove the sacrificial gate electrode layer **134** without removing the dielectric materials of the ILD layer **164**, the CESL **162**, and the gate spacers **138**. The sacrificial gate dielectric layer **132** is thereafter removed using plasma dry etching and/or wet etching. The removal of the sacrificial gate structure **130** (i.e., the sacrificial gate electrode layer **134** and the sacrificial gate dielectric layer **132**) forms a trench **166** in the regions where the sacrificial gate electrode layer **134** and the sacrificial gate dielectric layer **132** were removed. The trench **166** exposes the top and sides of the stack of layers **104** (e.g., the first semiconductor layers **106**, the second semiconductor layers **108**, and the dopant suppression layers **103**, as shown in FIG. **12**B).

[0050] FIGS. **13**A, **13**B, and **13**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance with some embodiments. As shown in FIGS. **13**A and **13**B, the second semiconductor layers **108** (e.g., **108***a*, **108***b*, **108***c*) are removed. The removal of the second semiconductor layers **108** exposes the dielectric spacers **144**, the first semiconductor layers **106** (e.g., **106***a*, **106***b*, **106***c*), and the dopant suppression layers **103** (e.g., **103***a*-**1030**. The removal process may be any suitable etch processes, such as dry etch, wet etch, or a combination thereof. The etch process may be a selective etch process that removes the second semiconductor layers **108** but not the gate spacers **138**, the CESL **162**, the dielectric material **125**, the first semiconductor layers **106**, and the dopant suppression layers **103**. As a result, openings **151** are formed around the first semiconductor layers **106** and the dopant suppression layers **103**, as shown in FIG. **13**B. That is, portions of the first semiconductor layers **106** and the dopant suppression layers **103** not covered by the dielectric spacers **144** are exposed to the openings **151**.

[0051] FIGS. **14**A, **14**B, and **14**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance

with some embodiments. As shown in FIGS. **14**A and **14**B, a gate dielectric layer **170** is formed to surround the exposed surfaces of the first semiconductor layers **106** and the dopant suppression layers **103**. A gate electrode layer **172** is then formed on the gate dielectric layer **170**. The gate dielectric layer **170** and the gate electrode layer **172** may be collectively referred to as a gate structure.

[0052] In some embodiments, the gate dielectric layer **170** includes an interfacial layer (IL) **148** and a high-K (HK) dielectric layer **150**. FIG. **14**D illustrates an enlarged view of a portion of the nanosheet channels showing the IL **148** and the HK dielectric layer **150**. In one embodiment, the IL **148** is in contact with the exposed surfaces of the first semiconductor layers **106***a*, **106***b*, **106***c*. The IL **148** is also in contact with the dopant suppression layers **103***a*, **103***b*, **103***c*, **103***d*, **103***e*, **103***f*. In some embodiments, the IL **148** may also form on the well portion **116** of the substrate **101**. The HK dielectric layer **150** is formed to surround and in contact with the IL **148**. The IL **148** may include or be made of an oxygen-containing material or a silicon-containing material, such as silicon oxide, silicon oxynitride, oxynitride, hafnium silicate, etc. The IL **148** may be formed by CVD, ALD or any suitable conformal deposition technique. In one embodiment, the IL **148** is formed using ALD.

[0053] The HK dielectric layer **150** may include or made of one or more layers of a dielectric material, such as silicon oxide, silicon nitride, or high-K dielectric material. Examples of HK dielectric material **150** may include, but are not limited to, hafnium oxide (HfO_2), hafnium silicate (HfSiO), hafnium silicon oxynitride (HfSiON), hafnium aluminum oxide (HfAlO), hafnium lanthanum oxide (HfLaO), hafnium zirconium oxide (HfZrO), hafnium tantalum oxide (HMO), hafnium titanium oxide (HfTiO), lanthanum oxide (LaO), aluminum oxide (AlO), aluminum silicon oxide (AlSiO), zirconium oxide (ZrO), titanium oxide (TiO), tantalum oxide (Ta**2**O**5**), yttrium oxide (Y_2O_3), silicon oxynitride (SiON), hafnium dioxide-alumina (HfO_2-Al_2O_3) alloy, or other suitable high-k materials. The HK dielectric layer **150** may be a conformal layer formed by a conformal process, such as an ALD process or a CVD process.

[0054] The gate electrode layer **172** may include one or more layers of conductive material, such as polysilicon, aluminum, copper, titanium, tantalum, tungsten, cobalt, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, metal alloys, other suitable materials, and/or any combinations thereof. The gate electrode layer **172** may be formed by CVD, ALD, electro-plating, or other suitable deposition technique. The gate electrode layer **172** may be also deposited over the upper surface of the ILD layer **164**. The gate dielectric layer **170** and the gate electrode layer **172** formed over the ILD layer **164** are then removed by using, for example, CMP, until the top surface of the ILD layer **164** is exposed.

[0055] FIG. **14**D shows the longitudinal surfaces of the first semiconductor layers **106** (e.g., first semiconductor layers **106***a*, **106***b*) are covered by the dopant suppression layers **103** (e.g., **103***a*, **103***b*). The dopant suppression layers **103** prevent or at least minimize diffusion of dopants into the nanosheet channels (e.g., first semiconductor layers **106**) from the (S/D) regions through the interfaces between the nanosheet channels (e.g., first semiconductor layers **106***a*, **106***b*) and the layers abutting against the nanosheet channels.

[0056] FIGS. **15**A, **15**B, and **15**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A, line B-B, and line C-C of FIG. **6**, respectively, in accordance with some embodiments. In FIGS. **15**A and **15**C, source/drain (S/D) contacts **176** are formed in the ILD layer **164**. Prior to forming the S/D contacts **176**, contact openings are formed in the ILD layer **164** to expose the epitaxial S/D features **146**. Suitable photolithographic and etching techniques are used to form the contact openings through various layers, including the ILD layer **164** and the CESL **162** to expose the epitaxial S/D features **146**. In some embodiments, the upper portions of the epitaxial S/D features **146** are etched.

[0057] After the formation of the contact openings, a silicide layer **178** is formed on the epitaxial S/D features **146**. The silicide layer **178** conductively couples the epitaxial S/D features **146** to the subsequently formed S/D contacts **176**. The silicide layer **178** may be formed by depositing a metal source layer over the epitaxial S/D features **146** and performing a rapid thermal annealing process. During the rapid anneal process, the portion of the metal source layer over the epitaxial S/D features **146** reacts with silicon in the epitaxial S/D features **146** to form the silicide layer **178**. Unreacted portion of the metal source layer is then removed. For n-channel FETs, the silicide layer **178** may be made of a material including one or more of TiSi , CrSi, TaSi, MoSi, ZrSi, HfSi , ScSi, Ysi, HoSi, TbSI, GdSi, LuSi, DySi, ErSi, YbSi, or combinations thereof. For p-channel FETs, the silicide layer **178** may be made of a material including one or more of NiSi, CoSi, MnSi, Wsi, FeSi, RhSi, PdSi, RuSi, PtSi, IrSi, OsSi, or combinations thereof. In some embodiments, the silicide layer **178** is made of a metal or metal alloy silicide, and the metal includes a noble metal, a refractory metal, a rare earth metal, alloys thereof, or combinations thereof. Next, a conductive material is formed in the contact openings and form the S/D contacts **176**. The conductive material may be made of a material including one or more of Ru, Mo, Co, Ni. W, Ti, Ta, Cu, Al, TiN and TaN. While not shown, a barrier layer (e.g., TiN, TaN, or the like) may be formed on sidewalls of the contact openings prior to forming the S/D contacts **176**. Then, a planarization process, such as CMP, is performed to remove excess deposition of the contact material and expose the top surface of the gate electrode layer **172**.

[0058] It is understood that the semiconductor device structure **100** may undergo further complementary metal oxide semiconductor (CMOS) and/or back-end-of-line (BEOL) processes to form various features such as transistors, contacts/vias, interconnect metal layers, dielectric layers, passivation layers, etc. The semiconductor device structure **100** may also include backside contacts (not shown) on the backside of the substrate **101** so that either source or drain of the epitaxial S/D features **146** is connected to a backside power rail (e.g., positive voltage VDD or negative voltage VSS) through the backside contacts.

[0059] FIG. **16**A illustrates a cross-sectional side view of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A of FIG. **6** in accordance with some embodiments. The embodiment shown in FIG. **16**A is substantially identical to the embodi-

ment shown in FIG. **15**A except that the dopant suppression layer **103** is further extended to cover the entire exposed surfaces of the first semiconductor layers **106**. In this embodiment, after the dielectric spacers **144** are formed in the cavities (formed as the result of removal of the edge portions of the second semiconductor layers **108**, e.g., FIG. **8**A), an extended dopant suppression layer **103***g*, such as the dopant suppression layer **103**, is formed on the exposed surfaces of the first semiconductor layers **106***a*, **106***b*, **106***c*. The extended dopant suppression layer **103***g* may use the same material as the dopant suppression layer **103**. In the embodiment shown in FIG. **16**A, the extended dopant suppression layer **103***g* and the dopant suppression layer **103***a* together cover and in contact with the exposed surfaces of the first semiconductor layer **106***a*, the extended dopant suppression layer **103***g* and the dopant suppression layers **103***b* and **103***c* together cover and in contact with the exposed surfaces of the first semiconductor layer **106***b*, the extended dopant suppression layer **103***g* and the dopant suppression layers **103***d* and **103***e* together cover and in contact with the exposed surfaces of the first semiconductor layer **106***c*, and the extended dopant suppression layer **103***g* and the dopant suppression layer **103***f* together cover and in contact with the exposed surfaces of the well portion **116** of the substrate **101** and the second semiconductor layer **108***c*.

[0060] The extended dopant suppression layer **103***g* may be formed on the first semiconductor layers **106** by a selective deposition process, such as selective ALD process. The selective ALD process allows the extended dopant suppression layer **103***g* to be selectively deposited on the exposed surfaces of the first semiconductor layers **106** relative to the sidewall of the gate spacers **138** and the dielectric spacers **144**. The extended dopant suppression layer **103***g* may also form on the dopant suppression layers **103***a*-**103***f*. The extended dopant suppression layer **103***g* may have the same thickness as the dopant suppression layer **103**.

[0061] FIG. **16**B illustrates a cross-sectional side view of one of various stages of manufacturing the semiconductor device structure **100** taken along line A-A of FIG. **6** in accordance with an alternative embodiment. The embodiment shown in FIG. **16**B is substantially identical to the embodiment shown in FIG. **16**A except that the extended dopant suppression layer **103***g* is formed from a material different than that of the dopant suppression layer **103**. In this embodiment, an extended dopant suppression layer **103***h* is formed to cover the entire exposed surfaces of the first semiconductor layers **106**. Particularly, the extended dopant suppression layer **103***h* and the dopant suppression layer **103***a* cover and in contact with the exposed surfaces of the first semiconductor layer **106***a*, the extended dopant suppression layer **103***h* and the dopant suppression layers **103***b* and **103***c* cover and in contact with the exposed surfaces of the first semiconductor layer **106***b*, the extended dopant suppression layer **103***h* and the dopant suppression layers **103***d* and **103***e* cover and in contact with at the exposed surfaces of the first semiconductor layer **106***c*, and the extended dopant suppression layer **103***h* and the dopant suppression layer **103***f* cover and in contact with the exposed surfaces of the well portion **116** of the substrate **101**.

[0062] Suitable materials for the extended dopant suppression layer **103***h* may include, but are not limited to, a silicon-containing layer or a carbon-containing layer, such as silicon carbide, carbon doped silicon, silicon carbonitride (nitride-bonded silicon carbide or silicon carbide doped with nitrogen), or any suitable material that contains at least the elements silicon and carbon; arsenic doped silicon carbide, arsenic doped silicon, or any suitable material containing at least the elements silicon and arsenic, which may contain one or more additional elements, such as carbon; and fluorine-rich silicon, such as silicon fluoride or any suitable material containing at least the elements silicon and fluorine.

[0063] After the formation of the extended dopant suppression layers **103***g* (FIG. **16**A) or **103***h* (FIG. **16**B), the semiconductor device structure **100** is subjected to various processes as discussed above with respect to FIGS. **9**A-**9**C to **15**A-**15**C. FIGS. **17**A-**17**C illustrate cross-sectional side views of the semiconductor device structure **100** of FIG. **16**A after the processes discussed above with respect to **9**A-**9**C to **15**A-**15**C are performed on the semiconductor device structure **100**. FIG. **17**D illustrates an enlarged view of a portion of the nanosheet channels according to some embodiments of the present disclosure. As can be seen in FIG. **17**D, the exposed surfaces of the first semiconductor layers **106** (e.g., first semiconductor layers **106***a*, **106***b*) are entirely covered by the dopant suppression layers **103** (e.g., **103***a*, **103***b*) and the extended dopant suppression layer **103***g*. The dopant suppression layers **103** prevent or at least minimize diffusion of dopants from the epitaxial S/D features **146** into the nanosheet channels (e.g., first semiconductor layers **106**) through the interfaces between the nanosheet channels and the layers abutting against the nanosheet channels. The dopant suppression layers **103** (e.g., **103***a*, **103***b*) and the extended dopant suppression layer **103***g* also help confine the dopants at the edge of the epitaxial S/D features **146** near the nanosheet channels (e.g., regions near and along the extended dopant suppression layer **103***g* and the dielectric spacers **144**), thereby forming lightly doped source and drain region. The lightly doped source and drain region minimizes hot electron injection into the gate and improves the speed and reliability of the semiconductor device structure **100**.

[0064] FIG. **17**D further illustrates a gate dielectric layer (e.g., the gate dielectric layer **170**) is formed to surround the first semiconductor layers **106** and the dopant suppression layers **103**. The gate dielectric layer may include an interfacial layer (IL) (e.g., IL **148**) and a high-K (HK) dielectric layer (e.g., HK dielectric layer **150**). A gate electrode layer (e.g., the gate electrode layer **172**) is formed on the gate dielectric layer **170**. Contact openings are formed through the ILD layer **164** and the CESL **162** to expose the epitaxial S/D features **146**. A silicide layer, such as the silicide layer **178**, is formed on the epitaxial S/D features **146**. The silicide layer **178** conductively couples the epitaxial S/D features **146** to the subsequently formed S/D contacts (e.g., S/D contacts **176**), as discussed above with respect to FIGS. **15**A-**15**C. Then, a planarization process, such as CMP, is performed to remove excess deposition of the contact material and expose the top surface of the gate electrode layer **172**.

[0065] FIG. **18** illustrates a perspective view of a semiconductor device structure **200** in accordance with some alternative embodiments. The embodiment shown in FIG. **18** is similar to the embodiment of FIG. **1** except that dopant suppression layers are formed in the first semiconductor layers. As can be seen in FIG. **18**, the semiconductor device structure **200** includes a stack of layers **204** formed over a front side of a substrate **201**. The substrate **201** can be

formed from the same material as the substrate **101** discussed above, and the substrate **201** may include various regions that have been doped with p-type or n-type impurities. Similar to the stack of layers **104**, the stack of layers **204** includes alternating first semiconductor layers **206** (**206***a*-**206***c*) and second semiconductor layers **208** (**208***a*-**208***c*). For example, the second semiconductor layer **208***a* is disposed between the first semiconductor layer **206***a* and the first semiconductor layer **206***b*, the second semiconductor layer **208***b* is disposed between the first semiconductor layer **206***b* and the first semiconductor layer **206***c*, and the second semiconductor layer **208***c* is disposed between the first semiconductor layer **206***c* and the substrate **201**. The first and second semiconductor layers **206**, **208** can be formed from the same material as that of the first and second semiconductor layers **106**, **108**. In one embodiment, the first semiconductor layers **206** may be made of Si and the second semiconductor layers **208** may be made of SiGe. The first and second semiconductor layers **206**, **208** may have the same thickness as that of the first and second semiconductor layers **106**, **108**.

[0066] While three first semiconductor layers **206** and three second semiconductor layers **208** are illustrated in FIG. **18**, any number of the first and second semiconductor layers **206**, **208** can be formed in the stack of layers **204**, and the number of layers depending on the predetermined number of channels for the semiconductor device structure **200**.

[0067] The stack of layers **204** also includes a plurality of dopant suppression layers **203** (**203***a*-d) formed over the front side of the substrate **101**. The dopant suppression layers **203** can be formed from the same material as the dopant suppression layers **103**, such as silicon carbide, carbon doped silicon, arsenic doped silicon carbide, or fluorine-rich silicon, etc., as discussed in various embodiments above. In some embodiments, one or more dopant suppression layers **203** are formed in the first semiconductor layer **206**. Stated differently, each first semiconductor layer **206***a*, **206***b*, **206***c* has an upper portion and a lower portion, and the dopant suppression layer **203***a*, **203***b*, **203***c* is sandwiched between the upper portion and the lower portion of each of the first semiconductor layers **206***a*, **206***b*, **206***c*, respectively. In the embodiment shown in FIG. **18**, for example, the dopant suppression layer **203***a* is disposed in the first semiconductor layer **206***a* and has its top and bottom surfaces in contact with the first semiconductor layer **206***a*, the dopant suppression layer **203***b* is disposed in the first semiconductor layer **206***b* and has its top and bottom surfaces in contact with the first semiconductor layer **206***b*, the dopant suppression layer **203***c* is disposed in the first semiconductor layer **206***c* and has its top and bottom surfaces in contact with the first semiconductor layer **206***c*, and the dopant suppression layer **203***d* is disposed between and in contact with the substrate **101** and the second semiconductor layer **208***c*. Likewise, each of the dopant suppression layers **203** may have the same thickness as that of the dopant suppression layers **103**.

[0068] FIGS. **19**A, **19**B, **19**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **200** after the processes discussed above in FIGS. **2**-**6** are performed on the semiconductor device structure **200**. A sacrificial gate structure **230**, such as the sacrificial gate structure **130**, is formed on the semiconductor device structure **200**. The sacrificial gate structure **230** includes a sacrificial gate dielectric layer **232** (e.g., sacrificial gate dielectric layer **132**), a sacrificial gate electrode layer **234** (e.g., sacrificial gate electrode layer **134**), and a mask layer **236** (e.g., mask layer **136**). Gate spacers **238** (e.g., gate spacers **138**) are then formed on sidewalls of the sacrificial gate structures **230**. FIGS. **19**A, **19**B, and **19**C show cross-sectional side views of the semiconductor device structure **200** taken along a first line parallel to an extension direction along the fin structures (e.g., line A-A of FIG. **6**), a second line parallel to an extension direction perpendicular to the first line and along the gate structure (e.g., line B-B of FIG. **6**), and a third line parallel to an extension direction perpendicular to the first line and along the source or drain regions (e.g., line C-C of FIG. **6**), respectively. The fin structures in the S/D regions (e.g., regions on opposite sides of the sacrificial gate structure **130**) are recessed down below the top surface of an insulating material **218** (e.g., insulating material **118**).

[0069] FIGS. **20**A, **20**B, and **20**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **200** taken along the first line (e.g., line A-A of FIG. **6**), the second line (e.g., line B-B of FIG. **6**), and the third line (e.g., line C-C of FIG. **6**), respectively, in accordance with some embodiments. Like the processes shown in FIG. **8**A, edge portions of each second semiconductor layer **208** are removed horizontally along the X direction. A dielectric spacer **244** (e.g., dielectric spacers **144**) is then formed in the cavities formed as the result of removal of the edge portions of the second semiconductor layers **208**, as shown in FIG. **20**A. The dielectric spacers **244** may be formed of the same material as the dielectric spacers **144**.

[0070] FIGS. **21**A, **21**B, and **21**C are cross-sectional side views of one of various stages of manufacturing the semiconductor device structure **200** taken along the first line (e.g., line A-A of FIG. **6**), the second line (e.g., line B-B of FIG. **6**), and the third line (e.g., line C-C of FIG. **6**), respectively, in accordance with some embodiments. Like the processes shown in FIG. **16**A, after the formation of the dielectric spacers **244**, an extended dopant suppression layer **203***g*, such as the dopant suppression layer **103***g*, is formed on the exposed surfaces of the first semiconductor layers **206***a*, **206***b*, **206***c*. The extended dopant suppression layer **203***g* may use the same material as the dopant suppression layer **103**. In the embodiment shown in FIG. **21**A, the extended dopant suppression layer **203***g* and the dopant suppression layer **203***a* together form the shape of a capital "H" (with respect to the cross-sectional view of the semiconductor device structure) and are in contact with the first semiconductor layer **206***a*, the extended dopant suppression layer **203***g* and the dopant suppression layers **203***b* together form the shape of a capital "H" (with respect to the cross-sectional view of the semiconductor device structure) and are in contact with the first semiconductor layer **206***b*, the extended dopant suppression layer **203***g* and the dopant suppression layers **203***c* together form the shape of a capital "H" (with respect to the cross-sectional view of the semiconductor device structure) and are in contact with the first semiconductor layer **206***c*, and the extended dopant suppression layer **203***g* and the dopant suppression layer **203***d* are in contact with the exposed surfaces of the well portion **116** of the substrate **101** and the second semiconductor layer **208***c*.

[0071] In some embodiments, the extended dopant suppression layer **203***g* is formed from a material different than that of the dopant suppression layer **203** (e.g., **203***a*-**203***d*),

such as the material used for the extended dopant suppression layer **103***h* discussed above in FIG. **16**B.

[0072] Likewise, the extended dopant suppression layer **203***g* may be formed on the first semiconductor layers **206** by a selective deposition process, such as selective ALD process used for forming the extended dopant suppression layer **103***g*. The extended dopant suppression layer **203***g* may also form on the dopant suppression layers **203***a*-**203***d*. The extended dopant suppression layer **203***g* may have the same thickness as the dopant suppression layer **103***g*.

[0073] After the formation of the extended dopant suppression layers **203***g*, the semiconductor device structure **200** is subjected to various processes, as discussed above with respect to FIGS. **9**A-**9**C to **15**A-**15**C. FIGS. **22**A-**22**C illustrate cross-sectional side views of the semiconductor device structure **200** of FIG. **21**A after the processes discussed above with respect to **9**A-**9**C to **15**A-**15**C are performed on the semiconductor device structure **200**. FIG. **22**D is an enlarged view of a portion of the nanosheet channels of the semiconductor device structure **200** according to some embodiments of the present disclosure.

[0074] In FIG. **22**A, a gate electrode layer **272** (e.g., gate electrode layer **172**) is formed on the gate dielectric layer **270**. Contact openings are formed through an ILD layer **264** (e.g., ILD layer **164**) and a CESL **262** (e.g., CESL **162**) to expose epitaxial S/D features **246** (e.g., epitaxial S/D features **146**). A silicide layer **278**, such as the silicide layer **178**, is formed on the epitaxial S/D features **246**. The silicide layer **178** conductively couples the epitaxial S/D features **246** to the subsequently formed S/D contacts **276** (e.g., S/D contacts **176**), as discussed above with respect to FIGS. **15**A-**15**C. Then, a planarization process, such as CMP, is performed to remove excess deposition of the contact material and expose the top surface of the gate electrode layer **272**.

[0075] As can be seen in FIG. **22**D, a gate dielectric layer **270** (e.g., gate dielectric layer **170**) is formed to surround the first semiconductor layers **206** (e.g., first semiconductor layers **206***a*, **206***b*). The gate dielectric layer **270** may include an IL **248** (e.g., IL **148**) and a HK dielectric layer **250** (e.g., HK dielectric layer **150**). The dopant suppression layer **203***a* extends through the first semiconductor layer **206***a* to join the extended dopant suppression layers **203***g* that covers and in contact with the exposed surfaces of the first semiconductor layers **206** (e.g., first semiconductor layers **206***a*). Stated differently, the first semiconductor layer **206***a* has an upper portion **206***a*-**1** and a lower portion **206***a*-**2**, and the dopant suppression layer **203***a* is sandwiched between the upper portion **206***a*-**1** and the lower portion **206***a*-**2** of the first semiconductor layer **206***a*. Likewise, the dopant suppression layer **203***b* extends through the first semiconductor layer **206***b* to join the extended dopant suppression layers **203***g* that covers and in contact with the exposed surfaces of the first semiconductor layers **206** (e.g., first semiconductor layers **206***b*). Stated differently, the first semiconductor layer **206***b* has an upper portion **206***b*-**1** and a lower portion **206***b*-**2**, and the dopant suppression layer **203***b* is sandwiched between the upper portion **206***b*-**1** and the lower portion **206***b*-**2** of the first semiconductor layer **206***b*.

[0076] The extended dopant suppression layers **203***g* prevent or at least minimize diffusion of dopants from the epitaxial S/D features **246** into the nanosheet channels (e.g., first semiconductor layers **206***a*, **206***b*). The extended dopant suppression layers **203***g* also help confine the dopants at the edge of the epitaxial S/D features **246** near the nanosheet channels (e.g., regions near and along the extended dopant suppression layer **203***g* and the dielectric spacers **244**), thereby forming lightly doped source and drain region. The lightly doped source and drain region minimizes hot electron injection into the gate and improves the speed and reliability of the semiconductor device structure **200**.

[0077] Embodiments of the present disclosure provide a semiconductor device structure having exposed surfaces of nanosheet channels covered by a dopant suppression layer to prevent dopant diffusion from source/drain (S/D) features into the nanosheet channels, which in turn mitigates electron mobility degradation. The dopant suppression layer also confines the dopants at the interface between the S/D features and the nanosheet channels, which improves S/D junction abruptness and reduces contact resistance at or near the nanosheet channels. Reduction of dopants in the nanosheet channels allows for fuller depletion in the nanosheet channels and results in less short-channel effects due to steeper sub-threshold current swing (SS) and smaller drain induced barrier lowering (DIBL). In addition, dopant suppression layers using carbon doped silicon also produce tensile strained nanosheet channels, which in turn enhances electron mobility of the semiconductor structure device.

[0078] An embodiment is a semiconductor device structure. The structure includes a first channel layer having a first surface and a second surface opposing the first surface, a second channel layer having a first surface and a second surface opposing the first surface of the second channel layer, and the first and second channel layers are formed of a first material. The structure also includes a first dopant suppression layer in contact with the second surface of the first channel layer, and a second dopant suppression layer parallel to the first dopant suppression layer. The second dopant suppression layer is in contact with the first surface of the second channel layer, and the first and second dopant suppression layers each comprises carbon or fluorine. The structure further includes a gate dielectric layer in contact with the first and second dopant suppression layers and the first surface of the first channel layer, and a gate electrode layer disposed on the gate dielectric layer.

[0079] Another embodiment is a semiconductor device structure. The structure includes a first channel layer formed of a first material, the first channel layer includes a first portion and a second portion, wherein the first portion has a first surface, a second surface opposing the first surface, a third surface, and a fourth surface opposing the third surface. The first surface connects the third surface to the fourth surface, and the second surface connects the third surface to the fourth surface. The second portion has a first surface, a second surface opposing the first surface of the second portion, a third surface, and a fourth surface opposing the third surface of the second portion. The surface of the second portion connects the third surface to the fourth surface of the second portion, and the second surface of the second portion connects the third surface to the fourth surface of the second portion. The structure also includes a dopant suppression layer. The dopant suppression layer includes a first part in contact with the second surface of the first portion and the first surface of the second portion, a second part connecting to the first part and in contact with the third surface of the first portion and the third surface of the second portion, and a third part connecting to the first part and in contact with the

fourth surface of the first portion and the fourth surface of the second portion. The first part, the second part, and the third part form a shape of a capital "H" with respect to a cross-sectional view of the semiconductor device structure. The structure further includes a gate dielectric layer in contact with the first surface of the first portion and the second surface of the second portion, and a gate electrode layer disposed on the gate dielectric layer.

[0080] A further embodiment is a semiconductor device structure. The structure includes a first channel layer formed of a first semiconductor material, a second channel layer disposed adjacent and in parallel to the first channel layer, the second channel layer being formed of the first semiconductor material, a first dopant suppression layer in contact with sidewalls and a bottom surface of the first channel layer, a second dopant suppression layer in contact with sidewalls and top and bottom surfaces of the second channel layer, wherein the first and second dopant suppression layers each comprises carbon or fluorine, a gate dielectric layer in contact with the first and second dopant suppression layers, and a gate electrode layer disposed on the gate dielectric layer to surround portions of the first and second channel layers.

[0081] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

1. A semiconductor device structure, comprising:

a first channel layer having a first surface and a second surface opposing the first surface, the first channel layer being formed of a first material;

a second channel layer having a first surface and a second surface opposing the first surface of the second channel layer, the second channel layer being formed of the first material;

a first dopant suppression layer in contact with the second surface of the first channel layer;

a second dopant suppression layer parallel to the first dopant suppression layer, the second dopant suppression layer being in contact with the first surface of the second channel layer, wherein the first and second dopant suppression layers each comprises carbon or fluorine;

a gate dielectric layer in contact with the first dopant suppression layer, the second dopant suppression layer, and the first surface of the first channel layer; and

a gate electrode layer disposed on the gate dielectric layer.

2. The semiconductor device structure of claim **1**, wherein each of the first dopant suppression layer and the second dopant suppression layer further comprises silicon, arsenic, or a combination thereof.

3. The semiconductor device structure of claim **2**, wherein the first dopant suppression layer and the second dopant suppression layer are silicon carbide, carbon doped silicon, or arsenic doped silicon carbide.

4. The semiconductor device structure of claim **1**, further comprising:

a first source/drain feature in contact with the first dopant suppression layer and the second dopant suppression layer; and

a second source/drain feature in contact with the first dopant suppression layer and the second dopant suppression layer.

5. The semiconductor device structure of claim **1**, further comprising:

a third dopant suppression layer in contact with a third surface of the first channel layer, the third surface connecting the first surface to the second surface of the first channel layer; and

a fourth dopant suppression layer in contact with a fourth surface of the first channel, the fourth surface opposing the third surface, and the fourth surface connecting the first surface to the second surface of the first channel layer.

6. The semiconductor device structure of claim **5**, wherein the third and fourth dopant suppression layers are formed of the same material as the first dopant suppression layer.

7. The semiconductor device structure of claim **5**, wherein the third and fourth dopant suppression layers are in contact with the first dopant suppression layer.

8. The semiconductor device structure of claim **5**, further comprising:

a first source/drain feature in contact with the third dopant suppression layer; and

a second source/drain feature in contact with the fourth dopant suppression layer.

9. The semiconductor device structure of claim **8**, further comprising:

a fifth dopant suppression layer in contact with the second surface of the second channel layer.

10. The semiconductor device structure of claim **9**, further comprising:

a sixth dopant suppression layer disposed between and in contact with the second channel layer and the first source/drain feature; and

a seventh dopant suppression layer disposed between and in contact with the second channel layer and the second source/drain feature,

wherein the sixth and seventh dopant suppression layers are formed of the same material as the third and fourth dopant suppression layers.

11. The semiconductor device structure of claim **10**, wherein the second dopant suppression layer, the fifth dopant suppression layer, the sixth dopant suppression layer, and the seventh dopant suppression layer surround and in contact with the second channel layer.

12. A semiconductor device structure, comprising:

a first channel layer formed of a first material, the first channel layer comprising a first portion and a second portion, wherein the first portion has a first surface, a second surface opposing the first surface, a third surface, and a fourth surface opposing the third surface, the first surface connecting the third surface to the fourth surface, and the second surface connecting the third surface to the fourth surface, and wherein the second portion has a first surface, a second surface opposing the first surface of the second portion, a third surface, and a fourth surface opposing the third surface of the second portion, wherein the first surface of the

second portion connecting the third surface to the fourth surface of the second portion, and the second surface of the second portion connecting the third surface to the fourth surface of the second portion;

a dopant suppression layer, comprising:

a first part in contact with the second surface of the first portion and the first surface of the second portion;

a second part connecting to the first part and in contact with the third surface of the first portion and the third surface of the second portion; and

a third part connecting to the first part and in contact with the fourth surface of the first portion and the fourth surface of the second portion, wherein the first part, the second part, and the third part form a shape of a capital "H" with respect to a cross-sectional view of the semiconductor device structure;

a gate dielectric layer in contact with the first surface of the first portion and the second surface of the second portion; and

a gate electrode layer disposed on the gate dielectric layer.

13. The semiconductor device structure of claim **12**, wherein the dopant suppression layer comprises carbon or fluorine.

14. The semiconductor device structure of claim **13**, wherein the dopant suppression layer further comprises silicon, arsenic, or a combination thereof.

15. The semiconductor device structure of claim **14**, wherein the dopant suppression layer is silicon carbide, carbon doped silicon, or arsenic doped silicon carbide.

16. The semiconductor device structure of claim **13**, further comprising:

a first source/drain feature in contact with the second part of the dopant suppression layer; and

a second source/drain feature in contact with the third part of the dopant suppression layer.

17. The semiconductor device structure of claim **13**, further comprising:

a second channel layer formed of the first material, wherein the second channel layer is aligned with the first channel layer and in contact with the gate dielectric layer.

18. A semiconductor device structure, comprising:

a first channel layer formed of a first semiconductor material;

a second channel layer disposed adjacent and in parallel to the first channel layer, the second channel layer being formed of the first semiconductor material;

a first dopant suppression layer in contact with sidewalls and a bottom surface of the first channel layer;

a second dopant suppression layer in contact with sidewalls and top and bottom surfaces of the second channel layer, wherein the first and second dopant suppression layers each comprises carbon or fluorine;

a gate dielectric layer in contact with the first and second dopant suppression layers; and

a gate electrode layer disposed on the gate dielectric layer to surround portions of the first and second channel layers.

19. The semiconductor device structure of claim **18**, wherein each of the first dopant suppression layer and the second dopant suppression layer further comprises silicon, arsenic, or a combination thereof.

20. The semiconductor device structure of claim **18**, wherein the second dopant suppression layer contacting the sidewalls of the first channel comprises a first material, and the first dopant suppression layer contacting the top and bottom surfaces comprises a second material that is chemically different from the first material.

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