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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors: **KARPOV, Elijah V.**; 3964 NW Brookview Way, Portland, Oregon 97229 (US). **KALAVADE, Pranav**; 6385 Slida Drive, San Jose, California 95129 (US). **MAJHI, Prashant**; 1754 Indigo Oak Lane, San Jose, California 95121 (US). **DOYLE, Brian S.**; 11156 NW Montreux Lane, Portland, Oregon 97229 (US).

(74) Agent: **BRASK, Justin, K.** et al.; Schwabe, Williamson & Wyatt, 1211 SW 5th Ave., Suite 1900, Portland, OR 97204 (US).

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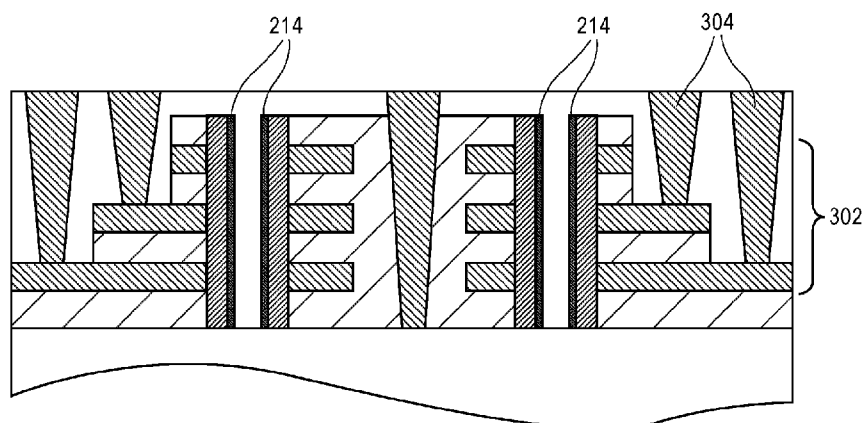


FIG. 3

(57) Abstract: Embedded non-volatile memory structures based on ferroelectric field effect transistors (FeFETs) are described. In an example, an integrated circuit structure includes a vertical arrangement of a plurality of gate electrodes in an inter-layer dielectric (ILD) layer above a substrate. A trench is through the vertical arrangement of a plurality of gate electrodes in the ILD layer, the trench having sidewalls. A ferroelectric oxide material is continuous along the sidewalls of the trench. The ferroelectric oxide material is in contact with the vertical arrangement of the plurality of gate electrodes. A semiconductor channel material is adjacent to the ferroelectric oxide material along the sidewalls of the trench.



EMBEDDED NON-VOLATILE MEMORY BASED ON FERROELECTRIC FIELD EFFECT TRANSISTORS

TECHNICAL FIELD

5 Embodiments of the disclosure are in the field of integrated circuit structures and, in particular, embedded non-volatile memory structures based on ferroelectric field effect transistors (FeFETs).

BACKGROUND

10 For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips.

 For example, shrinking transistor size allows for the incorporation of an increased
15 number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant. In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes,
20 tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and compatibility with the existing high-yielding bulk silicon substrate infrastructure. Scaling multi-gate transistors has not been without consequence, however. As the dimensions of these
fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of
25 fundamental building blocks fabricated in a given region is increased, the constraints on the semiconductor processes used to fabricate these building blocks have become overwhelming.

 The performance of a thin-film transistor (TFT) may depend on a number of factors. For example, the efficiency at which a TFT is able to operate may depend on the sub threshold swing of the TFT, characterizing the amount of change in the gate-source voltage needed to achieve a
30 given change in the drain current. A smaller sub threshold swing enables the TFT to turn off to a lower leakage value when the gate-source voltage drops below the threshold voltage of the TFT.

 Variability in conventional and state-of-the-art fabrication processes may limit the possibility to further extend them into the, e.g. 10 nm or sub-10 nm range. Consequently, fabrication of the functional components needed for future technology nodes may require the
35 introduction of new methodologies or the integration of new technologies in current fabrication

processes or in place of current fabrication processes.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B illustrate cross-sectional views of two different states of a ferroelectric field effect transistor (FeFET), in accordance with an embodiment of the present disclosure.

Figures 2A-2F illustrate cross-sectional views of various stages in a method of fabricating an embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs), in accordance with an embodiment of the present disclosure.

Figure 3 illustrates a cross-sectional view of an embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs), in accordance with an embodiment of the present disclosure.

Figures 4A-4F illustrate cross-sectional views of various stages in a method of fabricating another embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs), in accordance with another embodiment of the present disclosure.

Figure 5 illustrates a cross-sectional view of another embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs), in accordance with another embodiment of the present disclosure.

Figure 6 illustrates a cross-sectional view of an embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs) and integrated with underlying CMOS periphery and overlying interconnects, in accordance with an embodiment of the present disclosure.

Figures 7A and 7B are top views of a wafer and dies that include one or more embedded non-volatile memory structures based on ferroelectric field effect transistors (FeFETs), in accordance with one or more of the embodiments disclosed herein.

Figure 8 illustrates a block diagram of an electronic system, in accordance with an embodiment of the present disclosure.

Figure 9 is a cross-sectional side view of an integrated circuit (IC) device assembly that may include one or more embedded non-volatile memory structures based on ferroelectric field effect transistors (FeFETs), in accordance with one or more of the embodiments disclosed herein.

Figure 10 illustrates a computing device in accordance with one implementation of an embodiment of the disclosure.

DESCRIPTION OF THE EMBODIMENTS

Embedded non-volatile memory structures based on ferroelectric field effect transistors (FeFETs) are described. In the following description, numerous specific details are set forth,

such as specific material and structural regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as single or dual damascene processing, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale. In some cases, various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, “below”, “bottom,” and “top” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

Embodiments described herein may be directed to front-end-of-line (FEOL) semiconductor processing and structures. FEOL is the first portion of integrated circuit (IC) fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are patterned in the semiconductor substrate or layer. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers. Following the last FEOL operation, the result is typically a wafer with isolated transistors (e.g., without any wires).

Embodiments described herein may be directed to back end of line (BEOL) semiconductor processing and structures. BEOL is the second portion of IC fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are interconnected with wiring on the wafer, e.g., the metallization layer or layers. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections. In the BEOL part of the fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC processes, more than 10 metal layers may be added in the BEOL.

Embodiments described below may be applicable to FEOL processing and structures, BEOL processing and structures, or both FEOL and BEOL processing and structures. In particular, although an exemplary processing scheme may be illustrated using a FEOL processing

scenario, such approaches may also be applicable to BEOL processing. Likewise, although an exemplary processing scheme may be illustrated using a BEOL processing scenario, such approaches may also be applicable to FEOL processing.

One or more embodiments described herein are directed to ferroelectric field effect transistors. Embodiments may be directed to BEOL thin film ferroelectric field effect transistors. Embodiments may include or pertain to back end transistors for, e.g., embedded non-volatile memory (eNVM). In one embodiment, a FeFET described herein can be used as a stand-alone two-state memory. Embodiments may be directed to fabrication of three-dimensional (3D) embedded nonvolatile memory, such as embedded 3D NAND based on FeFETs, and the resulting structures.

To provide context, state-of-the-art embedded memories have large bitcell sizes, e.g., typically greater than $9F^2$. Additionally, state-of-the-art embedded memories are typically based on planar devices, which are limited in scaling to smaller dimensions, since only two-dimensional (2D) scaling is possible.

In accordance with one or more embodiments of the present invention, fabrication processes are described for a vertically integrated memory. In particular embodiments, the density of such memory is $4F^2$. In an embodiment, such a memory array is fabricated in BEOL layers of an integrated circuit. The performance of such memory may be faster than flash memory, and may be made with higher density than flash memory. In some embodiments, array efficiency is reduced by placing periphery complementary metal oxide semiconductor (CMOS) structures below such a memory array. In accordance with one or more embodiments of the present disclosure, a vertical string of ferroelectric memory elements is described. Such an architecture may provide the most dense memory architecture possible since it is a vertical array in contrast to a planar memory array.

To exemplify the operation of a ferroelectric field effect transistor, Figures 1A and 1B illustrate cross-sectional views of two different states of a ferroelectric field effect transistor (FeFET), in accordance with an embodiment of the present disclosure.

Referring to Figure 1A, an integrated circuit structure 100 includes a semiconductor channel layer 104 above a substrate 102. A ferroelectric oxide material 106 is above the semiconductor channel layer 104. A gate electrode 108 is on the ferroelectric oxide material 106. The gate electrode 108 has a first side and a second side opposite the first side. A first source/drain region 110 is at the first side of the gate electrode 108, and a second source/drain region 112 is at the second side of the gate electrode 108. In the state shown for Figure 1A, I_d is high, and a state “1” is read.

Referring to Figure 1B, the integrated circuit structure of Figure 1A is shown as

integrated circuit structure 150, where I_d is low, and a state “0” is read. To program the cell 100/150, a positive or negative gate voltage (V_g) is applied to switch polarization (P) of the ferroelectric layer downward (layer 106 of Figure 1A) or upward (layer 106' of Figure 1B), respectively, as is depicted in Figures 1A and 1B. A memory cell based on devices of the type 5 100/150 may effectively operate similar to flash cell, since a memory window is determined by the shift in the threshold voltage of the device.

Referring to Figures 1A and 1B, in an embodiment, the semiconductor channel layer 104 is an amorphous or a polycrystalline material. In an embodiment, the semiconductor channel layer 104 includes silicon or indium gallium zinc oxide (IGZO). In a latter such embodiment, the 10 IGZO layer has a gallium to indium ratio of 1:1, a gallium to indium ratio greater than 1 (e.g., 2:1, 3:1, 4:1, 5:1, 6:1, 7:1, 8:1, 9:1, or 10:1), or a gallium to indium ratio less than 1 (e.g., 1:2, 1:3, 1:4, 1:5, 1:6, 1:7, 1:8, 1:9, or 1:10). A low indium content IGZO may refer to IGZO having more gallium than indium (e.g., with a gallium to indium ratio greater than 1:1), and may also be referred to as high gallium content IGZO. Similarly, low gallium content IGZO may refer to 15 IGZO having more indium than gallium (e.g., with a gallium to indium ratio less than 1:1), and may also be referred to as high indium content IGZO.

In an embodiment, the ferroelectric oxide material 106/106' is selected from the group consisting of lead zirconate titanate (PZT), strontium bismuth tantalum oxide (SBT), and lanthanum-doped lead zirconium titanate (PLZT). In another embodiment, the ferroelectric 20 oxide material 106/106' includes hafnium and oxygen. In one such embodiment, a hafnium oxide material having a structural geometry that provides for a switchable polarization direction is used as the ferroelectric oxide material 106/106'. In another embodiment, the ferroelectric oxide material 106/106' is a hafnium zirconium oxide material.

In an embodiment, the integrated circuit structures of Figures 1A and 1B, further include 25 an insulator material layer 114 between and in contact with the ferroelectric oxide material 106/106' and the semiconductor channel layer 104, as is depicted. In one such embodiment, the insulator material layer 114 is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride. In another embodiment, the ferroelectric oxide material 106/106' is directly on the semiconductor channel layer 104.

30 As an exemplary processing scheme involving fabrication of a vertical FeFET NAND array having a continuous ferroelectric layer, Figures 2A-2F illustrate cross-sectional views of various stages in a method of fabricating an embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs), in accordance with an embodiment of the present disclosure.

35 Referring to Figure 2A, a method of fabricating an integrated circuit structure includes

forming a stack 204 of alternating first 206 and second 208 insulating layers above a substrate 202. In one embodiment, the stack 202 of alternating first 206 and second 208 insulating layers is a stack of alternating silicon dioxide and silicon nitride layers. First trenches 210 are then formed in the stack of alternating first and second insulating layers.

5 Referring to Figure 2B, a ferroelectric oxide material 212 is formed continuous along the sidewalls of the first trenches 210. A semiconductor channel material 214 is then formed adjacent to the ferroelectric oxide 212 material along the sidewalls of the first trenches 210.

In an embodiment, the ferroelectric oxide material 212 is formed using an atomic layer deposition (ALD) process. In an embodiment, forming the ferroelectric oxide material 212
10 includes forming a material selected from the group consisting of a material including hafnium and oxygen, a lead zirconate titanate (PZT) material, a strontium bismuth tantalum oxide (SBT) material, and a lanthanum-doped lead zirconium titanate (PLZT) material. In an embodiment, the semiconductor channel material 214 is formed using an atomic layer deposition (ALD) process. In an embodiment, forming the semiconductor channel material 214 includes forming a
15 silicon layer or an indium gallium zinc oxide (IGZO) layer.

Referring to Figure 2C, a second trench 216 is formed in the stack 204 of alternating first and second insulating layers. The second trench 216 is between the first trenches 210.

Referring to Figure 2D, the second insulating layers 208 are removed from the stack of alternating first and second insulating layers 204. In one embodiment, the second insulating
20 layers 208 are removed from the stack of alternating first and second insulating layers 204 using a wet etch process.

Referring to Figure 2E, a vertical arrangement of a plurality of gate electrodes 218 is formed in locations where the second insulating layers were removed. In one such embodiment, the vertical arrangement of a plurality of gate electrodes 218 is formed using a tungsten (W) and
25 subsequent W cut process to isolate the gate electrodes 218, which may effectively act as word lines.

Referring to Figure 2F, a source contact 220 and ILD 222 fill process is performed. It is to be appreciated that the source contact 220 may make contact to a conductive layer on substrate 202, the conductive layer coupled to the semiconductor channel material 214.

30 As an optional next process operation, Figure 3 illustrates a cross-sectional view of an embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs), in accordance with an embodiment of the present disclosure.

Referring to Figure 3, the structure of Figure 2F is patterned to provide steps 302. The steps 302 sequentially expose different ones of the gate electrodes 218. Gate contacts 304 are
35 fabricated to make electrical contact with each of the gate electrodes 218. Additional processing

may involve fabrication of drain contacts (not shown) coupled to semiconductor channel material 214, e.g., at the upper surface of the structure of Figure 3.

Referring collectively to Figures 2A-2F and 3, in an embodiment, an integrated circuit structure includes a vertical arrangement of a plurality of gate electrodes 218 in an inter-layer dielectric (ILD) layer 206/222 above a substrate 202. A trench 210 is through the vertical arrangement of a plurality of gate electrodes 218 in the ILD layer 206/222, the 210 trench having sidewalls. A ferroelectric oxide material 212 is continuous along the sidewalls of the trench 210. The ferroelectric oxide material 212 is in contact with the vertical arrangement of the plurality of gate electrodes 218. A semiconductor channel material 214 is adjacent to the ferroelectric oxide material 212 along the sidewalls of the trench 210.

In an embodiment, the integrated circuit structure further includes an insulator material layer between and in contact with the ferroelectric oxide material 212 and the semiconductor channel layer 214, as was described in association with Figures 1A and 1B. In an embodiment, the sidewalls of the trench 210 are substantially flat, as is depicted in Figure 2A.

In an embodiment, the ferroelectric oxide material 212 includes hafnium and oxygen. In another embodiment, the ferroelectric oxide material 212 is selected from the group consisting of lead zirconate titanate (PZT), strontium bismuth tantalum oxide (SBT), and lanthanum-doped lead zirconium titanate (PLZT).

In an embodiment, the semiconductor channel material 214 is an amorphous or a polycrystalline material. In an embodiment, the semiconductor channel material 214 includes silicon or indium gallium zinc oxide (IGZO).

As an exemplary processing scheme involving fabrication of a vertical FeFET NAND array having a discontinuous or discrete ferroelectric layer, Figures 4A-4F illustrate cross-sectional views of various stages in a method of fabricating another embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs), in accordance with another embodiment of the present disclosure.

Referring to Figure 4A, a method of fabricating an integrated circuit structure includes forming a vertical arrangement 404 of a plurality of conductive layers 406 in an inter-layer dielectric (ILD) layer 408 above a substrate 402.

Referring to Figure 4B, a trench 410 is formed through the vertical arrangement 404 of the plurality of conductive layers 406 in the ILD layer 408. In one embodiment, the trench has substantially flat sidewalls.

Referring to Figure 4C, the conductive layers 406 of the vertical arrangement 404 of the plurality of conductive layers 406 are laterally recessed to provide a vertical arrangement of a plurality of gate electrodes 412 in the ILD layer and to provide corrugated sidewalls for the

trench 410'. In one embodiment, laterally recessing the conductive layers 406 of the vertical arrangement 404 of the plurality of conductive layers 406 to provide the vertical arrangement of a plurality of gate electrodes 412 involves wet etching the vertical arrangement of the plurality of conductive layers 406 selective to or mostly selective to the ILD layer 408.

5 Referring to Figure 4D, an insulating layer 414 is optionally formed continuous along the corrugated sidewalls of the trench 410', the insulating layer in contact with the vertical arrangement of the plurality of gate electrodes. It is to be appreciated that in another embodiment, the formation of insulating layer 414 is omitted.

10 Referring to Figure 4E, a ferroelectric oxide material 416 is formed in the trench 410'. In an embodiment, the ferroelectric oxide material 416 is formed using an atomic layer deposition (ALD) process. In an embodiment, forming the ferroelectric oxide material 416 includes forming a material selected from the group consisting of a material including hafnium and oxygen, a lead zirconate titanate (PZT) material, a strontium bismuth tantalum oxide (SBT) material, and a lanthanum-doped lead zirconium titanate (PLZT) material.

15 Referring to Figure 4F, the ferroelectric oxide material 416 is made discontinuous to form discontinuous ferroelectric oxide material 418. In one embodiment, the ferroelectric oxide material 416 is made discontinuous by anisotropically etching portions of the ferroelectric oxide material 416 exposed in trenches 410'.

20 Subsequently, a semiconductor channel material 420 is formed, as is depicted in Figure 4F. In an embodiment, the semiconductor channel material 420 is formed using an atomic layer deposition (ALD) process. In an embodiment, forming the semiconductor channel material 420 includes forming a silicon layer or a indium gallium zinc oxide (IGZO) layer.

25 As an optional next process operation, Figure 5 illustrates a cross-sectional view of another embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs), in accordance with another embodiment of the present disclosure.

30 Referring to Figure 5, the structure of Figure 4F is patterned to provide steps 502. The steps 502 sequentially expose different ones of the gate electrodes 412. Gate contacts (not shown) may be fabricated to make electrical contact with each of the gate electrodes 412, similar to the structure described in association with Figure 3. Additional processing may involve fabrication of drain contacts (not shown) coupled to semiconductor channel material 420, e.g., at the upper surface of the structure of Figure 5.

35 Referring collectively to Figures 4A-4F and 5, in an embodiment, an integrated circuit structure includes a vertical arrangement of a plurality of gate electrodes 412 in an inter-layer dielectric (ILD) layer 408 above a substrate 402. A trench 410 is through the vertical arrangement of a plurality of gate electrodes 412 in the ILD layer 408, the trench 410 having

sidewalls. An insulating layer 414 is continuous along the sidewalls of the trench 410. The insulating layer 414 is in contact with the vertical arrangement of the plurality of gate electrodes 412. A ferroelectric oxide material 418 is discontinuous along the sidewalls of the trench 410. The ferroelectric oxide material 418 is in contact with the insulating layer 414. A semiconductor channel material 420 is adjacent to the ferroelectric oxide 418 material along the sidewalls of the trench 410. In one embodiment, the semiconductor channel material 420 is continuous along the sidewalls of the trench 410.

In an embodiment, the integrated circuit structure further includes an insulator material layer between and in contact with the ferroelectric oxide material 418 and the semiconductor channel material 420, as was described in association with Figures 1A and 1B. In an embodiment, the sidewalls of the trench 410' are corrugated, as is depicted in Figure 4C.

In an embodiment, the ferroelectric oxide material 418 includes hafnium and oxygen. In another embodiment, the ferroelectric oxide material 418 is selected from the group consisting of lead zirconate titanate (PZT), strontium bismuth tantalum oxide (SBT), and lanthanum-doped lead zirconium titanate (PLZT).

In an embodiment, the semiconductor channel material 420 is an amorphous or a polycrystalline material. In an embodiment, the semiconductor channel material 420 includes silicon or indium gallium zinc oxide (IGZO).

In an embodiment, gate electrodes or gate material described herein includes at least one P-type work function metal or N-type work function metal. For a P-type transistors, metals that may be used for the gate electrode may include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides (e.g., ruthenium oxide). For an N-type transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals (e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide). In some embodiments, the gate electrode includes a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as to act as a barrier layer.

It is to be appreciated that the layers and materials described in association with embodiments herein are typically formed on or above an underlying semiconductor substrate, e.g., as FEOL layer(s). In other embodiments, the layers and materials described in association with embodiments herein are formed on or above underlying device layer(s) of an integrated circuit, e.g., as BEOL layer(s). In an embodiment, an underlying semiconductor substrate represents a general workpiece object used to manufacture integrated circuits. The

semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, although not depicted, structures described herein may be fabricated on underlying lower level back end of line (BEOL) interconnect layers. For example, in one embodiment, an embedded non-volatile memory structure is formed on a material composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride. In a particular embodiment, an embedded non-volatile memory structure is formed on a low-k dielectric layer of an underlying BEOL layer.

Figure 6 illustrates a cross-sectional view of an embedded non-volatile memory structure based on ferroelectric field effect transistors (FeFETs) and integrated with underlying CMOS periphery and overlying interconnects, in accordance with an embodiment of the present disclosure.

Referring to Figure 6, and integrated circuit structure 600 includes CMOS periphery 604 on a substrate 602. CMOS periphery 604 includes transistors 606 and overlying interconnects, such a metal 1 (M1) interconnects 608 and metal 2 (M2) interconnects 610. A vertical memory array 612, which includes embedded memory structures such as described above, is above the CMOS periphery 604. In one embodiment, the vertical memory array 612 has a memory area of approximately $4F^2/N$ defined cell area. Conductive contacts 613 and overlying interconnects/wiring 614 are above the vertical memory array 612.

In an embodiment, interconnect lines (and, possibly, underlying via structures) described herein are composed of one or more metal or metal-containing conductive structures. The conductive interconnect lines are also sometimes referred to in the art as traces, wires, lines, metal, interconnect lines or simply interconnects. In a particular embodiment, each of the interconnect lines includes a barrier layer and a conductive fill material. In an embodiment, the barrier layer is composed of a metal nitride material, such as tantalum nitride or titanium nitride. In an embodiment, the conductive fill material is composed of a conductive material such as, but not limited to, Cu, Al, Ti, Zr, Hf, V, Ru, Co, Ni, Pd, Pt, W, Ag, Au or alloys thereof.

Interconnect lines described herein may be fabricated as a grating structure, where the term “grating” is used herein to refer to a tight pitch grating structure. In one such embodiment, the tight pitch is not achievable directly through conventional lithography. For example, a

pattern based on conventional lithography may first be formed, but the pitch may be halved by the use of spacer mask patterning, as is known in the art. Even further, the original pitch may be quartered by a second round of spacer mask patterning. Accordingly, the grating-like patterns described herein may have conductive lines spaced at a constant pitch and having a constant width. The pattern may be fabricated by a pitch halving or pitch quartering, or other pitch division, approach.

In an embodiment, ILD materials described herein are composed of or include a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

In an embodiment, as is also used throughout the present description, patterning of trenches is achieved using lithographic operations performed using 193nm immersion lithography (i193), extreme ultra-violet (EUV) and/or electron beam direct write (EBDW) lithography, or the like. A positive tone or a negative tone resist may be used. In one embodiment, a lithographic mask is a trilayer mask composed of a topographic masking portion, an anti-reflective coating (ARC) layer, and a photoresist layer. In a particular such embodiment, the topographic masking portion is a carbon hardmask (CHM) layer and the anti-reflective coating layer is a silicon ARC layer.

The integrated circuit structures described herein may be included in an electronic device. As an example of one such apparatus, Figures 7A and 7B are top views of a wafer and dies that include one or more embedded non-volatile memory structures based on ferroelectric field effect transistors (FeFETs), in accordance with one or more of the embodiments disclosed herein.

Referring to Figures 7A and 7B, a wafer 700 may be composed of semiconductor material and may include one or more dies 702 having integrated circuit (IC) structures formed on a surface of the wafer 700. Each of the dies 702 may be a repeating unit of a semiconductor product that includes any suitable IC (e.g., ICs including one or more embedded non-volatile memory structures based on ferroelectric field effect transistors, such as described above. After the fabrication of the semiconductor product is complete, the wafer 700 may undergo a singulation process in which each of the dies 702 is separated from one another to provide discrete “chips” of the semiconductor product. In particular, structures that include FeFETs as disclosed herein may take the form of the wafer 700 (e.g., not singulated) or the form of the die 702 (e.g., singulated). The die 702 may include one or more embedded non-volatile memory

structures based on ferroelectric field effect transistors and/or supporting circuitry to route electrical signals, as well as any other IC components. In some embodiments, the wafer 700 or the die 702 may include an additional memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 702. For example, a memory array formed by multiple memory devices may be formed on a same die 702 as a processing device or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

Figure 8 illustrates a block diagram of an electronic system 800, in accordance with an embodiment of the present disclosure. The electronic system 800 can correspond to, for example, a portable system, a computer system, a process control system, or any other system that utilizes a processor and an associated memory. The electronic system 800 may include a microprocessor 802 (having a processor 804 and control unit 806), a memory device 808, and an input/output device 810 (it is to be appreciated that the electronic system 800 may have a plurality of processors, control units, memory device units and/or input/output devices in various embodiments). In one embodiment, the electronic system 800 has a set of instructions that define operations which are to be performed on data by the processor 804, as well as, other transactions between the processor 804, the memory device 808, and the input/output device 810. The control unit 806 coordinates the operations of the processor 804, the memory device 808 and the input/output device 810 by cycling through a set of operations that cause instructions to be retrieved from the memory device 808 and executed. The memory device 808 can include a non-volatile memory cell as described in the present description. In an embodiment, the memory device 808 is embedded in the microprocessor 802, as depicted in Figure 8. In an embodiment, the processor 804, or another component of electronic system 800, includes one or more embedded non-volatile memory structures based on ferroelectric field effect transistors

(FeFETs), such as those described herein.

Figure 9 is a cross-sectional side view of an integrated circuit (IC) device assembly that may include one or more embedded non-volatile memory structures based on ferroelectric field effect transistors (FeFETs), in accordance with one or more of the embodiments disclosed herein.

Referring to Figure 9, an IC device assembly 900 includes components having one or more integrated circuit structures described herein. The IC device assembly 900 includes a number of components disposed on a circuit board 902 (which may be, e.g., a motherboard). The IC device assembly 900 includes components disposed on a first face 940 of the circuit board 902 and an opposing second face 942 of the circuit board 902. Generally, components may be disposed on one or both faces 940 and 942. In particular, any suitable ones of the components of the IC device assembly 900 may include a number of embedded non-volatile memory structures based on ferroelectric field effect transistors, such as disclosed herein.

In some embodiments, the circuit board 902 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 902. In other embodiments, the circuit board 902 may be a non-PCB substrate.

The IC device assembly 900 illustrated in Figure 9 includes a package-on-interposer structure 936 coupled to the first face 940 of the circuit board 902 by coupling components 916. The coupling components 916 may electrically and mechanically couple the package-on-interposer structure 936 to the circuit board 902, and may include solder balls (as shown in Figure 9), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

The package-on-interposer structure 936 may include an IC package 920 coupled to an interposer 904 by coupling components 918. The coupling components 918 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 916. Although a single IC package 920 is shown in Figure 9, multiple IC packages may be coupled to the interposer 904. It is to be appreciated that additional interposers may be coupled to the interposer 904. The interposer 904 may provide an intervening substrate used to bridge the circuit board 902 and the IC package 920. The IC package 920 may be or include, for example, a die (the die 702 of Figure 7B), or any other suitable component.

Generally, the interposer 904 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 904 may couple the IC package 920 (e.g., a die) to a ball grid array (BGA) of the coupling components 916 for coupling to the circuit board

902. In the embodiment illustrated in Figure 9, the IC package 920 and the circuit board 902 are attached to opposing sides of the interposer 904. In other embodiments, the IC package 920 and the circuit board 902 may be attached to a same side of the interposer 904. In some embodiments, three or more components may be interconnected by way of the interposer 904.

5 The interposer 904 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 904 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 904 may include metal interconnects
10 908 and vias 910, including but not limited to through-silicon vias (TSVs) 906. The interposer 904 may further include embedded devices 914, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power
15 amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 904. The package-on-interposer structure 936 may take the form of any of the package-on-interposer structures known in the art.

 The IC device assembly 900 may include an IC package 924 coupled to the first face 940 of the circuit board 902 by coupling components 922. The coupling components 922 may take
20 the form of any of the embodiments discussed above with reference to the coupling components 916, and the IC package 924 may take the form of any of the embodiments discussed above with reference to the IC package 920.

 The IC device assembly 900 illustrated in Figure 9 includes a package-on-package structure 934 coupled to the second face 942 of the circuit board 902 by coupling components
25 928. The package-on-package structure 934 may include an IC package 926 and an IC package 932 coupled together by coupling components 930 such that the IC package 926 is disposed between the circuit board 902 and the IC package 932. The coupling components 928 and 930 may take the form of any of the embodiments of the coupling components 916 discussed above, and the IC packages 926 and 932 may take the form of any of the embodiments of the IC package
30 920 discussed above. The package-on-package structure 934 may be configured in accordance with any of the package-on-package structures known in the art.

 Figure 10 illustrates a computing device 1000 in accordance with one implementation of the disclosure. The computing device 1000 houses a board 1002. The board 1002 may include a number of components, including but not limited to a processor 1004 and at least one
35 communication chip 1006. The processor 1004 is physically and electrically coupled to the

board 1002. In some implementations the at least one communication chip 1006 is also physically and electrically coupled to the board 1002. In further implementations, the communication chip 1006 is part of the processor 1004.

Depending on its applications, computing device 1000 may include other components that may or may not be physically and electrically coupled to the board 1002. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some implementations of the disclosure, the integrated circuit die of the processor includes one or more embedded non-volatile memory structures based on ferroelectric field effect transistors, in accordance with implementations of embodiments of the disclosure. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also includes an integrated circuit die packaged within the communication chip 1006. In accordance with another implementation of embodiments of the

disclosure, the integrated circuit die of the communication chip includes one or more embedded non-volatile memory structures based on ferroelectric field effect transistors, in accordance with implementations of embodiments of the disclosure.

5 In further implementations, another component housed within the computing device 1000 may contain an integrated circuit die that includes one or more embedded non-volatile memory structures based on ferroelectric field effect transistors, in accordance with implementations of embodiments of the disclosure.

10 In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1000 may be any other electronic device that processes data.

15 Thus, embodiments described herein include embedded non-volatile memory structures based on ferroelectric field effect transistors (FeFETs).

The above description of illustrated implementations of embodiments of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

20 These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

30 Example embodiment 1: An integrated circuit structure includes a vertical arrangement of a plurality of gate electrodes in an inter-layer dielectric (ILD) layer above a substrate. A trench is through the vertical arrangement of a plurality of gate electrodes in the ILD layer, the trench having sidewalls. A ferroelectric oxide material is continuous along the sidewalls of the trench. The ferroelectric oxide material is in contact with the vertical arrangement of the plurality of gate electrodes. A semiconductor channel material is adjacent to the ferroelectric oxide material along the sidewalls of the trench.

35 Example embodiment 2: The integrated circuit structure of example embodiment 1, further including an insulator material layer between and in contact with the ferroelectric oxide material and the semiconductor channel layer.

Example embodiment 3: The integrated circuit structure of example embodiment 1 or 2, wherein the sidewalls of the trench are substantially flat.

Example embodiment 4: The integrated circuit structure of example embodiment 1, 2 or 3, wherein the semiconductor channel material is an amorphous or a polycrystalline material.

5 Example embodiment 5: The integrated circuit structure of example embodiment 1, 2, 3 or 4, wherein the semiconductor channel material includes silicon or indium gallium zinc oxide (IGZO).

Example embodiment 6: The integrated circuit structure of example embodiment 1, 2, 3, 4 or 5, wherein the ferroelectric oxide material includes hafnium and oxygen.

10 Example embodiment 7: The integrated circuit structure of example embodiment 1, 2, 3, 4 or 5, wherein the ferroelectric oxide material is selected from the group consisting of lead zirconate titanate (PZT), strontium bismuth tantalum oxide (SBT), and lanthanum-doped lead zirconium titanate (PLZT).

Example embodiment 8: An integrated circuit structure includes a vertical arrangement
15 of a plurality of gate electrodes in an inter-layer dielectric (ILD) layer above a substrate. A trench is through the vertical arrangement of a plurality of gate electrodes in the ILD layer, the trench having sidewalls. An insulating layer is continuous along the sidewalls of the trench, the insulating layer in contact with the vertical arrangement of the plurality of gate electrodes. A ferroelectric oxide material is discontinuous along the sidewalls of the trench, the ferroelectric
20 oxide material in contact with the insulating layer. A semiconductor channel material is adjacent to the ferroelectric oxide material along the sidewalls of the trench, the semiconductor channel material continuous along the sidewalls of the trench.

Example embodiment 9: The integrated circuit structure of example embodiment 8,
further including an insulator material layer between and in contact with the ferroelectric oxide
25 material and the semiconductor channel layer.

Example embodiment 10: The integrated circuit structure of example embodiment 8 or 9, wherein the sidewalls of the trench are corrugated.

Example embodiment 11: The integrated circuit structure of example embodiment 8, 9 or 10, wherein the semiconductor channel material is an amorphous or a polycrystalline material.

30 Example embodiment 12: The integrated circuit structure of example embodiment 8, 9, 10 or 11, wherein the semiconductor channel material includes silicon or indium gallium zinc oxide (IGZO).

Example embodiment 13: The integrated circuit structure of example embodiment 8, 9, 10, 11 or 12, wherein the ferroelectric oxide material includes hafnium and oxygen.

35 Example embodiment 14: The integrated circuit structure of example embodiment 8, 9,

10, 11 or 12, wherein the ferroelectric oxide material is selected from the group consisting of lead zirconate titanate (PZT), strontium bismuth tantalum oxide (SBT), and lanthanum-doped lead zirconium titanate (PLZT).

Example embodiment 15: A method of fabricating an integrated circuit structure includes forming a stack of alternating first and second insulating layers above a substrate. First trenches are formed in the stack of alternating first and second insulating layers. A ferroelectric oxide material is formed continuous along the sidewalls of the first trenches. A semiconductor channel material is formed adjacent to the ferroelectric oxide material along the sidewalls of the first trenches. A second trench is formed in the stack of alternating first and second insulating layers, the second trench between the first trenches. The second insulating layers are removed from the stack of alternating first and second insulating layers. A vertical arrangement of a plurality of gate electrodes is formed in locations where the second insulating layers were removed.

Example embodiment 16: The method of example embodiment 15, wherein forming the semiconductor channel material includes using an atomic layer deposition (ALD) process.

Example embodiment 17: The method of example embodiment 15 or 16, wherein the forming the semiconductor channel material includes forming a silicon layer or an indium gallium zinc oxide (IGZO) layer.

Example embodiment 18: The method of example embodiment 15, 16 or 17, wherein forming the ferroelectric oxide material includes using an atomic layer deposition (ALD) process.

Example embodiment 19: The method of example embodiment 15, 16, 17 or 18, wherein forming the ferroelectric oxide material includes forming a material selected from the group consisting of a material including hafnium and oxygen, a lead zirconate titanate (PZT) material, a strontium bismuth tantalum oxide (SBT) material, and a lanthanum-doped lead zirconium titanate (PLZT) material.

Example embodiment 20: A method of fabricating an integrated circuit structure includes forming a vertical arrangement of a plurality of conductive layers in an inter-layer dielectric (ILD) layer above a substrate. A trench is formed through the vertical arrangement of the plurality of conductive layers in the ILD layer, the trench having substantially flat sidewalls. The conductive layers of the vertical arrangement of the plurality of conductive layers are laterally recessed to provide a vertical arrangement of a plurality of gate electrodes in the ILD layer and to provide corrugated sidewalls for the trench. An insulating layer is formed continuous along the corrugated sidewalls of the trench, the insulating layer in contact with the vertical arrangement of the plurality of gate electrodes. A ferroelectric oxide material is formed vertically discontinuous along the trench, the ferroelectric oxide material in contact with the insulating layer. A

semiconductor channel material is formed adjacent to the ferroelectric oxide material in the trench.

Example embodiment 21: The method of example embodiment 20, wherein laterally recessing the conductive layers of the vertical arrangement of the plurality of conductive layers to provide the vertical arrangement of a plurality of gate electrodes includes wet etching the vertical arrangement of the plurality of conductive layers.

Example embodiment 22: The method of example embodiment 20 or 21, wherein forming the semiconductor channel material includes using an atomic layer deposition (ALD) process.

Example embodiment 23: The method of example embodiment 20, 21 or 22, wherein the forming the semiconductor channel material includes forming a silicon layer or a indium gallium zinc oxide (IGZO) layer.

Example embodiment 24: The method of example embodiment 20, 21, 22 or 23, wherein forming the ferroelectric oxide material includes using an atomic layer deposition (ALD) process.

Example embodiment 25: The method of example embodiment 20, 21, 22, 23 or 24, wherein forming the ferroelectric oxide material includes forming a material selected from the group consisting of a material including hafnium and oxygen, a lead zirconate titanate (PZT) material, a strontium bismuth tantalum oxide (SBT) material, and a lanthanum-doped lead zirconium titanate (PLZT) material.

CLAIMS

What is claimed is:

1. An integrated circuit structure, comprising:
 - 5 a vertical arrangement of a plurality of gate electrodes in an inter-layer dielectric (ILD) layer above a substrate;
 - a trench through the vertical arrangement of a plurality of gate electrodes in the ILD layer, the trench having sidewalls;
 - a ferroelectric oxide material continuous along the sidewalls of the trench, the
 - 10 ferroelectric oxide material in contact with the vertical arrangement of the plurality of gate electrodes; and
 - a semiconductor channel material adjacent to the ferroelectric oxide material along the sidewalls of the trench.
- 15 2. The integrated circuit structure of claim 1, further comprising:
 - an insulator material layer between and in contact with the ferroelectric oxide material and the semiconductor channel layer.
3. The integrated circuit structure of claim 1, wherein the sidewalls of the trench are
- 20 substantially flat.
4. The integrated circuit structure of claim 1, wherein the semiconductor channel material is an amorphous or a polycrystalline material.
- 25 5. The integrated circuit structure of claim 1, wherein the semiconductor channel material comprises silicon or indium gallium zinc oxide (IGZO).
6. The integrated circuit structure of claim 1, wherein the ferroelectric oxide material comprises hafnium and oxygen.
- 30 7. The integrated circuit structure of claim 1, wherein the ferroelectric oxide material is selected from the group consisting of lead zirconate titanate (PZT), strontium bismuth tantalum oxide (SBT), and lanthanum-doped lead zirconium titanate (PLZT).
- 35 8. An integrated circuit structure, comprising:

a vertical arrangement of a plurality of gate electrodes in an inter-layer dielectric (ILD) layer above a substrate;

a trench through the vertical arrangement of a plurality of gate electrodes in the ILD layer, the trench having sidewalls;

5 an insulating layer continuous along the sidewalls of the trench, the insulating layer in contact with the vertical arrangement of the plurality of gate electrodes;

a ferroelectric oxide material discontinuous along the sidewalls of the trench, the ferroelectric oxide material in contact with the insulating layer; and

10 a semiconductor channel material adjacent to the ferroelectric oxide material along the sidewalls of the trench, the semiconductor channel material continuous along the sidewalls of the trench.

9. The integrated circuit structure of claim 8, further comprising:

15 an insulator material layer between and in contact with the ferroelectric oxide material and the semiconductor channel layer.

10. The integrated circuit structure of claim 8, wherein the sidewalls of the trench are corrugated.

20 11. The integrated circuit structure of claim 8, wherein the semiconductor channel material is an amorphous or a polycrystalline material.

12. The integrated circuit structure of claim 8, wherein the semiconductor channel material comprises silicon or indium gallium zinc oxide (IGZO).

25

13. The integrated circuit structure of claim 8, wherein the ferroelectric oxide material comprises hafnium and oxygen.

14. The integrated circuit structure of claim 8, wherein the ferroelectric oxide material is
30 selected from the group consisting of lead zirconate titanate (PZT), strontium bismuth tantalum oxide (SBT), and lanthanum-doped lead zirconium titanate (PLZT).

15. A method of fabricating an integrated circuit structure, the method comprising:

forming a stack of alternating first and second insulating layers above a substrate;

35 forming first trenches in the stack of alternating first and second insulating layers;

forming a ferroelectric oxide material continuous along the sidewalls of the first trenches;
forming a semiconductor channel material adjacent to the ferroelectric oxide material
along the sidewalls of the first trenches;
forming a second trench in the stack of alternating first and second insulating layers, the
5 second trench between the first trenches;
removing the second insulating layers from the stack of alternating first and second
insulating layers; and
forming a vertical arrangement of a plurality of gate electrodes in locations where the
second insulating layers were removed.

10

16. The method of claim 15, wherein forming the semiconductor channel material comprises
using an atomic layer deposition (ALD) process.

15

17. The method of claim 16, wherein the forming the semiconductor channel material comprises
forming a silicon layer or a indium gallium zinc oxide (IGZO) layer.

18. The method of claim 15, wherein forming the ferroelectric oxide material comprises using
an atomic layer deposition (ALD) process.

20

19. The method of claim 18, wherein forming the ferroelectric oxide material comprises forming
a material selected from the group consisting of a material comprising hafnium and oxygen, a
lead zirconate titanate (PZT) material, a strontium bismuth tantalum oxide (SBT) material, and a
lanthanum-doped lead zirconium titanate (PLZT) material.

25

20. A method of fabricating an integrated circuit structure, the method comprising:

forming a vertical arrangement of a plurality of conductive layers in an inter-layer
dielectric (ILD) layer above a substrate;

forming a trench through the vertical arrangement of the plurality of conductive layers in
the ILD layer, the trench having substantially flat sidewalls;

30

laterally recessing the conductive layers of the vertical arrangement of the plurality of
conductive layers to provide a vertical arrangement of a plurality of gate electrodes in the ILD
layer and to provide corrugated sidewalls for the trench;

forming an insulating layer continuous along the corrugated sidewalls of the trench, the
insulating layer in contact with the vertical arrangement of the plurality of gate electrodes;

35

forming a ferroelectric oxide material vertically discontinuous along the trench, the

ferroelectric oxide material in contact with the insulating layer; and

forming a semiconductor channel material adjacent to the ferroelectric oxide material in the trench.

5 21. The method of claim 20, wherein laterally recessing the conductive layers of the vertical arrangement of the plurality of conductive layers to provide the vertical arrangement of a plurality of gate electrodes comprises wet etching the vertical arrangement of the plurality of conductive layers.

10 22. The method of claim 20, wherein forming the semiconductor channel material comprises using an atomic layer deposition (ALD) process.

23. The method of claim 22, wherein the forming the semiconductor channel material comprises forming a silicon layer or a indium gallium zinc oxide (IGZO) layer.

15

24. The method of claim 20, wherein forming the ferroelectric oxide material comprises using an atomic layer deposition (ALD) process.

20 25. The method of claim 24, wherein forming the ferroelectric oxide material comprises forming a material selected from the group consisting of a material comprising hafnium and oxygen, a lead zirconate titanate (PZT) material, a strontium bismuth tantalum oxide (SBT) material, and a lanthanum-doped lead zirconium titanate (PLZT) material.

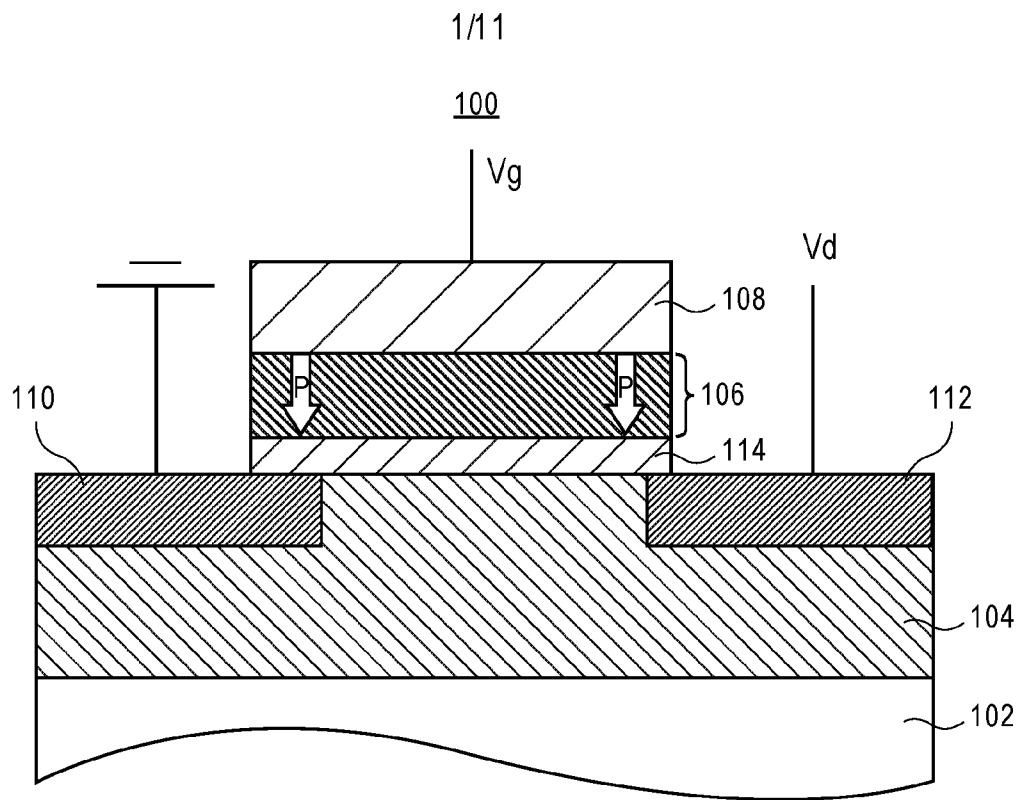


FIG. 1A

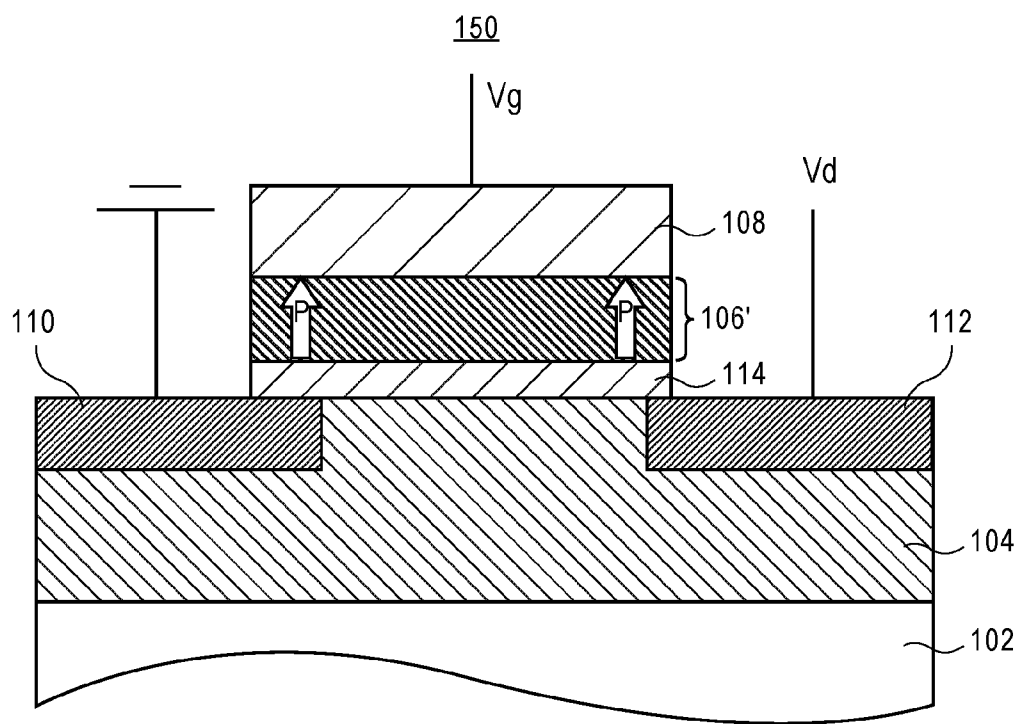


FIG. 1B

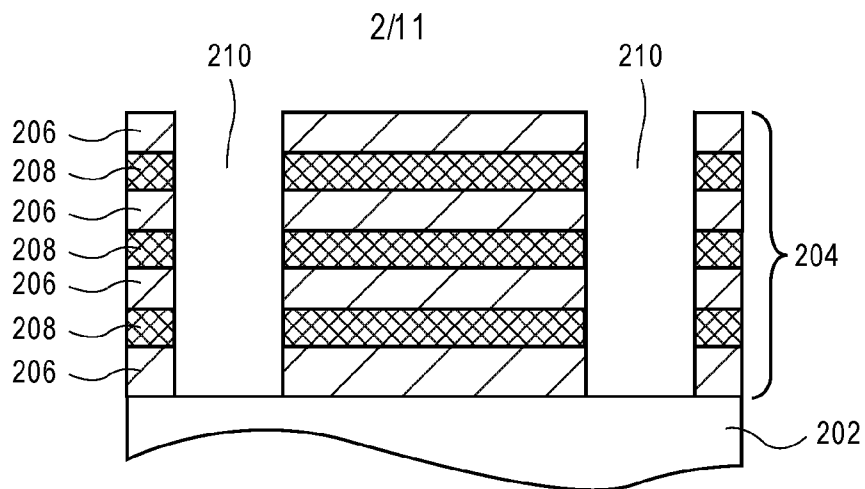


FIG. 2A

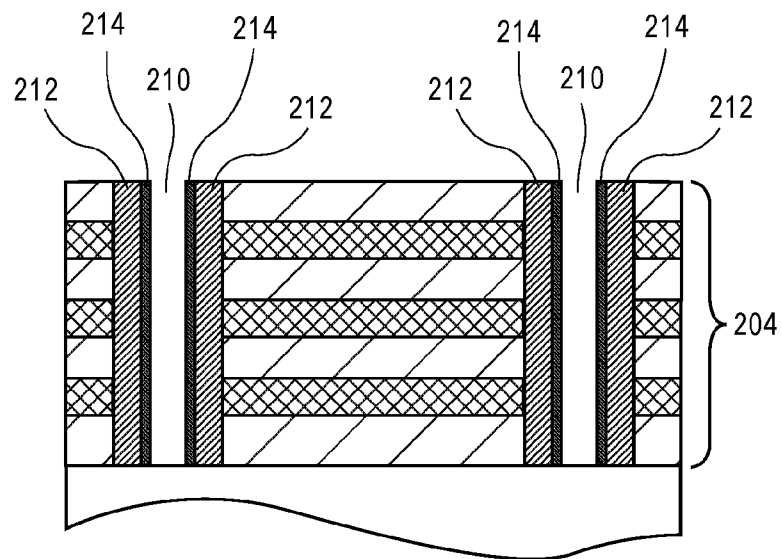


FIG. 2B

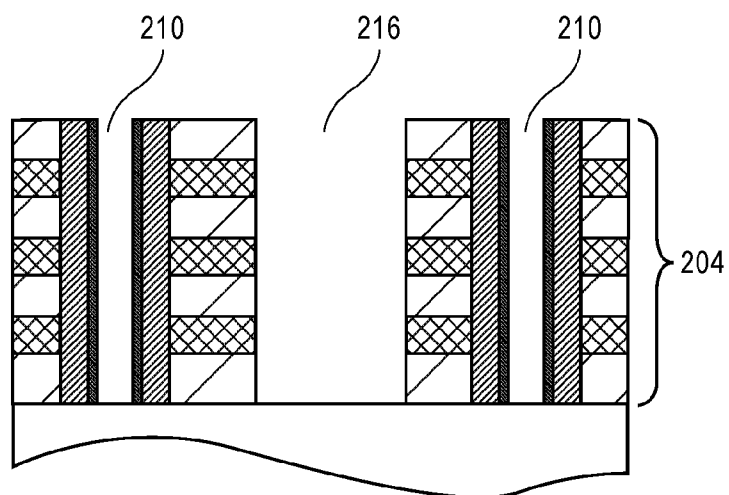


FIG. 2C

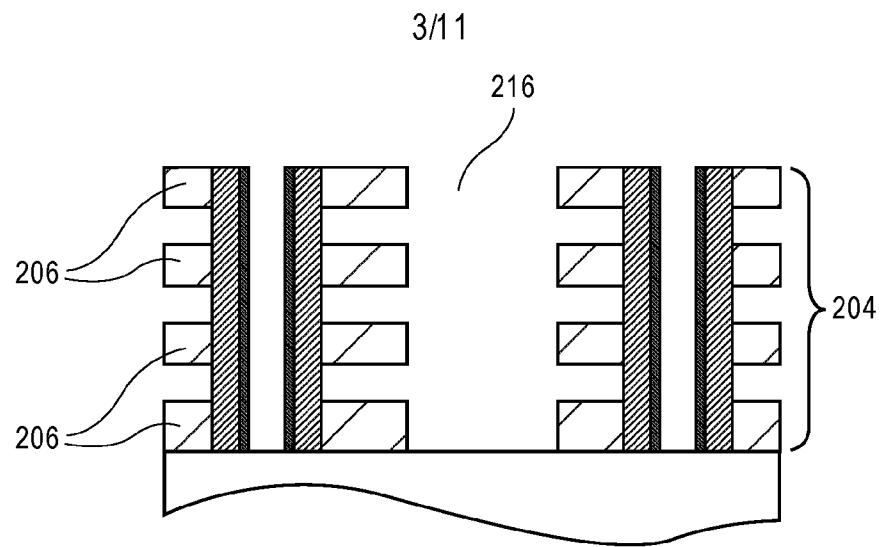


FIG. 2D

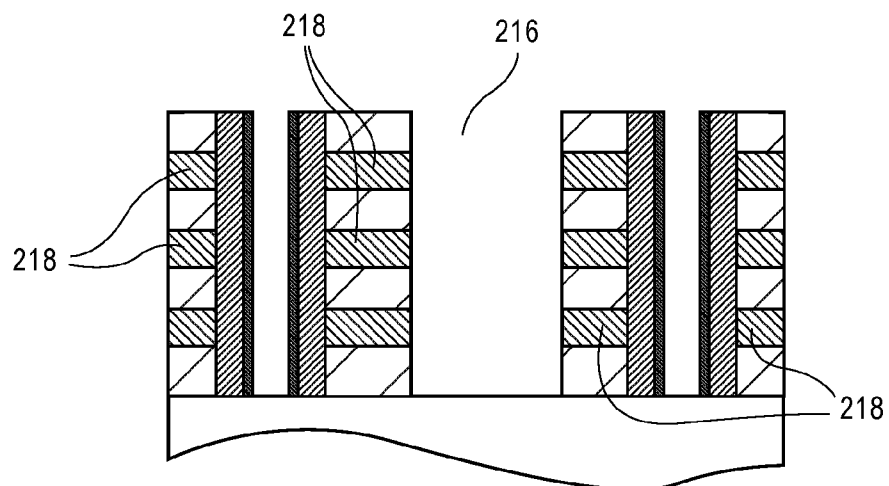


FIG. 2E

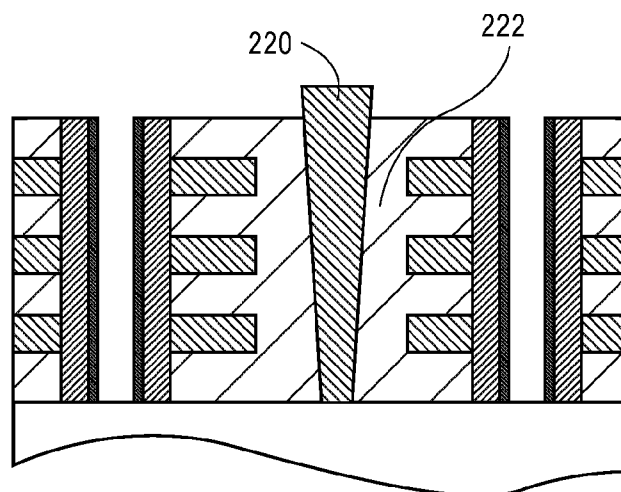


FIG. 2F

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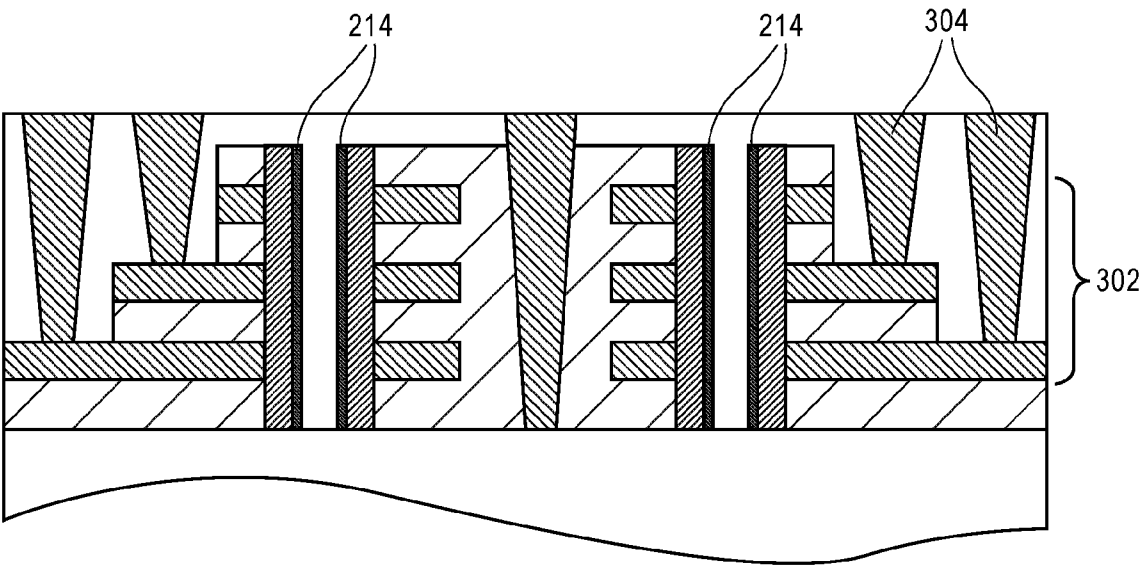


FIG. 3

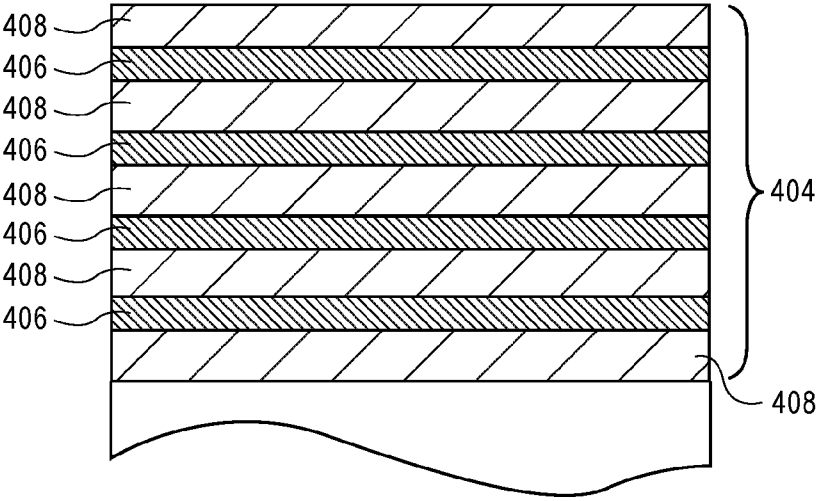


FIG. 4A

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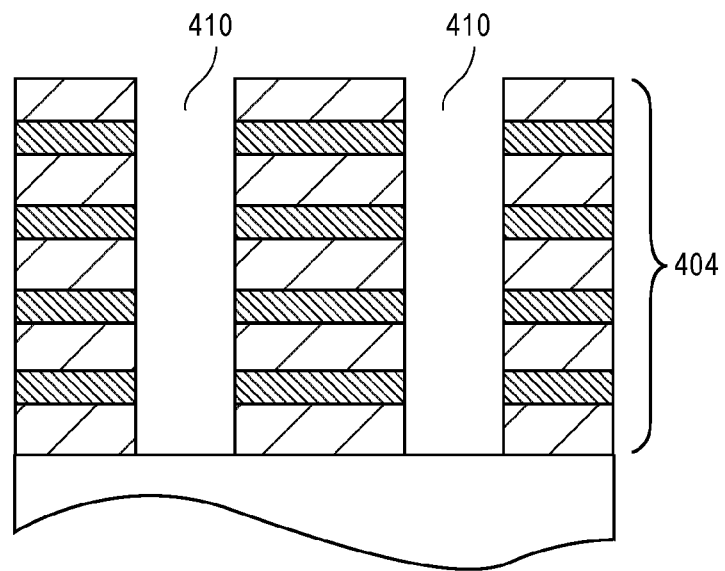


FIG. 4B

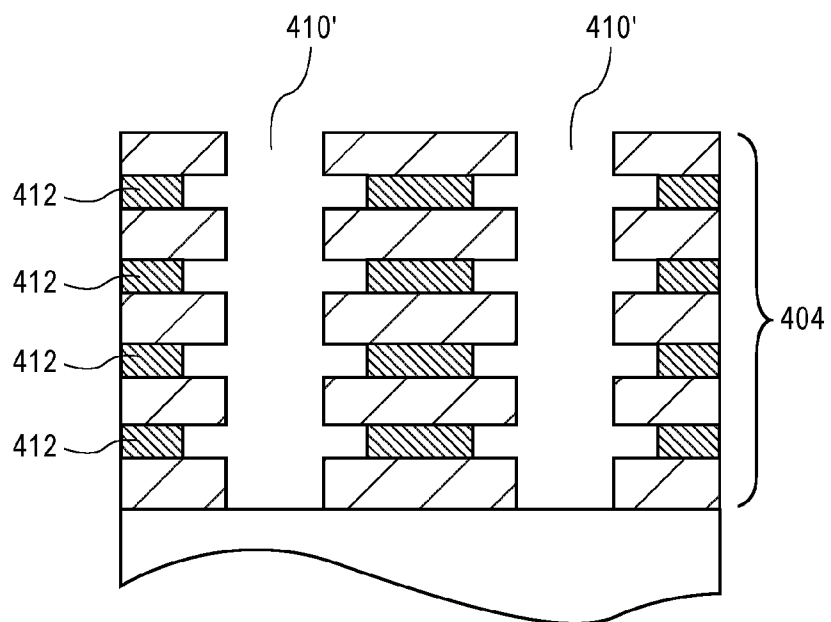


FIG. 4C

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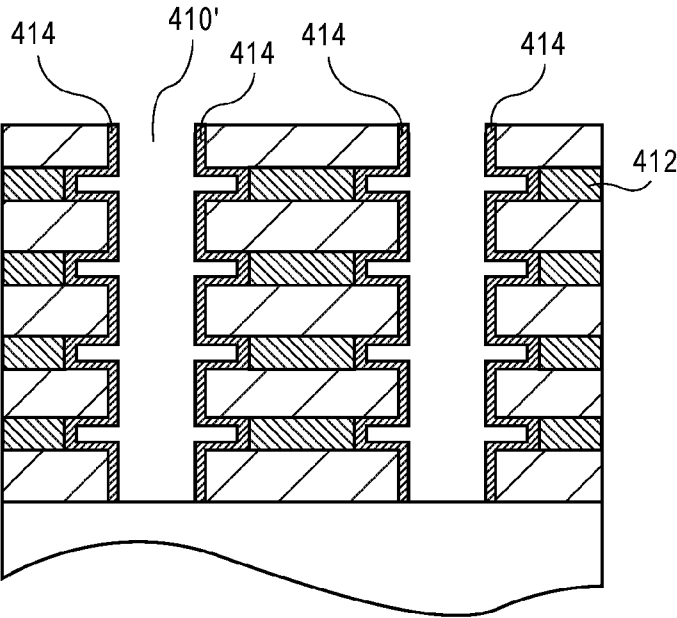


FIG. 4D

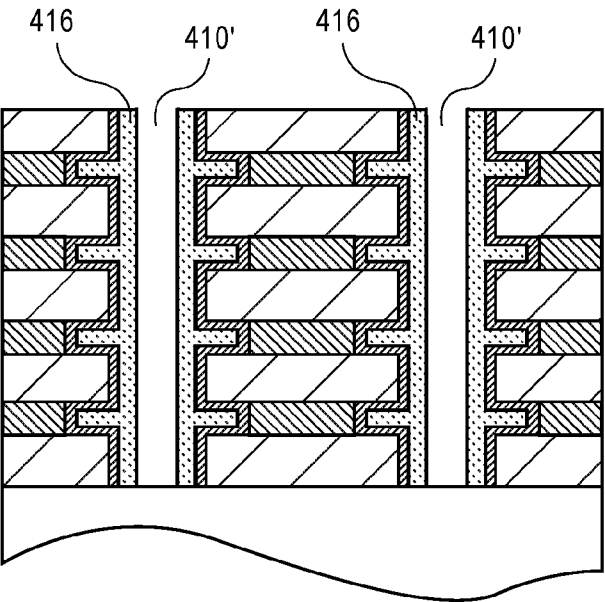


FIG. 4E

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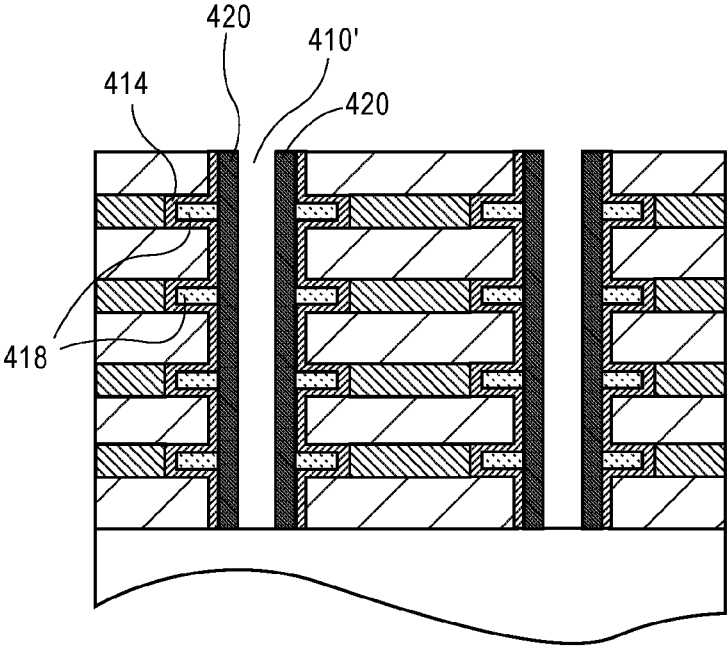


FIG. 4F

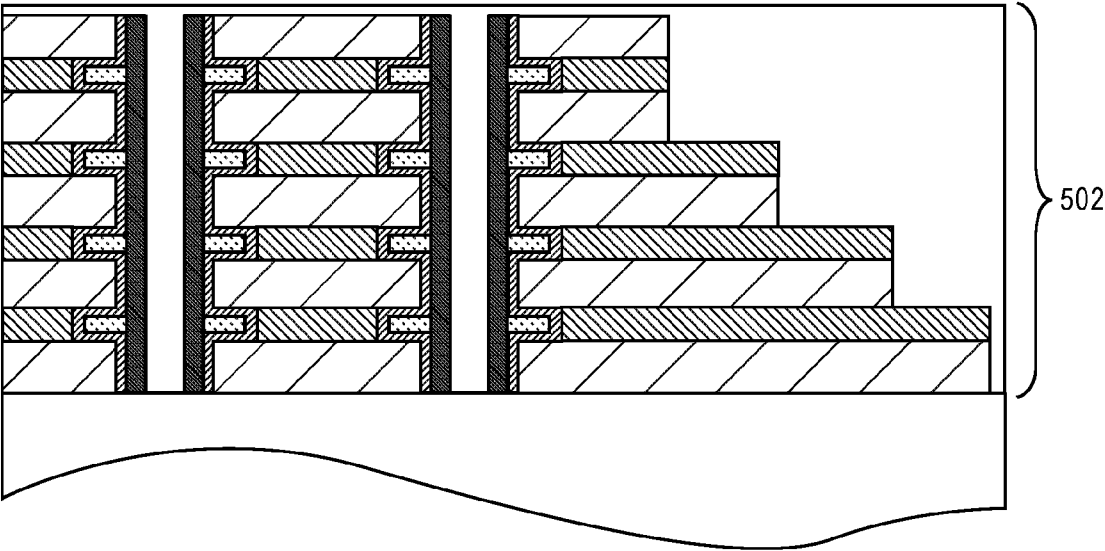


FIG. 5

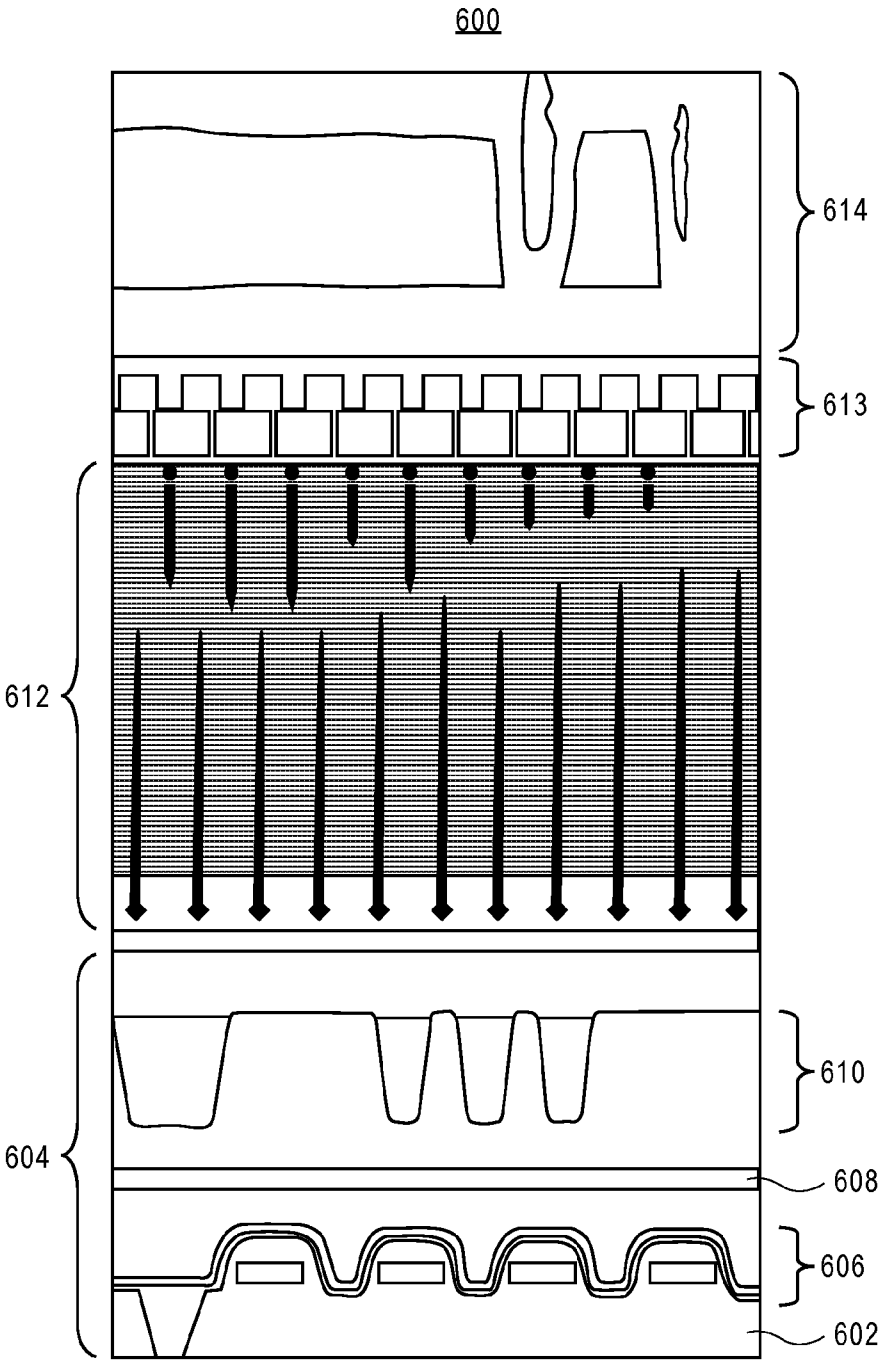


FIG. 6

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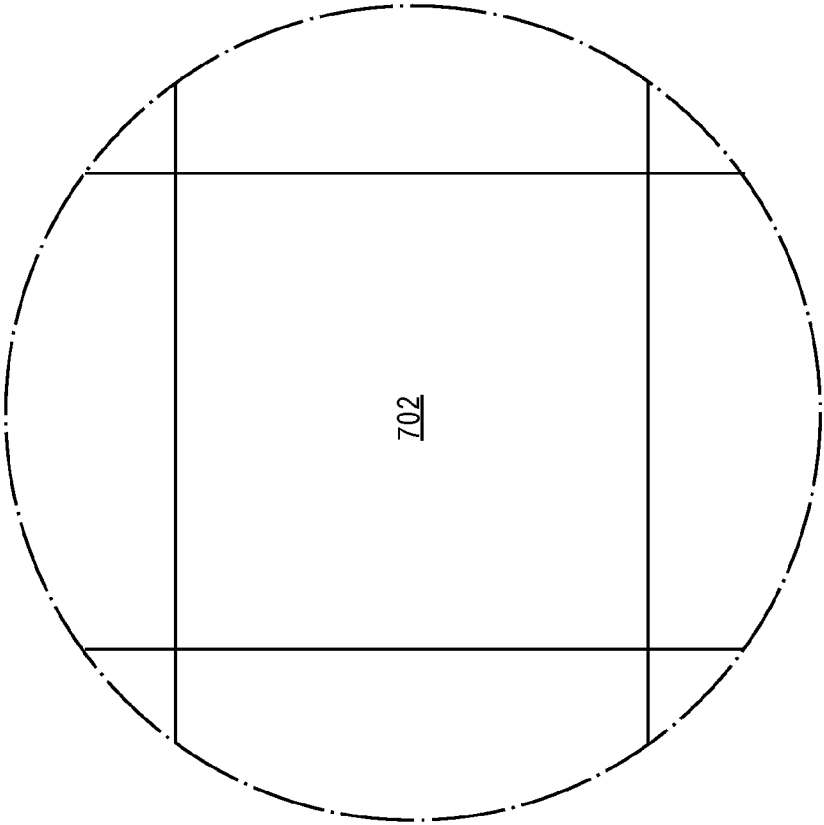


FIG. 7B

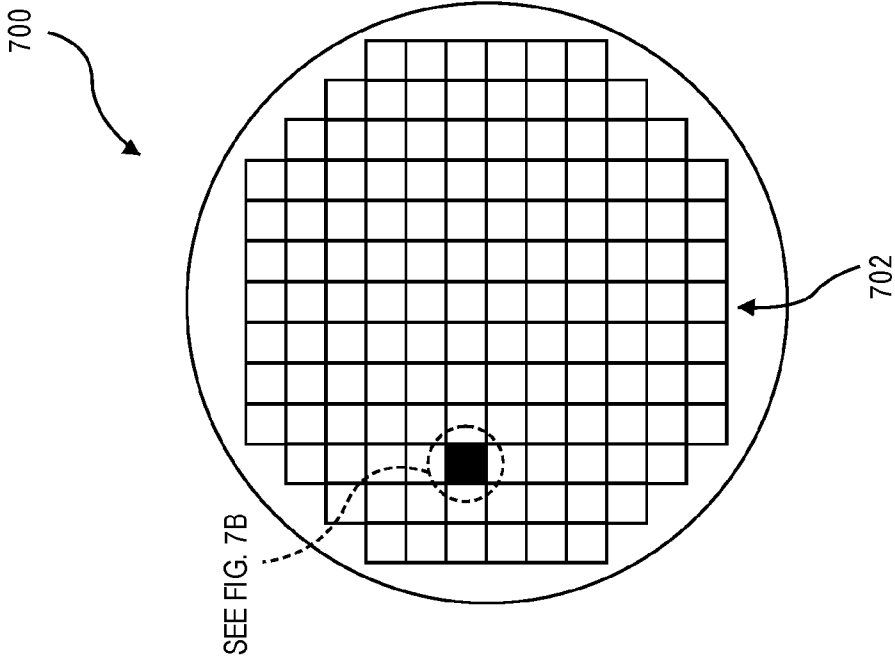
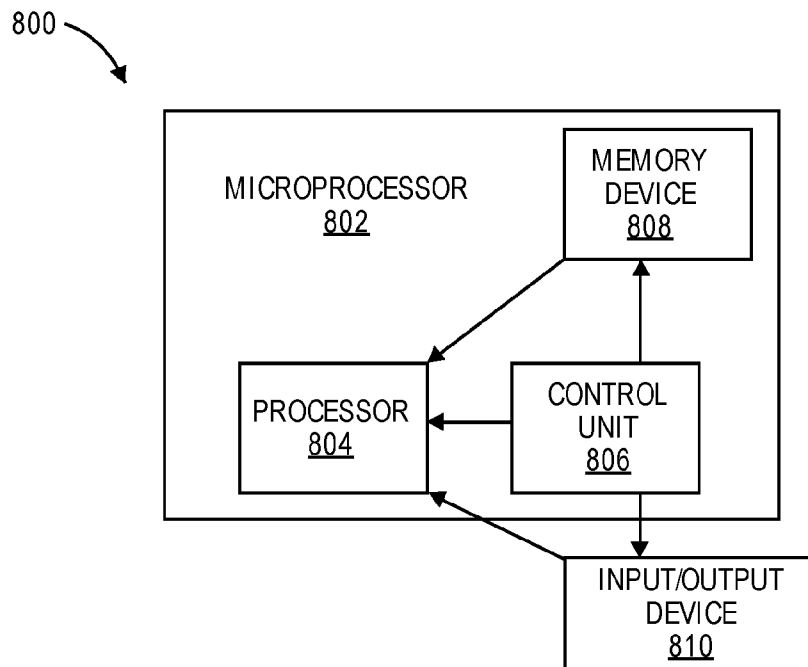
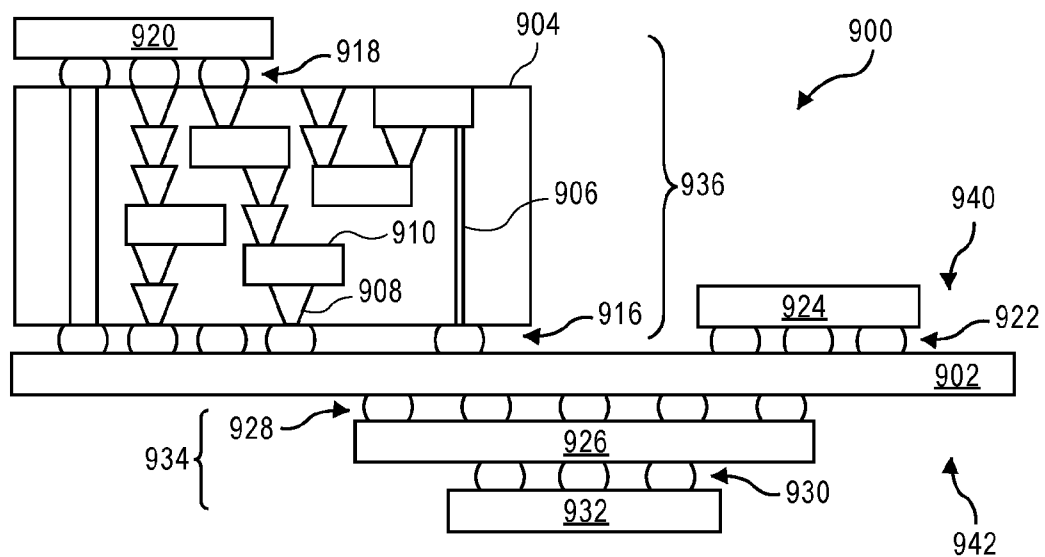


FIG. 7A

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**FIG. 8****FIG. 9**

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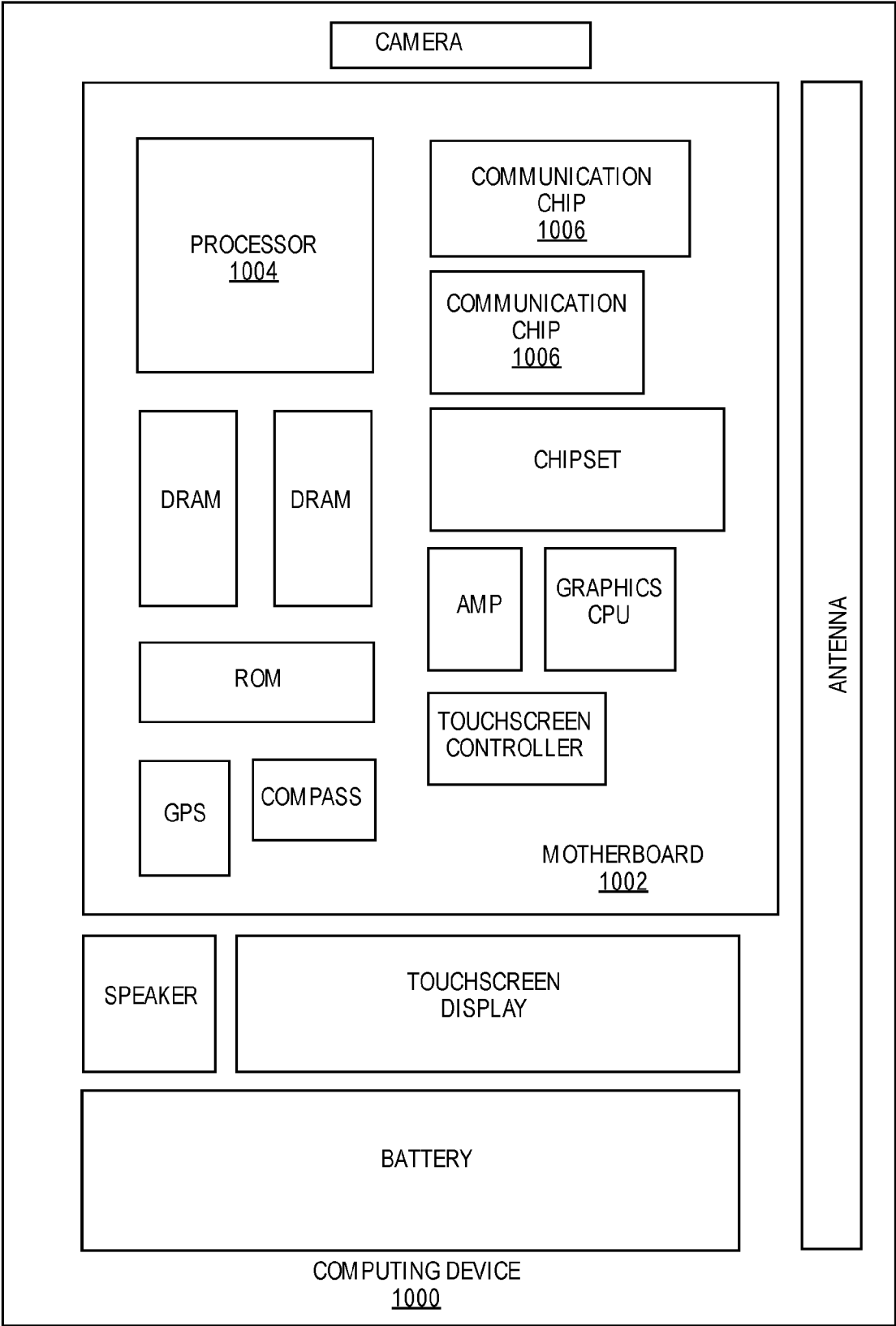


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/038378**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/78(2006.01)i, H01L 29/66(2006.01)i, H01L 29/51(2006.01)i, H01L 27/11585(2017.01)i, H01L 27/11539(2017.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 27/115; H01L 35/24; H01L 21/336; H01L 29/792; H01L 21/02; H01L 29/788; H01L 21/76; H01L 29/66; H01L 29/51; H01L 27/11585; H01L 27/11539

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: non-volatile memory, integrated circuit, gate electrode, ferroelectric, insulator

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2009-0184360 A1 (JIN et al.) 23 July 2009 See paragraphs [0032], [0050]-[0057]; and figures 2, 5-8, 10.	1-25
Y	US 2009-0061538 A1 (HEO et al.) 05 March 2009 See paragraphs [0066]-[0067]; and figure 10.	1-25
A	US 9287283 B2 (LIM et al.) 15 March 2016 See figures 4A-4E.	1-25
A	US 9245898 B2 (SANDISK TECHNOLOGIES INC.) 26 January 2016 See figures 7A-8B.	1-25
A	US 7265376 B2 (GRAHAM et al.) 04 September 2007 See figures 2A-2F.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 February 2018 (22.02.2018)

Date of mailing of the international search report

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Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

KANG, Sung Chul

Telephone No. +82-42-481-8405



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/038378

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