

Dec. 20, 1960

A. A. STERK
TIMER ARRANGEMENT

2,965,843

Filed Dec. 22, 1955

4 Sheets-Sheet 1

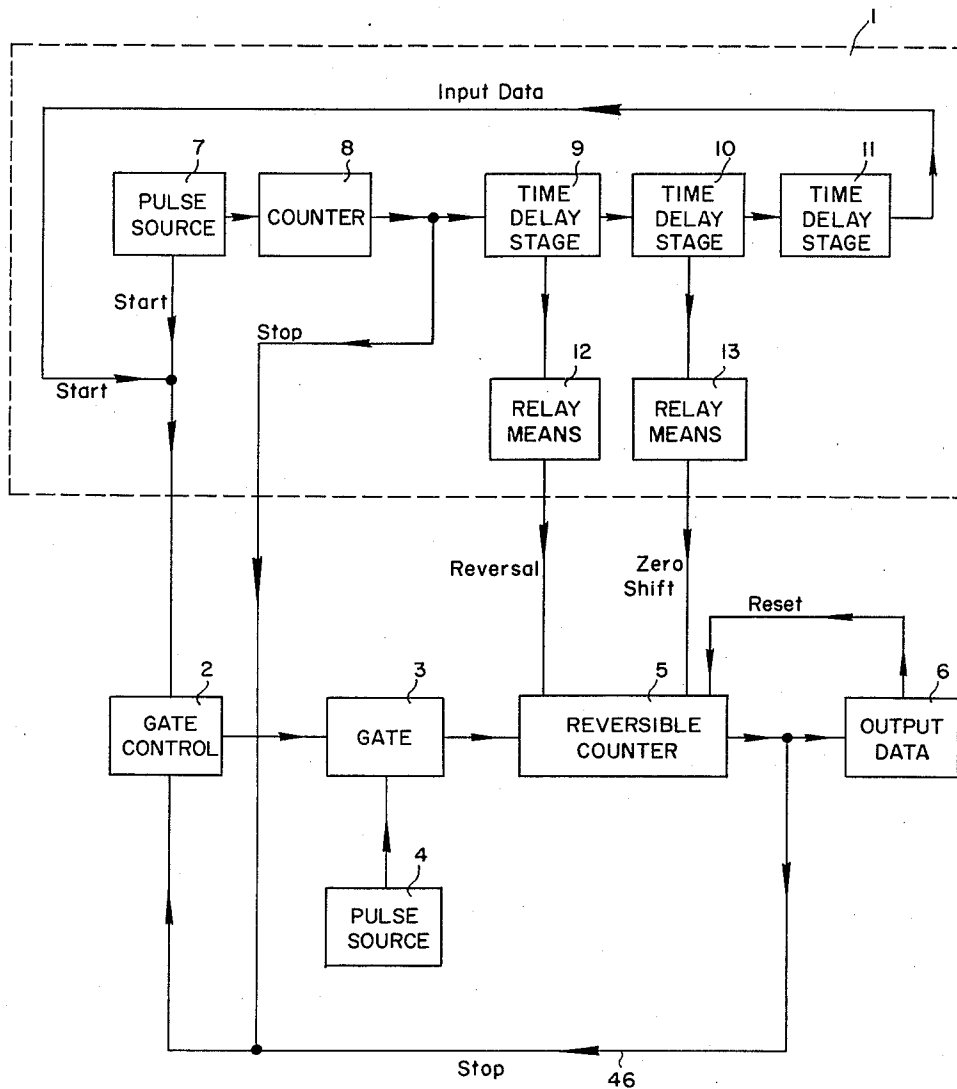


Fig. 1

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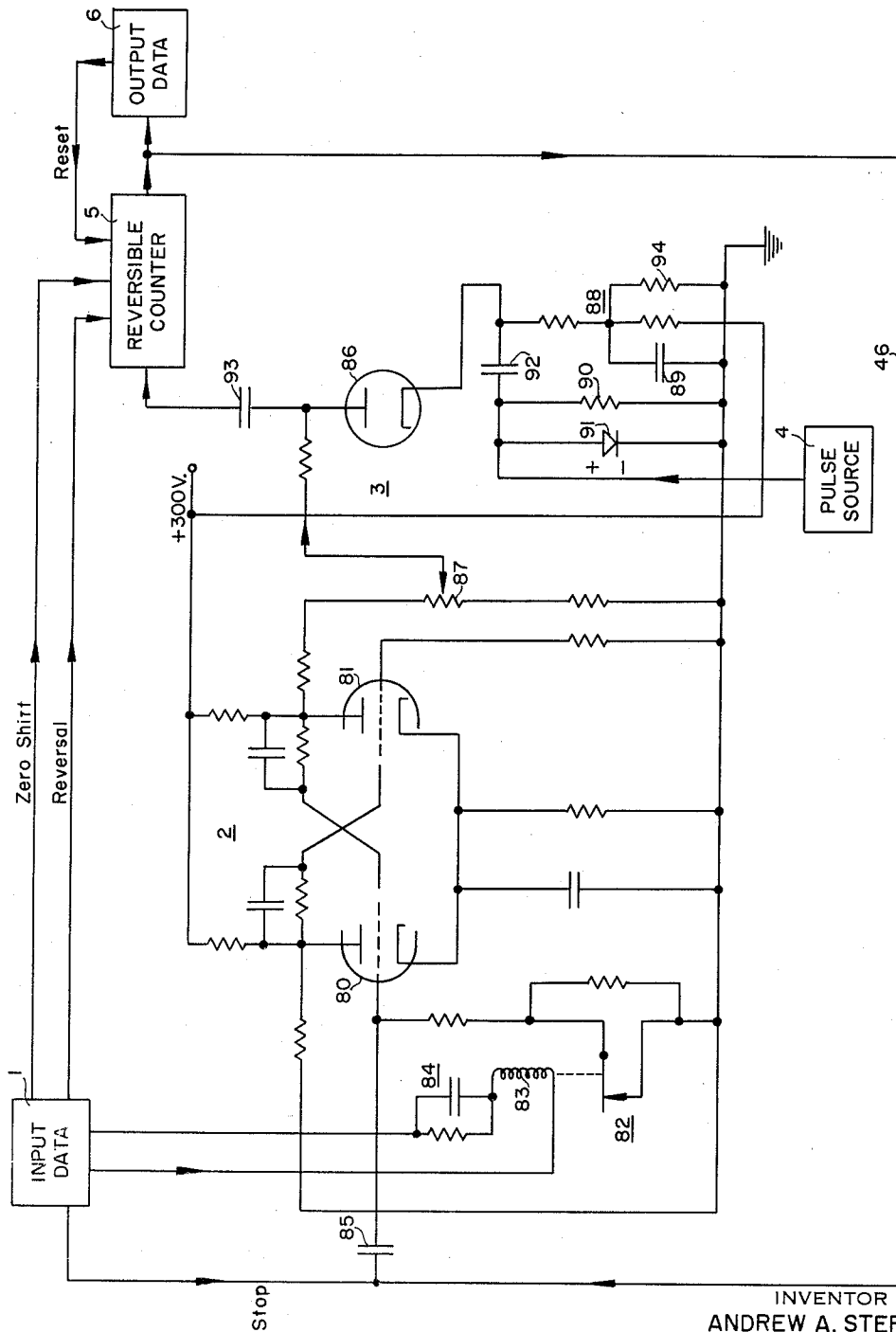
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4 Sheets-Sheet 2



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4 Sheets-Sheet 3

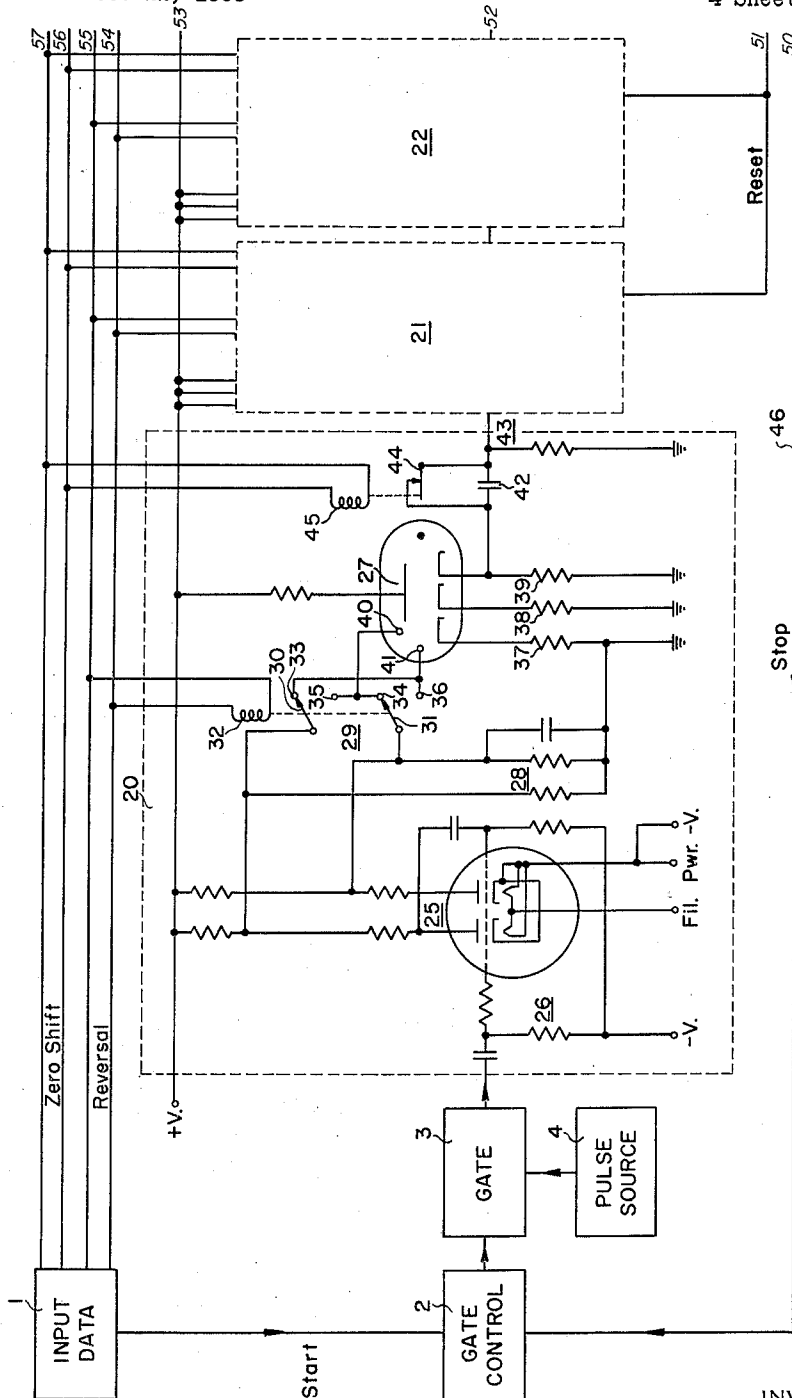


Fig. 3a

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4 Sheets-Sheet 4

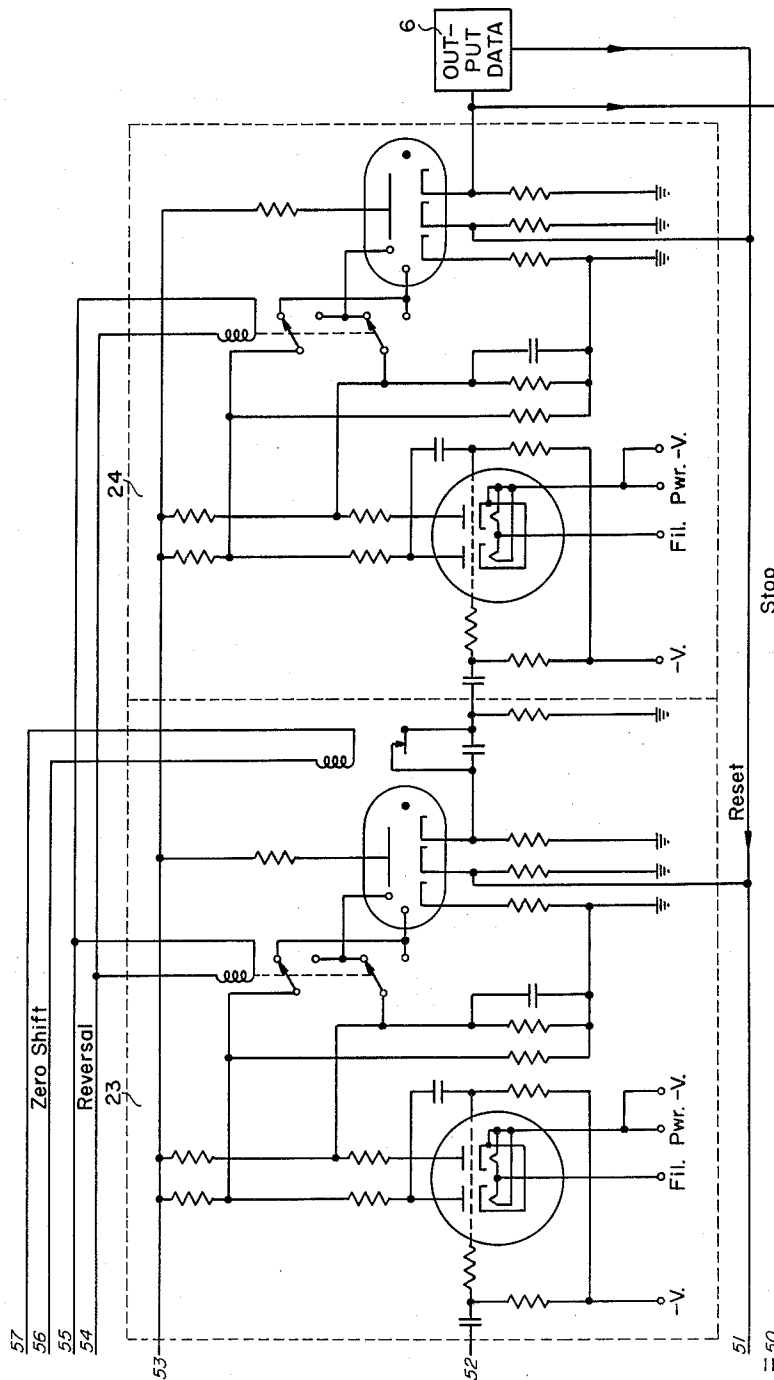


Fig. 3b

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2

2,965,843

TIMER ARRANGEMENT

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13 Claims. (Cl. 324—68)

This invention concerns a timer arrangement and more particularly an electronic timer circuit.

The principal object of this invention is the provision of an electronic timer arrangement for reproducing a time period substantially exactly.

An object of this invention is the provision of an electronic timer arrangement for reproducing a time period to an accuracy within a tenth of a microsecond.

An object of this invention is the provision of an electronic timer arrangement which is highly reliable and efficient in operation.

These and other objects and features of the invention will be apparent from a consideration of the following detailed description taken in connection with the accompanying drawing wherein:

Fig. 1 is a block diagram of the electronic timer arrangement of the present invention;

Fig. 2 is a schematic diagram of the electronic timer arrangement of Fig. 1 partly in block diagram form and partly in circuit schematic form;

Fig. 3a is a schematic diagram of a part of the electronic timer arrangement of Fig. 1 partly in block diagram form and partly in circuit schematic form; and

Fig. 3b is a schematic diagram of the remaining part of the electronic timer arrangement of Fig. 1 partly in block diagram form and partly in circuit schematic form.

In Fig. 1 the timer arrangement of the present invention is shown in block diagram form and comprises a source of input data 1, a gate control 2, a gate 3, a pulse source 4, a reversible counter 5 and a source of output data 6. The input data source 1 is connected to the gate control 2 and the reversible counter 5 and applies start, stop and start input data signals to said gate control and applies reversal and zero shift means actuation signals to said reversible counter in a manner to be described. The gate control 2 is connected to the input data source 1, the gate 3 and the output of the reversible counter 5 and receives start, stop and start input data signals from said input data source, receives stop signals from said reversible counter and applies control signals to said gate in a manner to be described. The gate 3 is connected to the gate control 2, the pulse source 4 and the reversible counter 5 and receives control signals from said gate, receives pulses from said pulse source and applies control signals to said reversible counter in a manner to be described. The pulse source 4 is connected to the gate 3 and applies pulses to said gate in a manner to be described. The reversible counter 5 is connected to the gate 3, the input data source 1, the gate control 2 and the output data source 6 and receives control signals from said gate, receives reversal and zero shift means actuation signals from said input data source, receives reset means actuation signals from said output data source, applies stop signals to said gate control and applies utilizable output data to said output data source in a manner to be described. The output data source 6 is connected to the reversible counter 5 and receives utilizable output data from said reversible counter and

applies reset means actuation signals to said reversible counter in a manner to be described.

The input data source 1 may comprise any suitable source of input data start, stop and start signals and reversal and zero shift means actuating signals. A suitable input data source 1 may comprise, for example, a pulse source 7, a counter 8 connected to said pulse source and actuated by pulses produced by said source, a plurality of time delay stages 9, 10 and 11 connected in the output of said counter, and relay means 12 and 13 connected to the time delay stages 9 and 10, respectively, and actuated to apply a D.C. of suitable magnitude to the reversal and zero shift circuits to actuate the reversal and zero shift means in the reversible counter 5 in suitable sequence. By any of many means known in the art the pulse source 7 of the input data source 1 may be made to produce a start signal, apply it to the gate control 2, to the counter 8 of said input data source 1, and maintain a supply of actuating pulses to said counter for a predetermined period of time. The counter 8 of the input data source 1 may be made to produce a stop signal when it has completed its count for said predetermined period of time and apply it to the gate control 2. The output signal of the counter 8 of the input data source 1 may then be applied through the time delay stages 9, 10 and 11 of said input data source to actuate the relay means 12 for applying a suitable D.C. to the reversal circuit to actuate the reversal means in the reversible counter 5, after a brief time delay; to then actuate the relay means 13 for applying a suitable D.C. to the zero shift circuit to actuate the zero shift means in said reversible counter 5, after a slightly longer time delay; and then, after a longer time delay, to apply itself to the gate control 2 as a start signal.

The pulse source 7, the counter 8, the time delay stages 9, 10 and 11 and the relay stages 12 and 13, of the input data source 1 may comprise any of many suitable circuits known in the art for performing their prescribed functions. The gate control 2, the gate 3, the pulse source 4 and the output data source 6 of the electronic timer arrangement of the present invention may also comprise any of many suitable circuits known in the art for performing their prescribed functions.

The pulse sources 4 and 7 may comprise, for example, a tuning fork, suitable electronic pulse generator, or source of X-ray radiations capable of producing a series of pulses of proper phase, frequency, shape and polarity to enable proper operation of the gate control 2 and the gate 3. The counter 8 may comprise, for example, a suitable decade counter of a type known in the art. The time delay stages 9, 10 and 11 may comprise, for example, suitable delay networks of known type. The relay means 12 and 13 may comprise, for example, suitable relays of known type which are normally open and close under the influence of a current flow through their energizing coils. The gate control 2 may comprise, for example, a bistable multivibrator, of a type known in the art, which is able to produce output signals to open the gate 3 under the control of an input start signal from the pulse source 7, to then close the gate 3 under the control of an input stop signal from the pulse source 7, to open the gate 3 again under the control of an input start signal from the time delay stage 11, and to close the gate 3 again under the control of an input stop signal from the reversible counter 5. The gate 3 may comprise, for example, a diode gating circuit, of known type, which is able to open under the control of an "open" signal from the gate control 2 and to close under the control of a "close" signal from the gate control 2. The output data source 6 may comprise, for example, suitable utilization means such as a printing converter and printer combination of a type known in the art.

The reversible counter stage 5 may comprise any suitable device responsive to external control such as, for example, a decade counter responsive to control by pulses produced by the pulse source 4.

Fig. 2 is a schematic diagram of the electronic timer arrangement of Fig. 1 partly in block diagram form and partly in circuit schematic form. Corresponding components of Figs. 1 and 2 are indicated by the same reference numerals. The gate control 2 may comprise a bistable multivibrator of known type and the gate 3 may comprise a diode gate of known type; a suitable gate control and gate circuit are shown in Fig. 2. The operation of the gate control and gate circuits of Figs. 1 and 2 to permit the application of pulses from the pulse source 4 to the reversible counter 5 upon the receipt of a start signal by the gate control 2 from the input data source 1 and to prevent the application of pulses from the pulse source 4 to the reversible counter 5 upon the receipt of a stop signal by the gate control 2 from the input data source 1, or from the reversible counter 5, is obvious and in accordance with the usual operation of such circuits.

Initially, the grids of multivibrator tubes 80 and 81 are at a potential such that the tube 80 is cut-off. In the initial condition of the circuit, a relay switch 82 is closed and a relay coil 83 is unenergized. An RC circuit 84 in the input line from the input data source 1 to the relay coil 83 effects a differentiating action to energize said relay coil momentarily, although the current from said input data source may be continuous. Thus, the application of a "start" signal from the input data source 1 produces a current flow in the circuit of the relay coil 83 which energizes said relay momentarily, under the influence of said current, due to the operation of the RC circuit 84. The energization of the relay coil 83 opens the relay switch 82 to release the initial potential across the grid of the tube 80 so that said tube conducts.

The application of a "stop" signal, which is preferably a negative pulse, from either the input data source 1 or the output of the reversible counter 5, through a capacitor 85 to the grid of the tube 80 cuts-off said tube. When the tube 80 is cut-off by the "stop" signal, the tube 81 conducts, and the multivibrator circuit 2 is back in its initial position.

Initially, the cathode of gate diode 86 is at a positive D.C. voltage and the anode of said diode is at a D.C. voltage derived from a potentiometer 87 connected in the output of the multivibrator circuit 2. In the initial condition of the circuit, the tube 80 of the multivibrator is cut-off and the voltage on the anode of the diode 86 is less positive than the voltage on the cathode of said diode, so that said diode is cut-off. When a "start" signal, applied from the input data source 1, causes the tube 80 of the multivibrator to conduct, the voltage on the anode of the diode 86 is more positive than the voltage on the cathode of said diode, and said diode conducts.

Thus, when a "start" signal is applied to the multivibrator 2, the diode 86 of the gate 3 conducts and said gate is open to permit the application of pulses from the pulse source 4 to the reversible counter 5; when a "stop" signal is applied to said multivibrator, said diode cuts-off and said gate is closed to prevent the application of pulses from said pulse source to said reversible counter.

A voltage divider 88 connected in the cathode circuit of the diode 86 aids in the establishment of a suitable voltage for application to the cathode of said diode. A capacitor 89, coupling the voltage divider 88 to ground, provides a high frequency by-pass to ground. A resistor 90, between the pulse source output and ground, aids in the establishment of a D.C. voltage level, and a rectifier 91, in parallel connection with said resistor, prevents the application of positive pulses from the multivibrator circuit to said cathode. Pulses from the pulse source 4 are applied to the cathode of the diode 86 through a

series connected capacitor 92, and from the anode of said diode to the reversible counter 5 through a series connected capacitor 93.

The operation of the electronic timer arrangement of the present invention may best be described in conjunction with Figs. 3a and 3b, which together comprise a schematic diagram of the electronic timer arrangement of Fig. 1 partly in block diagram form and partly in circuit schematic form.

In Figs. 3a and 3b the reversible counter 5 is shown in a preferred embodiment. Although a five stage reversible counter is shown, a single stage, two stages, three stages, four stages, six stages, or an even greater number of stages may be utilized as a suitable reversible counter. Corresponding components of Figs. 1, 2, 3a and 3b are indicated by the same reference numerals.

The counter stages 20, 21, 22, 23 and 24 are connected in series circuit arrangement between the output of the gate 3 and the input of the output data source 6. The counter stages 20, 21, 22, 23 and 24 are essentially similar to each other except for the provision of reset means for the stages 21, 22, 23 and 24 and the provision of zero shift means for the stages 20, 21, 22 and 23.

Each counter stage 20, 21, 22, 23 and 24 comprises a pulse shaping stage, labeled 25 in stage 20, a coupling connection between the pulse shaping stage and the output of the next preceding stage, labeled 26 in stage 20, a counter tube, labeled 27 in stage 20, a coupling connection between the pulse shaping stage and the counter tube, labeled 28 in stage 20, and reversal means, labeled 29 in stage 20.

In accordance with the present invention, the gate 3 opens, under the control of the input data source 1, to permit the application of a series of pulses from the pulse source 4 to the reversible counter 5, to direct said counter from an initial condition or count position, by uniform control, to a resultant condition or count position; the gate 3 then closes, under the direction of the input data source 1, to permit the energization of specified components of the reversible counter 5 by the input data source 1 and opens, under the direction of the input data source 1, to permit the application of a series of pulses from the pulse source 4 to said counter, to redirect said counter from said resultant condition, by said uniform control, to said initial condition; and the gate 3 then closes, under the direction of the reversible counter 5, to prevent the application of pulses to said counter from the pulse source 4 when said counter reaches said initial condition, thereby producing data at the output data source 6 which is an exact reproduction of the time period determined by said input data source.

The control of the counting direction of the counter tubes from an initial position to a resultant position and then back from the resultant position to the initial position may be effected at any suitable point in the timer circuit. The pulse source 4 may control the counter tubes by varying its produced pulses in a suitable manner, such as by varying the phase, frequency, amplitude, shape or polarity of said pulses, dependent upon the type of counter tubes utilized. The counter tube of each counter stage may also be controlled by varying the pulses in a similar manner, at a point in the circuit between the next preceding counter stage and the pulse shaping stage, or at a point between the pulse shaping stage and the counter tube. In the preferred embodiment of the invention, the counter tubes are controlled in counting direction by phase variation of the pulses applied to them at a point between the pulse shaping stage and the counter tube of each counter stage.

The pulse shaping stage 25 of each counter stage may comprise any suitable means for applying pulses of proper phase, frequency, shape or polarity to the counter tube

27 to control said tube. Furthermore, the pulse shaping stage should produce an output pulse which may be varied in phase in order to control the counting direction of the counter tube. The pulse shaping stage of each counter stage of the preferred embodiment of the invention, produces a phase-displaced dual output pulse of proper amplitude and shape for direction control of the counter tube which may be readily reversed in phase; the signal on one plate of the dual triode tube being phase-displaced from the signal on the other plate of said triode tube. Suitable plate and grid biasing potentials are provided as well as suitable filament power, to operate the dual triode pulse shaping stage in a suitable manner.

The coupling connection 26 between each pulse shaping stage and the next preceding stage and the coupling connection 28 between each pulse shaping stage and the counter tube 27 may comprise any suitable coupling for transmitting pulses. The coupling connections 26 and 28 of Fig. 3 are conventional RC networks.

Although the phase reversing means 29 included in the coupling connection 28 to each counter tube may comprise any suitable pulse varying means for controlling the counting direction of each counter tube, depending upon the type of said tube used in the circuit, in the preferred embodiment of the invention said means comprises phase reversing means. The phase reversing means 29 of each counter stage may comprise, for example, a double throw switch having contact arms 30 and 31 which are controlled as a unit by a reversing relay 32.

The reversing relay 32 of each counter stage is energized by a direct current at a predetermined point in the operation of the timer arrangement determined by the input data source 1, to throw the contact arms 30 and 31 to their other position and thereby reverse the phase of the pulses applied to each counter tube. The phase reversing switch of each counter stage may be so connected in the timer arrangement that when the reversing relay 32 is unenergized the contact arms 30 and 31 close with contacts 33 and 34, respectively, to apply a series of pulses of suitable phase to direct the counter tube 27 to count in a predetermined direction, and when the relay 32 is energized the contact arms 30 and 31 are thrown to close with contacts 35 and 36, respectively, to apply a series of pulses of reversed phase to direct the counter tube to count in a direction opposite to said predetermined direction.

The counter tube of each counter stage may comprise any suitable means responsive to being directed from an initial condition by uniform control to a resultant condition and to being redirected from said resultant condition by said uniform control to said initial condition. The counter tube may comprise, for example, any suitable counter tube capable of counting in either direction; that is, from an initial position or condition backward to a resultant position or condition, and from said resultant position forward to said initial position. A suitable counter tube 27 may comprise, for example, a beam switching tube of the magnetron type which is capable of counting in either direction and which may be closely controlled. The counter tube of each counter stage of the preferred embodiment of the invention may comprise a tube which has a counting direction determined by the phase of the pulses applied to it. Such a tube may comprise a gas-filled, multielectrode cold cathode tube which operates on the principle that the ionization of the gas around the cathode of a gas-discharge tube will lower the striking potential to an adjacent cathode. The counter tube may comprise a central anode connected through a load resistor to a positive bias potential and a plurality of counter cathodes arranged symmetrically around it and connected independently to ground. In order to clarify the presentation of the timer arrangement of the present invention only three cathodes 37, 38 and 39, of the plurality of cathodes which may be part of each counter

tube are shown for each counter tube in Figs. 3a and 3b. The counter tube may comprise guide pins or electrodes 40 and 41 positioned between the counter cathodes. Since all the cathodes have similar characteristics, the burning potential to a glowing cathode will be lower than the striking potential to any other cathode. Because of the partially ionized gas in the region, the striking potential from the anode to the two cathodes adjacent to the glowing one will be less than the more distant ones. The guide pins 40 and 41 are utilized to transmit glow in the proper direction from one counting cathode to another, thereby permitting the tube to count in either a forward or a backward direction in accordance with the phase of the pulses applied to said guide pins.

Each of the counter stages except stage 20 includes reset means for resetting the counter tube of each said stage to a predetermined position at the completion of the operation of the timer arrangement. The counter tube of each of the counter stages may be reset in a conventional manner, which may comprise applying a negative pulse from the output data source 6 to the cathode to which the tube is to be reset. In the embodiment of Figs. 3a and 3b, the reset means are controlled by the output data source 6 to reset the counter stages 21, 22, 23 and 24 to predetermined positions at the completion of the operation. In the preferred operation of the embodiment of Figs. 3a and 3b the counter tube 27 of the counter stage 20 is set to zero and the counter tube of each of the counter stages 21, 22, 23 and 24 is set and reset to position number nine.

The counter stages 20, 21, 22 and 23 further include zero shift means for shifting the counter tube of any of the stages 21, 22, 23 and 24 one step in the forward direction upon the occurrence of a zero resultant position in the next preceding counter tube. The zero shift pulse is produced by a counter stage in three situations; when the resultant position of the next preceding counter stage after the backward counting sequence is zero, when the resultant position of the next preceding counter stage becomes zero due to a single zero shift or carry pulse from the counter stage next preceding said next preceding counter stage, and when the counter stage is shifted from zero to one by a carry pulse from the next preceding stage. The zero shift means of each of the counter stages 20, 21, 22 and 23 may be any suitable means for applying a forward stepping pulse to a counter tube when the next preceding counter tube is at a zero resultant position at the completion of the first portion of the operation. A suitable zero shift means may comprise, for example a relay controlled capacitor discharge circuit. The zero shift means of the embodiment of Figs. 3a and 3b is identical for each of the counter stages 20, 21, 22 and 23 and comprises a capacitor, labeled 42 in stage 20, connected in series between the output of each counter stage, except the last, and the input of the next succeeding counter stage, said capacitor forming a part of a coupling connection, labeled 43 in stage 20, between stages. The capacitor 42 is short-circuited by an arm, labeled 44 in stage 20, of a zero shift relay, labeled 45 in stage 20. At the completion of the second portion of the operation, the capacitor 42 is short-circuited and said capacitor will not be charged. If the preceding counter stage is at the zero resultant position the capacitor 42 is charged with a positive voltage, since after the completion of the count the cathode at which the counter tube is positioned has a positive potential on it. The zero shift relay arm 44 short-circuits the capacitor 42 as long as the zero shift relay 45 is unenergized. When the zero shift relay 45 is energized, the arm 44 opens the short-circuit around the capacitor 42 and, if the cathode, labeled 39 in stage 20, has a positive voltage on it, said capacitor will charge; if the cathode 39 has no voltage on it, said capacitor will not charge. The zero shift relay 45 is then deenergized and the capacitor 42 discharges to

apply a single pulse to the next succeeding counter stage, thereby stepping the counter tube of said next counter stage forward one position. The zero shift relay of each of the counter stages 20, 21, 22 and 23, is energized by a direct current at a predetermined point in the operation of the timer arrangement to open and close the short-circuit around each capacitor 42 and thereby effect the application of a forward stepping pulse to the next succeeding counter stage under the conditions set forth.

The timer arrangement of the present invention, as shown in Figs. 1, 2 and 3, operates to reproduce a time period substantially exactly. In the first portion of the operation of the timer arrangement of the present invention the pulse source 7 of the input data source 1 produces a start signal which is applied to the counter 8 of said input data source to start its counting operation and which is also applied to the gate control 2 to direct said gate control to open the gate 3. The application of an "open" signal from the gate control 2 to the gate 3 opens said gate to permit the application of a series of pulses to the reversible counter 5 from the pulse source 4. This series of pulses is applied through the gate 3, the coupling connection 26, the pulse shaping stage 25, the coupling connection 28, the switch contact arms 30 and 31 and the switch contacts 33 and 34 of the phase reversing means 29 to the guide pins 41 and 40 of the counter tube 27, the short circuit arm 44, and the coupling connection 43 of the first counter stage 20. This series of pulses is then applied to the succeeding counter stages 21, 22, 23 and 24 in a similar manner. The pulses of this series of pulses have a phase-displacement which directs the counter tube of each counter stage to count in a backward direction from the initial position for a period of time determined by the input data source 1.

The initial position of the counter tube 27 of the counter stage 20 is set to the zero position, and the initial position of the counter tube of each of the counter stages 21, 22, 23 and 24 is set and reset to the position number nine. The counter tubes utilized in the timer arrangement are preferably of a type that produces an output pulse for each counting cycle of the tube from the zero position through the plurality of positions, preferably nine, back to zero. Thus, the greater the number of counter stages connected in the embodiment of Figs. 3a and 3b, the longer the time period that may be exactly reproduced. In the preferred embodiment of Figs. 3a and 3b, for example, 3000 pulses direct the counter stage 20 to complete 300 counting cycles, the counter stage 21 to complete 30 counting cycles, the counter stage 22 to complete 3 counting cycles, the counter stage 23 to step three positions and the counter stage 24 to remain unaffected.

When the counter 8 of the input data source 1 completes its predetermined count it produces an output signal which is applied to the gate control 2 to direct said gate control to close the gate 3 and which is also applied to the time delay stages 9, 10 and 11. The application of a "close" signal from the gate control 2 to the gate 3 closes said gate to prevent the application of pulses to the reversible counter 5 from the pulse source 4 and completes the first portion of the operation of the timer arrangement.

The application of an output signal to the time delay stages 9, 10 and 11 of the input data source 1 initiates the second portion of the operation of the timer arrangement of the present invention. At the initiation of the second portion of the operation, the backward count, which is of a magnitude determined by the predetermined time period of the input data source 1, is completed. The counter tubes of the counter stages are at the resultant positions and the application of pulses from the pulse source 4 to the counter stages is prevented. The output signal of the counter 8 is applied to the time delay stage 9 where it is delayed for a brief period by said time delay

stage and is applied to the relay means 12. The relay means 12 is actuated by the delayed output signal of the counter 8 to apply sufficient current to the reversing relay of each of the counter stages 20, 21, 22, 23 and 24 to energize the reversing relay of each said counter stage. Energization of the reversing relays 32 throws the switch arms 30 and 31 to the contacts 35 and 36, respectively, thereby reversing the phases of the pulses in said arms. Any following series of pulses produced by the pulse source 4 will then be applied to the guide pins of the counter tubes in a reverse phase from that of the pulses in the first portion of the operation. Thus, for example, if, when the switch arms are closed to contacts 33 and 34, the pulses applied to the guide pin 40 and the pulses applied to the guide pin 41 are so displaced in phase that the pulses applied to the pin 40 lead the pulses applied to the pin 41 so that the counter tube 27 counts in one direction, then when the switch arms are closed to contacts 35 and 36, the pulses applied to the guide pin 40 and the pulses applied to the guide pin 41 are phase reversed so that the pulses applied to the pin 41 lead the pulses applied to the pin 40 and the counter tube 27 counts in the opposite direction. The phase-displacement is such that the first counting direction is backward from the initial position and the second counting direction is forward from the resultant position. The output signal of the counter 8 is then applied to the time delay stage 10 where it is delayed for a brief period by said time delay stage and applied to the relay means 13. The relay means 13 is actuated by the delayed output signal of the counter 8 to apply sufficient current to the zero shift relay of each of the counter stages 20, 21, 22 and 23 to energize the zero shift relay of each said counter stage. Energization of the zero shift relays directs each counter tube, the next preceding counter tube to which is at zero resultant position, to count one step forward.

The output signal of the counter 8 is then applied to the time delay stage 11 where it is delayed for a period by said time delay stage and then applied to the input of the gate control 2 to complete the second portion of the operation of the timer arrangement and initiate the third portion of said operation. At the initiation of the third portion of the operation, the counter tube of each of the counter stages is conditioned to count in a forward direction from the resultant position, due to the energization, in the second portion of the operation, of the reversing relays. The application of the time delayed output signal of the counter 8 of the input data source 1 to the gate control 2 directs said gate control to apply said signal to the gate 3 to open said gate to permit the application of a series of pulses to the reversible counter 5 from the pulse source 4. This series of pulses is applied to the counter stages and directs the counter tube of each counter stage to count in a forward direction from the resultant position. The counter tubes count in the forward direction until the counter tube of the last actuated counter stage reaches its initial position. At such time, the last actuated counter tube produces an output signal which is applied through a connection 46 to the gate control 2, thereby directing said gate control to close the gate 3. The application of a "close" signal from the gate control 2 to the gate 3 closes said gate to prevent the application of pulses to the reversible counter 5 from the pulse source 4 and completes the third portion of the operation of the timer arrangement.

The output signal of the last actuated counter tube of the reversible counter 5 is also applied to the output data source 6 for utilization of the data indicating the reproduced time period determined by the input data source 1. Said output signal also actuates means in the output data source 6 for resetting the counter tubes of the last four stages of the timer arrangement to their number nine positions.

Since the counting direction of the counter tubes involves uniform control, the period of time it takes said tubes to count backward from the initial position of each tube to the resultant position of each tube is exactly the same as the period of time it takes said tubes to count forward from the resultant position of each tube to the initial position of each tube.

The operation of the timer arrangement embodiment of Figs. 3a and 3b may be illustrated by examples. We may assume that the time period of the first portion of the operation is so determined by the input data that 3 5 7 2 3 pulses are applied to the counter tube 27, and through it to the succeeding counter tubes, before the gate control 2 prevents the application of pulses to said tubes in accordance with the input data from the source 1 and initiates the reversal of the counting direction of the counter tubes. In this case each tube counts backward from the initial position, which is zero position for the counter tube 27 and number nine position for the counter tubes of the counter stages 21, 22, 23 and 24, to the resultant position. The resultant positions are thus

$$\begin{array}{r} 99990 \\ - 35723 \\ \hline 64277 \end{array}$$

which is so determined by subtracting unit from unit, without carryovers; 7 being the resultant position of counter tube 27, 7 being the resultant position of the counter tube of stage 21, 2 being the resultant position of the counter tube of the stage 22, 4 being the resultant position of the counter tube of the stage 23, and 6 being the resultant position of the counter tube of the stage 24.

The gate control 2 then permits the application of pulses to the counter tubes and each counter tube counts forward from the resultant position. When each tube reaches the initial position the tube of the counter stage 24 produces an output signal which prevents the application of further pulses to the counter tubes and at the same time causes the supply of output data indicating the reproduced time period to the output data source 6 where it may be utilized.

$$\begin{array}{r} 64277 \\ + 35723 \\ \hline 100000 \end{array}$$

Thus the counter tubes, in counting forward, substantially exactly duplicate the period of time required for them to count backward.

In another example, we may assume that the time period of the first portion of the operation is so determined by the input data that 1 9 0 pulses are applied to the counter tube 27. After backward counting, the resultant positions of the counter tubes are

$$\begin{array}{r} 99990 \\ - 190 \\ \hline 99700 \end{array}$$

The difference of 9 9 9 9 0 and 1 9 0 is 9 9 7 0 0 because, in the counter tube of counter stage 21 when nine is subtracted from nine the resultant is zero, and when there is a zero resultant a single pulse is produced and applied to the counter tube of the next succeeding counter stage 22. Thus, the single carry pulse applied to the counter tube of counter stage 22 effectively changes the subtraction of one from nine to a subtraction of two from nine to produce a resultant of seven. The sum of 9 9 7 0 0 and 1 9 0 is 9 9 8 9 0, which is insufficient to direct the counter tube of the counter stage 24 to produce an output pulse to direct the gate control 2 to prevent the application of pulses to the counting stage 20. To remedy this deficiency, in order to produce

proper operation of the timer arrangement, the gate control 2 energizes the zero shift relays during the second portion of the operation. In the second portion of the operation, after the gate control 2 prevents the application of pulses to the counter tubes, the reversal relays are energized, and the zero shift relays are energized to add a single step in the forward direction to each counter tube which next succeeds a counter tube which is at the zero resultant position. Therefore, at resultant positions 9 9 7 0 0, the counter tube 27 remains at the zero position and applies, through its zero shift relay, a single pulse to its next succeeding counter tube (of stage 21), so that the counter tube of stage 21 counts forward one step from the zero resultant position to the number one resultant position. The counter tube of stage 21 applies a single pulse to the next succeeding counter tube (of stage 22), because the counter tube of stage 21 was at the zero resultant position before the zero shift carry pulse from the counter tube 27 was applied to it. The counter tube of counter stage 22 is therefore shifted from the seven to the eight resultant position and the next succeeding counter tubes (of stages 23 and 24) remain respectively at the nine and nine resultant positions. Thus 9 9 8 1 0 are the resultant positions of the counter tubes before commencement of the third portion of the operation. The zero shift or carry pulses are sequentially applied to the counter tubes in the sequential order of counter stages 27, 21, 22, 23 and 24.

In the third portion of the operation the gate control 2 permits the application of pulses to the counter tubes, which count forward from the resultant positions 9 9 8 1 0. When each counter tube reaches the initial position the counter tube of counter stage 24 produces an output signal which prevents the application of further pulses to the counter tubes and at the same time causes the supply of output data indicating the reproduced time period to the output data source 6, where it may be utilized.

$$\begin{array}{r} 99810 \\ + 190 \\ \hline 100000 \end{array}$$

Thus the counter tubes, in counting forward, exactly duplicate the period of time required for them to count backward.

The timer arrangement of the present invention is especially suitable for use in radiation counting systems where very large numbers of pulses are produced in short time intervals. The time period which may be reproduced increases in magnitude with the number of counting stages utilized in the timer arrangement. The accuracy of reproduction of the time period increases with the frequency of production of pulses by the pulse source 4.

It is to be understood that the invention is not limited to the details disclosed but includes all such variations and modifications as fall within the spirit of the invention and the scope of the appended claims.

Having thus set forth the nature of my invention, what I claim is:

1. A circuit arrangement for reproducing a fixed time interval comprising a pulse counting device, a source of input data, control means connected to said device and to said source comprising pulse means for directing said device to count from an initial condition to a resultant condition for a period of time determined by input data from said source, pulse means for directing said device to count from said resultant condition back to said initial condition and means for stopping said control means at said initial condition whereby said period of time determined by said input data is exactly reproduced, and means for deriving data indicating said reproduced time period from said device.

2. A circuit arrangement for reproducing a fixed time

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interval comprising a pulse counting tube, a source of input data, control means connected to said tube and to said source comprising pulse means for directing said tube to count from an initial position to a resultant position for a period of time determined by input data from said source, pulse means for directing said tube to count from said resultant position back to said initial position and means for stopping said control means at said initial position whereby said period of time determined by said input data is exactly reproduced, and means for deriving data indicating said reproduced time period from said tube.

3. A circuit arrangement for reproducing a fixed time interval comprising a pulse counting tube having a plurality of electrodes, a source of input data, control means connected to said tube and to said source comprising means for applying a number of pulses of predetermined phase-displacement to selected ones of said electrodes thereby to direct said tube to count from an initial position in a predetermined direction to a resultant position, said number of pulses being determined by input data from said source, means for applying a series of pulses of reversed phase from said predetermined phase-displacement to said selected ones of said electrodes thereby to direct said tube to count from said resultant position in a direction opposite to said predetermined direction and means for stopping the application of pulses to said selected ones of said electrodes when said tube reaches said initial position whereby the time equivalent of said number of pulses determined by said input data is exactly reproduced, and means for deriving said reproduced time equivalent data from a selected electrode of said tube.

4. A circuit arrangement for reproducing a fixed time interval comprising a plurality of pulse counting tubes in series connection each having a plurality of electrodes, a source of input data, control means connected to the first of said tubes and to said source comprising means for applying a number of pulses of predetermined phase-displacement to selected ones of the electrodes of the first of said tubes thereby to direct said tubes to count from initial positions in a predetermined direction to resultant positions, said number of pulses being determined by input data from said source, means for applying a series of pulses of reversed phase from said predetermined phase-displacement to said selected ones of said electrodes thereby to direct said tubes to count from said resultant positions in a direction opposite to said predetermined direction and means for stopping the application of pulses to said selected ones of said electrodes when said tubes reach said initial positions whereby the time equivalent of said number of pulses determined by said input data is exactly reproduced, and means for deriving said reproduced time equivalent data from a selected electrode of the last of said tubes.

5. A circuit arrangement for reproducing a fixed time interval comprising a source of input data, a pulse source, control means connected to said sources comprising means for controlling the number of pulses derived from said pulse source in accordance with input data from said source of input data, pulse shaping means coupled to said control means for controlling the phase-displacement of the pulses derived from said control means, a pulse counting tube having a plurality of electrodes, coupling means coupling said pulse shaping means to selected ones of said electrodes for applying a number of pulses of predetermined phase-displacement to said selected ones of said electrodes thereby to direct said tube to count from an initial position in a predetermined direction to a resultant position, said number of pulses being determined by input data from said source of input data, and for applying a series of pulses of reversed phase from said predetermined phase-displacement to said selected ones of said electrodes in accordance with a signal from said control means thereby to direct said tube to count from said resultant position in a direction opposite to

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said predetermined direction, said coupling means comprising switching means and relay means energized by a signal from said control means for reversing said switching means, means connecting a selected one of said electrodes to said control means, said control means further comprising means for stopping the pulses derived from said pulse source in accordance with a signal from said selected one of said electrodes when said tube reaches said initial position whereby the time equivalent of the said number of pulses determined in accordance with said input data is exactly reproduced, and means for deriving said reproduced time equivalent data from said selected one of said electrodes.

6. A circuit arrangement as claimed in claim 5, wherein said initial position is the zero position of said tube.

7. A circuit arrangement for reproducing a fixed time interval comprising a source of input data, a pulse source, control means connected to said sources comprising means for controlling the number of pulses derived from said pulse source in accordance with input data from said source of input data, a plurality of counting stages in series circuit arrangement connected in series with said control means each comprising pulse shaping means for controlling the phase-displacement of the pulses derived from said control means, a pulse counting tube having a plurality of electrodes and coupling means coupling said pulse shaping means to selected ones of said electrodes for applying a number of pulses of predetermined phase-displacement to said selected ones of said electrodes thereby to direct said tube to count from an initial position in a predetermined direction to a resultant position, said number of pulses being determined by input data from said source of input data, and for applying a series of pulses of reversed phase from said predetermined phase-displacement to selected ones of said electrodes in accordance with a signal from said control means thereby to direct said tube to count from said resultant position in a direction opposite to said predetermined direction, said coupling means comprising switching means and relay means energized by a signal from said source of input data for reversing said switching means, means connecting a selected one of the electrodes of the pulse counting tube of the last of said counting stages to said control means, said control means further comprising means for stopping the pulses derived from said pulse source in accordance with a signal from said selected one of said electrodes when each said pulse counting tube reaches said initial position whereby the time equivalent of the said number of pulses determined in accordance with said input data is exactly reproduced, and means for deriving said reproduced time equivalent data from said selected one of said electrodes.

8. A circuit arrangement as claimed in claim 7, wherein the initial position of the pulse counting tube of the first of said counting stages is the zero position of said tube.

9. A circuit arrangement as claimed in claim 8, further comprising means energized by said signal from said selected one of said electrodes for resetting the pulse counting tube of each of said counting stages except said first of said counting stages to an initial position, each said initial position being the number nine position of each said tube.

10. A circuit arrangement as claimed in claim 9, further comprising means energized by a signal from said source of input data for applying a pulse of predetermined phase-displacement to said selected ones of said electrodes of the pulse counting tube of each of said counting stages except the last of said counting stages thereby to direct each said tube to count one position from said resultant position in a direction opposite to said predetermined direction upon the occurrence of a zero position resultant position in the pulse counting tube of the next preceding counting stage.

11. A circuit arrangement for reproducing a fixed

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time interval comprising a counting device, a source of input data and control means connected to said device and to said source comprising means for directing said device to count from an initial condition to a resultant condition for a period of time determined by input data from said source, means for directing said device to count from said resultant condition back to said initial condition and means for stopping said control means at said initial condition whereby said period of time determined by said input data is exactly reproduced.

12. A circuit arrangement for reproducing a fixed time interval comprising a pulse counting electron discharge device, a source of input data and control means connected to said device and to said source comprising means for directing said device to count from an initial condition to a resultant condition for a period of time determined by input data from said source, means for directing said device to count from said resultant condition back to said initial condition and means for stopping said control means at said initial condition whereby said period of time determined by said input data is exactly reproduced.

13. A circuit arrangement for reproducing a fixed time interval comprising a pulse counting electron discharge

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device having a plurality of electrodes, a source of input data and control means connected to said device and to said source comprising means connected to selected ones of said electrodes for directing said device to count from an initial condition to a resultant condition for a period of time determined by input data from said source, means connected to said selected ones of said electrodes for directing said device to count from said resultant condition back to said initial condition and means for stopping said control means at said initial condition whereby said period of time determined by said input data is exactly reproduced.

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