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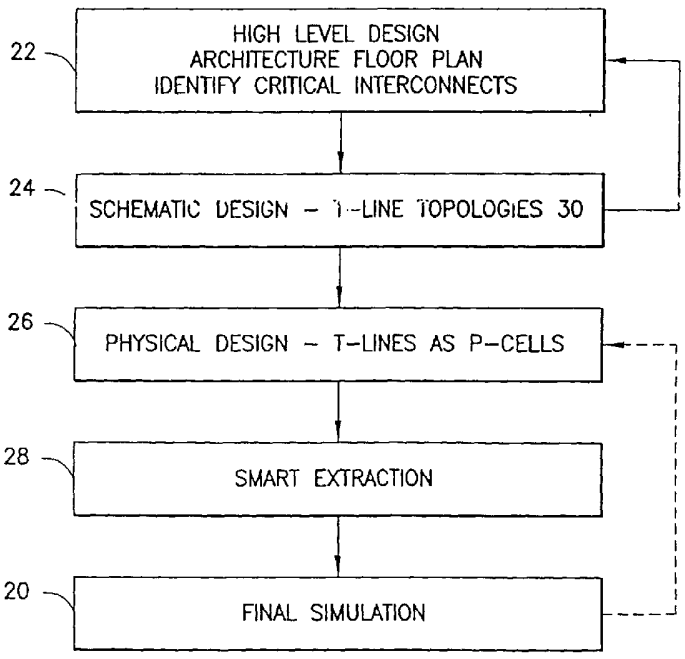
[Continued on next page]

(54) Title: AN INTERCONNECT-AWARE METHODOLOGY FOR INTEGRATED CIRCUIT DESIGN



(57) Abstract: An integrated circuit design kit including one or more circuit components topologies, and one or more critical interconnect lines topologies. The interconnect line topologies may be predefined. The kit may further include one or more circuit components models and one or more critical interconnect lines models.

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ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

PCT/IB 03/00819

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

INSPEC, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	GOREN D ET AL: "An interconnect-aware methodology for analog and mixed signal design, based on high bandwidth (over 40 GHz) on-chip transmission line approach" PROCEEDINGS 2002 DESIGN, AUTOMATION AND TEST IN EUROPE CONFERENCE AND EXHIBITION, PROCEEDINGS 2002 DESIGN, AUTOMATION AND TEST IN EUROPE CONFERENCE AND EXHIBITION, PARIS, FRANCE, 4-8 MARCH 2002, pages 804-811, XP002267256 2002, Los Alamitos, CA, USA, IEEE Comput. Soc, USA ISBN: 0-7695-1471-5 the whole document	19-30

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 January 2004	04/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Alonso Nogueiro, L

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	SYLVESTER D : "The Role of Interconnect in System-Level Performance: Delay, Power, Noise" FSA MODELING WORKSHOP, 'Online! May 1999 (1999-05), XP002267289 Retrieved from the Internet: <URL:http://www.eecs.umich.edu/{dennis/talks/workshop_notes.pdf> 'retrieved on 2004-01-19! page 31 -page 33 page 41 ---	19-30
Y	HE L: "Interconnect Modeling and Design" EDA LABORATORY, 'Online! February 2000 (2000-02), XP002267290 University of Wisconsin Retrieved from the Internet: <URL:http://eda.ece.wisc.edu/talks/umn.pdf > 'retrieved on 2004-01-19! page 8 -page 10 page 27 page 30 page 34 ---	19-30
A	HE L ET AL: "An Efficient Inductance Modeling for On-Chip Interconnects" EDA LABORATORY , 'Online! May 1999 (1999-05), XP002267291 Universoty of Wisconsin Retrieved from the Internet: <URL:http://eda.ece.wisc.edu/ECE902/ind.pdf> 'retrieved on 2004-01-19! page 2 -page 4 page 10 ---	19-30
A	RIESGO T ET AL: "DESIGN METHODOLOGIES BASED ON HARDWARE DESCRIPTION LANGUAGES" IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE INC. NEW YORK, US, vol. 46, no. 1, February 1999 (1999-02), pages 3-12, XP000831924 ISSN: 0278-0046 page 4-11 ---	19-30
A	US 6 342 823 B1 (DANSKY ALLAN HARVEY ET AL) 29 January 2002 (2002-01-29) column 3 column 5 ---	19-30

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	GALA K ET AL: "Inductance 101: analysis and design issues" PROCEEDINGS OF THE 38TH. ANNUAL DESIGN AUTOMATION CONFERENCE. (DAC). LAS VEGAS, NV, JUNE 18 - 22, 2001, PROCEEDINGS OF THE DESIGN AUTOMATION CONFERENCE, NEW YORK, NY: ACM, US, vol. CONF. 38, 18 June 2001 (2001-06-18), pages 329-334, XP010552409 ISBN: 1-58113-297-2 page 333 ---	19-30
A	YU CAO ET AL: "Effects of global interconnect optimizations on performance estimation of deep submicron design" IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER AIDED DESIGN. ICCAD - 2000. IEEE/ACM DIGEST OF TECHNICAL PAPERS (CAT. NO.00CH37140), PROCEEDINGS OF INTERNATIONAL CONFERENCE ON COMPUTER AIDED DESIGN (ICCAD), SAN JOSE, CA, USA, 5-9 NOV. 2000, pages 56-61, XP002267292 2000, Piscataway, NJ, USA, IEEE, USA ISBN: 0-7803-6445-7 page 56-58 -----	19-30

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 1-18

A "topology" describes in the area of "wiring" a way of connecting different elements of the circuit or how to distribute signals within the circuit. Examples of topologies are a tree, a bus, a ring, a star, etc. The terms "interconnect topology" or "line topology", as used in the application refer to the structure of an interconnect line, i.e. the relative positions and sizing of several signal and shielding wires used to propagate one or more signals (see figures 3a to 3f). The terms "geometry" or "structure" seem to describe with more precision the features meant by "topology" in the application.

Claim 1: A system must be characterized in terms of structural features. It cannot be decided what kind of system could be composed of designs at different levels, extracted parameters and results of simulations. It seems that claim 1 would rather be directed to a design method like claim 19.

Claim 2: It cannot be decided what features should be searched that define a circuit design kit. A component topology and an interconnect line topology are geometrical or structural relationships between parts of the component, resp. parts of the interconnect. It is not clear how this kind of relationships may define a circuit design kit.

Claim 6: A critical interconnect line in a circuit is an interconnect line that determines the performance of the circuit (typically the one with largest delay). The toplogy of such an interconnect line is neither a step of a process nor a structural feature of a system, it is rather a mathematical, abstract description of the shape of the interconnect line.

Claims 15 and 17: A method, or a corresponding computer program, must be characterized by mehtod steps. Both claims 15 and 17 lack any feature with could be used to define them.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

PCT/IB 03/00819

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 1-18
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

PCT/IB 03/00819

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6342823 B1	29-01-2002	NONE	