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**Declarations under Rule 4.17**:

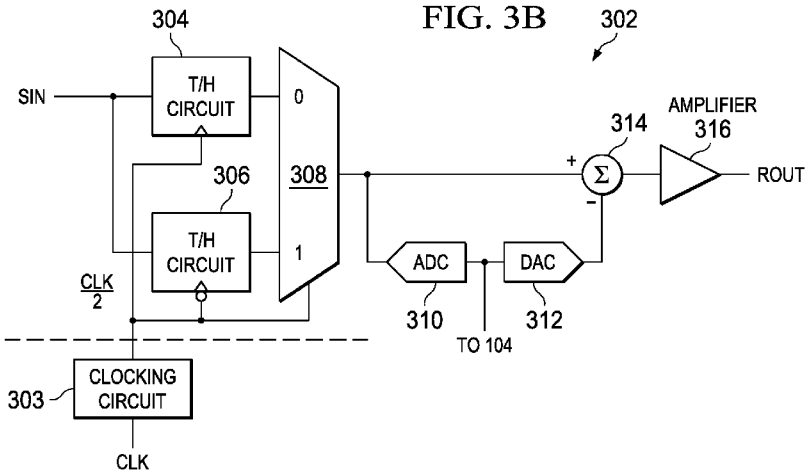
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

*[Continued on next page]*

(54) **Title**: POWER AND AREA EFFICIENT INTERLEAVED ADC

FIG. 3B




(57) **Abstract**: Pipeline analog-to-digital converters (ADCs) are commonly used for high frequency applications; however, operating at high sampling rates will often result in high power consumption or tight timing constraints. Here, though, an ADC is provided that allows for relaxed timing (which enables a high sampling rate) with low power consumption. This is accomplished through the use of multiplexed, front-end track- and-hold (T/H) circuits that sample on non-overlapping portions of a clocking signal in conjunction with "re-used" or shared analog processing circuitry. Parallel track- and-hold (T/H) circuits (304, 306) receive an analog input signal (AIN or prior residue) and are clocked at half clock cycles (CLK/2) by clocking circuit 303 to sample/hold on non- overlapping logic phases. The T/H circuits (304, 306) are respectively coupled to analog-to-digital converter (ADC 310) through multiplexer (308) and to digital-to-analog converter (DAC 312), adder (314) and amplifier (316) to perform analog processing to resolve sampled signals for digital output circuit (104) and to generate a residue signal (ROUT).

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# POWER AND AREA EFFICIENT INTERLEAVED ADC

**[0001]** The invention relates generally to analog-to-digital converters (ADCs) and, more particularly, to interleaved ADCs.

## BACKGROUND

**[0002]** High performance ADCs do not typically follow the "Moore's Law" area and power curves achieved by digital circuits in scaling CMOS process technology. The noise and resolution specifications of an ADC dictate power constraints (lower noise requires higher power) and area limits (to exceed component matching requirements). In addition, as the sampling rates of ADCs increase, typical architectures fail to deliver the required performance due to timing limitations.

**[0003]** Referring to FIG. 1A of the drawings, reference numeral 100 generally designates a conventional ADC 100. ADC 100 generally comprises several stages 102-1 to 102-N, an ADC 106 (which is typically a flash ADC), and a digital output circuit 104. The stages 102-1 to 102-N are generally coupled in series with one another in a sequence, where the first stage 102-1 receives the analog input signal and where each of the subsequent stages 102-2 to 102-N receives a residue signal from the previous stage 102-1 to 102-(N-1), respectively. ADC 106 is coupled to the last stage 102-N (receiving its residue signal). Based on its input signal (either a residue signal or the analog input signal), stages 102-1 to 102-N and ADC 106 are able to resolve a portion of the analog input signal, which is provided to digital output circuit 104. Digital output circuit 104 can then perform error correction or other digital processing to generate the digital output signal DOUT.

**[0004]** Turning now to FIGS. 1B and 1C, stages 102-1 to 102-N can be seen in greater detail (which are referred to hereinafter as stage 102 for the sake of simplicity). Stage 102 generally comprises a track-and-hold (T/H) circuit 108 (i.e., T/H amplifier), ADC 110, digital-to-analog converter (DAC) 112, adder 114, and a residue amplifier 116. In operation, the T/H

circuit 110 enters a track phase T during the logic high state of the clock signal CLK and a hold phase H during the logic low state of the clock signal CLK. During the track phase T, the T/H circuit samples its analog input signal SIN (which may be the analog input signal AIN or the residue signal from the previous stage). During the hold phase H, the sampled signal is provided to ADC 110 and adder 114. The ADC 110 resolves a portion of the signal SIN, providing the resolved bits to digital output circuit 104 and DAC 112. DAC 112 converts the resolved bits to an analog signal which is provided to adder 114. Adder 114 determines the difference between the sampled signal and the analog signal from DAC, which is amplified by amplifier 116 and output as a residue signal ROUT.

**[0005]** There are some drawbacks to ADC 100. In particular, timing can disadvantage the performance. In operation, analog processing (quantization by ADC 110 and DAC 112, subtraction by adder 114, and amplification by amplifier 116) occurs within a very tight time, namely within one-half of the period of the clock signal CLK (which operates as a sampling clock). While ADC 100 is well-suited for low noise systems, it is generally limited to low sampling rates to allow for sufficient time for analog processing.

**[0006]** Turning to FIGS. 2A through 2C, another example of a conventional ADC 200 can be seen. ADC 200 has the same general functionality as ADC 100. However, a difference exists in the pipeline; namely, stages 102-1 to 102-N have been replaced by stages 202-1 to 202-N and input amplifier 204. A difference between stage 102 (of FIG. 1B) and stage 202-1 to 202-N (hereinafter 202) is that an additional T/H circuit 206 is interposed between T/H circuit 108 and adder 114. T/H circuits 108 and 206 enter track phases T and hold phases H in opposite logic states of clock signal CLK. This arrangement allow for relaxed timing because a sampled signal is held for an entire period of the clock signal CLK, but the addition of T/H circuit 206 adds noise (i.e., about 3dB per T/H circuit 206). To compensate for noise degradation, the power consumption for each T/H circuit 108 and 206 is doubled, resulting in four times the power consumption of the single T/H system.

**[0007]** Therefore, there is a need for an improved ADC.

**[0008]** Some examples of other conventional circuits are described in: U.S. Patent Nos. 3,059,228; 3,735,392; 3,820,112; 5,180,932; and 5,391,936.

SUMMARY

**[0009]** An example embodiment of the invention, accordingly, provides an apparatus. The apparatus comprises a plurality of track-and-hold (T/H) circuits that receive an analog input signal; a multiplexer that is coupled to each of the T/H circuits; an analog-to-digital converter (ADC) that is coupled to the multiplexer; and a clocking circuit that receives a clock signal and that is coupled to each of the T/H circuits and the multiplexer, wherein the clocking circuit controls the T/H circuits such that tracking phases for the T/H circuits are generally non-overlapping, and wherein the clocking circuit controls the coupling between each T/H circuit and the ADC with the multiplexer.

**[0010]** In accordance with an example embodiment of the invention, the apparatus further comprises a digital-to-analog converter (DAC) that is coupled to the ADC; an adder that is coupled to the DAC and the multiplexer so as to determine the difference between output signals of the DAC and multiplexer; and an amplifier that is coupled to the adder.

**[0011]** In accordance with an example embodiment of the invention, the clock circuit further comprises a clock divider.

**[0012]** In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a plurality of stages that are coupled in series with one another in a sequence, wherein the first stage of the sequence receives an analog input signal, and wherein each stage outputs a residue signal, and wherein each stage includes: a plurality of T/H circuits that receive the analog input signal or the residue signal from the previous stage; a multiplexer that is coupled to each of the T/H circuits; and a first ADC that is coupled to the multiplexer; and a clocking circuit that receives a clock signal and that is coupled to each of the T/H circuits and the multiplexer, wherein the clocking circuit controls the T/H circuits such that tracking phases for the T/H circuits for each stage are generally non-overlapping, and wherein the clocking circuit controls the coupling between each T/H circuit for each stage and each first ADC with the multiplexer for each stage; a second ADC that is coupled to the last stage of the sequence so as to receive its residue signal; and a digital output circuit that is coupled to each stage and the second ADC so as to generate a digital output signal.

**[0013]** In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a plurality of stages that are coupled in series with one another in a sequence, wherein the first stage of the sequence receives an analog input signal, and

wherein each stage outputs a residue signal, and wherein each stage includes: a first T/H circuit that receives the analog input signal or the residue signal from the previous stage; a second T/H circuit that receives the analog input signal or the residue signal from the previous stage; a multiplexer that is coupled to the first and second T/H circuits; and a first ADC that is coupled to the multiplexer; and a clocking circuit that receives a clock signal and that is coupled to each of the T/H circuits and the multiplexer, wherein the clocking circuit controls the T/H circuits such that tracking phases for the T/H circuits for each stage are generally non-overlapping, and wherein the clocking circuit controls the coupling between each T/H circuit for each stage and each first ADC with the multiplexer for each stage; a second ADC that is coupled to the last stage of the sequence so as to receive its residue signal; and a digital output circuit that is coupled the each stage and the second ADC so as to generate a digital output signal.

**[0014]** In accordance with an example embodiment of the invention, each stage further comprises: a DAC that is coupled to the first ADC; an adder that is coupled to the DAC and the multiplexer so as to determine the difference between output signals of the DAC and multiplexer; and an amplifier that is coupled to the adder.

**[0015]** In accordance with an example embodiment of the invention, the clock divider is a divide-by-2 clock divider so as to generate a halved clock signal at one half the frequency.

**[0016]** In accordance with an example embodiment of the invention, each first T/H circuit is in its track phase when the halved clock signal is in a first logic state and in its hold phase in when the halved clock signal is in a second logic state, and wherein each first T/H circuit is coupled to its first ADC through its multiplexer when the halved clock signal is in the second logic state.

**[0017]** In accordance with an example embodiment of the invention, each second T/H circuit is in its hold phase when the halved clock signal is in the first logic state and in its track phase when the halved clock signal is in the second logic state, and wherein each second T/H circuit is coupled to its first ADC through its multiplexer when the halved clock signal is in the first logic state.

**[0018]** In accordance with an example embodiment of the invention, the first logic state is logic high, and wherein the second logic state is logic low.

**[0019]** The foregoing has outlined rather broadly the features and technical advantages of the invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0020]** Example embodiments are described with reference to accompanying drawings, wherein:

**[0021]** FIGS. 1A and 1B are circuit diagrams for an example of a conventional ADC;

**[0022]** FIG. 1C is a timing diagram for the ADC of FIGS. 1A and 1B;

**[0023]** FIGS. 2A and 2B are circuit diagrams for an example of a conventional ADC;

**[0024]** FIG. 2C is a timing diagram for the ADC of FIGS. 2A and 2B;

**[0025]** FIGS. 3A and 3B are circuit diagrams for an example of an ADC in accordance with an example embodiment of the invention; and

**[0026]** FIG. 3C is a timing diagram for the ADC of FIGS. 3A and 3B.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

**[0027]** In FIG. 3A, an ADC 300 in accordance with an example embodiment of the invention is given. ADC 300 has the same general functionality as ADC 100. However, a difference exists in the pipeline; namely, stages 102-1 to 102-N have been replaced by stages 302-1 to 302-N and clocking circuit 303.

**[0028]** Looking to FIG. 3B and 3C, stages 302-1 to 203-N (hereinafter 302) can be seen in greater detail. In operation, T/H circuit 304 and 306 are coupled to receive an analog input signal (either the analog input signal AIN or a residue signal from the previous stage). Since these T/H circuits 304 and 306 are arranged in parallel with one another, T/H circuits 304 and 306 can be timed so as to sample on generally non-overlapping logic stages or phases of a clock signal. Preferably, clocking circuit 303 generally comprises a clock divider (i.e., divide-by-2 clock divider) to generate a halved clock signal CLK/2. This halved clock signal CLK/2 can be provided to T/H circuits 304 and 306 where the T/H circuits 304 and 306 enter track phases T

and hold phases H on opposite logic levels of halved clock signal CLK/2. Additionally, the halved clock signal CLK/2 can be provided to multiplexer 308 so as to operate as a select signal so that, when T/H circuits 304 and 306 is in their respective hold phases H, T/H circuits 304 and 306 are respectively coupled to ADC 310 through multiplexer 308. ADC 310, DAC 312, adder 314, and amplifier 316 can then perform analog processing to resolve sampled signals for digital output circuit 104 and to generate a residue signal ROUT.

**[0029]** Effectively, the configuration of ADC 300 operates as a two way (for example) interleaved ADC, which results in the realization of several benefits. By interleaving T/H circuits 304 and 306 at one-half of the sampling rate (i.e., set by clock signal CLK), both relaxed timing and low power consumption (compared to ADCs 100 and 200) can be achieved. Moreover, because ADC 310, DAC 312, adder 314, and amplifier 316 are shared or "re-used," ADC 310, DAC 312, adder 314, and amplifier 316 can be fully utilized instead of remaining idle for part of the time (i.e., one-half of the time), as with an non-interleaved designs. Additionally, because of the re-use of ADC 310, DAC 312, adder 314, and amplifier 316, the amount of area used can be reduced.

**[0030]** Embodiments having different combinations of one or more of the features or steps described in the context of example embodiments having all or just some of such features or steps are intended to be covered hereby. Those skilled in the art will appreciate that many other embodiments and variations are also possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a plurality of track-and-hold (T/H) circuits that receive an analog input signal;

a multiplexer that is coupled to each of the track-and-hold circuits;

an analog-to-digital converter (ADC) that is coupled to the multiplexer; and

a clocking circuit that receives a clock signal and that is coupled to each of the track-and-hold circuits and the multiplexer, wherein the clocking circuit controls the track-and-hold circuits such that tracking phases for the track-and-hold circuits are generally non-overlapping, and wherein the clocking circuit controls the coupling between each track-and-hold circuit and the ADC with the multiplexer.

2. The apparatus of Claim 1, wherein the apparatus further comprises:

a digital-to-analog converter (DAC) that is coupled to the analog-to-digital converter;

an adder that is coupled to the digital-to-analog converter and the multiplexer so as to determine the difference between output signals of the digital-to-analog converter and multiplexer; and

an amplifier that is coupled to the adder.

3. The apparatus of Claim 2, wherein the clock circuit further comprises a clock divider.

4. An apparatus comprising:

a plurality of stages that are coupled in series with one another in a sequence, wherein the first stage of the sequence receives an analog input signal, and wherein each stage outputs a residue signal, and wherein each stage includes:

a plurality of track-and-hold (T/H) circuits that receive the analog input signal or the residue signal from the previous stage;

a multiplexer that is coupled to each of the track-and-hold circuits; and

a first analog-to-digital converter (ADC) that is coupled to the multiplexer; and

a clocking circuit that receives a clock signal and that is coupled to each of the track-and-hold circuits and the multiplexer, wherein the clocking circuit controls the track-and-hold circuits such that tracking phases for the track-and-hold circuits for each stage are generally non-overlapping, and wherein the clocking circuit controls the coupling between each track-and-hold circuit for each stage and each first analog-to-digital converter with the multiplexer for each stage;

a second analog-to-digital converter that is coupled to the last stage of the sequence so as to receive its residue signal; and

a digital output circuit that is coupled the each stage and the second analog-to-digital converter so as to generate a digital output signal.

5. The apparatus of Claim 4, wherein each stage further comprises:

a digital-to-analog converter (DAC) that is coupled to the first analog-to-digital converter;

an adder that is coupled to the digital-to-analog converter and the multiplexer so as to determine the difference between output signals of the digital-to-analog converter and multiplexer; and

an amplifier that is coupled to the adder.

6. The apparatus of Claim 5, wherein the clock circuit further comprises a clock divider.

7. An apparatus comprising:

a plurality of stages that are coupled in series with one another in a sequence, wherein the first stage of the sequence receives an analog input signal, and wherein each stage outputs a residue signal, and wherein each stage includes:

a first track-and-hold (T/H) circuit that receives the analog input signal or the residue signal from the previous stage;

a second track-and-hold circuit that receives the analog input signal or the residue signal from the previous stage;

a multiplexer that is coupled to the first and second track-and-hold circuits; and

a first analog-to-digital converter (ADC) that is coupled to the multiplexer; and

a clocking circuit that receives a clock signal and that is coupled to each of the track-and-hold circuits and the multiplexer, wherein the clocking circuit controls the track-and-hold circuits such that tracking phases for the track-and-hold circuits for each stage are generally non-overlapping, and wherein the clocking circuit controls the coupling between each track-and-hold circuit for each stage and each first analog-to-digital converter with the multiplexer for each stage;

a second analog-to-digital converter that is coupled to the last stage of the sequence so as to receive its residue signal; and

a digital output circuit that is coupled the each stage and the second analog-to-digital converter so as to generate a digital output signal.

8. The apparatus of Claim 7, wherein each stage further comprises:

a digital-to-analog converter (DAC) that is coupled to the first analog-to-digital converter;

an adder that is coupled to the digital-to-analog converter and the multiplexer so as to determine the difference between output signals of the digital-to-analog converter and multiplexer; and

an amplifier that is coupled to the adder.

9. The apparatus of Claim 8, wherein the clock circuit further comprises a clock divider.

10. The apparatus of Claim 9, wherein the clock divider is a divide-by-2 clock divider so as to generate a halved clock signal.

11. The apparatus of Claim 10, wherein each first track-and-hold circuit is in its track phase when the halved clock signal is in a first logic state and in its hold phase in when the halved clock signal is in a second logic state, and wherein each first track-and-hold circuit is coupled to its first analog-to-digital converter through its multiplexer when the halved clock signal is in the second logic state.

12. The apparatus of Claim 11, wherein each second track-and-hold circuit is in its hold phase when the halved clock signal is in the first logic state and in its track phase in when the halved clock signal is in the second logic state, and wherein each second track-and-hold circuit is coupled to its first analog-to-digital converter through its multiplexer when the halved clock signal is in the first logic state.

13. The apparatus of Claim 12, wherein the first logic state is logic high, and wherein the second logic state is logic low.

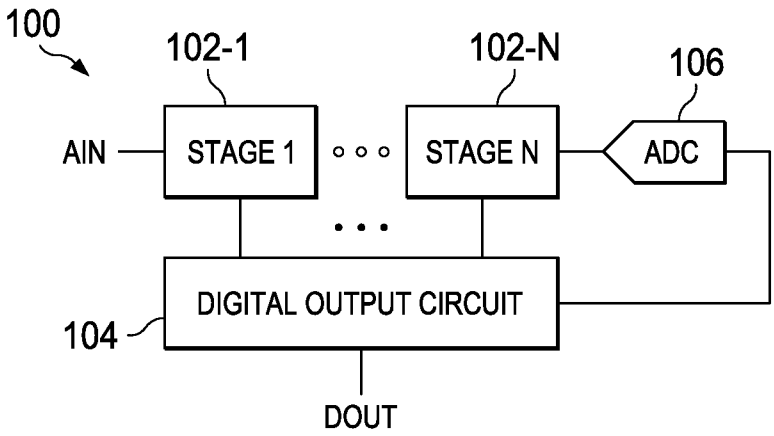



FIG.1A
(PRIOR ART)

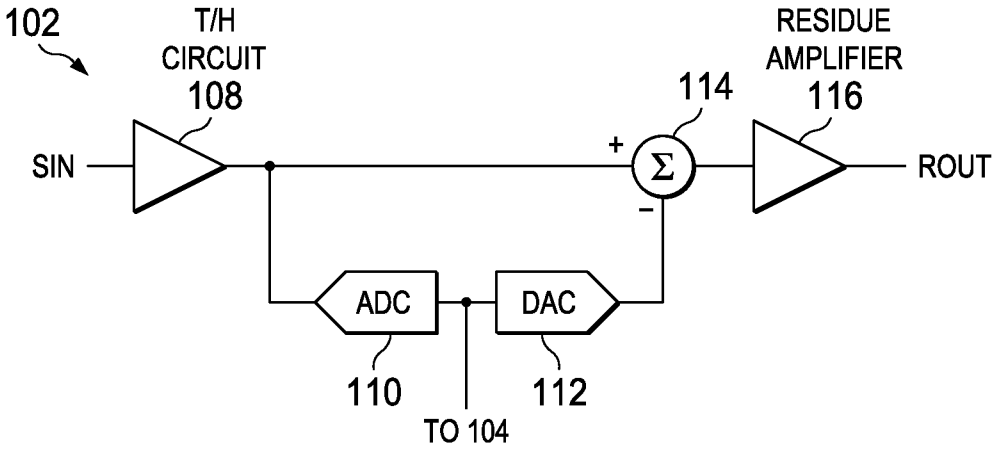



FIG. 1B
(PRIOR ART)

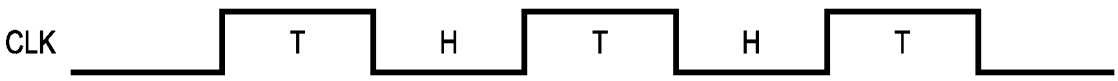



FIG. 1C
(PRIOR ART)

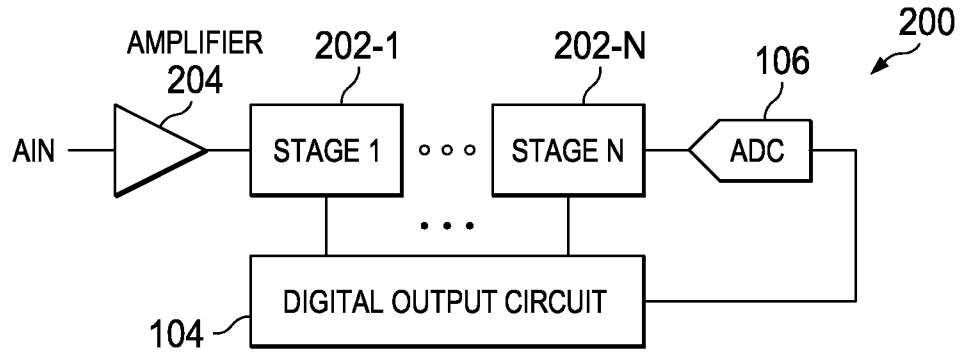



FIG. 2A
(PRIOR ART)

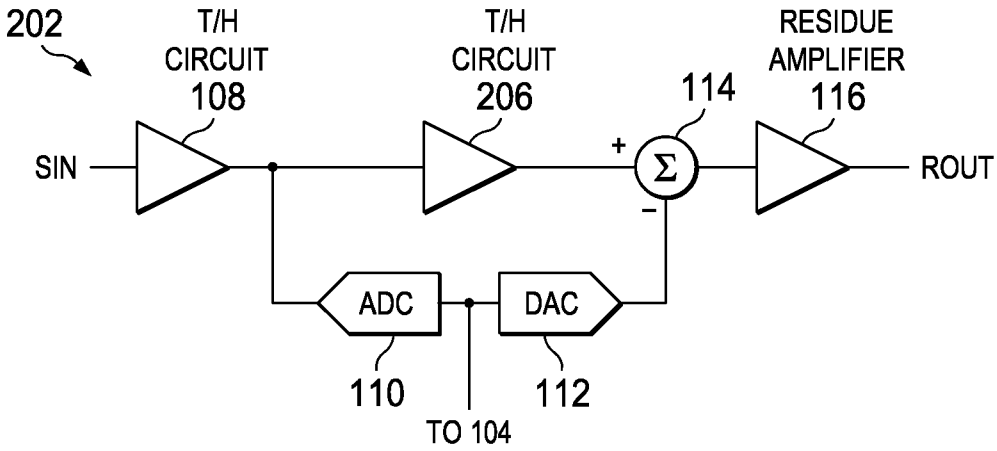



FIG. 2B
(PRIOR ART)

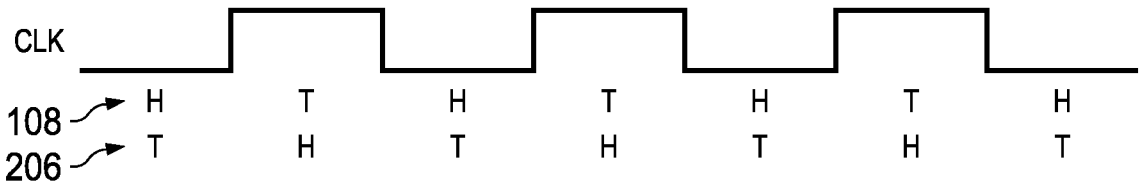



FIG. 2C
(PRIOR ART)

FIG. 3A

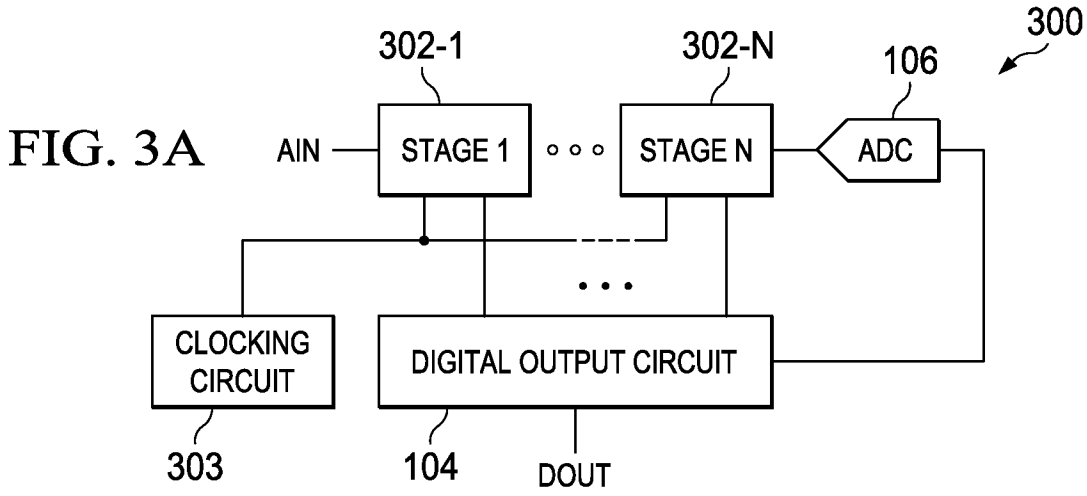



FIG. 3B

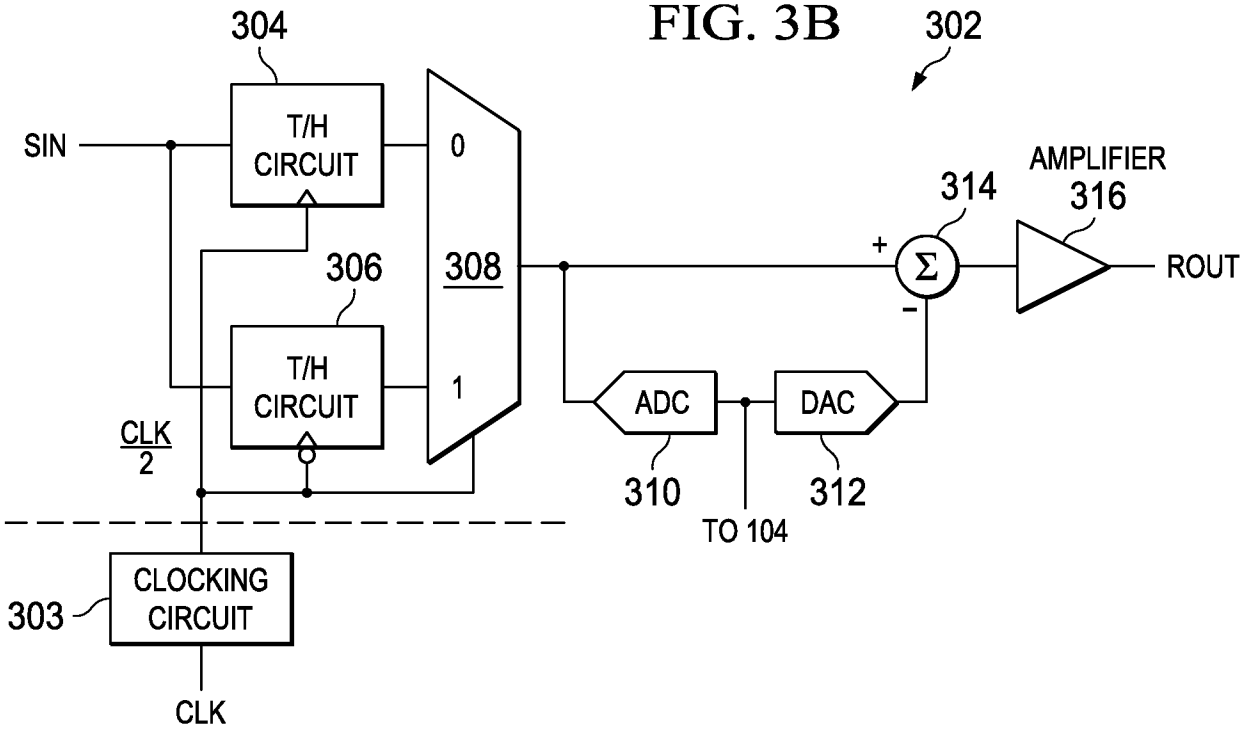
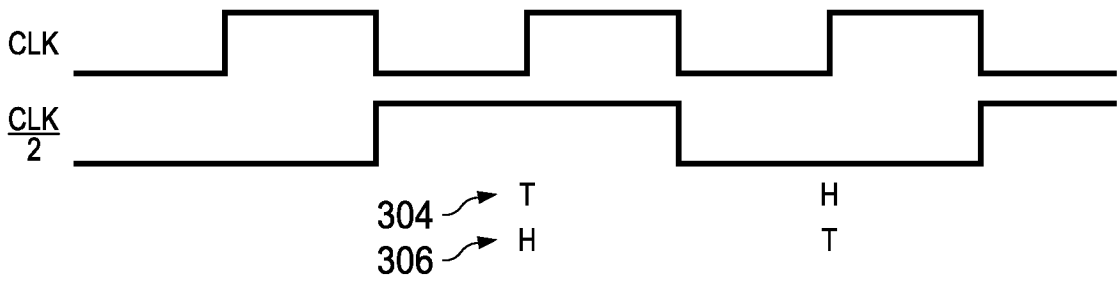



FIG. 3C



**INTERNATIONAL SEARCH REPORT**

International application No.
**PCT/US2010/061546**

**A. CLASSIFICATION OF SUBJECT MATTER**

***H03M 1/12(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
H03M 1/12; H03M 1/00; H03M 1/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: ADC, pipelined, interleaved

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | US 2007-0001891 A1 (Salman Mazhar) 04 January 2007<br>See abstract, figures 2,4, pages 5,6. | 1-13 |
| Y | KR 10-2008-0085797 A (TEXAS INSTRUMENTS INC.) 24 September 2008<br>See abstract, figures 3,4,6a, pages 5-7. | 1-13 |
| A | US 7126515 B1 (BRYAN KRIS) 24 October 2006<br>See abstract, figure 1, columns 3,4. | 1-13 |
| A | US 2001-0050624 A1 (KRISHNASWAMY NAGARAJ) 13 December 2001<br>See abstract, figure 4a,4b,5, pages 1,2. | 1-13 |
| A | KR 10-2001-0041292 A (INTEL CORP.) 15 May 2001<br>See abstract, figures 1,2, page 3. | 1-13 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 28 SEPTEMBER 2011 (28.09.2011) | **29 SEPTEMBER 2011 (29.09.2011)** |

Name and mailing address of the ISA/KR
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| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 2007-0001891 A1 | 04.01.2007 | CN 101213737 A0 | 02.07.2008 |
| | | EP 1900093 A1 | 19.03.2008 |
| | | JP 2008-545339 A | 11.12.2008 |
| | | KR 10-2008-0030635 A | 04.04.2008 |
| | | US 7277040 B2 | 02.10.2007 |
| | | WO 2007-005392 A1 | 11.01.2007 |
| KR 10-2008-0085797 A | 24.09.2008 | EP 1168367 A1 | 02.01.2002 |
| | | EP 1168367 B1 | 11.10.2006 |
| | | JP 2002-109896 A | 12.04.2002 |
| | | KR 10-0894378 B1 | 22.04.2009 |
| US 7126515 B1 | 24.10.2006 | CN 101160724 A0 | 09.04.2008 |
| | | EP 1875611 A1 | 09.01.2008 |
| | | EP 1875611 B1 | 06.04.2011 |
| | | WO 2007-038537 A1 | 05.04.2007 |
| US 2001-0050624 A1 | 13.12.2001 | US 6414611 B1 | 02.07.2002 |
| KR 10-2001-0041292 A | 15.05.2001 | AU 1999-26622 A1 | 15.09.1999 |
| | | GB 2350979 A | 13.12.2000 |
| | | JP 2002-505538 A | 19.02.2002 |
| | | US 06094153A A | 25.07.2000 |
| | | WO 99-44288 A1 | 02.09.1999 |