United States Patent [19]

Konopka

[11] **3,746,886**

[45] **July 17, 1973**

[54] **MEMORY CIRCUIT**

[75] Inventor: **John G. Konopka,** Mundelein, Ill.

[73] Assignee: **Warwick Electronics Inc.,** Chicago, Ill.

[22] Filed: **Oct. 15, 1971**

[21] Appl. No.: **189,637**

[52] **U.S. Cl.**.....**307/223,** 325/468, 328/48, 331/57, 334/15

[51] **Int. Cl.**..... **H03k 23/02,** H03k 23/18

[58] **Field of Search**..... 307/223, 223 B, 238; 331/57; 334/15; 325/335, 469, 470, 468; 328/48, 49

[56] **References Cited**

UNITED STATES PATENTS

3,503,018	3/1970	Cavanagh	334/15
3,290,515	12/1966	Procter	307/223 R
3,047,817	7/1962	Schneider	307/223 R
2,691,725	10/1954	Gardner	325/469 X
3,345,569	10/1967	Casterline et al.	307/223 R
3,528,044	9/1970	Manicki	307/320 X
3,596,183	7/1971	Spies	334/15 X
3,602,822	8/1971	Evans et al.	325/470 X

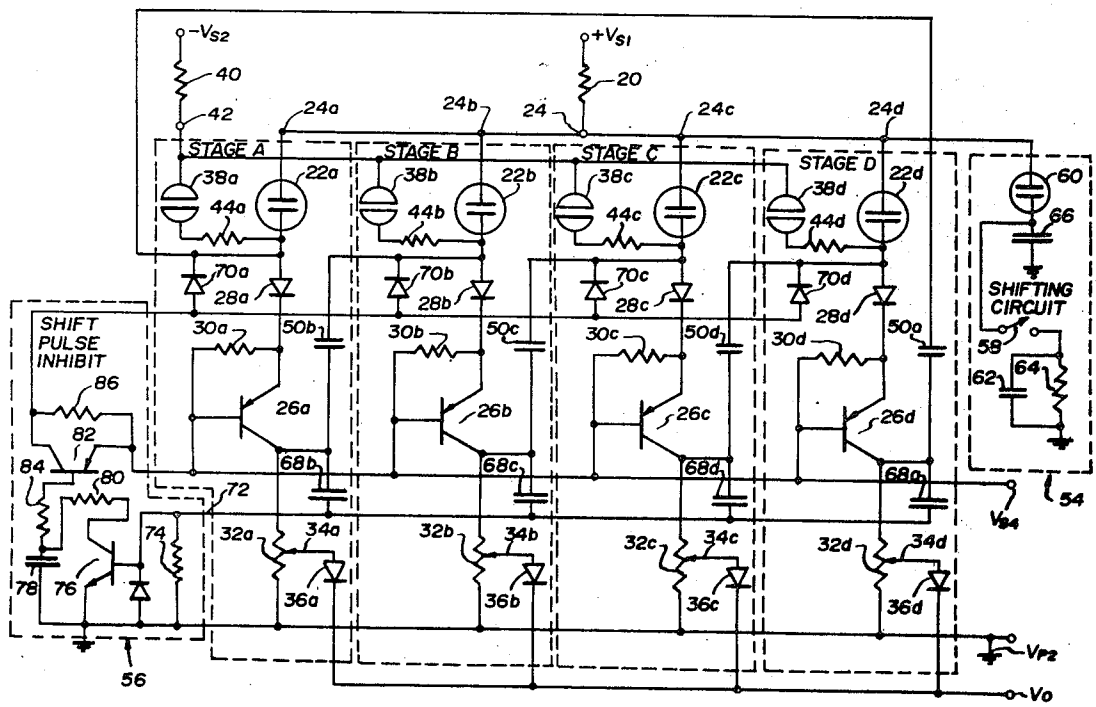
Primary Examiner—John Zazworsky

Attorney—Hofgren, Wegner, Allen, Stellman & McCord

[57] **ABSTRACT**

A triggered neon lamp memory circuit selectively produces control voltages for an electrically controlled rado wave receiver. Each stage comprises a neon lamp, a transistor and a control voltage potentiometer coupled in series between a common source of sustaining potential and a point of reference potential. When the neon lamp of a given stage is triggered, the associated transistor is turned on to effectively couple a fixed voltage to the control voltage potentiometer. When the neon lamp turns off, the transistor turns off to remove the fixed voltage from the control voltage potentiometer while, at the same time, enabling the voltage at one terminal of the neon lamp to remain substantially above the reference potential to thereby reduce the voltage across the neon lamp to a point substantially below the trigger level. In one embodiment, the neon lamp of any one stage is triggered on by temporarily coupling a trigger potential to the neon lamp by manually actuating a touch contact. The triggering of any one lamp lowers the common sustaining potential to thereby extinguish the neon lamp of the previously activated stage. In another embodiment, a shifting circuit, either remotely or locally activated, successively triggers each lamp so that the circuit functions in the nature of a ring counter. In the remote control embodiment, programming means are provided to cause the shifting circuit to selectively prefer preselected ones of the plurality of stages by providing a greater selection period therefor.

24 Claims, 3 Drawing Figures



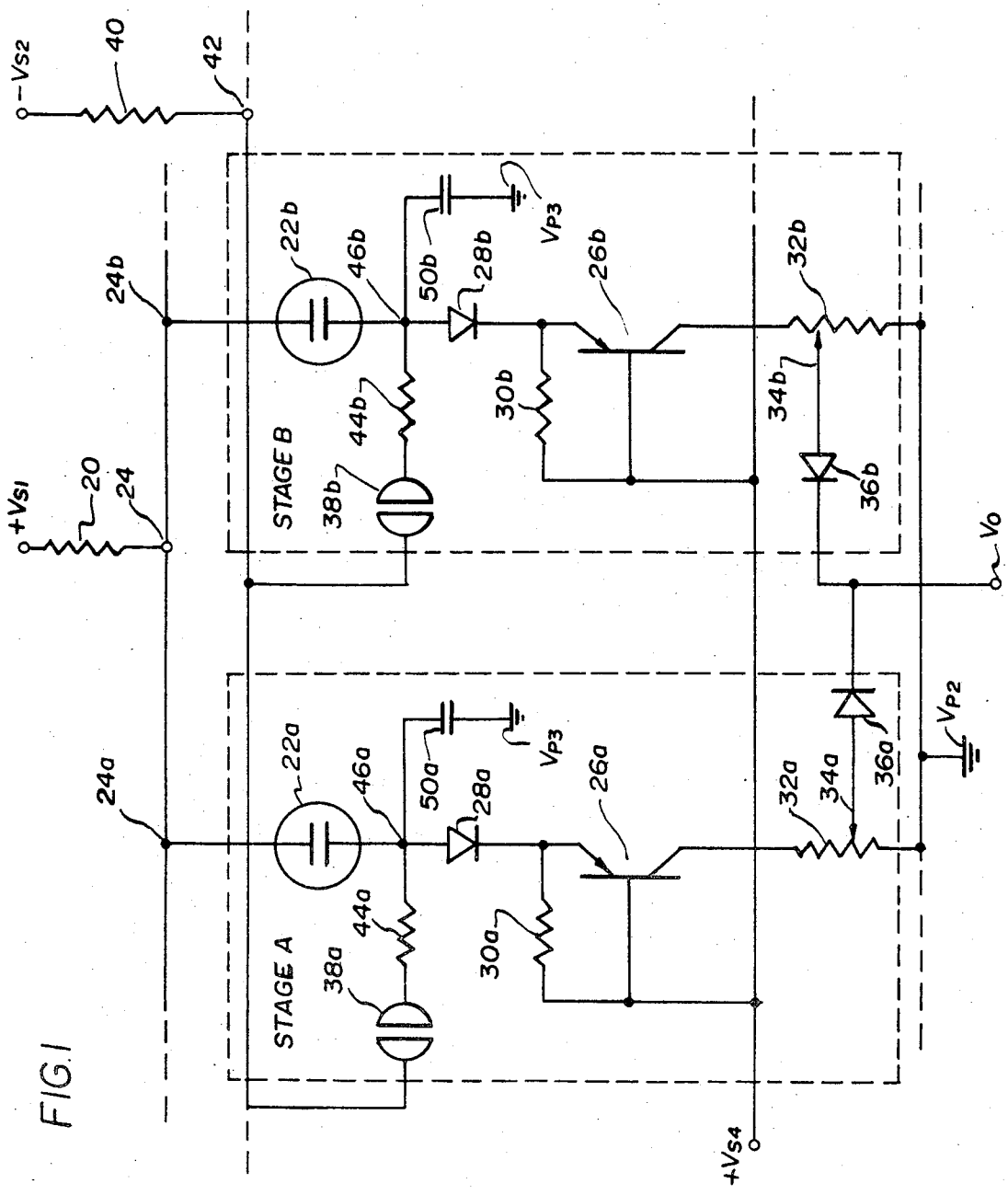

-Vs2
40
42
+Vs1
20
24
24b
22b
46b
50b
28b
VP3
26b
32b
34b
36b
30b
44b
38b
STAGE B
Vo
24a
22a
46a
50a
28a
VP3
26a
32a
34a
36a
VP2
30a
44a
38a
STAGE A
+Vs4

FIG 1

3 Sheets-Sheet 2

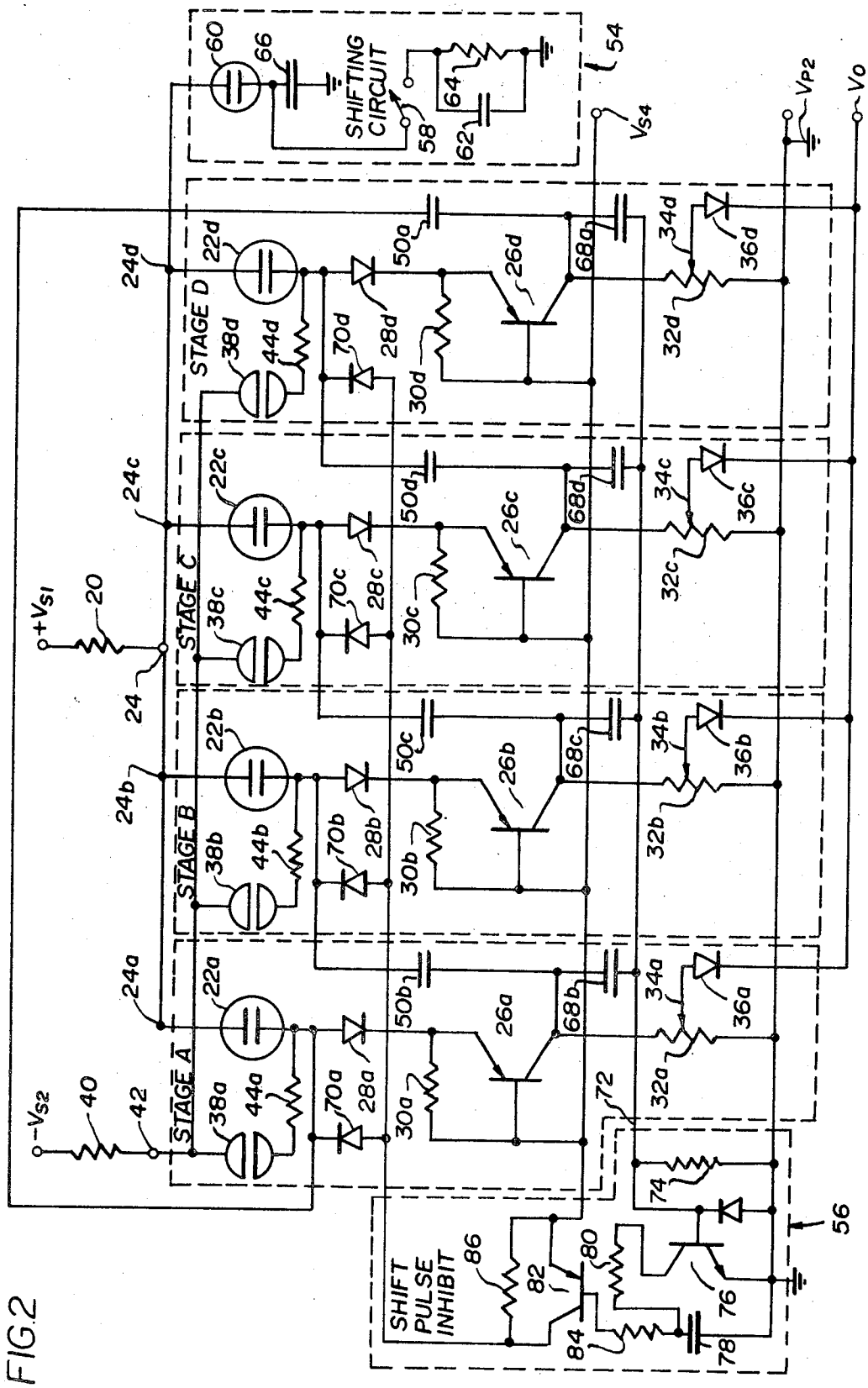
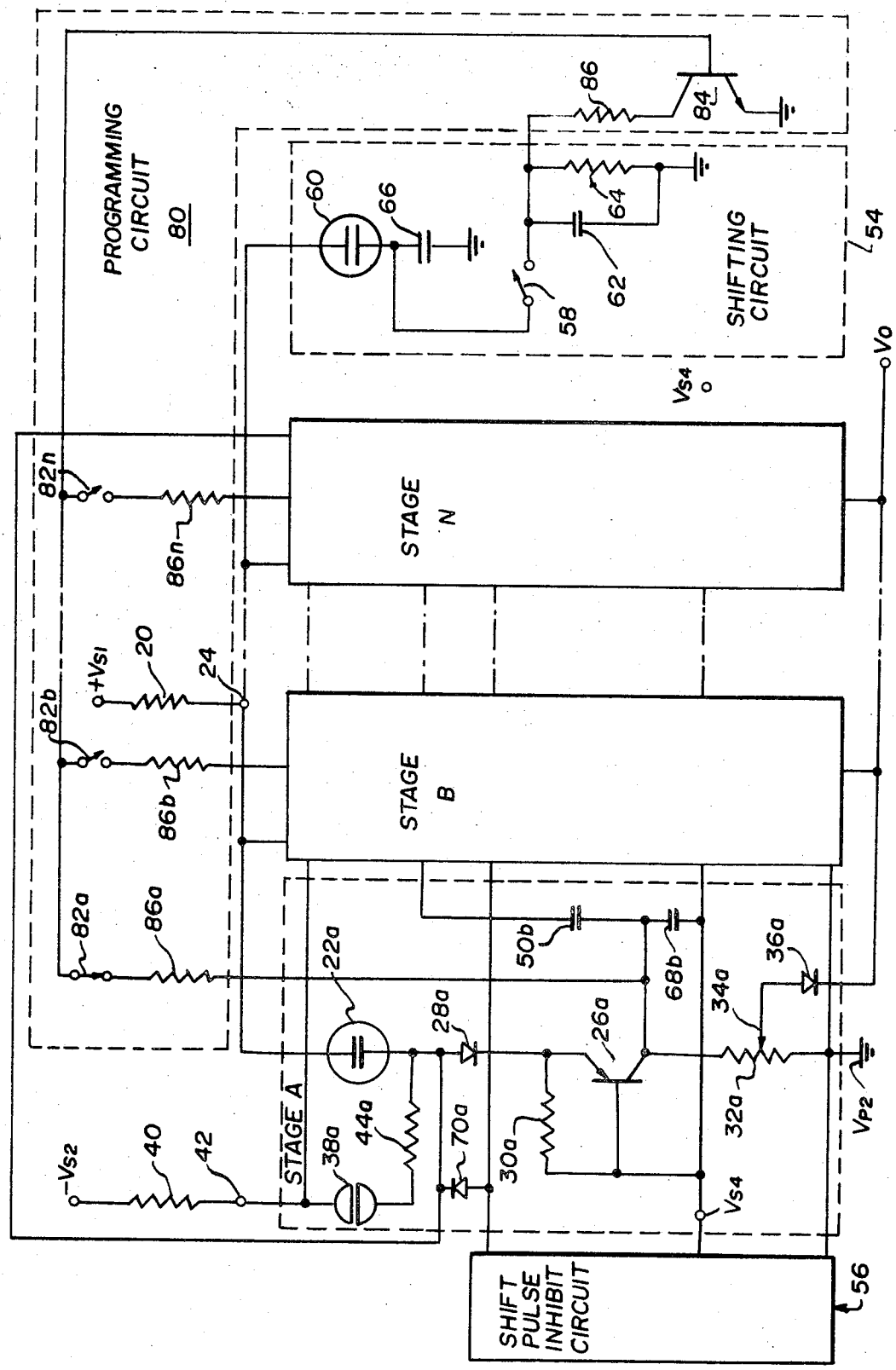


FIG.2

FIG. 3


PROGRAMMING CIRCUIT
80
SHIFTING CIRCUIT
54
STAGE N
STAGE B
STAGE A
SHIFT PULSE INHIBIT CIRCUIT
56
Vo
Vs4
Vs4
Vs2
Vp2
+Vs1
-Vs2
20
22a
24
26a
28a
30a
32a
34a
36a
38a
40
42
44a
50b
58
60
62
64
66
68b
70a
82a
82b
82n
84
86
86a
86b
86n

MEMORY CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates generally to electronic memory switching circuits and, in particular, to a discrete control voltage developing circuit utilizing a breakdown device such as a neon lamp as a memory and switching element.

DESCRIPTION OF THE PRIOR ART

Conventional television receivers commonly are provided with a manually operated tuner having a selection control knob that is manually rotated by the user to select any desired channel. Some television receivers have tuners that are operated by stepping motors. More recently, Varactor tuners, which operate electrically rather than mechanically, have beem employed. Varactors, which are variable capacitance diodes, are employed as filter elements in the tuner. Different control voltages applied to the diodes vary their capacitance and thus control the frequency characteristics of the tuner. The use of all electrical Varactor tuners has, of course, eliminated the problem of mechanical wear, one of the principal factors contributing to tuner maladjustment.

Various circuits have been developed for selectively applying different control voltages to Varactor tuners. In one known circuit, a neon lamp is utilized as the switching and memory element. A neon lamp is one of several breakdown devices, which, when in a high impedance state, switch to a low impedance state in response to the voltage thereacross assuming a trigger level, and which, when in a low impedance state, switch to a high impedance state in response to the voltage thereacross decreasing below a sustaining level which is less than the trigger level. In this previous known circuit, the neon lamp is coupled from a source of sustaining potential to ground through a resistor. When the neon lamp assumes its low impedance state, a voltage at the junction between the lamp and the resistor actuates a transistor which, in response thereto, couples a control voltage developing potentiometer with a source of power.

In prior known circuits, the sustaining voltage across a triggered or activated lamp plus the voltage drop across the series resistor is very close to the trigger potential of the extinguished lamps of the other stages. Since the stages are connected in parallel, this vgltage appears substantially entirely across the extinguished lamps of the other stages because of the high impedance of the extinguished lamps relative to the series resistor. Due to the fact that the trigger potential of neon lamps varies from lamp to lamp, this voltage across the extinguished lamps can cause intolerable, inadvertent firing of nonselected stages.

SUMMARY OF THE INVENTION

The present invention is concerned with an improved memory circuit for producing control voltages for Varactor tuners and the like.

A plurality of stages, one stage for each control voltage to be reproduced, are connected in parallel from a reference potential, such as ground, through a common resistor to a source of operating voltage. Each stage comprises a neon lamp or other suitable breakdown device connected in series between the common resistor and ground reference potential.

A regulated voltage source is coupled to the transistor of each stage, such that, when its associated neon lamp is triggered, the transistor will turn on to effectively couple a regulated voltage across the tuning voltage potentiometer, thereby developing the desired tuning voltage at its wiper contact. When this invention is used to control a Varactor tuner of a television receiver, for example, each of the control voltage potentiometers are set to produce a separate and distinct tuning voltage corresponding to the various channels of the receiver.

When the neon lamp is extinguished, the series transistor is cut off to remove the voltage from the tuning voltage potentiometer, and also alters the potential at the junction between the neon lamp and the transistor to decrease the voltage across the lamp sufficiently below the trigger potential to prevent inadvertent triggering thereof.

In one embodiment of the invention, the various channels are selected by physically touching a pair of contacts associated with the desired switching stage to complete a circuit, through the skin resistance of the operator's finger, between a source of negative trigger potential and a junction of the neon lamp of the selected stage. The actuation of any one stage by triggering its neon lamp, causes the voltage at the common junction of the lamp to decrease to a level insufficient to maintain conduction in the neon lamp of the previously activated stage. Conduction continues in the newly triggered lamp by reason of the fact that the negative trigger potential at a junction thereof is substantially below the potential at the corresponding junction of the remaining lamp.

In another embodiment, means are provided so that the various channels may be also remotely selected. A separate oscillator circuit, upon remote actuation, periodically lowers the voltage at the common junction of the neon lamps below the requisite level necessary to maintain the previously triggered neon lamp in its low impedance state. A capacitor coupled between successive stages transmits a trigger or shift pulse from the stage turned off to the next successive stage which turns on in response thereto. When that stage turns off, in response to the sustaining potential again being lowered by the oscillator circuit, the next stage is turned on. This sequential activation process continues in a ring counter fashion until the desired channel has been selected by either remotely or locally disabling the oscillator to terminate further shifting. A further circuit is provided to inhibit the trigger pulse when a manual selection is made, so that the stage immediately preceding it, is not turned on thereby.

In yet another embodiment, a further circuit is also provided to increase the frequency of the oscillator until any one of a plurality of preselected stages is triggered, at which time the frequency of the oscillator is decreased. This causes the memory circuit to rapidly step through the memory stages corresponding to channels not used in a given broadcast area, and to dwell or pause for a longer selection period at the preselected stages corresponding to desired channels at which television programs are available.

Thus, a principal feature of the invention is the provision of a switching device connected with a neon lamp to selectively lower the voltage across the neon lamp substantially below the trigger level to prevent inadvertent triggering.

Another feature of the invention is the provision of a neon lamp memory in which selective triggering of one lamp lowers the common sustaining potential to thereby turn off any previously activated lamps.

Still a further feature of the invention is the provision of a channel shifting circuit which provides successive switching from one memory stage to another upon single actuation of either a remote control or a local channel change switch until the selected channel is reached and the switch is deactivated.

Yet, another feature of the invention is the provision of a programming circuit which enables an operator to preselect desired stages of the memory whereby a shifting circuit will rapidly step through the stages not preselected and dwell for a relatively longer selection period at the preselected desired stages to allow selection thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

These and further features and advantages of the invention will be made more apparent in the following specification taken in conjunction with the following drawings, in which:

FIG. **1** is a circuit diagram of one embodiment of the invention in which only manual means for selection are provided;

FIG. **2** is a schematic circuit diagram of a second embodiment of the invention in which the circuit has been altered to enable remote selection in addition to manual selection; and

FIG. **3** is a schematic circuit diagram, partially in block form, of the circuit of FIG. **2** with the addition of a programming circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In FIG. **1**, a circuit diagram of a first embodiment of the memory circuit of this invention is shown. The invention will be described for use in a multiple channel selector for a Varactor tuner, but it should be appreciated that the circuit could be used in any application where it is desired to selectively generate preselected voltages. For purposes of illustration and simplification, the memory circuit is shown in FIG. **1** as comprising only two stages, but of course, any number of similar stages could be added for each voltage level or channel to be selected. Since each of the stages is more or less identical, corresponding elements in each stage have geen given the same reference numeral followed by a subscript a, b, etc., respectively corresponding to the stages A, B, etc., in which it is located.

While the operation of the memory circuit will be described as utilizing a neon lamp, any other similar voltage breakdown device could be used to achieve similar results. Neon lamps are preferred because the light energy generated therefrom can be utilized for giving an indication of the channel which has been activated. The term "voltage breakdown device" is defined, and intended to cover, any device which assumes one impedance state in response to the voltage thereacross exceeding a trigger level and assumes another impedance state in response to the voltage thereacross decreasing below a sustaining level.

Neon lamps suitable for use in this circuit may have a trigger voltage or trigger level of approximately 110 volts and a sustaining voltage or sustaining level of approximately 75 volts. Each of the stages of the memory circuit is connected in parallel from a first voltage source V_{s1} through a common series resistor **20** to a second source of potential V_{p2}, the voltage difference $V_s - V_p$ of which may be approximately 200 volts. A second voltage source V_{s2} may be at a negative 100 volts with respect to the second source of potential or ground reference potential V_{p2}. When power is first applied, the voltage across all of the neon lamps, as lamps **22***a* and **22***b* of FIG. **1** will increase toward the trigger level. However, due to unavoidable inherent variations in the exact trigger level of the lamps, or due to purposeful selection, one of the neon lamps will have a lower trigger level than all of the rest, and that lamp will be the first to turn on and assume a low impedance state. When this lamp turns on, it couples a voltage at terminal **24**, which is substantially below the requisite trigger potential of the other lamps, thereby preventing the remaining lamps from becoming activated. The resistance value of resistor **20**, coupled between the first voltage source V_{s1} and terminal **24**, relative to the total resistance of an activate stage, is chosen to limit the current therethrough to a value for optimizing lamp life and light output.

Assuming lamp **22***a* of Stage A has a lower trigger level than that of lamp **22***b* of Stage B, lamp **22***a* will be the first to turn on, thereby disabling activation of Stage B. When lamp **22***a* turns on, a sufficient amount of base current to turn on a series transistor **26***a* is coupled through lamp **22***a*, diode **28***a* and base bias resistor **30***a*. The base of transistor **26***a* is directly coupled to a regulated source of voltage V_{s4}, and when transistor **26***a* turns on, the collector **26***a* is clamped to regulated supply voltage V_{s4} by the diode action of its base-collector junction. The collector, in turn, is coupled to ground reference potential V_{p2} through a potentiometer resistor **32***a* which provides a suitable means for developing a control voltage. The control voltage is taken off a wiper contact **34***a* of potentiometer **32***a* and coupled through an isolation diode **36***a* to the final output V_o. The output V_o, of course, is dependent upon the setting of wiper contact **34***a* of tuning potentiometer **32***a*. Diode **36***a* is provided to isolate the tuning voltage output V_o from the tuning voltage potentiometer **32***a* when it is not energized.

When the touch contacts **38***b* of the Stage B are now touched, memory Stage B will be activated and memory Stage A, in response thereto, will be deactivated. Specifically, when the touch contacts **38***b* are touched, a circuit is completed from negative supply voltage V_{s2} through a current limiting supply resistor **40**, common terminal **42**, touch contacts **38***b* and series resistor **44***b*, to a second junction **46***b* of neon lamp **22***b*. Junction **46***b* is also coupled to a third source of potential V_{p3}, which may suitably be ground potential, through a capacitor **50***b*. When this circuit is completed, capacitor **50***b* discharges toward negative supply voltage V_{s2} through the circuit until the voltage across junctions **24***b* and **46***b* of neon lamp **22***b* exceeds the trigger level thereof. Neon lamp **22***b* then assumes a low impedance or high conduction state to provide base drive current for a switching transistor **26***b* which has its transconductive inputs in series therewith through an isolation diode **28***b*.

When either lamp **22***a* or **22***b* turns on, it remains on so long as the voltage thereacross exceeds the sustaining level, even though the touch contact is subsequently opened. In effect, the neon lamp may be con-

sidered as a memory element in that it remembers that it was triggered. Diode **28***b* isolates the regulated supply voltage V_{s4} to maximize the rate of decrease of the potential at junction **46***b*.

When neon lamp **22***b* and transistor **26***b* turn on due to closure of touch contacts **38***b*, the common sustaining potential on bus **24** is pulled down to the voltage at junction **46***b*, minus the sustaining voltage of neon lamp **22***b*. This decreases the potential across neon lamp **22***a* sufficiently so that the total voltage across neon lamp **22***a* is below the sustaining level, causing neon lamp **22***a* to assume a high impedance state. When this occurs, base drive is removed from transistor **26***a* which turns off in response thereto, thereby removing regulated voltage source V_{s4} from potentiometer **32***a*.

A principal advantage resulting from the switching transistor in series with the neon lamp is that when the transistor, or any other suitable switching device, turns off, a high impedance is developed between the second junction of the lamp and the second source of potential V_{p2}, thus allowing a voltage approximately equal to the regulated source voltage V_{s4} to be developed at the second junction. This, of course, limits the voltage across the lamp to a value substantially below the requisite trigger level.

When, for example, neon lamp **22***a* and its series switching transistor **26***a* turn off, capacitor **50***a* is charged toward the sustaining potential at junction **24***a* by leakage current from neon lamp **22***a*, to lower the voltage drop across the lamp. Diodes **28***a* and **28***b*, respectively clamp junctions **46***a* and **46***b* to regulated supply voltage V_{s4}, through bias resistors **30***a* and **30***b* so that the voltages thereat cannot increase above regulated voltage source V_{s4}.

If transistor **26***a*, for example, were eliminated from the circuit and replaced by a short circuit, the impedance between junction **46***a* and the second source of potential V_{p2} would be so small in comparison with the high impedance of neon lamp **22***a*, when in its high impedance state, that capacitor **50***a* would be unable to build up a charge from leakage current therethrough. Under these circumstances, the neon lamp, when in its off-state, would have a voltage thereacross dangerously close to the trigger level, and due to tolerances in trigger levels from lamp to lamp, a very unstable situation would exist. However, with transistor **26***a* in series with lamp **22***a*, the potential at junction **46***a* is maintained at a high level such that the total voltage across neon lamp **22***a* is safely below the trigger level. Thus, a more reliable circuit results from the addition of a switching device in series with the neon lamp.

When touch contacts **38***a* are touched, with lamp **22***a* in a high impedance state and lamp **22***b* in a low impedance state, capacitor **50***a* discharges toward the negative trigger potential at junction **42** until the voltage across neon lamp **22***a* again exceeds the trigger level and turns on in response thereto. Neon lamp **22***b* is then turned off in identical fashion as described with regard to the turning off of lamp **22***a*. Also, transistor **26***b* will turn off to remove the regulated voltage source V_{s4} from potentiometer **32***b* while maintaining the voltage at junction **46***b* to avoid inadvertent triggering of lamp **22***b*.

Referring now to FIG. **2**, a second embodiment of the memory circuit is shown which is adapted to enable remote selection or sequential selection in addition to manual or direct selection. Elements in the circuit of FIG. **2** which correspond to elements in FIG. **1** have been given the same designation. Unlike FIG. **1**, the capacitors previously coupled from the second junctions of the lamps to ground reference potential, capacitors **50***a* and **50***b*, are not coupled to ground in the circuit of FIG. **2**, but rather are coupled back to the collector of the series switching transistor of the preceding stage. For example, capacitor **50***b* of Stage B is coupled from junction **46***b* of neon lamp **22***b* to the collector of transistor **26***a* of Stage A.

With the various stages interconnected in this manner, the deactivation of one stage will automatically cause activation of the next succeeding stage. For example, Stage B will be activated in response to the deactivation of Stage A, and Stage C will be activated in response to the deactivation of Stage B. The final stage, Stage D, is interconnected with Channel A through capacitor **50**a so that deactivation of Channel D will cause activation of Channel A.

The touch contacts may be retained in the circuit to allow manual selection, so that an operator may still switch from Channel A to Channel D without passing through Channels B and C in the process. When such a manual selection means is provided and a channel is manually selected, a shift pulse inhibit circuit generally designated by reference numeral **56** is operative to inhibit the shifting pulses so that when, for example, Channel A is turned off by manual activation of Channel D, the shift pulse of Channel A will be prevented from activating Channel B.

In the remote or sequential mode of operation, the shifting circuit **54** is activated by the closure of a single-throw, single pole switch **58** to periodically lower the source of sustaining potential at junction **24** below the requisite level to maintain the neon lamp in a low impedance stage. A neon lamp **60** of shifting circuit **54** coupled to common terminal **24** is selected to have a trigger level less than that of the other neon lamps **22***a*–**22***b* so that, upon coupling of the second junction of neon lamp **60** to ground reference potential, neon lamp **60** assumes a low impedance state notwithstanding the fact that one of the other neon lamps **22***a*–**22***b* is also in a low impedance state. The triggering of neon lamp **60** results in the lowering of the common source of sustaining potential at terminal **24** to a point below which the voltage across all of the other neon lamps is below the sustaining level. This is basically the same type of action that was previously discussed with regard to the turning off of one of the lamps in the circuit of FIG. **1**.

The deactivation of one channel or stage automatically activates the next succeeding stage. For example, if lamp **22***a* is in a low impedance state, the closure of switch **58** results in a deactivation of State A. Transistor **26***a* turns off in response to neon lamp **22***a* turning off. When transistor **26***a* turns off, a negative going shift pulse, which may be considered to be a temporary source of trigger potential, is coupled through capacitor **50***b* to the second junction **46***b* of neon lamp **22***b*. After a certain period of time, depending upon the time constant of the charging circuit of a capacitor **62** of shifting circuit **54**, neon lamp **60** switches off to allow the source of sustaining potential at junction **24** to return to its previous high potential stage. The time constant of the charging circuit of capacitor **50***b* relative to that of capacitor **62** is such that when the sources of sustaining potential recovers to its normal state, the

voltage across neon lamp **22***b* is greater than the trigger level and lamp **22***b* turns on.

Switch **58** of shifting circuit **54** could, of course, be directly connected between the source of sustaining potential and ground and would function to create, upon closure, the required negative going shift pulse. However, this would require a separate actuation of the switch **58** each time it was desired to shift from one channel to the next successive channel.

The parallel circuit of capacitor **62** and a resistor **64**, coupled between switch **58** and ground, forms a relaxation oscillator which oscillates in response to the closure of switch **58.** During remote operation, capacitor **62** begins to charge upon the closure of switch **58.** If switch **58** remains closed, neon lamp **60** will switch to a high impedance state when the voltage across capacitor **62** reaches a sufficient value to decrease the total voltage across the neon lamp **60** below its sustaining level. When neon lamp **60** turns off, capacitor **62** discharges through resistor **64** until the voltage thereacross decreases to a level sufficient to increase the total voltage across neon lamp **60** above its trigger level. When the voltage across neon lamp **60** again exceeds trigger level, neon lamp **60** again turns on and remains on until capacitor **62** again discharges to the requisite voltage necessary to reduce the total voltage across the lamp below its sustaining level. Neon lamp **60** alternately switches on and off in this fashion until switch **58** is opened.

A capacitor **66** coupled between neon lamp **60** and ground is used to compensate for intermittent contact of switch **58.** Should switch **58** open momentarily, neon lamp **60** would turn off if capacitor **66** were not persent. Capacitor **66** temporarily provides an alternate current path so that the current may continue to flow through neon lamp during these momentary switch openings.

The touch contact circuitry is retained in the circuit of FIG. **2** to allow for manual or nonremote selection of the various channels. In manual operation, it is necessary to inhibit the shift pulse to prevent it from turning on the stage adjacent the stage that was on prior to manual selection. This inhibiting action is provided by the shift pulse inhibit circuit **56,** capacitors **68***a*–**68***d* and diodes **70***a*–**70***d*. Capacitors **68***b*, **68***c*, **68***d* and **68***a* are respectively coupled from the collectors of transistors **26***a*–**26***d* to a common input **72** of the shift pulse inhibit circuit **56.** When a neon lamp turns on in response to a manual selection thereof, a positive pulse is coupled from the corresponding capacitor to the shift pulse inhibit circuit **56** which in response thereto clamps a voltage to each of the shift pulse coupling capacitors **50***a*–**50***d* to remove a negative going shift pulse therefrom.

When a neon lamp turns on, a positive pulse is coupled to the corresponding shift pulse inhibit capacitor to the shift pulse inhibit circuit **56,** which, in response thereto, clamps a voltage to each of the shift pulse coupling capacitors to remove the negative going shift pulse therefrom. For example, assume neon lamp **22***a* is on and it is desired to turn on neon lamp **22***c*. The operator upon touching touch contact **38***c* will turn on lamp **22***c*, as previously explained. Upon lamp **22***c* turning on, a positive pulse is coupled across resistor **74** of shift pulse inhibit circuit **56** through capacitors **50***c* and **68***c*. When neon lamp **22***c* turns on, the source of sustaining potential at terminal **24** rapidly decreases to turn off neon lamp **22***a*. Without a shift pulse inhibit circuit, a negative going shift pulse would be coupled through capacitor **50***b* to turn on neon lamp **22***b* when neon lamp **22***a* and transistor **26***a* turn off.

The shift pulse inhibit circuit **56** prevents this from happening. In response to the positive pulse coupled across resistor **74,** a transistor **76** turns on to discharge a capacitor **78** through a collector resistor **80** of transistor **76.** After a short time delay determined by the RC time constant of capacitor **78** and resistor **80,** a transistor **82** coupled through a resistor **84** turns on to shortout resistor **86** coupled in parallel therewith to provide a low impedance path from regulated supply voltage V_{84} to the anodes of each of the diodes **70***a*–**70***d*. Capacitors **50***b* and **68***b* are charged through diode **70***b* and the relative time constants are such that the positive going inhibit pulse overrides the negative going shift pulse to prohibit turn on of neon lamp **22**b. That is, although the shift pulse does occur, it can have no effect until the bus **24** recovers. The capacitors are charged before the recovery of the bus. Thus, the negative shift pulse does not appear at junction **46***b* at the time required to trigger on neon lamp **22***b*.

The time delay established by capacitor **78** and resistor **80** is provided so that neon lamp **22***c* will be completely ionized before its junction is coupled to regulated supply voltage V_{84} through transistor **82.** This prevents neon lamp **22***c* from being turned off by the shift pulse inhibit circuit action. Base feed resistor **84** of transistor **82** is provided to delay the turnoff time of transistor **82** to insure that the shift pulse is completely inhibited.

Turning now to FIG. **3**, a circuit diagram of a programming circuit for the sequential selection circuit of FIG. **2** is shown. The purpose of this programming circuit is to facilitate selection of only desired stages of the memory circuit. It is contemplated that where the memory circuit is used to control a Varactor tuner in a television receiver, a separate memory stage will be provided for selecting each of the 12 basic VHF channels, and one or more UHF channels. The programs in any particular area in which the receiver is situated are usually transmitted on less than all of the channels. Since it will never be desired to select these channels for viewing, the programming circuit provides a means for rapidly stepping through the undesired channels, and only pausing upon activation of a preselected desired channel in order to allow selection thereof by termination of the stepping process. For example, in an area where programs are available on channels **2, 5,** and **7,** but not available on intermediate channels **3, 4** and **6,** the programming circuit, upon actuation of the shifting circuit, would cause the shifting circuit to rapidly step through channels **3** and **4,** pause at channel **5,** rapidly step through channel **6,** and again pause at channel **7,** thereby facilitating selection of only channels **2, 5** and **7.** Switches are provided so that the programming circuit may readily be adapted to the particular broadcast area in which the receiver is situated.

Referring specifically to FIG. **3,** the basic circuit of FIG. **2** is shown with Stage B through State N, the last stage of the memory circuit, and the shift pulse inhibit circuit **56** shown in block form. This circuit operates as already discussed above with regard to FIG. **2.** The programming circuit generally designated by reference numeral **80** includes two basic circuits, a plurality of program switches **82***a*–**82***n*, respectively associated with

Stages A–N to preselect the desired ones of these stages, and a switching transistor **84** for altering the selection period of each of the stages in accordance with the established program.

Each program switch **82** has one side coupled to the collector of the series switching transistor **26** of the corresponding stage through a resistor **86**, and has the other side directly coupled to the base of transistor **84**. As previously explained, the stepping rate of the neon memory is determined by the discharge time of capacitor **62** which, in turn, is determined by the effective resistance in parallel therewith. When transistor **84** is in a high impedance state, the effective resistance in parallel with capacitor **62** is the value of resistor **64**, and the discharge time of capacitor **62** is relatively long. When transistor **84** is in a low impedance state, resistor **86** is coupled in parallel with resistor **64** to substantially reduce the effective resistance in parallel with capacitor **62**, and, thus, the discharge time of capacitor **62** is substantially decreased to increase stepping rate.

The desired channels are preselected by placing their programming switch in an open position. When a program switch is in an open position, the activation of the corresponding stages, of course, has no effect upon transistor **84**. Transistor **84** thus remains in its normally high impedance state, to enable selection of these stages for a relatively long selection period.

Stages which are not preselected, such as illustrated for Stage A, have their program switches in a closed position. When a stage not selected is activated and its series switching transistor is turned on, a positive pulse is coupled from the collector of the series switching transistor through the base resistor **86** and the closed programming switch **82** to the base of transistor **84**, which turns on in response thereto to couple resistor **86** in parallel with capacitor **62**. Capacitor **62** rapidly discharges through resistor **86** to raise the voltage across neon lamp **60** above its trigger level. This rapidly turns off the undesired activated stage. The deactivation of this stage, as previously explained, causes activation of the next succeeding stage, which turns on the response thereto. This next successive stage is immediately deactivated, or is allowed to remain activated for a relatively longer selection period, depending upon whether its programming switch is in a closed or open position, respectively.

I claim:

1. In a memory circuit having a plurality of individually selectable stages for generating a plurality of different DC output voltages, each stage comprising a variable impedance and a voltage breakdown device triggerable from a low to a high state of conduction when a voltage thereacross exceeds a trigger potential, the improvement in each stage for preventing inadvertent triggering of the voltage breakdown device, comprising:

switching means having a pair of electrodes with a first state and a second state of conduction therebetween under control of a control electrode;

first circuit means for connecting said pair of electrodes between said voltage breakdown device and said variable impedance; and

second circuit means coupled to said control electrode and responsive to said breakdown device assuming its high conduction state for switching said switching means to its first state to continuously apply a fixed voltage across the variable impedance in order to gen-erate one of said DC output voltages, said second circuit means being further responsive to said breakdown device assuming its low conduction state for switching the switching means to its second state to remove the fixed voltage from the variable impedance and to maintain the voltage across the breakdown device substantially below the trigger potential.

2. The memory circuit of claim **1** wherein said circuit means couples said switching means in series with said breakdown device.

3. The memory circuit of claim **1** wherein said first and second states of the switching means respectively comprise high and low conduction states.

4. In a memory circuit having a plurality of individually selectable, parallel connected stages, each stage comprising a series connection of a voltage developing impedance and a voltage breakdown device having first and second junctions and triggerable from a low to a high state of conduction when a voltage thereacross exceeds a trigger potential, the improvement in each stage for preventing inad-vertent triggering of the voltage breakdown device, comprising:

switching means having a first state and a second state of conduction and connected with said voltage breakdown device and said voltage developing impedance; a source of sustaining potential coupled to one of the junctions of said breakdown device; and circuit means responsive to said breakdown device assuming its high conduction state for switching said switching means to its first state to apply a fixed voltage across the voltage developing impedance, said circuit means being further responsive to said breakdown device assuming its low conduction state for switching the switching means to its second state to remove the fixed voltage from the voltage developing impedance and to raise the potential at the other junction of the breakdown device toward the sustaining potential in response to said switching means switching to said low conduction state in order to maintain the voltage across the breakdown device substantially below the trigger potential.

5. The memory circuit of claim **4** including means for altering the sustaining potential toward the potential at the other junction to lower the voltage across said breakdown device below the sustaining level, whereby said breakdown device, if in the high conduction state, will switch to the low conduction state in response thereto.

6. The memory circuit of claim **1** including means for generating a trigger signal, and means for temporarily coupling the trigger signal to the breakdown device to switch to the high conduction state.

7. The memory circuit of claim **6** wherein said temporary coupling means comprises a switch.

8. The memory circuit of claim **6** wherein said temporary coupling means comprises a capacitor.

9. The memory circuit of claim **6** wherein said generating means comprises a second breakdown device.

10. The memory circuit of claim **6** including a second breakdown device switchable from a second to a first state, said temporary coupling means coupling said source of trigger potential to said first breakdown device in response to said second breakdown device switching to its first state.

11. A selector circuit for a plural stage memory having at least first, second and third stages, comprising:

individual selector means including first selection means for activating selected ones of said stages;

sequential selector means for sequentially activating said stages including coupling means coupled between adjacent stages for activating each stage in response to deactivation of the stage precedent thereto; and

inhibit means responsive to activation of any stage by said individual selector means for preventing said coupling means from activating said stages.

12. The selector circuit of claim 11 wherein said sequential selector means includes means for deactivating any previously activated stage to initiate sequential activation of the next stage by said coupling means.

13. The selection circuit of claim 11 wherein said individual selector means includes deactivation means responsive to activation of a selected one of said stages for deactivating any other previously activated stage.

14. The selector circuit of claim 13 wherein said sequential selector means includes means for deactivating any previously activated stage to initiate sequential activation of the next stage by said coupling means.

15. The selector circuit of claim 11 wherein said sequential selector means activates successive stages for selection only during corresponding successive selection periods, program means for facilitating selection of only desired stages including means for preselecting said desired stages, and means for establishing a longer selection period for the preselected stages than for the stages not preselected.

16. The program means of claim 15 in which said establishing means includes

means responsive to activation of a stage not preselected for establishing a first rate of activation; and

means responsive to activation of a preselected stage for establishing a second rate of activation slower than said first rate.

17. The program means of claim 15 in which said preselecting means includes for each stage a program switch having two states, each stage being preselected when its program switch is in one of said stages and not preselected when its program switch is in the other of said states.

18. The program means of claim 17 in which each program switch is commonly coupled with said establishing means.

19. In a circuit for selecting individual stages of a plural stage memory in which successive stages are enabled for selection only during corresponding successive selection periods, program means for facilitating selection of only desired stages, comprising:

means for preselecting said desired stages; and

means for establishing a longer selection period for the preselected stages than for the stages not preselected, including an oscillator and means for altering the frequency of the oscillator in accordance with the stages which are preselected.

20. The program means of claim 19 in which said frequency altering means includes a semiconductor switch responsive to activation of a preselected stage for controlling the oscillator to oscillate at a first frequency and responsive to activation of a stage not preselected for controlling the oscillator to oscillate at a second frequency which is greater than said first frequency.

21. A selector circuit for a plural stage memory having at least first, second, and third stages, comprising:

ring circuit means connecting said stages for sequential activation of each stage in a predetermined order;

sequential selector means for activating said ring circuit means and for deactivating said ring circuit means at any desired stage which is to be selected; and

individual selector means for directly activating said desired stage which is to be selected without sequential activation of each stage in said predetermined order.

22. The selector circuit of claim 21 wherein said ring circuit means includes coupling means for each stage and coupled to an adjacent stage for activating each stage in response to deactivation of the stage precedent thereto, said individual selector means includes trigger means associated with each stage and individually actuable to activate the associated stage, and inhibit means effective during operation of said trigger means for effectively disabling said coupling means.

23. The selector circuit of claim 22 wherein said coupling means generates a first shift pulse of one polarity for activating the next adjacent stage, and said inhibit means is effective to generate a second shift pulse of opposite polarity, said second shift pulse overriding said first shift pulse.

24. The selection circuit of claim 21 wherein each memory stage comprises a voltage breakdown device triggerable from a first to a second conduction state in response to a trigger potential and a variable resistance for generating a DC output voltage thereacross when said device is in one conduction state, said individual selector means includes a manually actuable switch means for each stage, a source of said trigger potential coupled to all of said switch means, and a circuit individually connecting each switch means to the device of the associated stage for triggering thereof when the associated switch means is manually actuated.

* * * * *