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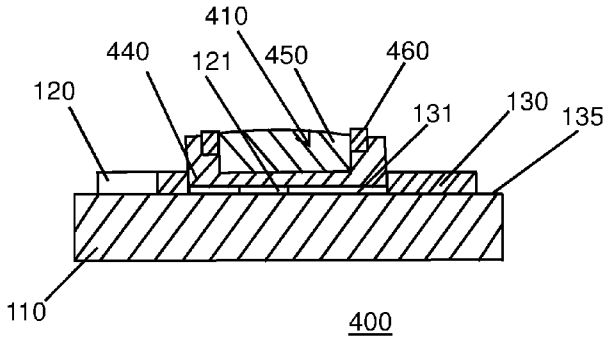

Fig. 4

(57) Abstract: A method of operating a magneto-resistive (MR) Field Effect Transistor and a MR Field Effect Transistor are described. The MR Field Effect Transistor has first and second magnetic electrodes arranged to define a in a semiconductor material. A gate terminal is separated from the semiconductor material by a gate layer and a length of the channel is greater than an effective thickness of the gate layer.

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MAGNETO-RESISTIVE FIELD EFFECT TRANSISTOR

[0001] This invention relates to Magneto-Resistive (MR) transistors and in particular to MR Field Effect Transistors (FETs).

BACKGROUND

[0002] Magneto-Resistive (MR) transistors have a MR channel disposed between electrodes. The MR channel's electrical characteristics are dependent on magnetic field or fields influences and thus current flowing through a MR transistor may be controlled by varying a magnetic field strength passing through the transistor.

[0003] When considering MR FETs, problems exist with their relatively low tolerance to fabrication inaccuracies and the MR effect or such transistors is relatively low.

[0004] It is an object of embodiments of the invention to at least mitigate one or more of the problems of the prior art.

BRIEF SUMMARY OF THE DISCLOSURE

[0005] In accordance with one embodiment there is provided a magneto-resistive (MR) Field Effect Transistor, comprising: first and second magnetic electrodes arranged to define a channel having a length there-between in a semiconductor material; and a gate terminal separated from the semiconductor material by a gate layer having an effective thickness, wherein the length of the channel is greater than the effective thickness of the gate layer.

[0006] In accordance with one embodiment there is provided a method of operating a magneto-resistive (MR) Field Effect Transistor, the transistor comprising source and drain magnetic electrodes arranged to define a channel having a length there-between in a semiconductor material, and a gate terminal separated from the semiconductor material by a gate layer having an effective thickness, wherein the length of the channel is greater than the effective thickness of the gate layer, the method comprising: applying a primary voltage across the source and drain magnetic electrodes; applying a gate voltage to the gate terminal to cause a current to flow between the magnetic electrodes; and applying a magnetic field to the transistor to thereby change a magnetisation polarisation of at least one of the magnetic electrodes thereby varying the current flow there-between.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Embodiments of the invention will now be described by way of example only, with reference to the accompanying figures, in which:

[0008] Figure 1 shows a plan view of a partially formed magneto-resistive (MR) Field Effect Transistor (FET) according to an embodiment of the invention;

[0009] Figure 2 shows a cross sectional side view the partially formed MR Field Effect Transistor through 2-2' of Figure 1;

[0010] Figure 3 shows a perspective view of the partially formed MR Field Effect Transistor of Figure 1, according to an embodiment of the invention;

[0011] Figure 4 shows a cross sectional side view, through 2-2', of a MR Field Effect Transistor formed from the partially formed MR Field Effect Transistor of Figure 1, according to an embodiment of the invention;

[0012] Figure 5 shows a plan view of the MR Field Effect Transistor of Figure 4, according to an embodiment of the invention;

[0013] Figure 6 shows an enlarged cross sectional side view, through 6-6', of the MR Field Effect Transistor of Figure 5;

[0014] Figure 7 shows a cross sectional side view, through 2-2', of a MR Field Effect Transistor formed from the partially formed MR Field Effect Transistor of Figure 1, according to another embodiment of the invention;

[0015] Figure 8 is a plan view illustrating an alternative configuration of source and drain electrodes, according to another embodiment of the present invention;

[0016] Figure 9 is a plan view illustrating another alternative configuration of source and drain electrodes, according to another embodiment of the present invention;

[0017] Figure 10 shows a plan view of a MR Field Effect Transistor according to a further embodiment of the present invention; and

[0018] Figure 11 is a flow chart illustrating a method of operating a MR Field Effect Transistor, according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0019] Referring to Figures 1 to 3 there is shown a partially formed magneto-resistive (MR) Field Effect Transistor (FET) 100 according to an embodiment of the invention. The partially formed magneto-resistive (MR) Field Effect Transistor 100 comprises a substrate 110 which is typically formed of Silicon base with an upper oxide layer, although it will be realised that other insulating or dielectric substrates may be used, for example Magnesium Oxide or Gallium Arsenide. A source terminal 120 and a drain terminal 130 are located

(typically by a masked metal depositing process) on an upper surface 135 of the substrate 110 and are spaced apart by a minimum channel length 125 which is a minimum distance between the source and drain electrodes 121, 131.

[0020] The source and drain terminals 120, 130 provide electrical connection to their respective source electrode 121 and drain electrode 131 that are formed (located) on the upper surface 135. The upper surface 135 is typically planar and the source and drain terminals 120, 130 may be formed from gold or titanium although it will be appreciated that other electrically conductive materials may be used.

[0021] The source and drain electrodes 121, 131 are magnetic electrodes that have imbalanced conduction electron spin polarizations. Furthermore, the electrodes 121 and 131 are configured to have different, magnetic responses when under the influence of a magnetic field. Consequently, when under the influence of a magnetic field, the imbalanced spin polarisation of each of the electrodes 121 and 131 will be affected in a manner that is dependent on the polarisation and a threshold level of the applied magnetic field. As such, the source electrode 121 may have a first magnetic response MR1 and the drain electrode 131 may have a second magnetic response MR2 that is different than the first magnetic response MR1.

[0022] The electrodes 121, 131 may be formed from ferromagnetic material, a ferrimagnetic material (e.g. ferrites) or an anti-ferromagnetic material. The first and second magnetic responses MR1, MR2 of the electrodes 121, 131 allow the electrodes to have different magnetisation configurations. The source and drain electrodes 121, 131 are, in one embodiment, nanowires which are formed on the upper surface 135, such as by patterning. It will be appreciated, however, that the electrodes 121, 131 may be formed in other shapes which assume different magnetic responses MR1, MR2.

[0023] In other embodiments the different magnetic responses MR1, MR2 may be controlled by the inclusion of, for instance, a magnetic domain wall in one of the electrodes 121, 131. The domain wall may be moved, for example back and forth, with an applied magnetic field or electric current through the respective electrode to change the magnetisation of the electrode region close to its neighbour electrode while leaving the magnetisation of the neighbour electrode unchanged.

[0024] The domain wall can be provided by the inclusion of a pad region 122 forming part of electrode 121 which allows for separating the magnetic fields used to switch each electrode 121, 131. As shown, the pad region 122 is arranged on an inner end of the source electrode 121 which is proximal its respective terminal (the source terminal 120 in this example) and which is distal from the end of the drain electrode 121. The pad region 122 is a region of the electrode 121 of greater width than a region of the electrode 121 distal from its respective terminal. The smaller aspect ratio (greater width against length)

of the pad 122 leads to this section of the electrode 121 reversing its magnetisation at lower fields than the electrodes 121, 131. This smaller aspect ratio results in a magnetic domain wall being formed at a junction of the pad 122 and electrode 121, which is then injected into the electrode 121 at a slightly higher magnetic field. However, this is arranged to be a much lower field than required to switch an electrode with no pad. Used in this manner, the inclusion of the pad 122 creates a significant reduction in switching field of the electrode 121, 131 to which it is attached. This can be used with or without electrodes 121, 131 having different widths to separate their switching fields (magnetic responses).

[0025] The electrodes 121, 131 may be formed from a nickel-iron alloy, for example $Ni_{80}Fe_{20}$ although this is merely exemplary and other materials may be used. The electrodes in one embodiment 121, 131 are arranged such that magnetisation is caused to lie along a length of the electrodes 121, 131. In this way, the magnetic configuration of the two electrodes 121, 131 when considered together may be one of parallel or anti-parallel in the described embodiment. However in other embodiments the electrodes 121, 131 may be arranged to have another magnetic configuration, such as that which exhibits a gradual switching response. This may include magnetisation becoming rotated towards a magnetic hard axis due to an applied magnetic field. In this way a linear response of magnetisation to the applied magnetic field can be obtained.

[0026] In one embodiment, one of the source and drain electrodes 121, 131 is configured to be wider than the other electrode 121, 131. The difference in the widths causes the electrodes 121, 131 to have different switching fields (magnetic responses).

[0027] In one embodiment each electrode 121, 131 has a length of around 100 μm, although it will be realised that other lengths may be used. The width of each electrode 121, 131 is in the nanoscale (nm) region to ensure single magnetic domain configuration within the electrode 121, 131 given the length of each electrode 121, 131 in one embodiment is about 100 μm. However it will be realised that the width of the electrodes is not limited to the nanoscale region. Furthermore, it is envisaged that the each electrode 121, 131 may comprise multilayer wires made of different layers of magnetic and non-magnetic materials as long as the overall effect is to maintain a conduction electron spin polarization.

[0028] In one embodiment the drain electrode 131 has a width of 500 nm and the source electrode a width of 1000 nm. It will be appreciated that other width configurations may be used e.g. 100 nm/200 nm, 200/400nm, 300/600 nm, 400/800 nm. A narrower electrode provides a higher switching field and greater resistance. The thickness or depth of each electrode is around 30 nm. However the thickness may be in the range from 20 nm up to 100 nm, although this range is not limiting and other thicknesses may be envisaged. The lower the thickness of the electrode, the higher the electrical resistance. Electrodes

thicker than the minimum channel length 125 may be problematic due to interfering with the transistor operation.

[0029] Referring to Figures 4 to 6 there is illustrated a MR Field Effect Transistor 400 formed from the partially formed MR Field Effect Transistor 100, in accordance with a preferred embodiment of the present invention. The MR Field Effect Transistor 400 includes a semiconductor material 440, such as silicon, deposited to cover the source and drain electrodes 121, 131. The semiconductor material 440 is deposited to also form a channel 510 between the source and drain electrodes 121, 131 at least at the region of the minimum channel length 125.

[0030] The semiconductor material 440 may also at least partly cover the source and drain terminals 120, 130. In one embodiment the semiconductor material 440 is an organic semiconductor material. The organic material may be poly(alkyl thiophene) (P3HT). In other embodiments the semiconductor material 440 may be formed from an inorganic semiconductor material, for example a zinc oxide (ZnO) may be useful. The semiconductor material 440 is provided to selectively allow conduction between the source and drain electrodes 121, 131 via the channel 510 which may be doped with any suitable impurity. In this embodiment, semiconductor material 440 is deposited by a masking process that forms a rectangular well 410 with an internal well rim upon which is deposited an electrically conductive material such as copper to form a gate terminal 460.

[0031] The MR Field Effect Transistor 400 includes an electrolyte 450 deposited in the rectangular well 410 and contacts the gate terminal 460 and thus forms a gate electrode. The electrolyte 450 may be a liquid located on the semiconductor material 440 directly above the channel 510. However, as will be described other arrangements without a liquid electrolyte are envisaged.

[0032] The electrolyte 450 may be an ionic liquid such as water, although it will be realised that other liquid and solid electrolyte materials may be used. For example, solid electrolytes such as polystyrene sulfonic acid, Nafion, PEO/LiClO3 or ionic liquids which may be particularly useful for use with higher gate voltages such as those above 4V. As will be apparent to a person skilled in the art, the well 410 can be covered by any suitable encapsulating material so that the electrolyte 450 is sealed in the well 410.

[0033] The gate terminal 460 allows a gate voltage to be applied to the electrolyte 450. When a sufficient voltage is applied to the gate terminal 460 there is induced an electric double layer at the interface of the liquid electrolyte 450 and semiconductor material (layer) 440, thereby creating a strong electric field in the channel 510. In embodiments of the invention, the minimum channel length 125 is greater than an effective thickness of the gate medium.

[0034] The gate electrode in one embodiment may have a spacing of less than 120nm from the upper surface of the semiconductor layer 440. Since such an arrangement may be difficult to fabricate, the use of a liquid electrolyte allows the physical effective thickness of the gate electrode to be greater than the separation between the source and drain electrodes 121, 131.

[0035] When an electrolyte 450 is arranged between the gate terminal 460 and semiconductor material 440, an effective thickness of the gate medium is determined by a thickness of an electric double layer (EDL). The EDL is formed by the presence of the electrolyte 450 upon the semiconductor material 440, as will be appreciated. The EDL is of the order of molecular dimensions even when the physical distance between the gate terminal 460 and semiconductor material 440 is large. Thus, the effective thickness is just the thickness of one of the electric double layers, which is extremely thin and is approximately the size of a single solvated ion (which is just a few Angstroms or a nanometre at most). Accordingly, the electrolyte 450 causes the effective gate thickness to be less than the channel length between the source and drain electrodes 121, 131 as determined by the EDL thickness. More specifically, in operation the effective thickness of the gate layer is a layer over which substantially all of a voltage applied to the gate electrode drops which is normally at an interface between the electrolyte 450 and the semiconductor material 440.

[0036] The channel 510 is defined in the region between adjacent sides of the elongate electrodes 121, 131 having a minimum separation (the minimum channel length 125). However in other embodiments the channel 510 may be formed, for example, between proximal ends of the electrodes 121, 131. In an exemplary embodiment the separation is 120nm although it will be realised that other separation distances may be selected down to an atomic separation distance. The separation between the electrodes 121, 131 is a length of the channel 510 via which conduction controllably occurs in the Field Effect Transistor 400.

[0037] Without wishing to be bound by the foregoing, it is suggested that the large MR values arise from an applied voltages creating a change in the magnetic properties of a very thin (few atomic layers) layer. The change may affect (a) the layers in the electrodes 121, 131 closest to the electrode-semiconductor interface and/or (b) the electronic and magnetic nature of the electrode-semiconductor interface itself. The applied voltage may also affect the nature of electron propagation in the semiconductor and change its spin-diffusion length. So, far this has been observed as changes in 'magnetocrystalline anisotropy', i.e. how strongly different directions of magnetisation are preferred. One possibility with our effect is that the applied voltage is changing the Fermi energy level near the surface of the magnetic electrodes, which will change the 'spin polarisation' of

conduction electrons in this surface region. It is also possible that the applied voltage induces surface chemical changes that affect the magnetisation.

[0038] Figure 7 illustrates another embodiment of a MR Field Effect Transistor 700 formed from the partially formed MR Field Effect Transistor 100, according to another embodiment of the present invention. The MR Field Effect Transistor 700 includes a semiconductor material 740, such as silicon, deposited to cover the source and drain electrodes 121, 131. The semiconductor material 740 is deposited to also form a channel 710 between the source and drain electrodes 121, 131 at least at the region of the minimum channel length 125. A gate terminal 760 is arranged upon an insulating gate medium 650 to form a gate electrode. The insulating gate medium 750 is formed on a semiconductor material 740 and the semiconductor material 740 may be doped with any suitable impurity.

[0039] Figure 8, is a plan view illustrating an alternative configuration 800 of source and drain electrodes 821, 831, according to another embodiment of the present invention. In this configuration the minimum channel length 825 is between the proximal ends of the electrodes 821, 831.

[0040] Figure 9, is a plan view illustrating another alternative configuration 900 of source and drain electrodes 921, 931, according to another embodiment of the present invention. In this configuration distal ends of the electrodes 921, 931. In this configuration the minimum channel length 925 is between adjacent sides of the electrodes 921, 931.

[0041] Figure 10 shows a plan view of a further embodiment of an MR FET 1000 according to another embodiment of the present invention. The MR FET 1000 has a co-planar gate terminal 1060 fabricated on the same substrate 110 as magnetic electrodes 1021 and 1031. A semiconductor material 1040 covers both magnetic electrodes 1021 and 1031 and a solid or gel based electrolyte layer 1050 covers the semiconductor material 1040 and the gate terminal 1060. However, a liquid electrolyte can be employed if a well is fabricated for the gate electrode. This arrangement reduces the number of layers required to fabricate the MR FET but its operation will remain the same as all other MR FETs described herein.

[0042] In some embodiments, such as those shown in Figure 7 and 10, the effective thickness of the gate medium may be dependent on the physical thickness “D” of the gate medium or gate insulator material 750, 1050, between the semiconductor material 440, 1440 and gate terminal 460, 1060. More specifically, the effective thickness of the gate insulator material is the physical thickness “d” of the gate insulator material divided by the dielectric constant K of the gate insulator material.

[0043] Figure 11 is a flow chart illustrating a method 1100 of operating a MR Field Effect Transistor, according to an embodiment of the present invention. The method 1100, by

way of example only, will be explained with reference to the MR Field Effect Transistor 400. After a start block 1110 there is performed, at a block 1120, an applying of a primary voltage (VDS) across the magnetic electrodes 121, 131. Next at a block 1130 there is performed an applying of a gate voltage to the gate electrode (gate terminal 460) to cause a current (IDS) to flow between the magnetic electrodes 121, 131. At a block 1140 a magnetic field B is applied to the Field Effect Transistor to thereby affect (change) a magnetisation polarisation of at least one of the magnetic electrodes 121, 131 thereby varying the current IDS flow there-between. Furthermore, the current IDS flow is responsive to the gate voltage VDS and thus the current IDS flow cane be controlled by varying either the gate voltage VDS or the magnetic field B. The method 1100 then terminates at a block 1150.

[0044] Embodiments of the invention may be used as a magnetic field sensor. In such embodiments one of the magnetic electrodes 121, 131 either source or drain may be more sensitive to any magnetic field than the other. The device may have a linear response to an applied magnetic field. However, embodiments of the device may comprise an 'exchange biased' sense layer that is arranged to return to a fixed magnetisation state once the magnetic field is removed and switches digitally above a certain threshold field value in a particular direction. In any case, the analogue field sensor (analogue in the sense of a gradual change in signal) is probably the easiest application of this device to achieve.

[0045] In some embodiments the MR Field Effect Transistor may be used as a magnetically-reconfigurable electronic component. For example a magnetically-operated switch which may be used a circuit e.g. field-programmable gate array.

[0046] Advantageously, the MR Field Effect Transistor exhibits a significant variation in the magneto-resistance effect whereby an electrical resistance of the Field Effect Transistor between two terminals 121, 131 changes in response to variations in a magnetic field applied to the Field Effect Transistor.

[0047] All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

[0048] Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

[0049] The invention is not restricted to the details of any foregoing embodiments. The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed. The claims should not be construed to cover merely the foregoing embodiments, but also any embodiments which fall within the scope of the claims.

[0050] Throughout the description and claims of this specification, the words "comprise" and "contain" and variations of them mean "including but not limited to", and they are not intended to (and do not) exclude other moieties, additives, components, integers or steps. Throughout the description and claims of this specification, the singular encompasses the plural unless the context otherwise requires. In particular, where the indefinite article is used, the specification is to be understood as contemplating plurality as well as singularity, unless the context requires otherwise.

[0051] Features, integers, characteristics, compounds, chemical moieties or groups described in conjunction with a particular aspect, embodiment or example of the invention are to be understood to be applicable to any other aspect, embodiment or example described herein unless incompatible therewith. All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive. The invention is not restricted to the details of any foregoing embodiments. The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A magneto-resistive (MR) Field Effect Transistor, comprising:

first and second magnetic electrodes arranged to define a channel having a length there-between in a semiconductor material; and

a gate terminal separated from the semiconductor material by a gate layer having an effective thickness,

wherein the length of the channel is greater than the effective thickness of the gate layer.

2. The MR Field Effect Transistor of claim 1, wherein the gate terminal includes an electrolyte and the gate layer is an interface between the electrolyte and a semiconductor material.

3. The MR Field Effect Transistor of claim 2, wherein the electrolyte is a liquid or a gel or a solid.

4. The MR Field Effect Transistor of claim 2 or 3, wherein the effective thickness of the gate layer is determined by an electric double layer formed by the interface between the electrolyte and a semiconductor material.

5. The MR Field Effect Transistor of claim 4, wherein the electric double layer is a layer over which substantially all of a voltage applied to the gate electrode drops.

6. The MR Field Effect Transistor of claim 1, wherein the gate layer is a gate insulator material and the effective thickness of the gate layer is a physical thickness of the gate insulator material divided by the dielectric constant of the gate insulator material.

7. The MR Field Effect Transistor of any preceding claim, wherein the first and second electrodes have first and second magnetic responses.

8. The MR Field Effect Transistor of claim 7, wherein the first and second electrodes have first and second shapes.

9. The MR Field Effect Transistor of claim 8, wherein one of the first and second electrodes has a greater width than the other, respective, electrode.

10. The MR Field Effect Transistor of any preceding claim, wherein the first and second magnetic electrodes are first and second elongate nanowires.

11. The MR Field Effect Transistor of any of claims 7 to 10, wherein the first electrode comprises a portion arranged to have a lower magnetic switching field.

12. The MR Field Effect Transistor of any preceding claim wherein the channel is arranged between the first and second electrodes.

13. The MR Field Effect Transistor of claim 12 when dependent upon claim 10, wherein the channel is arranged between adjacent sides of the nanowires.

14. The MR Field Effect Transistor of any preceding claim wherein the semiconductor material is an organic material.

15. The MR Field Effect Transistor of any preceding claim wherein the gate terminal is fabricated in the same plane as the first and second magnetic electrodes.

16. A magnetic field sensor comprising the MR Field Effect Transistor of any preceding claim.

17. A method of operating a magneto-resistive (MR) Field Effect Transistor, the transistor comprising source and drain magnetic electrodes arranged to define a channel having a length there-between in a semiconductor material, and a gate terminal separated from the semiconductor material by a gate layer having an effective thickness, wherein the length of the channel is greater than the effective thickness of the gate layer, the method comprising:

applying a primary voltage across the source and drain magnetic electrodes;

applying a gate voltage to the gate terminal to cause a current to flow between the magnetic electrodes; and

applying a magnetic field to the transistor to thereby change a magnetisation polarisation of at least one of the magnetic electrodes thereby varying the current flow there-between.

18. The method of claim 17, wherein the magnetic field causes the magnetic electrodes to assume different magnetisation configurations.

19. The method of any of claims 17 or 18, wherein the current flow is responsive to the gate voltage.

20. The method of any of claims 17 to 19, wherein the gate terminal is fabricated in the same plane as the first and second magnetic electrodes.

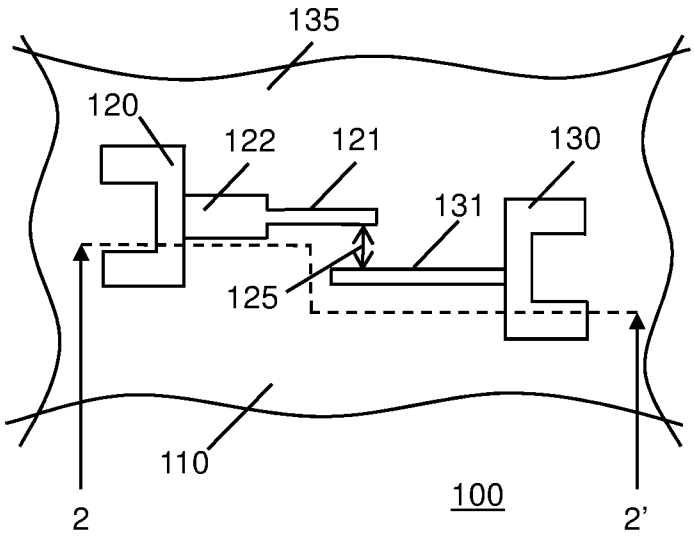
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Fig. 1

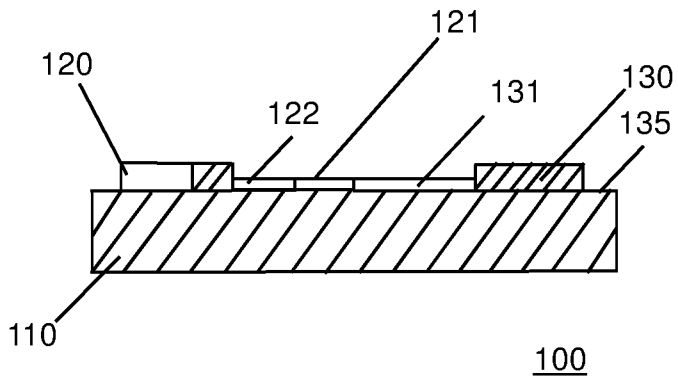
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Fig. 2

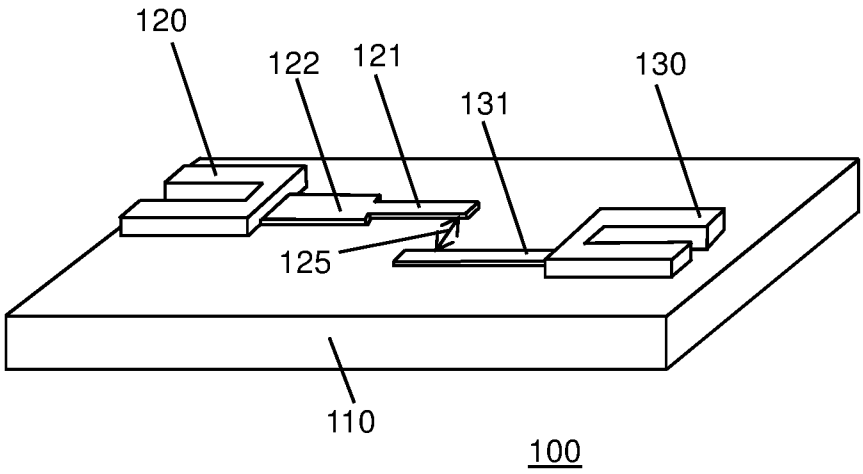
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Fig. 3

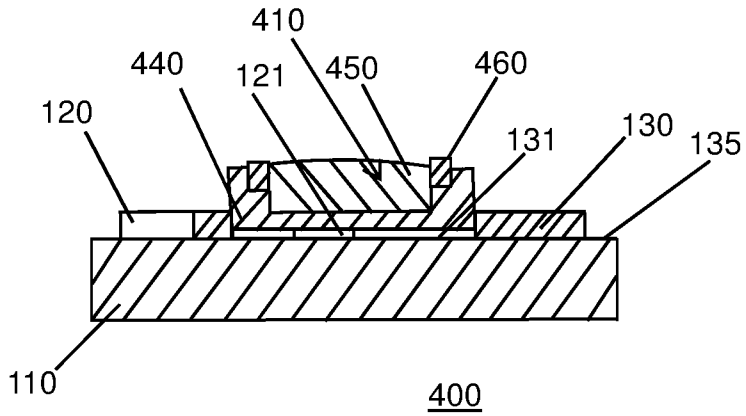
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Fig. 4

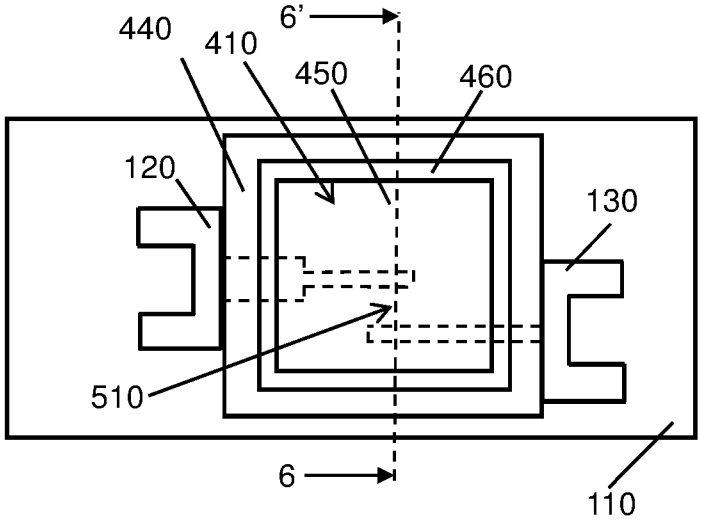
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Fig. 5

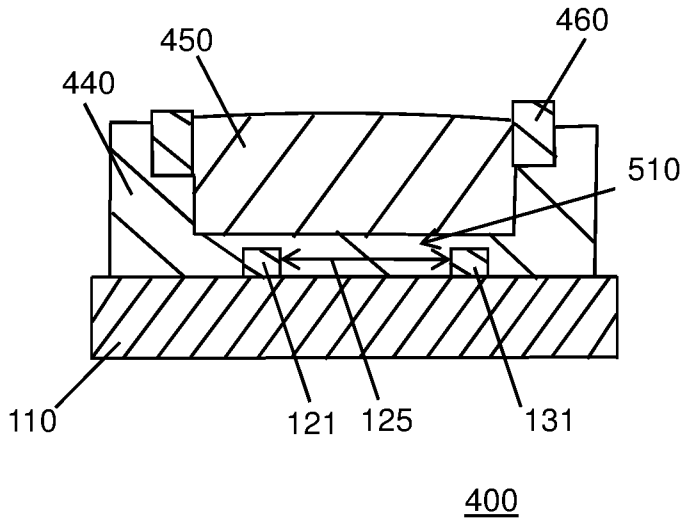
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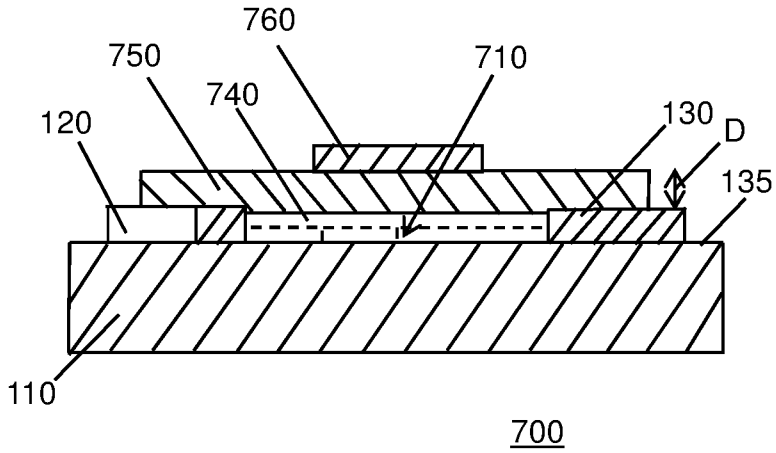
Fig. 6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700

Fig. 7

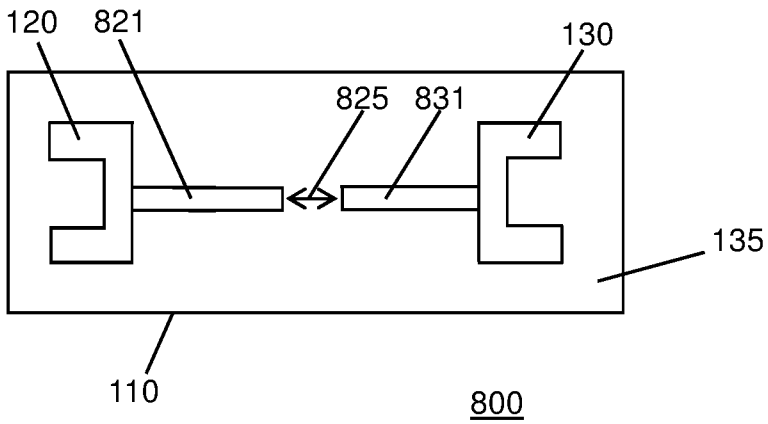
120
821
130
825
831
135
110
800

Fig. 8

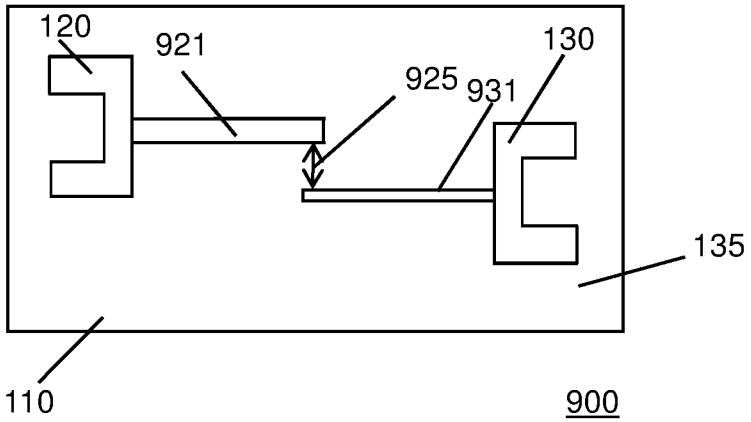
120
921
925
931
130
135
110
900

Fig. 9

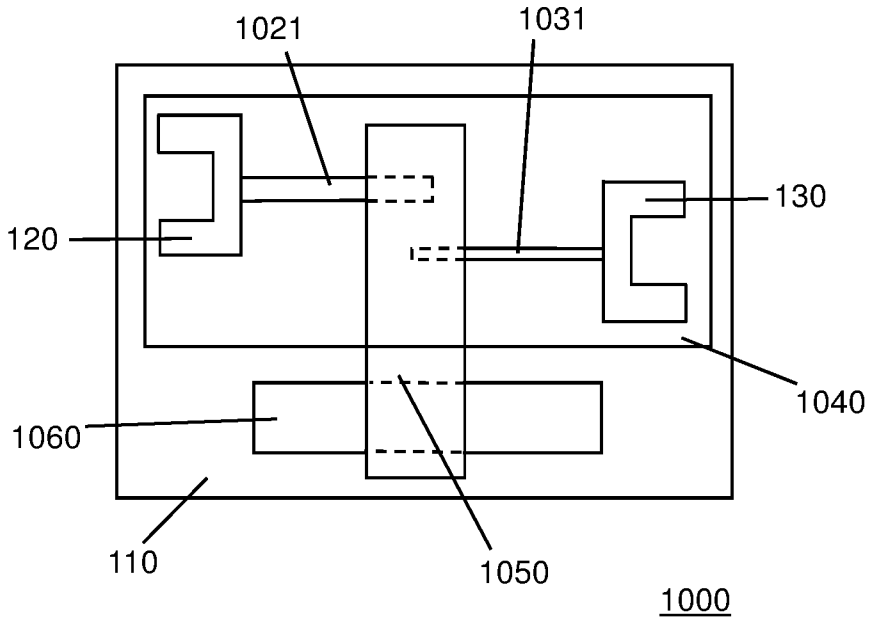
1021
1031
130
120
1040
1060
110
1050
1000

Fig. 10

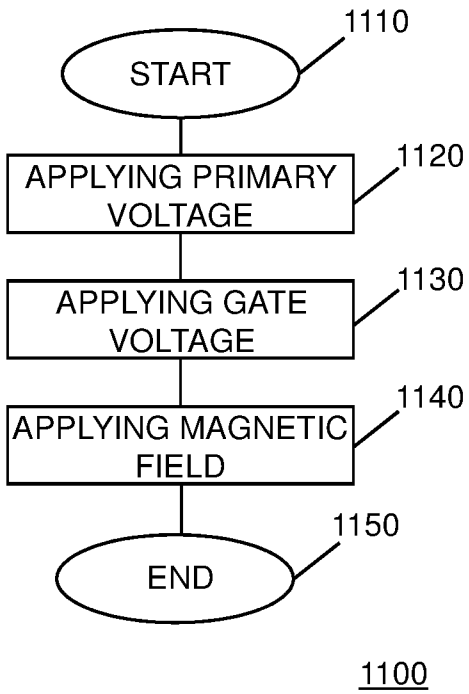
1110
START
1120
APPLYING PRIMARY VOLTAGE
1130
APPLYING GATE VOLTAGE
1140
APPLYING MAGNETIC FIELD
1150
END
1100

Fig. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2014/051785

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01R33/00 G01R33/09
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2013/140606 A1 (KOO HYUN CHEOL [KR] ET AL) 6 June 2013 (2013-06-06) abstract; figure 1 paragraph [0032] - paragraph [0053] -----	1-8, 10-20 9
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
27 August 2014	04/09/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Böhm-Pélissier, A

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	abstract; figure 9 Section IV. FIELD-EFFECT SPIN-TRANSISTORS I	9

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Information on patent family members

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