Chemical Mechanical Polishing of Dielectric Materials

A semiconductor wafer (1) has an underlying dielectric layer (3) with non-planarity features at its surface due to damascene topology, and a successive dielectric layer (9) that is without damascene topology overlying the first dielectric layer (3), the successive dielectric layer (9) having a smooth polished planar surface (10) that minimizes cumulative non-planarity. The surface is polished by chemical-mechanical planarization with a reactive liquid borne by an aqueous polishing fluid applied at an interface of the successive dielectric layer (3) and a polishing pad.
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The invention relates to planarization of a semiconductor wafer to minimize cumulative non-planarity, caused by a topology of non-planar features on successive layers of the wafer being stacked one on another.

According to US patent 5,676,587, a semiconductor wafer is provided with a dielectric layer having a damascene topology of surface imbedded, circuit interconnects, which are fabricated, for example, by a known damascene process. Each semiconductor wafer must have a smooth planar polished surface, which provides a base on which is to be fabricated, one or more than one, successive layers, each having imbedded circuit interconnections. However, the damascene topology contributes to a topology of non-planar features on the polished surface.

As successive layers are fabricated, one on another, and are polished, the topology of non-planar features on respective layers are stacked one on another. Thereby, the non-planar features on the respective layers become cumulative, and contribute to cumulative non-planarity of the surface of the wafer. Cumulative non-planarity contributes to difficulty in controlling the dimensions of successive layers that are fabricated on the wafer. A need exists for a semiconductor wafer of such a construction that minimizes cumulative non-planarity caused by successive layers on the wafer. A further need exists for a process for fabricating a semiconductor wafer in a manner that minimizes cumulative non-planarity caused by successive layers on the wafer.

Polishing by chemical mechanical planarization, CMP, is known for polishing a semiconductor wafer to remove a top layer of excess metallization, which leaves behind metal in trenches to provide the circuit interconnections. A desired result of a CMP polishing operation is to provide a smooth planar polished surface that extends over the dielectric layer and the metal in trenches. One of the problems to be overcome, is that CMP polishing leaves behind imperfections in the surface of a polished wafer. For example, CMP polishing leaves behind recessed dishing of the metal in the trenches. In the event that CMP polishing is allowed to continue for an extended duration, recessed erosion of the dielectric layer will occur from excessive polishing or overpolishing. The topology of non-planar features, as caused by the polishing operation, comprises, dishing of the metal in trenches, and further comprises, erosion of the dielectric layer, as caused by the polishing operation. Each successive dielectric layer with applied metallization is
similarly polished by CMP, leaving behind a topology of non-planar features on each successive polished layer.

According to an embodiment of the invention, a method is disclosed for minimizing cumulative non-planarity caused by successive layers on a semiconductor wafer.

An advantage of the invention resides in a method that provides a semiconductor wafer having a smooth planar polished surface on a dielectric layer that is without damascene topology, which minimizes variations in planarity due to the topology of non-planarity features on the underlying dielectric layer.

According to a further embodiment of the invention, a semiconductor wafer comprises, a successive dielectric layer that is without damascene topology overlying a first dielectric layer with damascene topology, the successive dielectric layer having a smooth polished planar surface that minimizes cumulative non-planarity.

Embellishments of the invention will now be described by way of example with reference to the accompanying drawings, according to which:

Figure 1 is a fragmentary enlarged view of a portion of a semiconductor wafer with an exemplary underlying dielectric layer and a layer of metallization; Figure 2 is a view similar to Fig. 1, and discloses the wafer after a first step polishing operation;

Figure 3 is a view similar to Fig. 2, and discloses the wafer after a second step polishing operation, having a topology of non-planar features, and a successive dielectric layer provided with a smooth planar polished surface that minimizes cumulative non-planarity; and Figure 4 is a view similar to Fig. 3, and discloses a successive dielectric layer and a thicker dielectric layer provided with a smooth planar polished surface that minimizes cumulative non-planarity.

Fig. 1 discloses a semiconductor wafer 1 having a thinly sliced, silicon substrate 2, on which is applied an underlying dielectric layer 3 having one of multiple trenches 4 in which metal 5 is imbedded to provide surface imbedded circuit interconnections.

Further, the wafer 1 comprises, a thin barrier film 6 covering the underlying dielectric layer 3. The underlying dielectric layer 3 is any one of a number of underlying dielectric layers with trenches 4 that are to be covered by a successive layer on the wafer 1. For the
purpose of illustration, Fig 1 discloses the underlying dielectric layer 3 as being the first underlying dielectric layer on the wafer 1.

The underlying dielectric layer 3 has a surface to be used as a base on which multilevel layers are to be fabricated. The metal filled trenches 4 in the underlying dielectric layer 3 comprise a damascene topology. The thin barrier film 6 is between the metal 5 in the trenches 4 and the underlying dielectric layer 3. The barrier film 6 provides a barrier to migration of the metal into the underlying dielectric layer 3.

Fabrication by a known damascene process, includes, the barrier film 6 being deposited, for example, by chemical vapor deposition, to cover the surface of the underlying dielectric layer 3, including each trench 4. For example, the barrier film 6 covering the underlying dielectric layer 3 of SiO₂, comprises, tantalum, meaning elemental Tantalum and/or a tantalum compound including tantalum nitride, or, alternatively, the barrier film 6 comprises, an silicon carbide, SiC, based material applied by chemical vapor deposition over an underlying dielectric layer 3 of organosilicate glass. Metallization 7, for example, copper metallization, is applied over the underlying barrier film 6 to fill each of the trenches 4 of the underlying dielectric layer 3 with metal 5. For example, the metallization 7 is applied as a thin film by chemical vapor deposition, followed by a thicker amount applied by a known electroplating process. The metallization 7 further comprises excess metallization covering the surface of the dielectric layer 3.

According to accepted practices, a first step polishing operation is performed to remove the copper metallization 7 to the level of the underlying barrier film 6. The wafer 1 is polished according to a known CMP polishing system. The CMP polishing system operates to move the wafer 1 against a moving polishing pad of the known CMP polishing system, and uses a combination of the moving polishing pad with polishing fluid at an interface with the wafer 1 being polished, to remove the metallization 7 by polishing friction and chemical reaction of the metallization 7 to the polishing fluid.

The wafer 1 disclosed in Fig. 2 was subjected to a first step CMP polishing operation that polishes the barrier film 6 to a planar surface, and that polishes the metal 5 in each trench 4 to the same height as that of the barrier film 6. However, as further disclosed by Fig. 2, some of the metal 5 in each trench 4 is removed during polishing, by chemical reaction to the polishing fluid and by polishing friction, which causes concave
dishing 8 of the metal 5 in each dished trench 4. Dishing 8 of the damascene topology undesirably provides non-planarity features that contribute to variations in planarity of the wafer 1. As disclosed by Fig. 2, CMP polishing of the surface of the wafer 1 accomplishes removal of the surface layer of copper metallization 7 to expose the surface of the barrier film 6, and to leave metal 5 in the trenches 4. Fig. 2 further discloses recessed dishing 8 of the metal 5 in each trench 4 that results from the first step polishing operation.

The first step polishing operation is followed by a second step polishing operation. With reference to Fig. 3, the second step polishing operation removes the barrier film 6 to the surface of the underlying dielectric layer 3, and which further results in the underlying dielectric layer 3 being polished with a smooth planar polished surface that is suitable for subsequent fabrication of successive layers of material. The wafer 1 is left with metal 5 in the trenches 4 to provide circuit interconnections. Further recessed dishing 8 of the metal 5 in each trench 4 results from the second step polishing operation.

In the event that CMP polishing is allowed to continue for an extended duration, recessed erosion of the dielectric layer 3 of the damascene topology will occur from excessive polishing or overpolishing. The recessed erosion undesirably provides further non-planarity features that contribute to variations in planarity of the wafer 1.

A desired result of CMP polishing is for both the underlying dielectric layer 3 and the metal 5 in the trenches 4 to attain the same planarity with a smooth planar polished surface resulting from polishing. The CMP polishing operation would desirably result in a polished planar surface of the wafer 1, without residual metal films on the polished surface of the dielectric layer 3, and with all of the trenches 4 having metal 5 at heights that are even with the level of the polished surface. However, chemical reaction and mechanical friction, applied by the polishing operation, results in undesired removal of metal 5 from the trenches 4, referred to as dishing 8 of such metal 5. Some dishing 8 is acceptable, as dishing 8 of the metal 5 is compensated for, by precisely controlling the dimensions of the width of each trench 4. Known mathematical calculations indicate that the impedance of a circuit interconnection, as provided by the metal 5 in a trench 4, is dependent to a greater extent upon controlling the dimensions of the width of each trench 4, and is dependent to a lesser extent upon variations in the height of dished metal 5.
As dielectric layers are fabricated, one on another, and are polished, the topology of non-planar features on multiple dielectric layers become stacked one on another. Thereby, the non-planar features become cumulative and contribute to cumulative non-planarity of the surface of the wafer 1. Cumulative non-planarity contributes to difficulty in controlling the dimensions of successive dielectric layers with imbedded metallization.

Fig. 3 discloses a semiconductor wafer 1 that comprises, a silicon substrate 2, an underlying dielectric layer 3 with trenches 4 and with imbedded metal 5 providing circuit interconnections. The underlying dielectric layer 3 has non-planarity features at its surface due to dished metal 5 in the trenches 4. In the past, the dished metal 5 would have contributed to cumulative non-planarity of the surface of the wafer 1, when the underlying dielectric layer 3 was used as a base on which to apply a successive layer of material on the wafer 1.

With further reference to Fig. 3, an embodiment of the invention provides a wafer 1 of minimized cumulative non-planarity at its surface. The wafer 1 has a successive dielectric layer 9 without forms of damasocene topology, such as trenches, overlying the first dielectric layer 3. The successive dielectric layer 9 has a smooth polished planar surface 10 that minimizes cumulative non-planarity due to the presence of non-planarity features in the underlying dielectric layer 3. The non-planarity features result from a process step of, polishing the semiconductor wafer 1 to remove excess metallization from the surface of the underlying dielectric layer 3, leaving the underlying dielectric layer 3 with a topology of non-planarity features in the form of dished metal 5 in trenches 4. The polished surface 10 of the successive dielectric layer 9 minimizes cumulative non-planarity of the wafer 1, and provides a base for subsequently fabricated layers of materials. For example, the successive dielectric layer 9 itself is of sufficient thickness for subsequent fabrication of metal receiving trenches 4, as shown by broken outline.

With further reference to Fig. 4, another embodiment of the successive dielectric layer 9 is of sufficient thickness to become reduced in thickness upon being polished. The successive dielectric layer 9 is polished to a smooth planar polished surface 10, to minimize cumulative non-planarity of the wafer 1. The successive dielectric layer 9 is without forms of damasocene topology, such as trenches. The successive dielectric layer is first, polished to a smooth planar polished surface 10, to minimize cumulative non-planarity...
planarity of the wafer 1. The polished surface 10 of the successive dielectric layer 9 minimizes cumulative non-planarity of the wafer 1, and provides a base for subsequently fabricated layers of materials. After being polished, to minimize cumulative non-planarity of the wafer 1, the successive dielectric layer 9 is followed by fabrication of a thicker dielectric layer 9a. The thicker dielectric layer 9a has an unpolished surface 10a that provides a base for subsequently fabricated layers of materials. For example, the thicker dielectric layer 9a and the dielectric layer 9 are of combined sufficient thickness to provide a base for subsequent fabrication of metal receiving trenches 4 therein, as shown by broken outline.

According to an embodiment of the invention, a method is disclosed for minimizing cumulative non-planarity of a surface of a semiconductor wafer 1. An embodiment of the method includes the steps of; applying a successive dielectric layer 9 that is without forms of damascene topology that would contribute non-planarity features. The successive dielectric layer 9 is applied over both the underlying dielectric layer 3 and the topology of non-planarity features of the underlying dielectric layer 3. The successive dielectric layer 9 has a sufficient thickness to become reduced in thickness upon being polished, and the method includes the step of polishing the successive dielectric layer 9, for example, by CMP, chemical mechanical planarization, to provide on the successive dielectric layer 9 a smooth planar polished surface 10 that minimizes non-planarity due to the topology of non-planarity features on the underlying dielectric layer 3.

Another embodiment of the method includes the steps of;

polishing a semiconductor wafer 1 to remove excess metallization from the surface of an underlying dielectric layer 3, leaving the underlying dielectric layer 3 with a topology of non-planarity features;

applying a successive dielectric layer 9 that is without damascene topology over both the underlying dielectric layer 3 and the topology of non-planarity features, the successive dielectric layer 9 having a sufficient thickness to become reduced in thickness upon being polished, and

polishing the successive dielectric layer 9 to provide on the successive dielectric layer 9 a smooth planar polished surface that minimizes non-planarity due to the topology of non-planarity features on the underlying dielectric layer 3.
An advantage of the invention resides in a method that provides a semiconductor wafer 1 having a smooth planar polished surface 10 on a successive dielectric layer 9 that is without trenches, which minimizes variations in planarity due to the topology of non-planarity features on the underlying dielectric layer 3.

The successive dielectric layer 9 is fabricated from material alternatives that comprises, for example, SiO₂, a fluorinated-silicate glass, a hydrogen silsequixane, an organic polymer, such as, a polyarylene and a poly-arylene-ether, or an organosiloxane polymer, or an organosilicate glass, such as carbon-doped SiO₂ with added methyl groups obtained by reaction of tetramethylsilane or trimethylsilane precursors, or a fluoropolymer, such as, polytetrafluoroethylene, which materials are applied, respectively, by spin-on or chemical-vapor deposition. The dielectric constant K is further reduced by increased porosity of the materials. The successive dielectric layer 9 is without damasocene topology, and is polished with a smooth planar polished surface 10 suitable as base on which are fabricated one or more than one layer of a wafer 1 having multilevel, circuit interconnections.

An etchant or, reactive liquid, is borne by an aqueous polishing fluid during a CMP polishing operation to polish the successive dielectric layer 9 that is made of a material that forms soluble reaction products with the reactive liquid. A combination of polishing friction and chemical reaction of the successive dielectric layer 9 with the reaction liquid to produce soluble dissolution of the surface of the successive dielectric layer 9, will polish the successive dielectric layer 9 with a smooth planar polished surface 10.

By way of example, CMP polishing of a successive dielectric layer 9 of carbon-doped SiOₓ, where x<2, and polishing of silica and other silicates, is accomplished by polishing with dilute Hydrofluoric HF acid as a reactive liquid in an aqueous polishing fluid that is applied during the polishing operation at an interface between the successive dielectric layer 9 and a polishing pad of a known CMP polishing apparatus. A combination of polishing friction and chemical reaction of the silicates with the HF reaction liquid to produce soluble reaction products, will polish the successive dielectric layer 9 with a smooth planar polished surface 10. According to a further embodiment of the invention, a kit of parts having materials for application to a surface of a semiconductor wafer 1, includes: a low K dielectric of carbon-doped SiOₓ, where x<2;
and a chemical reagent for dissolution of the surface of the low K dielectric during CMP polishing, comprising; dilute Hydrofluoric HF acid as a reactive liquid in an aqueous polishing fluid for CMP polishing of the low K dielectric.

According to a further embodiment of the invention, a kit of parts having materials for polishing a surface of a semiconductor wafer, includes: a low K dielectric material and a reactive liquid for soluble dissolution of the surface of the low K dielectric material during CMP polishing to be used as a reactive liquid borne by a polishing fluid for dissolution of the low K dielectric material during CMP polishing of the low K dielectric material to provide a smooth planar polished surface on the low K dielectric material.
Claims:

1. A method for minimizing cumulative non-planarity of a semiconductor wafer comprising the steps of;
   applying a successive dielectric layer that is without damascene topology over both an underlying dielectric layer and a topology of non-planarity features on the underlying dielectric layer, the successive dielectric layer having a sufficient thickness to become reduced in thickness upon being polished, and polishing the successive dielectric layer to provide on the successive dielectric layer a smooth planar polished surface that minimizes non-planarity due to the topology of non-planarity features on the underlying dielectric layer.

2. The method as recited in claim 1, further comprising the step of; polishing the semiconductor wafer prior to applying the successive dielectric layer, to remove excess metallization from the surface of the underlying dielectric layer, leaving the underlying dielectric layer with the topology of non-planarity features.

3. A semiconductor wafer comprises, an underlying dielectric layer with non-planarity features at its surface provided by damascene topology, and a successive dielectric layer that is without damascene topology overlying the underlying dielectric layer, the successive dielectric layer having a smooth polished planar surface that minimizes cumulative non-planarity.

4. The semiconductor wafer according to claim 3, and further comprising: the underlying dielectric layer having non-planarity features at its surface due to dished metal in trenches in the underlying dielectric layer.

5. The semiconductor wafer according to claim 3, and further comprising: the underlying dielectric layer having non-planarity features at its surface due to recessed erosion of the underlying dielectric layer.

6. A kit of parts having materials for application to a surface of a semiconductor wafer, comprises: a low K dielectric material, and a reactive liquid for soluble dissolution of the surface of the low K dielectric during CMP polishing using the reactive liquid in a polishing fluid during CMP polishing to provide a smooth planar polished surface on the low K dielectric material.

7. A kit of parts having materials for polishing a surface of a semiconductor wafer, comprises: a low K dielectric material and a reactive liquid for soluble dissolution
of the surface of the low K dielectric material during CMP polishing to be used as a reactive liquid borne by a polishing fluid for dissolution of the low K dielectric material during CMP polishing of the low K dielectric material to provide a smooth planar polished surface on the low K dielectric material.