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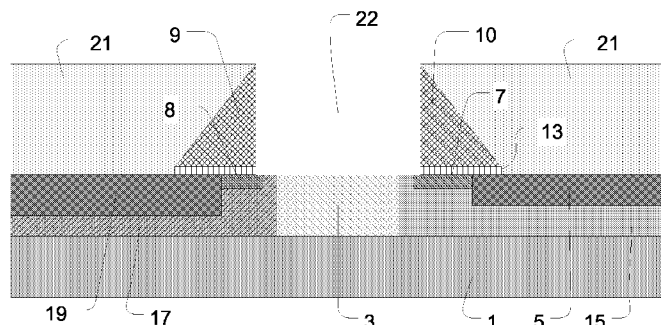
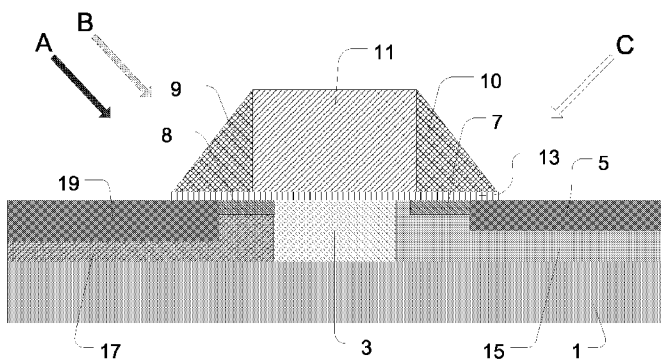
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(54) Title: LATERAL BIPOLAR TRANSISTOR



(57) Abstract: The invention provides a CMOS-based lateral bipolar transistor and a method of fabricating the same. A CMOS device forms the basis of the CMOS-based lateral bipolar transistor. The CMOS device is provided on a silicon, SOI or SSOI substrate and comprises a source and drain region, CMOS spacers (9, 10) and a removed gate electrode. An emitter region (41) and a collector region (45) are disposed in the source and drain regions, and a base region (43), comprising SiGe or p-type silicon, is provided adjacent to the emitter region (41) and the collector region (45). The base region (43) has a relatively large exposed area, because it is not covered by the, formerly removed, gate electrode. The base resistance may be reduced by providing a metal layer (29) and an electrical contact (33) on the exposed area of the base region (43).



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C. DOCUMENTS CONSIDERED TO BE RELEVANT		
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X	US 5 952 706 A (BASHIR RASHID [US]) 14 September 1999 (1999-09-14)	1,2
Y	column 5, line 23 - column 8, line 37; figures 4A-4H	4,5,7,8
X	GOMEZ R ET AL: "Lateral bipolar transistor fabricated on a deep-submicron technology" UNIVERSITY/GOVERNMENT/INDUSTRY MICROELECTRONICS SYMPOSIUM, 1999. PROCEEDINGS OF THE THIRTEENTH BIENNIAL MINNEAPOLIS, MN, USA 20-23 JUNE 1999, PISCATATWAY, NJ, USA, IEEE, US, 20 June 1999 (1999-06-20), pages 37-42, XP010345883 ISBN: 0-7803-5240-8 the whole document	1-3
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<input checked="" type="checkbox"/>	Further documents are listed in the continuation of Box C.	<input checked="" type="checkbox"/> See patent family annex.
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