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GB 1579873
GB 1569257

(58) Field of search
H4K

(54) **Telephone security device**

(57) A telephone security device for inhibiting certain calls being set up comprises a RAM memory to store inhibited call codes, and also permitted call codes which are allowed irrespective of the call codes inhibited. A lock switch permits various combinations of inhibited call codes to be selected and allows permitted call codes to be entered. A CPU controls the operation of the device, and a program store stores the program to direct the device. A buffer between the lock switch and the CPU is addressable by the CPU. Line voltage, current and dial tone detector circuits are connected to the CPU, and a power supply circuit powered by an exchange line powers the device. A dual tone multi-frequency receiver is also provided.

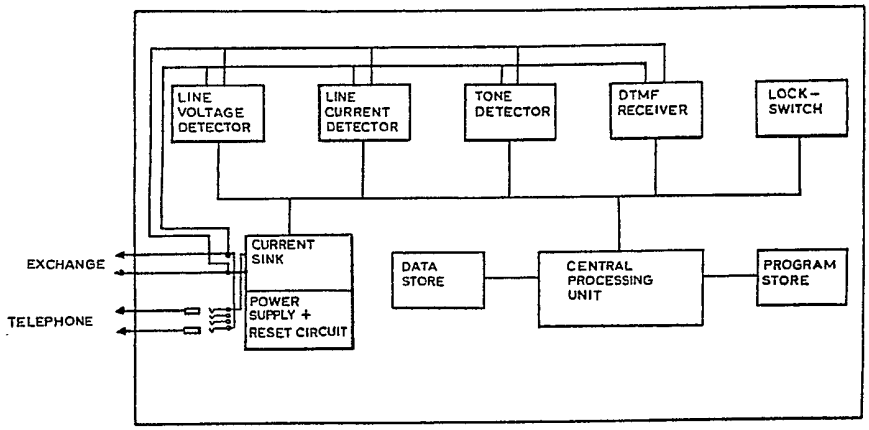

FIG. 2.

GB 2 146 507 A

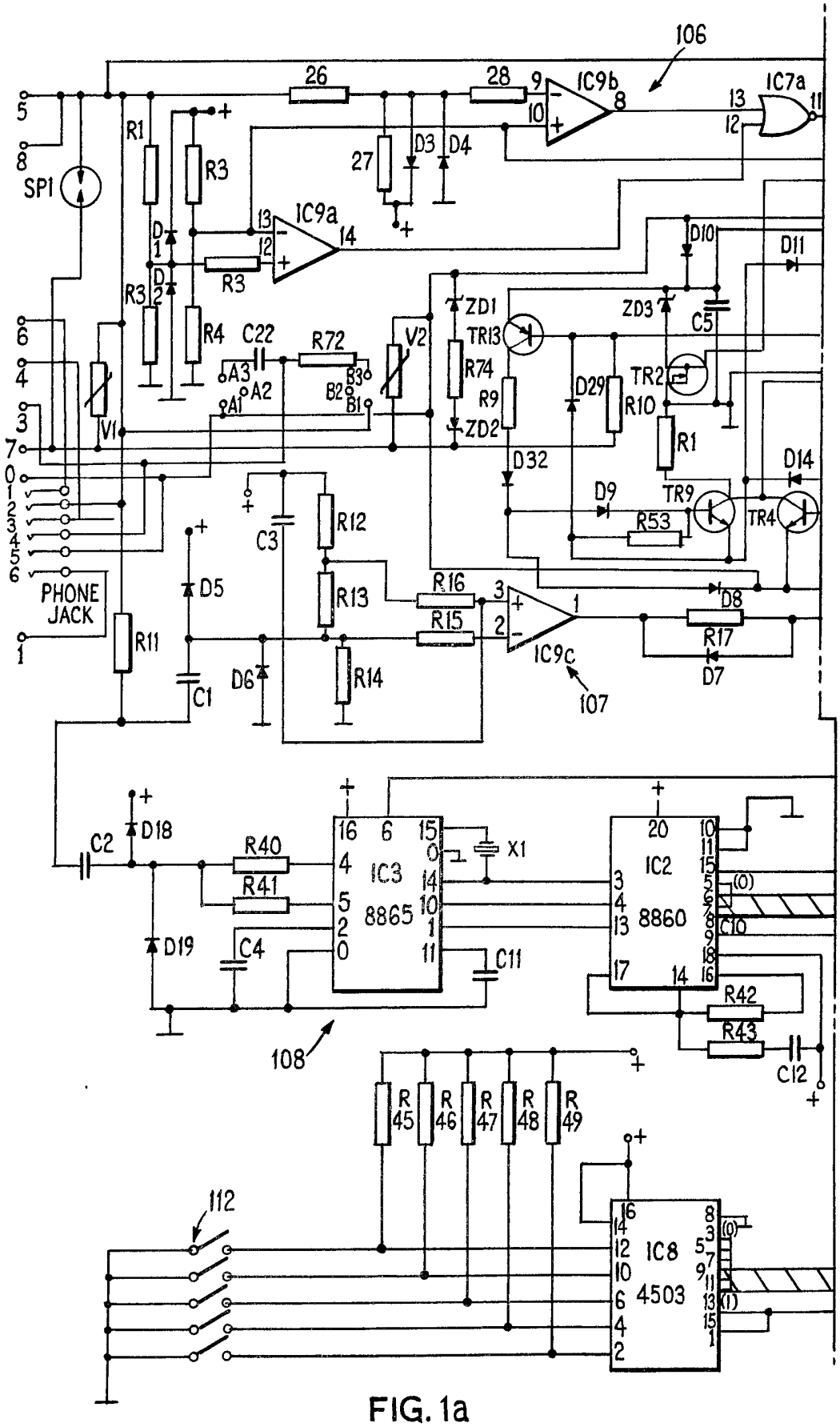
106
IC9b
IC7a
IC9a
SP1
R1
R3
D1
D2
D3
D4
26
27
28
R4
C22
R72
V1
V2
A1
A2
A3
B1
B2
B3
ZD1
ZD2
ZD3
TR13
TR2
TR9
TR4
R74
R9
R10
D29
D32
D9
D10
D11
D14
R53
C5
R1
C3
R12
R13
R14
R15
R16
R11
C1
D5
D6
D7
D8
R17
IC9c
107
PHONE JACK
C2
D18
D19
R40
R41
C4
IC3
8865
X1
C11
IC2
8860
C10
R42
R43
C12
108
R45
R46
R47
R48
R49
112
IC8
4503

FIG. 1a

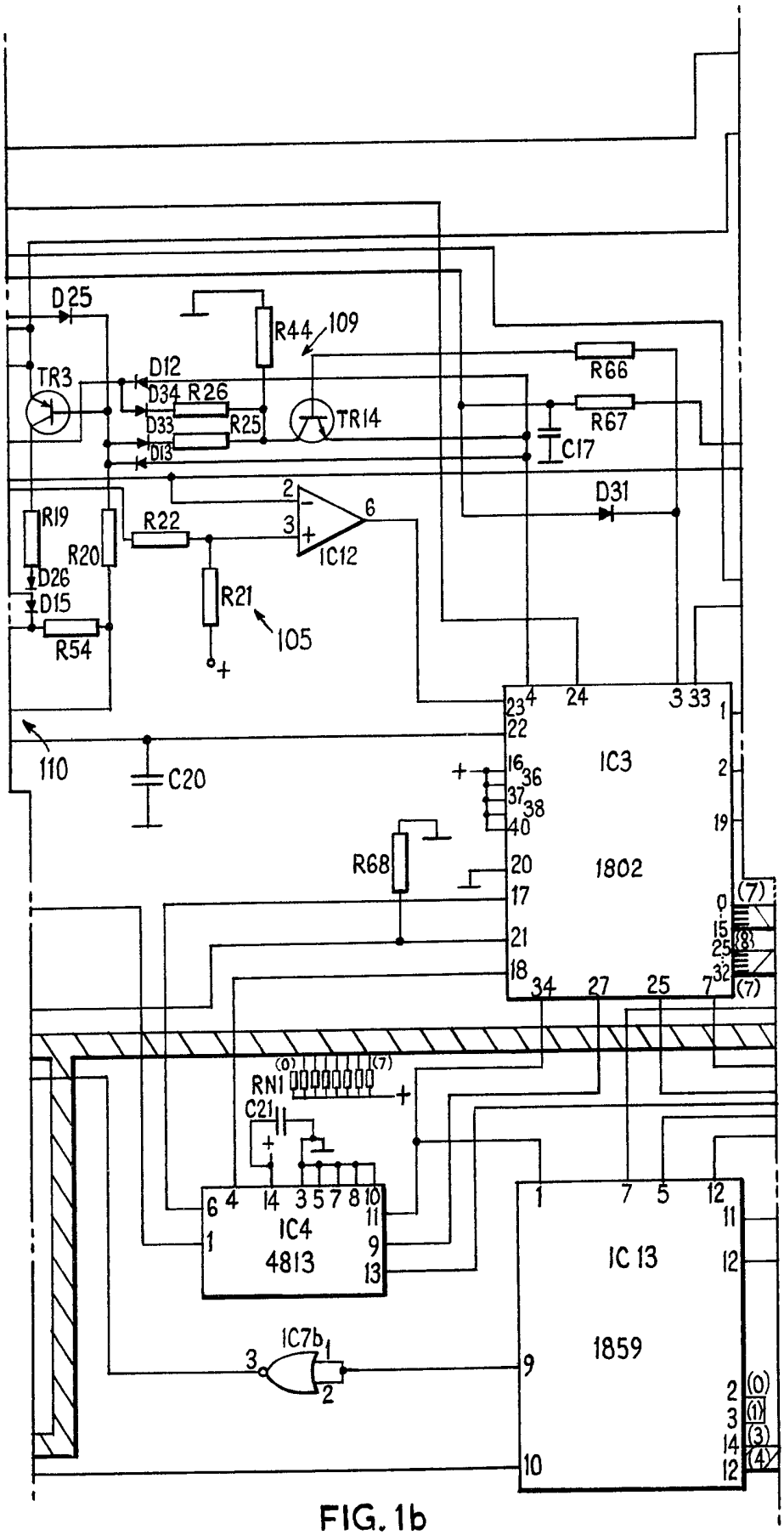
D25
R44
109
TR3
D12
D34
R26
D33
R25
D13
TR14
R66
R67
C17
D31
R19
R20
R22
2
3
6
IC12
D26
D15
R54
R21
105
110
C20
IC3
1802
R68
RN1
C21
IC4
4813
IC7b
IC 13
1859

FIG. 1b

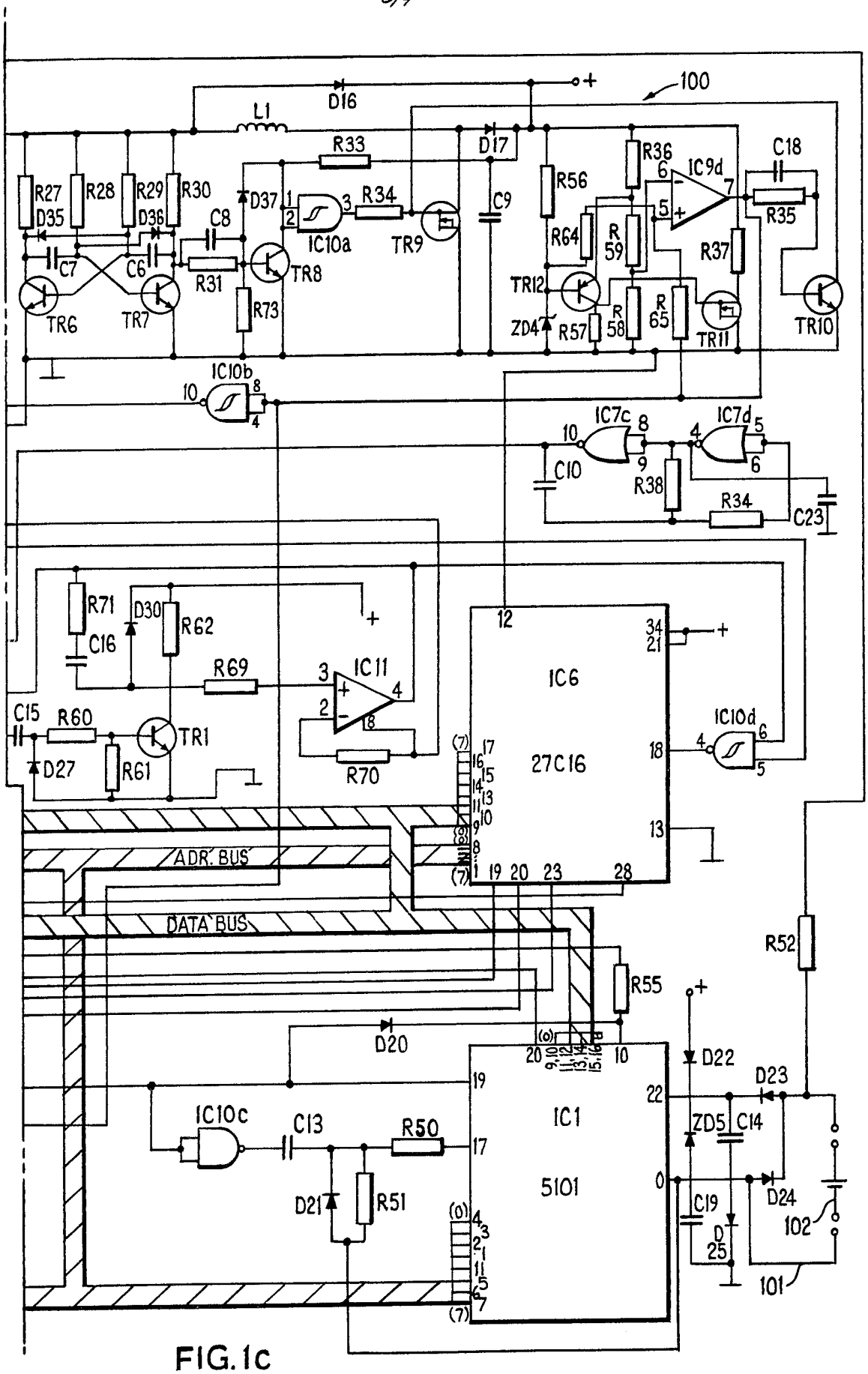
100
D16
L1
D17
R33
R27
R28
R29
R30
D35
D36
D37
C8
C7
C6
R31
R73
TR6
TR7
TR8
IC10a
R34
TR9
C9
R56
R36
IC9d
C18
R35
R64
R59
R37
TR12
ZD4
R57
R58
R65
TR11
TR10
IC10b
IC7c
IC7d
C10
R38
R34
C23
R71
D30
R62
C16
R69
IC11
C15
R60
TR1
D27
R61
R70
IC6
27C16
IC10d
ADR. BUS
DATA BUS
R52
R55
D20
IC10c
C13
R50
D21
R51
IC1
5101
D22
D23
ZD5
C14
C19
D25
D24
102
101

FIG.1c

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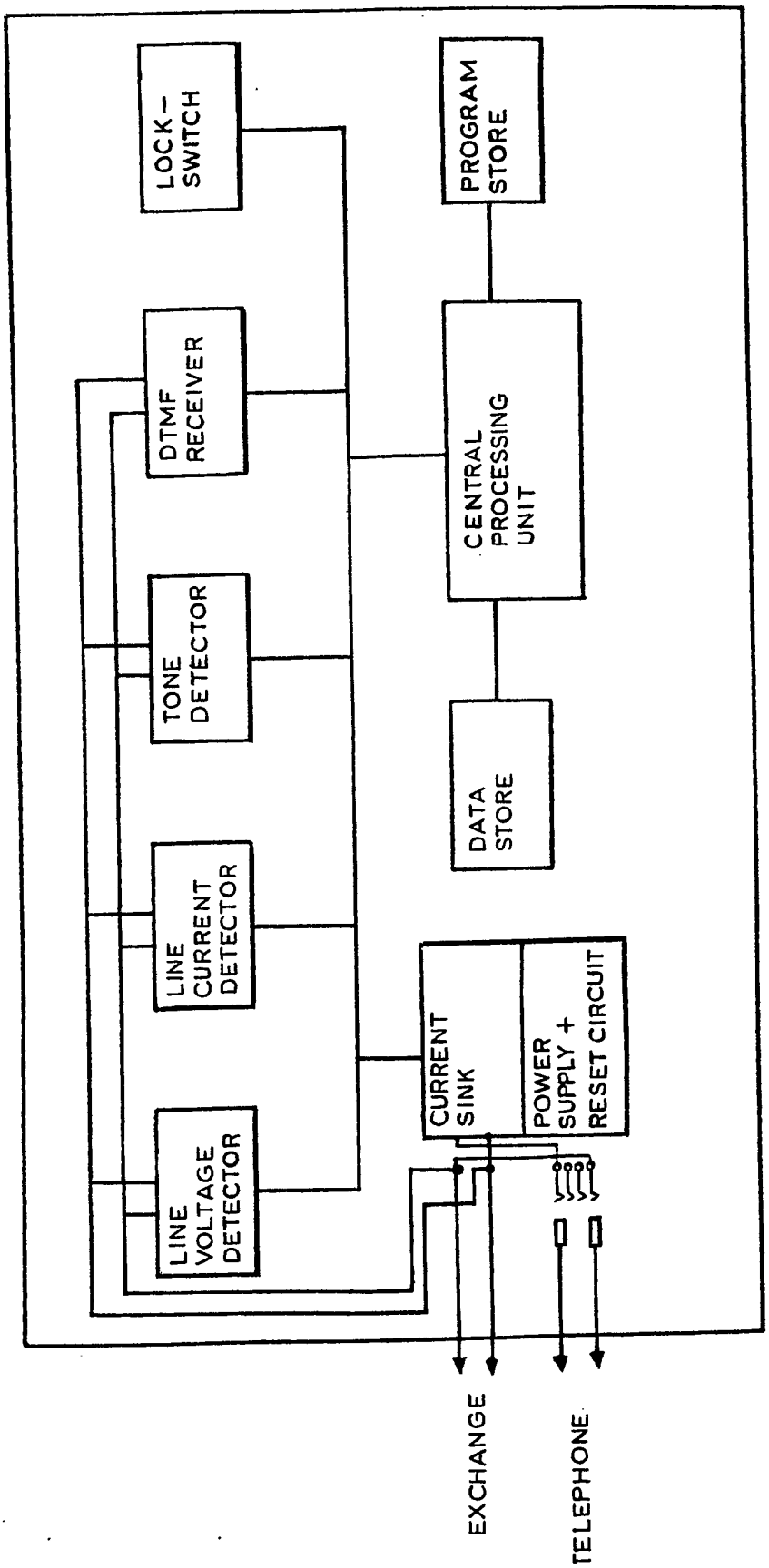

FIG. 2.

SPECIFICATION

Telephone security device

The present invention relates to a telephone security device, and in particular to a device for selectively preventing a call being set up, for example, a device for barring trunk calls, or other predetermined calls or the like.

Such devices are known, and in general, they operate in one mode only, in other words, once fitted to the phone system, they will inhibit the calls they are designed to inhibit only. It is not possible to change the calls to be barred during use. For example, if at one time one merely wishes to bar all trunk calls, and at another stage it is desired to bar all trunk calls and international calls, this is not possible. This, it will be appreciated, is a major disadvantage of such devices. In many cases it is desirable to be able to vary the range of calls barred, for example, when an executive is leaving his office unattended for a period of time, it may be desired to bar all international and all trunk calls, while when the executive is in the office no calls should be barred. Furthermore, in certain cases where trunk calls to certain areas are barred, it may be desirable to permit certain calls to be made to those areas, for example, calls to a company's subsidiary in a barred area. Unfortunately, devices for achieving this are not available. Therefore, there is a need for a device which will prevent certain predetermined calls from being set up, and also will enable the certain calls to be made to a barred area.

The present invention is directed towards providing such a device.

According to the invention there is provided a telephone security device for inhibiting a call being set up, the device comprising means to store a plurality of certain call codes which are to be inhibited, the device being operable in a plurality of modes in which different inhibited codes or different combinations of inhibited codes may be selected, means to select one or more of the inhibited calls codes by selecting one of the modes, means to detect a call being set up, means to compare the call code of the call being set up with the selected inhibited call codes, means to inhibit the call being set up if the call code compares with an inhibited call code, connection means to connect the device to a telephone and a public exchange line.

In one embodiment of the invention the means to store the inhibited call codes comprises means for storing and receiving a permitted call code of a call to be permitted irrespective of the inhibited call codes.

In another embodiment of the invention, the means for storing and receiving the permitted call code is programmable to permit the permitted call to be changed during use.

In one embodiment of the invention the means for storing and receiving the permitted call code has capacity for a plurality of call codes.

In another embodiment of the invention the means to compare the call code of a call being set up with the inhibited call codes also compares the call code of the call being set up with the permitted call codes, and if the call code is a permitted call code, allows the call to be set up.

In a further embodiment of the invention, the means to select a desired mode is provided by a switch means.

Advantageously, the switch means is provided by a switch means having a plurality of independent switches, each switch corresponding to a specific mode, and only one of which switches closes in each mode.

In one embodiment of the invention, the switch means comprises five independent switches.

In one case switch 1 of the switch means corresponds to mode 1 of the device, switch 2 corresponds to mode 2, switch 3 corresponds to mode 3, switch 4 corresponds to mode 4, and switch 5 corresponds to mode 5.

In another embodiment of the invention in mode 1 no calls are barred, in mode 2 international subscriber dial calls are barred, in mode 3 international subscriber dial and standard trunk dial calls are barred, in mode 4 all calls except emergency calls are barred, and in mode 5 permitted call codes are enterable into the means to store and receive the permitted call codes.

The invention will be more clearly understood from the following description of a preferred embodiment thereof, given by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a circuit diagram of a telephone security device according to the invention; and

Figure 2 is a block schematic diagram of the device of Figure 1.

Referring to the drawings, there is provided a telephone security device according to the invention, in this case a device for selectively barring certain calls or a certain range of trunk calls or international trunk calls. The device also permits certain call codes to be made even if they are in a selected inhibited area. The device in this case may be connected either directly into the public exchange line, or a private automatic branch exchange. A jack socket (not shown) is provided in the device into which a telephone is then connected. In Figure 1 terminals 7 and 5 are provided for connection to the telephone, and terminals 2 and 8 are provided for connection to the exchange line.

Briefly, the device comprises a power supply, reset circuit and line current sink circuit which is indicated generally by the reference numeral 100 which powers the device, and uses power from the exchange line. A power supply circuit, indicated by the reference numeral 101 to power the memory chip IC1 is fed from a trickle supply from the exchange line when the telephone is "on hook". A back up battery 102 is also provided. A line current detector circuit which detects line current is indicated by the reference numeral 105,

a line voltage detector circuit to detect voltage on the exchange line, is indicated by the reference numeral 106. A dial tone detector circuit indicated generally by the reference numeral 107, and a dual tone multifrequency (DTMF) reciever circuit 108 is provided. A barring circuit 109 for barring the inhibited calls comprises a transistor TR14 and a bridge circuit indicated by the reference numeral 110 comprises transistors TR3, 4, 5 and 13. A central processing unit, in this case a microprocessor IC5 controls the device.

The CPU IC5 is provided by an RCA 1802 cosmac microprocessor. An integrated circuit IC6 stores the programme to direct the CPU. The integrated circuit IC6 is provided by a 2K × 8, 27C16 CMOS EPROM. An integrated circuit IC1, in this case a 256 × 4 random access memory (RAM) stores the codes of the telephone numbers or trunk lines which are to be barred, and also the codes of the numbers which are to be permitted. The integrated circuit IC1 is addressable by the CPU IC5.

The device may be operated in any one of five modes, as is described below. In each of modes 1 to 4 a different call code or combination of call codes is barred. In mode 5 the permitted call codes are enterable by the user. The following are the calls which are barred in each of modes 1 to 4 in the case of the present device. In all of modes 1 to 4 permitted calls are allowed. Needless to say, it will be appreciated that any other calls or combination of calls could be arranged in each mode.

Mode 1 - No calls are barred.
Mode 2 - International subscriber dial (ISD) trunk calls are barred
Mode 3 - International subscriber dial (ISD) and subscriber trunk dia (STD) calls are barred.
Mode 4 - All calls except emergency calls are barred.
Mode 5 - Call codes of permitted calls are enterable.

Means to select a desired mode is provided by a five position lock switch indicated generally by the reference numeral 112. Each position corresponds to one operating mode of device. In each of the five positions, only one of the switch contacts 113, 114, 115, 116 and 117 are made. Switch 113 corresponds to mode 1 and so on up to switch 117 which corresponds to mode 5. A tristate buffer provided by an integrated circuit IC8, is provided between the switches and the CPU. By selecting the buffer IC8 the CPU determines the position of the lock switch 112. The information is read onto the CPU databus. The five lowest order lines are used. The line corresponding to the operated contact will have a logic low, whereas all other lines will be high. Address latches provided by integrated circuits IC4 and IC13 are provided.

Each of the above circuits and components and their operation are described in detail below, and for clarity separate headings are used.

Power supply, reset and line current sink

When a telephone (not shown) is taken off hook a loop is connected across the telephone terminals 2 and 5 (phone jack) and current flows in the exchange line. The current path through the device depends on the voltage polarity on the line. In the following description it is assumed that the line leg connected to terminal 8 is positive. When the telephone loop is connected current flows from terminal 8 to terminal 2 (telephone jack) via the telephone to terminal 5 (jack) a diode D10, to charge capacitor C9 in the power supply. The other side of the capacitor C9 is connected to earth of the device and current flows via a resistor R18 and a transistor TR5 to terminal 7 and the other leg of the line. As the voltage across the capacitor C9 builds up Voltage reference a zener diode ZD4 will clamp the + input of an integrated circuit IC9d at 2.5V.

The potential at the - input of IC9d is determined by a voltage divider consisting of resistors R36, R59 and R58. Initially this is below the potential of the + input. When the voltage across C9 reaches 4.5 volts the potential of the - input goes above 2.5 volts and the output of IC9d will go low. This signal turns off transistor TR10 which enables the switching converter power supply, consisting of the multivibrator circuits TR6 - TR7 and associated components, driver transistor TR9 and regulator TR11, TR12 and associated components, to take over charging of C9.

The output of IC9d is inverted by a Schmitt trigger IC10b and puts a high on the $\overline{\text{CLEAR}}$ line of the CPU IC5.

Transistor TR14 is now turned on via resistor R66. This in turn increases the base current of either transistors TR13 or TR3 depending on line voltage polarity. When transistor TR13 turns on a second path for line current becomes available via diode D10, emitter - collector of TR13, R9, D32, D9 and base-emitter of TR5.

The output of Ic10b is also applied via R67 to the gate of transistor TR2. This transistor TR2, however, does not carry significant current from the line except at shorter line lengths when the line current is greater. At higher line currents the voltage across C5 increases until it reaches the threshold at which zener diode ZD3 conducts. The line current may now flow via D10, ZD3, drain-source TR2, R18 and collector emitter of TR5.

The mechanism by which the device force releases a call is controlled from the Q output line, namely pin 4 of the processor. This line goes high which, via D12 turns off TR13. This stops the current to the base of TR5 which is turned off thus reducing the line current to zero. After a short interval (1 second) the Q line goes low again restoring the line current.

If the polarity of the line is opposite to that assumed in the above description the circuit behaves in a similar manner. The functions of transistors TR5 and TR13 of the bridge circuit are now carried out by transistors TR4 and TR3 respectively.

Transistors TR6 and TR7 and their associated components form a multivibrator for the switching mode DC converter. The multivibrator feeds transistor TR8 which, via a Schmitt trigger IC10a, drives a transistor TR9. During initial power-up the gate of TR9 is held low by TR10 until the output of IC9d goes low as described

above. At this point TR10 is turned off and TR9 is driven alternately on and off by the multivibrator. When TR9 is on, current builds up in an inductor L1. When TR9 turns off again the current flowing in the inductor L1 charges C9 via D7. The volage across C9 builds up to a maximum of 5.25 Volts and is stabilised by the regulator consisting of TR11 and TR12. If the voltage across C9 goes above 5.25 V the emitter voltage of TR12 goes above the base voltage which is held at 2.5 Volts by ZD4. TR12 then conducts and as a result turns on TR11 which discharges C9 until the voltage level is reduced to 5.25 V again.

Line current detector

When the exchange line is idle the line current is zero and there is no voltage drop across resistor R18. The - input of IC12 will be at the device earth potential. The potential on the + input will be 25 mV above earth, determined by the voltage divider R21 and R22. In this condition the output of IC12 which is connected to external flag $\overline{EF2}$ namely pin No. 23 of the CPU will be high.

When current flows in the line the voltage across R18 drops by a minimum of 50 mV resulting in a corresponding drop in the potential on the + input of IC12 bringing it below the - input and putting the output low.

Line voltage detector

The operation of the line voltage detector varies depending on line polarity. In the following, terminal 8 is assumed to be positive.

A voltage divider comprising resistors R4 and R2 maintain a potential of 2.5 Volts above earth on the - input of integrated circuit IC9a and at the + input of integrated circuit IC9b.

When the exchange voltage is connected, a voltage divider comprising resistors R1 and R3 will maintain the + input of IC9a at around 4 volts above earth thus keeping the output high. The - input of IC9b will be held at 5.25 volts above earth by diode D3 thus keeping the output low. The two output signals will give a low at the output of integrated circuit IC7 which is connected to external flag $\overline{EF1}$ in this case pin No. 24 of the CPU.

When the exchange voltage is removed the potential of terminal 8 drops to the earth of the device, resulting in the potential of the + input of IC9a going below the potential of the − input thus putting the output low. The potential of the − input of IC9b is held at 4 V by the potential divider, resistors R6 and R7 so that its output is unchanged. The output of IC7a will therefore go high.

When the polarity of the exchange line is reversed the functions of IC9a and IC9b are Interchanged. Thus the output of IC9b will change from high to low when the exchange voltage is disconnected.

Tone detector

A potential divider comprising R12, R13 and R14 maintains the + input of IC9c at 2.5 Volts above earth and the − input at a potential of 50 mVolts below this. The output of IC9c therefore is normally high.

When a tone is connected to the exchange line an a.c. signal will appear at the − input pulling it alternately above and below the + input which will be held at a fixed potential by capacitor C2. This will result in the output of IC9c going low in response to the tone. This output is connected to the external flag $\overline{EF3}$ of the processor via R17, C20 and D7. In this case flag $\overline{EF3}$ is provided by pin No. 22. When the output of IC9c goes low $\overline{EF3}$ is pulled low quickly by discharging C20 through diode D7. When the output goes high again C7 charges up through R17. This network has a time constant of 20 mS.

Central processing unit (CPU), program store, data store

The CPU IC5 is an RCA 1802 Cosmac Microprocessor. It is a single-chip CMOS 8-bit register orientated microprocessor. A detailed guide to the architecture and programming technique is contained in 'User Manual MPM-201C'.

The Program Store IC6 is a 2k × 8 27C16 CMOS EPROM, which holds the program for the device.

The Data Store IC1 is a 256 × 4 Random Access Memory.

At power-up the $\overline{CLEAR}$ line of the processor is held low until the voltage across C9 reaches 4.5 Volts. This ensures that the program does not run until all parts of the device are fully powered. When the $\overline{CLEAR}$ line goes high program execution begins from the first location in the Program Store.

The speed of operation of the processor is determined by the frequency of the clock signal (100 KHz). This is generated by a flip-flop oscillator provided by integrated circuits IC7c and IC7d.

The microprocessor has eight address lines. These eight lines supply a 16-bit address in the form of two consecutive 8-bit bytes. The higher order address byte appears on the address lines first followed by the lower order byte. The timing pulse TPA is used to strobe the 5 used bits of the higher order address byte into an address latch, namely integrated circuits IC13 and IC4.

The allocation of addresses in the system is as follows:

Program Store	0000	-	07FF
Data Store	0800		08FF
Lock-switch	1000		
DTMF Decoder	1800		

The address lines A11 and A12 are decoded in the integrated circuit IC13 and the decoded signal selects

one of the four devices above.

In order to reduce power consumption in the circuit the Program Store is deselected except for the duration of the timing pulse TPB since the information can only be read into the CPU during this period. In addition, should the $\overline{\text{WAIT}}$ line, pin No. 2 of the CPU go low at any time thereby halting program execution then the Program Store is deselected until the $\overline{\text{WAIT}}$ line goes high again.

The output port N1 is connected via C15 and R60 to the base of TR1. When N1 goes high TR1 is turned on for a short time. The collector voltage of TR1 drops and brings the + input of IC11 below the − input which is held at the 2.5 V reference. The output of IC11 will then go low pulling down the $\overline{\text{WAIT}}$ line of the CPU. TR1 is turned off again quickly but its collector will not go high until C16 charges up. When the collector voltage goes above the 2.5 V reference again the output of IC11 will go high and remove the wait state from the CPU. This timing circuit delays the CPU by 3.8 mS. Together with the execution time of the instructions which are used to activate it the timer gives a total delay of 5 mS which is used by the CPU for various timing functions in the program execution.

The reserve power supply for the Data Store may be provided by a battery 102 or by draining a trickle charge from the line in the idle state. If the battery is not provided the trickle charge is drawn as follows:

i) Exchange line on terminal 8 positive.
Terminal 8 - R52 - D23 - C14 - D25 - R18 - TR5 - Terminal 7
ii) Exchange line on terminal 7 positive.
Terminal 7 - D11 - D16 - D22 - C14 - D24 - R52 - Terminal 8

One of the select signals to the Data Store is AC coupled to ensure that the memory is not inadvertently selected during power-down.

Lock switch

The CPU can determine the position of the lock switch 112 by selecting the tri-state buffer IC8. In each of the five positions one and only one of the swtich contacts 113, 114, 115, 116 and 117 are made. The information is read onto the CPU data bus. The five lowest order lines are used. The line corresponding to the operated contact will have a logic low whereas all other lines will be high.

When the lock switch 112 is in mode 5, namely switch 117 is closed, permitted call codes are enterable into the data store IC1 by the user. Permitted call codes, either actual numbers or trunk prefixes or any combination of call codes or partial call codes are enterable by dialling the call code to be permitted. In this particular case a maximum of ten call codes may be entered in mode 5.

Dual tone multifrequency receiver

The dual toen multifrequency receiver contains two parts:

i) A filter (IC3) which separates the incoming DTMF signal into its upper and lower components. The component frequencies are fed out in the form of square waves.

ii) A decoder (IC2) which accepts the high group and low group square wave output signals from IC3 and provides a 4-bit binary output.

The presence of a DTMF signal is detected by the CPU by examination of the external flag EF4, pin No. 21.

The output lines of the decoder Pins. Nos. 5, 6, 7 and 8 are connected to the four lower order data bus lines and can be read by the CPU when the decoder is selected.

Protection

A varistor V1 and a gas discharge tube SP1 provide protection against atmospherically induced voltage surges on the line. Further protection is provided by diodes D1 and D2, D3 and D4, D5 and D6, and D18 and D19 at the Op. Amp and DTMF filter inputs.

The current in the exchange line flows through the device. The voltage drop across the device is 3 volts at low line currents and rises to 4.5 volts for higher line currents. This voltage is converted by the internal power supply to a stable 5.25 volts which is used to power the other elements in the circuit.

When the telephone is taken 'off hook' the circuit is immediately powered-up and the CPU IC5 begins execution of its program. The CUP monitors the line conditions - voltage and current - and the DTMF receiver.

If the lock-switch is in the 'Allow All Calls' position the CPU will pass all subscriber initiated signals and take no action. If the switch is in any of the barring positions the CPU records all digits dialled and checks that the digits do not correspond with the codes which are barred for that particular switch position. If a barred code is dialled the call is immediately force released.

If the signalling is loop-disconnect the unit checks that all makes, breaks etc. are within the permitted tolerances, and that breaks are due to subscriber dialling and not caused by temporary line disconnections in the exchange equipment. Invalid signals will result in force release of the call.

The device may also be connected into an extension line to bar calls from the extension. In this case the device is set up to operate on the extension by setting the lock switch to position 5 and dial the single digit required to obtain an exchange line. The mode in which the device is desired to operate in is then selected.

It will of course be appreciated that while specific components have been described for use in the device,

any other suitable components could be used. Additionally, it will be appreciated that while specific circuits for the power supply and current sink line V detector, line current detector, dial tone detector, have been described, other suitable circuits could also be used. It will of course be appreciated that while the apparatus has been described as having a tone detector and a DTMF receiver, these are not essential to the invention.

Furthermore, it will be appreciated that while specific integrated circuits have been described, other suitable integrated circuits could also be used.

Additionally, it will be appreciated that while the apparatus has been described as having a dual tone multifrequency receiver, this if desired could be dispensed with. Additionally, other suitable switch means for selecting the desired mode of the apparatus could be used. Additionally, it will of course be appreciated that the device could be provided to operate in more or less than five modes.

CLAIMS

1. A telephone security device for inhibiting a call being set up, the device comprising:
means to store a plurality of certain call codes which are to be inhibited, the device being operable in a plurality of modes in which different inhibited codes or different combinations of inhibited codes may be selected,
means to select one or more of the inhibited call codes by selecting one of the modes,
means to detect a call being set up,
means to compare the call code of the call being set up with the selected inhibited call codes,
means to inhibit the call being set if the call code compares with an inhibited call code,
connection means to connect the device to a telephone and a public exchange line.

2. A device as claimed in claim 1 in which the means to store the inhibited call codes comprises means for storing and receiving a permitted call code of a call to be permitted irrespective of the inhibited call codes.

3. A device as claimed in claim 2 in which the means for storing and receiving the permitted call code is programmable to permit the permitted call to be changed during use.

4. A device as claimed in claim 2 or 3 in which the means for storing and receiving the permitted call code has capacity for a plurality of call codes.

5. A device as claimed in any of claims 2 to 4 in which the means to compare the call code of a call being set up with the inhibited call codes also compares the call codes of the call being set up with the permitted call codes, and if the call code is a permitted call code, allows the call to be set up.

6. A device as claimed in any of claims 1 to 5 in which the means to select a desired mode is provided by a switch means.

7. A device as claimed in claim 6 in which the switch means is provided by a switch means having a plurality of independent switches, each switch corresponding to a specific mode, and only one of which switches closes in each mode.

8. A device as claimed in claim 7 in which the switch means comprises five independent switches.

9. A device as claimed in claim 8 in which switch 1 of the switch means corresponds to mode 1 of the device, switch 2 corresponds to mode 2, switch 3 corresponds to mode 3, switch 4 corresponds to mode 4, and switch 5 corresponds to mode 5.

10. A device as claimed in claim 9 in which in mode 1 no calls are barred, in mode 2 international subscriber dial calls are barred, in mode 3 international subscriber dial and standard trunk dial calls are barred, in mode 4 all calls except emergency calls are barred, and in mode 5 permitted call codes are enterable into the means to store and receive the permitted call codes.

11. A device as claimed in any of the preceding claims in which the means to store the inhibited call codes and the means to store and receive the permitted call codes is a random access memory provided by an integrated circuit.

12. A device as claimed in any preceding claim in which the means to compare the call code of a call being set up with an inhibited call code or a permitted call code is a central processing unit provided by a microprocessor.

13. A device as claimed in any preceding claim in which the means to detect a call being set up comprises a line voltage detector, a line current detector and a dial tone detector.

14. A device as claimed in claim 13 in which the means to detect a call being set up also comprises a dual tone multi-frequency receiver, comprising a filter provided by an integrated circuit and a decoder provided by an integrated circuit.

15. A device substantially as described herein with reference to and as illustrated in the accompanying drawings.

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