Oct. 11, 1960 R. BÉRANGER 2,955,757

DEVICES FOR CARRYING OUT A DIVISION

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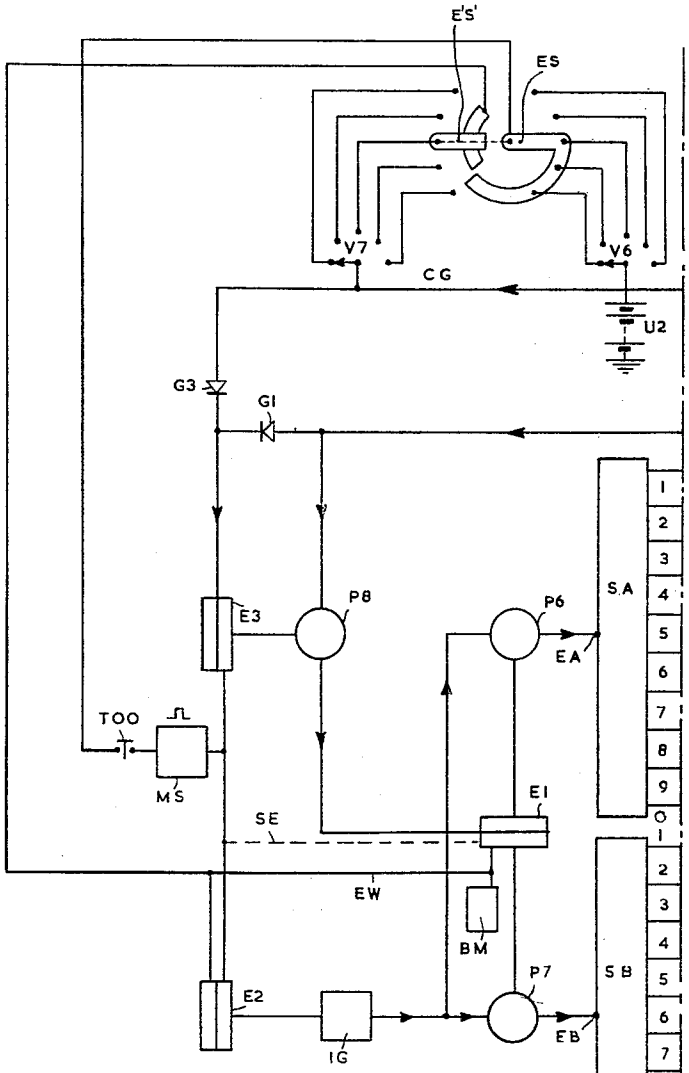


FIG 1a

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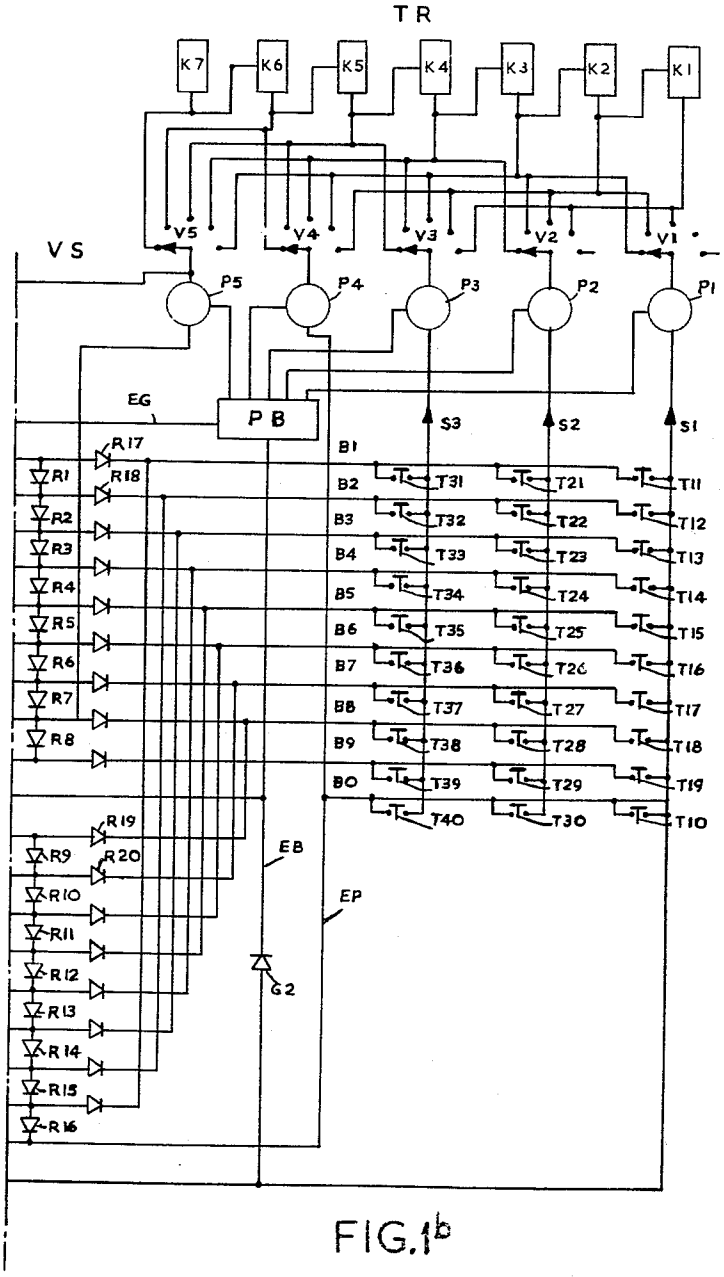


FIG. 1b

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DEVICES FOR CARRYING OUT A DIVISION

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This invention relates to devices for carrying out a division in the decimal system with the aid of a calculating machine.

Methods for carrying out a division with the use of a manually-controlled calculating machine are already known, in which the various figures of the dividend have initially been registered by a chain of decade counters of a totalisator register, so that at least the counters of the highest and the second highest rank register the figure 0 and the division is effected in a plurality of stages corresponding to the various figures of the quotient. During each stage, the complement of the divider with respect to 10^p, wherein p is an integer at least one larger than the number of figures of the divider, is added to the number registered in a given part of the totalisator which part is constituted by p-counters of sequential ranks. The carries which during these additions are supplied from the given part of the totalisator to the counter of next-higher rank serve to produce the quotient. After each stage, the given part of the totalisator is shifted one position with respect to the totalisator in the direction of lower rank. In this method, when the division is terminated the quotient is registered in a first part of the totalisator and the remainder of the division is registered in another part of the totalisator and may be read there. This known method has the disadvantage that the different operations cannot be carried out automatically in succession by the machine, but must be controlled individually by hand. This is connected with the fact that, if in a given stage the reduction has been carried out one step too far, so that the provisional remainder has, as it were, become negative, thus making it necessary to go one step back by adding the divider to the provisional remainder, the last figure produced of the quotient which already had acquired the correct value is varied and thus registered incorrectly. Consequently, in this method either the operator of the machine must evaluate whether a subsequent addition of the complement is still possible without producing a negative remainder, or a second register is required to remember the previous position of the totalisator register.

The object of the present invention is to enable divisions to be carried out fully automatically by the calculating machine with the use of the above-mentioned known method.

In the device according to the invention, the addition of the complement of the divider is repeated until no carry, as referred to above, is produced and subsequently the divider is added once to the number registered in the given part of the totalisator register, a correction figure being added to the counter of next higher rank, which correction figure is 9 for the last stage of the division and 8 for the other ones.

It be assumed, for example, that the number 56304

must be divided by 231, which operation is effected arithmetically as follows:

```
231/56304    /243
  462
  ---
 1010
  924
  ---
  864
  693
  ---
  171
```

The quotient is thus 243 and the remainder is 171. The process comprises a plurality of dividing operations each for producing a figure of the quotient, the divider during each operation being subtracted from the dividend or the provisional remainder so many times that the provisional remainder just does not become negative. For carrying out this division in accordance with the invention with the use of a calculating machine, the dividend 56304 is first registered in counters of a totalisator register, and for reasons specified hereinafter it is ensured that at least two counters of higher rank are provided which register the figure 0. The counters thus register, for example, 0,056,304. Subsequently, the complement of the divider with respect to 10^p, wherein p is an integer, which is at least one larger than the number of figures of the divider, is added to a given part of the dividend. In the example under consideration, the number of figures of the divider is 3, so that the complement with respect to 10,000 may be chosen. As is well-known, the complement may be found by taking the complement with respect to 9, for each of the figures of the number, except for the last figure, for which the complement with respect to 10 must be chosen. The relative complement of 231 with respect to 10,000 is thus equal to 9769. This complement is subsequently added several times to the dividend, during which process the following operations take place:

```
(0)   0056304
      9769
      -------
(1)   1033204
      9769
      -------
(2)   2010104
      9769
      -------
(3)   2987004
```

As may be seen, during the first two additions, which thus are substantially equivalent to the subtraction of the divider, a carry is supplied to the counter of the highest rank (most left-hand column), but a carry is not supplied during the third addition. This is connected with the fact that the divider may be substracted twice from the dividend, whilst a third time the provisional remainder becomes negative. The figure 2 in the counter of the highest rank indicates that the first figure of the quotient is 2. The absence of a carry in the third addition indicates that the reduction has proceeded too far and the remainder thus has, as it were, become negative, so that it is necessary to do a step backwards. For this purpose the divider itself is added to the provisional remainder, but a correction figure which is equal to 8 is then added to the first column:

```
(3)   2987004
      80231
      -------
(4)   1010104
```

The provisional remainder 10104 thus has acquired the correct value, but the first figure of the quotient is one too low. However, as will appear hereinafter, another

carry occurs during a subsequent operation, so that ultimately the correct result is obtained.

If the correction figure 8 were omitted, then by the addition of the divider in the fourth stage the number 3010104 would have been produced, so that ultimately the figure of the quotient would have become 1 too high. Subsequently, the complement of the divider, reduced one position in rank, is added several times to the provisional remainder for producing the second figure of the quotient.

(4) 1010104
9769

(5) 1107794
9769

(6) 1205484
9769

(7) 1303174
9769

(8) 1400864
9769

(9) 1498554

As may be seen, during the stages (5), (6), (7) and (8) a carry is added to the second column, but a carry is not added during stage (9), so that the second figure of the quotient is 4. Since during stage (9) the reduction has again proceeded too far, the divider as before is added to the provisional remainder, but now the correction figure 8 is added to the second column:

(9) 1498554
80231

(10) 2300864

The carry supplied to the first column gives the first figure of the quotient the correct value, viz. 2. However, the second figure of the quotient is still one too small. Subsequently, the complement of the divider, shifted one position to the right, is again added several times to the provisional remainder:

(10) 2300864
9769

(11) 2310633
9769

(12) 2320402
9769

(13) 2330171
9769

(14) 2339940

During the stages (11), (12) and (13), the third column receives a carry for producing the third figure of the quotient. During the stage (14), the said carry is absent, so that the third figure of the quotient is 3. Since the reduction has again proceeded too far, the divider must be added to the provisional remainder. Since the third figure has been assumed to be the last figure of the quotient, so that no further stages follow, the correction figure 9 instead of 8 is in this case supplied to the third column, so that the third figure directly acquires the correct value:

(14) 2339940
90231

(15) 2430171

Of the number ultimately registered in the totalisator viz. 2,430,171, the three first figures, viz. 243, constitute the quotient and the three last figures, viz. 171, constitute the remainder of the division.

The reason why the complement of the divider with respect to 10^4 has been chosen and hence a power of 10 which is larger than the number of figures of the divider, instead of for example, with respect to 10^3, is that no provisional remainder can then be present in the counter, in which during a subsequent operation a subsequent figure of the quotient must be formed. Thus, a separation between the provisional remainder and the quotient is always ensured, that is to say they cannot overlap.

If, for example, during the first stage, 769 that is the complement of 231 with respect to 1000 would have been added to the dividend:

056304
769

133204
769

210104
769

287004

then during the third addition again no carry would have been added to the first column and during the subsequent addition of the divider with the figure 8 as a correction in the first column, the following result would have been obtained:

287004
8231

110104

As may be seen, the figure 1 is registered, in the second column, in which during the subsequent operation the second figure of the quotient would have to be formed, that is to say in the counter concerned there is still a figure of the remainder which is not equal to zero, so that the second figure of the quotient would become wrong. However, it is fundamentally possible to choose the complement of the divider with respect to a power higher than 10^4, for example 10^5.

In order that the invention may be readily carried into effect, one embodiment will now be described, by way of example, with reference to the accompanying drawing.

Figs. 1*a* and 1*b* show a portion of a decimal calculating machine for carrying out divisions. The device comprises a key-board having a plurality of columns of keys T11, T12, etc., T21, T22, etc., T31, T32, etc., which columns correspond to different decades. For the sake of simplicity, the figure shows only three columns, but in practice this number may naturally be extended at will. By means of the keys, a connection may be established between the horizontal conductors B1, B2 . . . B0 and the vertical conductors S1, S2 and S3. The horizontal conductors are connected via decoupling rectifiers R17, R18, etc., R19, R20, etc., to outlets, 1, 2, 3 . . . 0 of dividing switches SA and SB. The inlets EA and EB of the dividing switches SA and SB are coupled via gating circuits P6 and P7 to a pulse generator IG. The gating circuits P6 and P7 are controlled by a bistable trigger circuit E1, so that in one condition, for example the operating condition, of trigger circuit E1 the gating circuit P6 can transmit the pulses from generator IG to the input EA and in the other condition, for example the rest condition, the gating circuit P7 can transmit the pulses to the input EB. The pulse generator IG is controlled by the bistable trigger circuit E2 in such manner that in the rest condition of this trigger circuit the pulse generator is cut off and in the operating condition it gives off pulses to the inputs of the gates P6 and P7. The dividing switches SA and SB are so designed as to supply successively positive pulses to the outlets 1, 2, 3 etc., when pulses are supplied to the associated inputs EA and EB. The dividing switches SA and SB are preferably of the electronic type and equipped, for example, with an electron-ray divider they are designed as a counting circuit having a plurality of outlets. The sequential outlets 1, 2, 3 . . . 9 are interconnected via rectifiers R1, R2 . . . R8 and R9, R10 . . . R16. The pulses appearing across the outlet 1 of device SA are supplied via rectifier R17 to the horizontal conductor B1 and also via rectifiers R2, R3 . . . R8 to the conductors B2, B3 . . . B9. The pulses across outlet 2 of device SA are supplied to conductor B2 and also via the rectifiers R2 . . . R8 to

the conductors B3 . . . B9. Thus, with each pulse cycle of the dividing switch SA, the horizontal conductors B1 . . . B9 and 1, 2, 3 . . . 9 receive pulses. When a given number, for example 231, is chosen by pushing the keys T32, T23 and T11, then during each pulse cycle of device SA there appear 1, 3 and 2 pulses on the vertical conductors S1, S2 and S3, in other words a number corresponding to the figures of the number chosen.

The conductors S1, S2 and S3 may be connected by means of a dividing switch VS via the gating circuits P1, P2 and P3 to different sections of a totalisator register TR. The totalisator register is designed in known manner with a chain of decade counters K1 to K7, for example electronic counting circuits, which each can count up to 10 pulses and supply a carrying pulse to the subsequent counter upon return to the zero-position. Although the dividing switch may fundamentally be of the electronic type, it is in the example under consideration designed as a mechanical switch of a type such as used in automatic telephone, systems having seven arms V1 to V7 which can be moved along outlet contacts under the control of a step magnet BM. In the rest position of VS, the conductors S1, S2 and S3 are connected via the gating circuits P1, P2 and P3 to the counters K3, K4, K5 and in its subsequent position are connected to the counters K2, K3, K4, etc. The gating circuits P1 to P5 are controlled by a device PB in such manner that these gates are successively made permeable to pulses. The object of this step is to prevent a counter from receiving any carrying pulse at the same moment at which a counting pulse would be received by this counter via dividing swicth VS. The device PB is so designed that, under the control of pulses received via the conductor EB, a releasing voltage is supplied in cyclic sequence to the gates P1 to P5, whilst at the end of each cycle, that is to say at the moment when gate P5 is cut off again, a pulse is given off to the conductor EG_1, which pulse will be indicated hereinafter as the final pulse. The number (231) chosen by means of the keys may be added to a number registered in the totalisator TR by causing dividing switch SA to produce a number of pulse cycles. During the first pulse cycle, the gate P1 transmits one pulse to counter K3, during the second cycle the gate P2 transmits three pulses to counter K4 and during the third cycle the gate P3 transmits two pulses to counter K5. At the end of each cycle, the device PB receives a pulse via outlet 0 of device SA, so that the subsequent gate is released.

For subtracting a number chosen by means of the keys, from a number registered in the totalisator TR, use is made of the dividing switch SB. This operation means, as is common practice in calculating machines, that the complement of the first number with respect to a suitably chosen power of 10 is added to the second number. To produce the complement of a number, the complement with respect to 9 is taken, for each figure, except for the figure of the lowest rank, for which the complement with respect to 10 must be chosen. For this purpose, the outlets 1 to 9 of dividing switch SB are so connected to the conductors B1 to B8 and B0 that these conductors during a pulse cycle of SB receive a number of pulses equal to the complement with respect to 9 of the number which would be supplied upon a pulse cycle of device SA. Thus, for example, the outlet 1 is connected to conductor B8, the outlet 2 is connected to conductor B7 and the outlet 9 is connected to conductor B0. Furthermore, the outlet 0 of SB is connected to conductor S1, so that conductor S1 receives a correction pulse upon each cycle of SB, so as to produce the complement with respect to 10 for the figures of the key column concerned. If a 0 would have been chosen as the last figure by pushing key T10, conductor S1 receives 10 pulses, resulting in a carry which is active as a correcting pulse for the penultimate figure so as to produce now the complement with respect to 10 for the penultimate figure.

For carrying out the division, the dividend 56,304 is first brought into the counters K5, K4, K3, K2 and K1 of the totalisator TR in a manner not shown, for example with the use of the keys, whereupon the divider (231) is formed on the key-board. In the embodiment shown, the number of counters is 7. The number of figures of the dividend may then be at most equal to 5, since at the beginning of the division the counters K6 and K7 must be "empty" for reasons specified hereinafter. Furthermore, the switch ES, which is mechanically coupled to the switch E'S', is given a determined position in accordance with the number of figures of the quotient to be produced.

The process is initiated by pushing key TOO, so that the voltage source U2 is connected via a switch contact U6, the switch ES and the key TOO to the monostable trigger circuit MS, which then gives off a starting pulse to the trigger circuits E2 and E3, causing the latter to assume the operating positions. The trigger circuit E1 initially is in the rest condition, gate P7 then being conducting and gate P6 being cut-off. If necessary, the said trigger circuit may be forced into the rest condition under the control of the starting pulse via the conductors SE (shown in dotted line). Trigger E2 decouples the pulse generator IG which subsequently supplies pulses via gate P7 to the device SB. During the first pulse cycle of SB, eight pulses are supplied via the conductor B1 and cycle T11 and a ninth pulse is supplied via outlet 0 of SB to gate P1, which transmits these pulses via switch section V1 to the counter K3 which passes into the condition 2 and supplies a carrying pulse to counter K4 passing through the zero-position. During the second pulse cycle, six pulses are supplied via conductor B3, key T23, gate P2 and switch section V2 to counter K4 which passes into condition 3 and supplies a carrying pulse to counter K5. During the third cycle, seven pulses are supplied via conductor B2, key T32, gate P3 and switch section V3, to counter K5 which passes into condition 3 and supplies a carrying pulse to counter K6. During the fourth cycle, nine pulses are transmitted via conductor ES, gate P4 and switch section V4 to counter K6, which returns to position 0 and transmits a carrying pulse ot counter K7, which carrying pulse is also supplied via switch section V5 and rectifier G3 to the trigger circuit E3, which returns to its rest position and cuts off gate P8. During the fifth pulse cycle, no pulses are supplied to the totalisator TR. The pulses which the device SB gives off to its outlet 0 at the end of each cycle are supplied via rectifier G2 and conductor EB to the device PB, which subsequently passes into the subsequent condition and releases the subsequent gate. After the fifth cycle, the device PB controls via conductor EG the final pulse as a sign that the first addition is completed. The said final pulse cannot pass through gate P8 the latter being cut off in the rest condition of the trigger circuit E3, and is supplied via rectifier G1 to trigger circuit E3 which returns to the operating position and releases gate P8 with a small retardation. 1,033,204 has now been registered in the totalisator register.

During the subsequent five cycles of SB, the complement of the divider is added in a similar manner to the totalisator for the second time, whereafter it registers the number 2,010,104. The carry controlled by counter K6 via switch section V5 and conductor CG restores the trigger E3 again to its rest position, whereafter the final pulse brings the trigger E3 again in the operating position via conductor EG and rectifier G1.

By the third series of five pulse cycles, the complement of the divider is added to the number of the totalisator TR, for the third time, so that it registers 2,987,004. However, in this case, the carrying pulse via conductor CG is absent, which means arithmetically that the reduction has proceeded too far and the remainder thus has, as

it were, become negative. The final pulse via conductor EG, which indicates the end of this operation, now brings the trigger E3 via rectifier G1 into the rest condition, but is still transmitted by gate P8 before this gate is cut off, since the change-over of trigger E3 takes up some time or the control of gate P8 by trigger E3 is artificially delayed a little. The pulse transmitted by gate P8 brings the trigger E1 into the operating condition gate P6 then being conducting and gate P7 being cut off. During the subsequent five pulse cycles of dividing switch SA, the divider together with a correcting term is added to the totalisator (operation 4). During the first pulse cycle, the counter K3 receives one pulse. During the second cycle the counter K4 receives three pulses and transmits a carrying pulse to counter K5. During the third cycle, counter K5 receives two pulses and transmits a carry to counter K6, which thus returns to the zero-position and, in turn, transmits a carry to counter K7, which carrying pulse also brings the trigger circuit E3 into the operating condition via switch section V5 and conductor CG. During the fourth cycle of the device SA, no pulses are supplied to the totalisator TR. During the fifth cycle at last, counter K7 receives 8 correcting pulses via outlet 8 of device SA, gate P5 and switch section V5. The totalisator now registers 1,010,104. The final pulse which occurs across conductor EG at the end of the fifth cycle is transmitted by gate P8 and brings the trigger E1 again into the rest condition, in which gate P7 is conducting. This pulse brings the trigger circuit E3 via rectifier G1 into the rest condition, so that gate P8 is cut off. Furthermore, the trigger circuit E1 gives off a pulse to the step magnet BM at the moment when it returns to the rest condition, so that the dividing switch VS passes into the subsequent position, in which now gate P1 is connected to counter K2, gate P2 is connected to counter K3, etc. The same pulse is supplied via conductor EW to the trigger E2 which passes into the rest condition and cuts off generator IG. When dividing switch VS passes into the subsequent position, the contact V6 transiently interrupts the above-mentioned connection between the voltage source U2 and the monostable trigger circuit MS via section V6, switch ES and key TOO. At the moment when the switch VS reaches the new position, this circuit is completed again and the monostable trigger circuit MS again gives off a pulse to the trigger circuit E2, which again passes into the operating condition and releases the generator IG. At the same time, the trigger circuit E3 as a result of this pulse returns to the operating condition.

The process is now repeated. At first, the complement of the divider is added five times to the totalisator TR (stages (5) to (9)), whereafter it registers 1,498,554. During the first four additions, the counter K5 each time transmits a carrying pulse to counter K6 for producing the second figure of the quotient. These carrying pulses bring trigger E3 via switch section V5 and conductor CG into the rest condition in the manner previously described, whereafter at the end of each addition the final pulses restore the trigger E3 to the operating condition via conductor EG and rectifier G1. However, during the fifth addition (operation 9) no carrying pulse is produced in counter circuit K5, so that the final pulse via conductor EG is transmitted by gate P8 and the trigger E1 passes into the operating condition. Subsequently, the divider together with its correcting term is added to the counters K2 to K6 (operation 10). During the last cycle of device SA, a carrying pulse occurs in counter K6, which brings counter K7 from position 1 to position 2, so that counter K7 now registers the correct value of the first figure of the quotient. The totalisator TR then registers 2,300,864. The second figure from the left, which corresponds to the second figure of the quotient, is now still one too low, but is given the correct value during the subsequent third stage. At the end of the second stage, switch VS is brought into the subsequent position, in which gate P1 is connected via switch section V1 to counter K1, gate P2 is connected via switch section V2 to counter K2, etc.

During the third stage, the complement of the divider is added 4 times to the number of the totalisator TR (stages 11 to 14). The first three times the counter K4 gives off a carrying pulse to counter K5 for producing the third figure of the quotient, but the fourth time this pulse is absent, so that the trigger circuit E1 again passes into the operating condition and releases gate P6. The totalisator then registers 2,339,940. Finally, the divider is added to the totalisator, but in this case nine correcting pulses instead of eight must be supplied to counter K5. The device SA again gives off five pulse cycles for this addition. During the fifth cycle, eight pulses are supplied to counter K5 via gate P5 and switch section V5, so that this counter passes into position 2 and gives off a carrying pulse to counter K6, when passing through the zero-position, so that the second figure of the quotient is given the correct value 4. The totalisator now registers 2,420,171. The third figure of the quotient thus is still one too low. At the end of the fifth cycle, the device PB again gives off a final pulse, so that the trigger E1 changes its condition and gives off a pulse to conductor EW and to the step magnet BM of the dividing switch VS, so that the latter makes one step. Switch section V6 now reaches a contact which is not connected via switch ES and key TOO to the monostable trigger MS, so that the latter cannot again produce a pulse and the process is terminated. However, before switch VS leaves the position occupied, the pulse across conductor EW is supplied via the switching arm E'S' (which before pushing key TOO has been adjusted to the position concerned), switching section V6, conductor CG and switching section V5 to counter K5, which thus receives the ninth correcting pulse and passes into position 3. The totalisator now registers 2,430,171. The number 243 registered in the counters K7, K6 and K5 indicates the quotient and the number 171 registered in the counters K3, K2 and K1 indicates the remainder of the division.

In the embodiment above described, the figures struck by the keys are transferred to the totalisator one after another under the control of the device. However, it is fundamentally also possible to supply these figures simultaneously to the totalisator, if care is taken that the carries are supplied to the counter of next-higher rank with some delay, so that these pulses do not coincide with the pulses supplied via the keys. In such a case, the gates P1 to P5 and the device PB may be omitted, the conductors S1 to S3 then being connected directly to the arms V1 to V3 of switch VS and the conductor EB being connected to the conductor EG.

What is claimed is:

1. A circuit for carrying out a division of a dividend by a divisor in the decimal system, comprising a chain of decade counters equal in number to at least two greater than the number of figures of the dividend, means for initially registering the figures of the dividend in said decade counters, respectively, at least the two highest-rank decade counters initially registering the figure zero, a plurality of division switches connected to actuate said chain of decade counters by delivering a sequence of pulses to said counters to effect a sequence of stages of the division process in which, during each stage of the division process, the division switches add pulses representative of the complement of the divisor with respect to 10^p, where p is an integer at least one larger than the number of figures of the divisor, to the number registered in a given part of said chain of decade counters constituted by p decade counters of sequential ranks, any carry pulses occurring during these additions being supplied from said given part of the chain of decade counters to the decade counter of next higher rank serving to produce the quotient, the figures registered in said given part of the chain of decade counters being shifted one position

in the direction of lower rank in said chain of decade counters after each said stage of the division, adding means responsive to the lack of a carry pulse in a stage of the division process for subsequently adding pulses representative of the divisor to the number then registered in said given part of the chain of decade counters, means for adding pulses representative of a correcting figure of eight to the number registered in said given part of decade counter in addition to said subsequently added pulses, and means for adding pulses representative of a correcting figure of nine in addition to said subsequently added pulse to the number registered in said given part of the decade counter when the least significant figure of the quotient is produced.

2. A circuit as claimed in claim 1, including a first pulse generator for producing a cycle of pulses and a second pulse generator for producing a cycle of pulses, and in which said division switches include switching means for selectively connecting said first pulse generator to said decade counters thereby to supply numbers of pulses to said decade counters corresponding to the figures of a number to be registered and to supply said eight correcting pulses to said decade counters, and switching means for selectively connecting said second pulse generator to said decade counters thereby to supply numbers of pulses to said decade counters corresponding to the figures representing said complement of the divisor, and means connected to control said pulse generators in response to the occurrence of said carry pulse and with respect to a final pulse produced at the end of a cycle by each of said pulse generators whereby an operative pulse generator produces a subsequent cycle of pulses upon the occurrence of both a final pulse and a carry pulse and whereby an operative pulse generator is cut off and the other pulse generator is made operative upon the occurrence of a final pulse only.

3. A circuit as claimed in claim 2, including first and second trigger circuits each adapted to alternately assume two electrically stable states, said first trigger circuit being connected to said first and second pulse generators whereby said first pulse generator is made operative when said first trigger circuit is in one stable state and said second pulse generator is made operative when said first trigger circuit is in the other stable state, means connected to feed said carry pulses and said final pulses to said second trigger circuit whereby said second trigger circuit changes from one stable state to the other when a pulse is received thereby, and a gate circuit connected to be controlled by said second trigger circuit and adapted to feed said final pulses to said first trigger circuit when rendered operative by said second trigger circuit.

4. A circuit as claimed in claim 2, including means for terminating the division process, said terminating means comprising means for causing said first pulse generator to generate an additional correcting pulse whereby nine correcting pulses are produced for adding said correcting figure of nine to the decade counter in which the least significant figure of the quotient is produced.

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