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(54) **Title**: SEMICONDUCTOR LIGHT EMITTING DEVICE AND METHOD FOR MANUFACTURING SAME

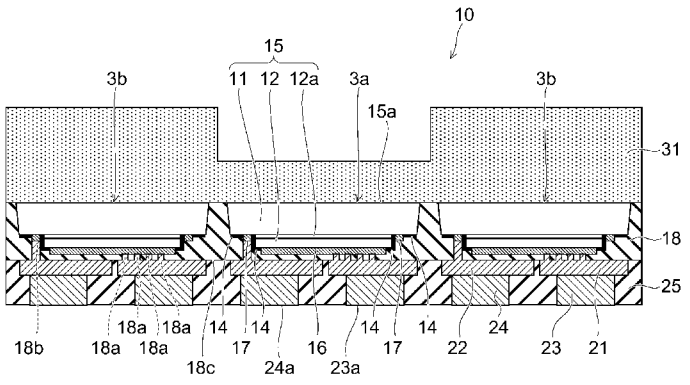

FIG. 1

(57) **Abstract**: According to one embodiment, a semiconductor light emitting device includes: not less than three chips (3a, 3b), each of the chips including a semiconductor layer (15) having a first face (15a), a second face formed on a side opposite to the first face, and a light emitting layer (12a), a p-side electrode (16) provided on the second face in a region having the light emitting layer, and an n-side electrode (17) provided on the second face in a region without having the light emitting layer; and fluorescent body layers (31) of a same kind provided on the first faces of the chips. The chips include: a central chip (3a) centrally positioned in a plan view, and at least two peripheral chips (3b) arranged symmetrically to each other sandwiching the central chip (3a) in the plan view. A thickness of the fluorescent body layer (31) on the first face is same among the peripheral chips, and the fluorescent body layer (31) on the first face of the central chip and the fluorescent body layers (31) on the first faces of the peripheral chips have thicknesses different from each other.

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Description

Title of Invention: SEMICONDUCTOR LIGHT EMITTING DEVICE AND METHOD FOR MANUFACTURING SAME

Field

[0001] Embodiments of the invention relates to a semiconductor light emitting device, and a method for manufacturing same.

Background

[0002] The reduction of chromaticity variation in the development of a white light emitting diode (LED) is one of major problems. In particular, in a wafer-level packaging technique which carries out formation of a wiring layer, protection resin, and a luminescent layer collectively for a plurality of chips within a wafer without performing a chip selection process, emission wavelength variation among the chips within the wafer affects the chromaticity variation considerably.

Citation List

Patent Literature

[0003] PTL 1: JP-A 2011-517090

PTL 2: JP-A 2010-147318

Brief Description of Drawings

[0004] FIG. 1 is a schematic cross-sectional view of a semiconductor light emitting device 10 of a first embodiment.

FIG. 2A is a schematic plan view of the semiconductor light emitting device of a first embodiment, and FIG. 2B is a schematic plan view of one chip.

FIG. 3A-3C show layouts of a plurality of chips in a semiconductor light emitting device of first embodiment.

FIG. 4 is a circuit diagram showing a connection relationship between a plurality of chips in a semiconductor light emitting device of a first embodiment.

FIGs. 5A-7D show cross sections showing a manufacturing method of the semiconductor light emitting device of a first embodiment.

FIGs. 8A-8E show cross sections showing a manufacturing method of the semiconductor light emitting device of a second embodiment.

FIGs. 9A-9D show cross sections showing a manufacturing method of the semiconductor light emitting device of a third embodiment.

FIGs. 10A-11D show cross sections showing a manufacturing method of the semiconductor light emitting device of a fourth embodiment.

FIGs. 12A-12C show cross sections showing a manufacturing method of the semiconductor light emitting device of a fifth embodiment.

FIGs. 13A-13C show cross sections showing a manufacturing method of the semiconductor light emitting device of a sixth embodiment.

FIGs. 14A and 14B show cross sections showing a manufacturing method of the semiconductor light emitting device of a seventh embodiment.

FIG. 15 is a CIExy chromaticity diagram showing adjustable range of chromaticity of a semiconductor light emitting device of a first embodiment.

FIG. 16A is a CIExy chromaticity diagram showing adjustable range of chromaticity of semiconductor light emitting devices of a fourth and sixth embodiments, and FIG. 16B is a CIExy chromaticity diagram showing adjustable range of chromaticity of a semiconductor light emitting device of a fifth embodiment.

Detailed Description

[0005] According to one embodiment, a semiconductor light emitting device includes: not less than three chips, each of the chips including a semiconductor layer having a first face, a second face formed on a side opposite to the first face, and a light emitting layer, a p-side electrode provided on the second face in a region having the light emitting layer, and an n-side electrode provided on the second face in a region without having the light emitting layer; and fluorescent body layers of a same kind provided on the first faces of the chips. The chips include: a central chip centrally positioned in a plan view, and at least two peripheral chips arranged symmetrically to each other sandwiching the central chip in the plan view. A thickness of the fluorescent body layer on the first face is same among the peripheral chips, and the fluorescent body layer on the first face of the central chip and the fluorescent body layers on the first faces of the peripheral chips have thicknesses different from each other.

[0006] Embodiments of the invention will now be described with reference to the drawings. In each of the drawings, like components are marked with like reference numerals.

[0007] (First embodiment)

FIG. 1 is a schematic cross-sectional view of a semiconductor light emitting device 10 of a first embodiment.

FIG. 2A is a schematic plan view of the semiconductor light emitting device 10, and FIG. 2B is a schematic plan view of one chip.

[0008] The semiconductor light emitting device 10 is a multi-tip device including a plurality of chips 3a and 3b in a package structure body which is formed at a wafer level to be described below. The plurality of chips 3a and 3b are separated from one another. Each of the chips 3a and 3b has a semiconductor layer 15, a p-side electrode 16, and an n-side electrode 17.

[0009] The plurality of chips are denoted by different numerals 3a and 3b depending on a positional difference in the plan view shown in FIG. 2A. However, the chip 3a and the chip 3b have the same structure, and are sometimes denoted simply by a numeral 3

representatively without discrimination between the chips 3a and 3b.

[0010] The semiconductor layer 15 has a first face (upper face in FIG. 1) 15a and a second face formed on the side opposite thereto. The electrodes and wirings are provided on the second face side. Light is emitted to the outside mainly from the first face 15a on the side opposite to the second face.

[0011] Furthermore, the semiconductor layer 15 has a first semiconductor layer 11 and a second semiconductor layer 12. The first semiconductor layer 11 and the second semiconductor layer 12 are made of material containing, for example, gallium nitride. The first semiconductor layer 11 includes, for example, a foundation buffer layer, an n-type layer, and the like, and the n-type layer functions as a lateral current pathway. The second semiconductor layer 12 includes a p-type layer and a light emitting layer (active layer) 12a.

[0012] The second face side of the semiconductor layer 15 is processed into a convex-concave shape. The convex part formed on the second face side includes the light emitting layer 12a. On the surface of the second semiconductor layer 12 being the surface of the convex part thereof, a p-side electrode 16 is provided. That is, the p-side electrode 16 is provided on a region having the light emitting layer 12a.

[0013] On the periphery of the convex part on the second face side of the semiconductor layer 15, a region which does not have the second semiconductor layer 12 including the light emitting layer 12a is provided, and, on the face of the first semiconductor layer 11 in the region, an n-side electrode 17 is provided. That is, the n-side electrode 17 is provided on the region without including the light emitting layer 12a.

[0014] In the plan view of the second face shown in FIG. 2B, the n-side electrode 17 surrounds the periphery of the p-side electrode 16 continuously. The plan view layout of the p-side electrode 16 and the n-side electrode 17 is not limited to the layout shown in FIG. 2B and another layout can be used.

[0015] On the second face side, the area of the second semiconductor layer including the light emitting layer 12a is larger than the area of the first semiconductor layer 11 which does not include the light emitting layer 12a. Furthermore, the area of the p-side electrode 16 is larger than the area of the n-side electrode 17. Accordingly, it is possible to obtain a large light emitting region.

[0016] On a side face of the second semiconductor layer 12 including the light emitting layer 12a, an insulating film 14 is provided. Moreover, the insulating film 14 is also provided on the second face on which the p-side electrode 16 and the n-side electrode 17 are not provided. The insulating film 14 is an inorganic insulating film such as, for example, a silicon oxide film and a silicon nitride film.

[0017] The second face side, on which the insulating film 14, the p-side electrode 16, and the n-side electrode 17 are provided, is covered by a first insulating layer (hereinafter,

simply referred to as insulating layer) 18. The first face 15a is not covered by the insulating layer 18.

[0018] Furthermore, the insulating layer 18 fills a space between the chips 3a and 3b separated from each other, and covers sides of the chips 3a and 3b. A side of the semiconductor layer 15 continuing from the first face 15a is covered by the insulating layer 18. The insulating layer 18 covering each side face of the chips 3a and 3b constitutes a side face of the semiconductor light emitting device 10 together with a resin layer 25 covering a side of a wiring part which will be described below.

[0019] The insulating layer 18 is a resin such as polyimide or the like having a good patterning properties for a fine opening, for example. Alternatively, an inorganic material such as silicon oxide or silicon nitride may be used for the insulating layer 18.

[0020] In the insulating layer 18, a first via 18a reaching the p-side electrode 16 and a second via 18b reaching the n-side electrode 17 are formed. Moreover, the insulating layer 18 has a wiring face 18c on the side opposite to the first face 15a.

[0021] On the wiring face 18c, a p-side wiring layer 21 and an n-side wiring layer 22 are provided apart from each other. For each one of the chips 3a and 3b, one p-side wiring layer 21 and one n-side wiring layer 22 are provided.

[0022] The p-side wiring layer 21 is also provided within the first via 18a. The p-side wiring layer 21 is electrically connected to the p-side electrode 16 through the plurality of first vias 18a.

[0023] The n-side wiring layer 22 is also provided within the second via 18b. The n-side wiring layer 22 is electrically connected to the n-side electrode 17 through one, for example, second via 18b.

[0024] On the face of the p-side wiring layer 21 on the side opposite to the chips 3a and 3b, a p-side metal pillar 23 is provided. The p-side metal pillar 23 has a thickness larger than the thickness of the p-side wiring layer 21. The p-side wiring layer 21 and the p-side metal pillar 23 constitute a p-side wiring part in the embodiment.

[0025] On the face of the n-side wiring layer 22 on the side opposite to the chips 3a and 3b, an n-side metal pillar 24 is provided. The n-side metal pillar 24 has a thickness larger than the thickness of the n-side wiring layer 22. The n-side wiring layer 22 and the n-side metal pillar 24 constitute an n-side wiring part in the embodiment.

[0026] Furthermore, on the wiring face 18c of the insulating layer 18, a resin layer 25 is provided as a second insulating layer. The resin layer 25 covers the periphery of the p-side wiring part and the periphery of the n-side wiring part.

[0027] The face of the p-side wiring layer 21 except a connection face with the p-side metal pillar 23 and the face of the n-side wiring layer 22 except a connection face with the n-side metal pillar 24 are covered by the resin layer 25. Furthermore, the resin layer 25 is provided between the p-side metal pillar 23 and the n-side metal pillar 24, and covers a

side face of the p-side metal pillar 23 and a side face of the n-side metal pillar 24. The resin layer 25 fills a space between the p-side metal pillar 23 and the n-side metal pillar 24.

[0028] The face of the p-side metal pillar 23 on the side opposite to the p-side wiring layer 21 is exposed without being covered by the resin layer 25, and functions as a p-side external terminal 23a which is to be bonded to a mounting substrate. The face of the n-side metal pillar 24 on the side opposite to the n-side wiring layer 22 is exposed without being covered by the resin layer 25, and functions as an n-side external terminal 24a which is to be bonded to the mounting substrate.

[0029] The respective thicknesses of the p-side wiring part, the n-side wiring part, and the resin layer 25 are larger than each of the thickness of the chips 3a and 3b. The aspect ratio (ration of a thickness to a planar size) of the p-side metal pillar 23 and the n-side metal pillar 24 is not limited to a value not smaller than one and the ratio may be smaller than one.

[0030] The p-side metal pillar 23, the n-side metal pillar 24, and the resin layer 25 which reinforces the metal pillars function as a support body for the chips 3a and 3b. Accordingly, even when a substrate used for forming the semiconductor layer 15 is removed as will be described below, the support body including the p-side metal pillar 23, the n-side metal pillar 24, and the resin layer 25 supports the chips 3a and 3b stably, and can increase the mechanical strength of the semiconductor light emitting device 10.

[0031] Furthermore, in a state in which the semiconductor light emitting device 10 is mounted on the mounting substrate, it is possible to reduce a stress applied to the semiconductor layer 15, by causing the p-side metal pillar 23 and the n-side metal pillar 24 to absorb the stress.

[0032] As the material for the p-side wiring layer 21, the n-side wiring layer 22, the p-side metal pillar 23, and the n-side metal pillar 24, copper, gold, nickel, silver, or the like can be used. When copper is used among these materials, it is possible to obtain a good thermal conductivity, a high migration resistance and a distinguished adhesion to insulating material.

[0033] As the resin layer 25, it is preferable to use a resin having a coefficient of thermal expansion the same as or close to the coefficient of the mounting substrate. An example of such resin can include, for example, epoxy resin, silicone resin, fluorine resin, or the like.

[0034] Furthermore, the resin layer 25 may be caused to contain carbon black to be provided with light-shielding properties for the light emitted from the light emitting layer 12a. In addition, the resin layer 25 may be caused to contain powder having a reflectivity for the light emitted from the light emitting layer 12a.

[0035] The first semiconductor layer 11 is electrically connected to the n-side metal pillar 24 including the n-side external terminal 24a via the n-side electrode 17 and the n-side wiring layer 22. The second semiconductor layer 12 including the light emitting layer 12a is electrically connected to the p-side metal pillar 23 including the p-side external terminal 23a via the p-side electrode 16 and the p-side wiring layer 21.

[0036] A part of the n-side wiring layer 22 overlaps the insulating layer 18 on a light emitting region including the light emitting layer 12a. The area of the n-side wiring layer 22 is larger than the n-side electrode 17. Furthermore, the area of the n-side wiring layer 22 expanded on the insulating layer 18 is larger than the area connecting the n-side wiring layer to the n-side electrode 17 through the second via 18b.

[0037] It is possible to obtain a high light output by the light emitting layer 12a formed over a region larger than the n-side electrode 17. And also, it is possible to realize a structure in which the n-side electrode 17 provided in a region, which is smaller than the light emitting region and does not include the light emitting layer 12a, is rearranged on the mounting face side as the n-side wiring layer 22 having an area larger than the area of this region.

[0038] The area connecting the p-side wiring layer 21 to the p-side electrode 16 through the plurality of first vias 18a is larger than the area connecting the n-side wiring layer 22 to the n-side electrode 17 through the second via 18b. Accordingly, it is possible to improve current distribution to the light emitting layer 12a and also to improve radiation properties of heat generated in the light emitting layer 12a.

[0039] On the first face 15a of the semiconductor layer 15, a fluorescent body layer 31 is provided. The fluorescent body layer 31 contains phosphor particles capable of absorbing the emitted light (excited light) from the light emitting layer 12a and capable of emitting wavelength-converted light. The phosphor particles are dispersed in transparent resin which is transparent to the light from the light emitting layer 12a and the wavelength-converted light of the phosphor particles. The semiconductor light emitting device 10 can emit mixed light of the light from the light emitting layer 12a and the wavelength-converted light of the phosphor particles.

[0040] For example, when the phosphor particles are set to yellow phosphor particles emitting yellow light, it is possible to obtain white color or light bulb color as a mixed color between blue light from the light emitting layer 12a which is made of GaN-based fluorescent material and yellow light which is the wavelength-converted light in the fluorescent body layer 31.

[0041] For example, as shown in FIGS. 2A and 2B, the outer shape of the semiconductor light emitting device 10 in the plan view is formed in a rectangular shape, and three chips including one central chip 3a and two peripheral chips 3b are aligned in the longitudinal direction of the rectangle (one-dimensional direction).

[0042] The central chip 3a is positioned at the center of the three chips in the one-dimensional alignment direction. The two peripheral chips 3b are arranged symmetrically to each other sandwiching the central chip 3a in the one-dimensional alignment direction.

[0043] On the central chip 3a and the peripheral chips 3b, the same kind of fluorescent body layers 31 are provided. For example, the fluorescent body layers 31 containing the same kind of yellow phosphor particles are provided on the central chip 3a and the peripheral chips 3b.

[0044] The thicknesses of the fluorescent body layers 31 provided on the first faces 15a of the respective two peripheral chips 3b are the same.

[0045] The thickness of the fluorescent body layer 31 on the first face 15a in the central chip 3a is different from the thickness of the fluorescent body layers 31 on the first faces 15a in the peripheral chips 3b. In an example shown in FIG. 1, the fluorescent body layer 31 on the central chip 3a has a thickness smaller than the thickness of the fluorescent body layers 31 on the peripheral chips 3b.

[0046] As will be described below, the process of forming the fluorescent body layer 31 has a process of collectively supplying a liquid transparent resin in which phosphor particles are dispersed, on a plurality of chips in a wafer state and a process of performing thermal curing. Accordingly, the concentration (density) of the phosphor particles is approximately uniform within the wafer face.

[0047] Accordingly, a relatively thin fluorescent body layer 31 contains a smaller amount of the phosphor particles and a relatively thick fluorescent body layer 31 contains a larger amount of the phosphor particles. By adjusting the thickness of the fluorescent body layer 31, it is possible to adjust the chromaticity of the mixed light of the light emitted from the chips 3a and 3b and the wavelength-converted light in the fluorescent body layer 31.

[0048] FIG. 15 shows a CIExy chromaticity diagram. The coordinates A show the chromaticity of the blue light emitted from a GaN-based chip, and the coordinates B show the chromaticity of the light emitted from a yellow fluorescent body layer alone.

[0049] By adjusting the thickness of the fluorescent body layer 31, it is possible to adjust chromaticity along a straight line shown by the broken line between the coordinates A and the coordinate B. The chromaticity can be adjusted toward the coordinates A side when the fluorescent body layer 31 is relatively thin, and the chromaticity can be adjusted toward the coordinates B side when the fluorescent body layer 31 is relatively thick.

[0050] Furthermore, FIG. 4 is a circuit diagram showing a connection relationship between the central chip 3a and the peripheral chip 3b.

[0051] The central chip 3a and the peripheral chips 3b are connected in parallel to a power

supply 100. The two peripheral chips 3b are connected in series.

[0052] By adjusting power supplied from the power supply 100 to each of the central chip 3a and the peripheral chips 3b which are connected in parallel, it is possible to adjust a ratio of light emission intensity between the central chip 3a and the peripheral chips 3b.

[0053] For example, by changing an input current amount relatively between the central chip 3a and the peripheral chips 3b, it is possible to adjust the ratio of the light emission intensity between the central chip 3a and the peripheral chips 3b. Alternatively, by adjusting a duty ratio of the input power between the central chip 3a and the peripheral chips 3b, it is possible to adjust the ratio of the light emission intensity between the central chip 3a and the peripheral chips 3b.

[0054] When the input power (current) is increased for the central chip 3a in which the fluorescent body layer 31 is relatively thin, the semiconductor light emitting device 10 emits mixed light having a larger amount of a blue component. When the input power (current) for the peripheral chips 3b in which the fluorescent body layers 31 are relatively thick, the semiconductor light emitting device 10 emits mixed light having a larger amount of a yellow component.

[0055] That is, by changing the thickness of the fluorescent body layer 31 provided on the first face 15a between the central chip 3a and the peripheral chips 3b and also by adjusting the input power between the central chip 3a and the peripheral chips 3b which are connected in parallel, it is possible to adjust the chromaticity of the mixed light emitted from the semiconductor light emitting device 10.

[0056] Moreover, according to the embodiment, while the thickness of the fluorescent body layer 31 is changed between the center and the periphery in the plan view from the light emitting face side, the fluorescent body layers 31 which have the same thickness and arranged symmetrically to each other with respect to the center are provided on the periphery. Accordingly, when the semiconductor light emitting device 10 is viewed from the fluorescent body layer 31 side in FIG. 1, a uniform color mixing effect and light distribution can be obtained.

[0057] FIGS. 3A to 3C show other specific examples for the plan view layout of the central chip 3a and the peripheral chip 3b.

[0058] The plurality of chips including the central chip 3a and the peripheral chip 3b may be aligned in two-dimensional directions in a plane as shown in FIGS. 3A to 3C, not limited to the one dimensional direction. The number of the central chips 3a is not limited to one and may be not less than two. At least not less than two chips 3b are arranged symmetrically to each other sandwiching the central chip 3a, on the periphery of the central chip 3a.

[0059] FIG. 3A shows a layout in which four peripheral chips 3b are aligned in a cross

shape on the periphery of one central chip 3a.

FIG. 3B show a layout in which eight peripheral chips 3b are aligned in a grid pattern on the periphery of one central chip 3a.

FIG. 3C shows a layout in which 12 peripheral chips 3b are aligned in a grid pattern on the periphery of four central chips 3a.

[0060] In any of the specific examples of FIGS 3A to 3C, the thickness of the fluorescent body layer 31 provided on the first face 15a is changed between the central chip 3a and the peripheral chip 3b, and also the fluorescent body layers 31 having the same thickness are provided on the plurality of peripheral chips 3b. Accordingly, when the semiconductor light emitting device is viewed from the light emitting face side, a uniform color mixing effect and light distribution can be obtained.

[0061] Next, with reference to FIG. 5A to FIG. 7D, a manufacturing method of the semiconductor light emitting device 10 of the embodiment will be explained.

[0062] FIG. 5A shows a cross section of a wafer on which the semiconductor layer 15 including the first semiconductor layer 11 and the second semiconductor layer 12 is formed on a major face of the substrate 5. The first semiconductor layer 11 is formed on the major face of the substrate 5, and the second semiconductor layer 12 is formed on this first semiconductor layer 11.

[0063] For example, the first semiconductor layer 11 and the second semiconductor layer 12 which are made of gallium nitride-based material can be grown epitaxially on a sapphire substrate by an MOCVD (metal organic vapor deposition) method.

[0064] The first semiconductor layer 11 includes the foundation buffer layer and the n-type GaN layer. The second semiconductor layer 12 includes the light emitting layer 12a (shown in FIG. 1) and the p-type GaN layer. For the light emitting layer 12a, it is possible to use material emitting light of blue, violet, blue violet, near ultraviolet, ultraviolet, or the like. The face contacting the substrate 5 in the first semiconductor layer 11 is the first face 15a of the semiconductor layer 15.

[0065] After the semiconductor layer 15 has been formed on the substrate 5, the second semiconductor layer 12 is selectively removed as shown in FIG. 5B by RIE (Reactive Ion Etching) using a resist which is not shown in the drawing, and the first semiconductor layer 11 is exposed selectively. The region where the first semiconductor layer 11 is exposed does not include the light emitting layer 12a.

[0066] Next, as shown FIG. 5C, the p-side electrode 16 is formed on the face of the second semiconductor layer 12 and the n-side electrode 17 is formed on the face of the first semiconductor layer 11. The p-side electrode 16 and the n-side electrode 17 are formed by a sputter method, an evaporation method, or the like, for example. For the p-side electrode 16 and the n-side electrode 17, either one may be formed first and both ones may be formed with the same material at the same time.

[0067] Here, while illustration will be omitted from the process cross-sectional views after FIG. 5C, the insulating film 14 shown in FIG. 1 is formed on the second face side.

[0068] Next, a groove 6 reaching the substrate 5 is formed in the semiconductor layer 15 as shown in FIG. 5C by RIE, for example, using a resist mask which is not shown in the drawing. The grooves 6 are formed, for example, in a planar layout of a grid pattern, on the substrate 5 in a wafer state. The semiconductor layer 15 is divided into the plurality of chips 3 by the grooves 6.

[0069] The process dividing the semiconductor layer 15 into the plurality of chips 3 may be performed in the step shown in FIG. 5B before the electrodes 16 and 17 are formed.

[0070] Next, the whole exposed part on the substrate 5 is covered by the insulating layer 18 shown in FIG. 6A. After that, the first via 18a and the second via 18b are formed in the insulating layer 18 by etching using a resist mask which is not shown in the drawing. The first via 18a reaches the p-side electrode 16 and the second via 18b reaches the n-side electrode 17.

[0071] Next, a metal film, which is not shown in the drawing, functioning as a seed metal for plating is formed on the wiring face 18c which is the upper face of the insulating layer 18, the inner wall of the first via 18a, and the inner wall of the second via 18b. Then, resist which is not shown in the drawing is formed selectively on the metal film, and Cu electrolytic plating using the metal film as a current path is performed.

[0072] By this plating, on the wiring face 18c, as shown in FIG. 6B, the p-side wiring layer 21 and the n-side wiring layer 22 are formed selectively. The p-side wiring layer 21 and the n-side wiring layer 22 are made of copper materials, for example, which are formed by plating at the same time.

[0073] The p-side wiring layer 21 is also formed within the first via 18a and electrically connected to the p-side electrode 16 via the metal film of the seed metal. The n-side wiring layer 22 is also formed within the second via 18b and electrically connected to the n-side electrode 17 via the metal film of the seed metal.

[0074] Next, Cu electrolytic plating is performed using resist which is not shown in the drawing as a mask and using the still remaining metal film as a current path. By this plating, as shown in FIG. 6C, the p-side metal pillar 23 and the n-side metal pillar 24 are formed. The p-side metal pillar 23 is formed on the p-side wiring layer 21, and the n-side metal pillar 24 is formed on the n-side wiring layer 22.

[0075] After the p-side metal pillar 23 and the n-side metal pillar 24 have been formed, the exposed part of the metal film which has been used as the seed metal is removed. Accordingly, the metal film connecting the p-side wiring layer 21 and the n-side wiring layer 22 is cut out.

[0076] Next, the resin layer 25 shown in FIG. 1 is formed. Then, in a state in which the chip 3 is supported by the support body including the p-side metal pillar 23, the n-side metal

pillar 24, and the resin layer 25, the substrate 5 is removed by a laser lift-off method, for example.

[0077] A laser beam is directed toward the first semiconductor layer 11 from the rear face side of the substrate 5. The laser beam has a permeability to the substrate 5 and has a wavelength in the absorption region of the first semiconductor layer 11.

[0078] When the laser beam reaches the boundary face between the substrate 5 and the first semiconductor layer 11, the first semiconductor layer 11 near the boundary face absorbs the laser beam energy and is decomposed. For example, the first semiconductor layer 11 of the GaN-based material is decomposed into gallium (Ga) and nitrogen gas. By this decomposition reaction, a minute gap is formed between the substrate 5 and the first semiconductor layer 11, and the substrate 5 and the first semiconductor layer 11 are separated from each other. The laser irradiation is performed plural times for respective predetermined regions over the whole wafer and the substrate 5 is removed.

[0079] Since the semiconductor layer 15 is supported by the support body thicker than the semiconductor layer 15 and a wafer state can be kept even when the substrate 5 is removed. Furthermore, the resin constituting the resin layer 25 and the metal constituting the p-side metal pillar 23 and the n-side metal pillar 24 are soft material in comparison with the semiconductor layer 15 of the GaN-based material. Accordingly, even when a large internal stress generated in the epitaxial growth forming the semiconductor layer 15 on the substrate 5 is released in a single burst at the peeling of the substrate 5, it is possible to avoid the breakage of the chip 3.

[0080] After the removal of the substrate 5, the first face 15a is cleaned and is subjected to frost processing forming unevenness as needed. By forming the minute unevenness on the first face 15a, it is possible to improve a light extraction efficiency. After that, as shown in FIG. 7A, on the first face 15a, the fluorescent body layer 31 is formed.

[0081] The process of forming the fluorescent body layer 31 includes a process of supplying liquid-state transparent resin in which the phosphor particles are dispersed onto the first face 15a by a method of printing, potting, molding, compression molding, or the like and a process of performing thermal curing of the transparent resin.

[0082] After the formation of the fluorescent body layer 31, the fluorescent body layer 31 is cut to be thinned selectively by mechanical cutting work, for example. Therefore, as shown in FIG. 7B, the variation in thickness of the fluorescent body layer 31 is given within the wafer.

[0083] The cut amount of the fluorescent body layer 31, that is, the thickness of the fluorescent body layer 31 is set based on the measurement result of the wavelength of the light obtained on the upper face side of the fluorescent body layer 31 when each of the chips 3a and 3b are caused to emit light in a wafer state.

[0084] After that, the wafer is cut at the position of the groove 6 and divided into pieces of the plurality of the semiconductor light emitting devices 10. As shown in FIG. 7C, the semiconductor light emitting device 10 is divided from the wafer as a unit including one central chip 3a and two peripheral chips 3b arranged symmetrically to each other sandwiching the central chip 3a.

[0085] As described above, the thicknesses of the fluorescent body layers 31 provided on the two peripheral chips 3b are the same as each other and the fluorescent body layers 31 provided on the peripheral chips 3b is thicker than the fluorescent body layer 31 provided on the central chip 3a.

[0086] Alternatively, as shown in FIG. 7D, the fluorescent body layers 31 provided on the peripheral chips 3b may be thinner than the fluorescent body layer 31 provided on the central chip 3a. Also in this structure of FIG. 7D, a uniform color mixing effect and light distribution can be obtained when the semiconductor light emitting device is viewed from the light emitting face side.

[0087] In dicing, since the hard sapphire substrate 5 is already removed, it is not necessary to cut the substrate 5 and it becomes easy to perform the dicing.

[0088] Furthermore, in the groove 6, the semiconductor layer 15 is not formed but the insulating layer 18 of resin is provided. Moreover, in the lower part of the groove 6 in FIG. 7B, the resin layer 25 is provided. Accordingly, in the dicing region, the semiconductor layer 15 is not provided but the resin which is softer than the semiconductor layer 15 is provided. Therefore, it is possible to avoid a damage the semiconductor layer 15 receives during the dicing. In addition, in the dicing region, also the wiring layer or the metal pillar is not provided.

[0089] Each of the processes before the dicing is collectively performed in a wafer state. Accordingly, after the dicing, it is not necessary to form the support body and protect chips by the insulating material, for each of the semiconductor light emitting devices 10, and thus it become possible to reduce production cost significantly. In a state of being divided into pieces, the side faces of the chips 3a and 3b is already covered and protected by the insulating layer 18.

[0090] (Second embodiment)

FIG. 8D is a schematic cross-sectional view of a semiconductor light emitting device of a second embodiment.

[0091] This semiconductor light emitting device, as the first embodiment, also includes, for example, one central chip 3a and two peripheral chips 3b arranged symmetrically to each other sandwiching the central chip 3a. The configurations of the chip and a support body supporting the chip are the same as the configurations in the first embodiment.

[0092] Furthermore, the central chip 3a and the peripheral chips 3b are connected in parallel

to a power supply, and by adjusting power supplied from the power supply to each of the central chip 3a and the peripheral chips 3b, it is possible to adjust a ratio of light emission intensity between the central chip 3a and the peripheral chips 3b.

[0093] The thicknesses of the fluorescent body layers 31 provided on the two peripheral chips 3b are the same as each other. Moreover, the thickness of the fluorescent body layer 31 on the central chip 3a and the thickness of the fluorescent body layers 31 on the peripheral chips 3b are different from each other. In the second embodiment, the fluorescent body layer 31 is not provided on the central chip 3a and the thickness of the fluorescent body layer 31 on the central chip 3a is zero. That is, the expression in which the thickness of the fluorescent body layer 31 is different between the central chip 3a and the peripheral chips 3b includes the presence or absence of the fluorescent body layer 31.

[0094] Also in the second embodiment, by varying the thickness of the fluorescent body layer 31 between the central chip 3a and the peripheral chips 3b and also by adjusting input power between the central chip 3a and the peripheral chips 3b which are connected in parallel, it is possible to adjust the chromaticity of mixed light emitted from the semiconductor light emitting device.

[0095] Moreover, the fluorescent body layers 31 which are arranged symmetrically to each other with respect to the center and which have the same thickness are provided on the peripheral. Accordingly, it is possible to obtain a uniform color mixing effect and light distribution when the semiconductor light emitting device is viewed from the fluorescent body layer 31 side.

[0096] Furthermore, when the thickness of the fluorescent body layer 31 is varied between the central chip 3a and the peripheral chips 3b, the thickness of the fluorescent body layer 31 on the central chip 3a is set to zero, that is, the fluorescent body layer 31 is not provided on the central chip 3a. Accordingly, the usage of the fluorescent body layer 31 can be reduced and cost reduction is realized.

[0097] Here, from the central chip 3a, light is emitted also in a direction oblique to the first face 15a and the light can travel in the fluorescent body layers 31 on the peripheral chips 3b. Accordingly, the fluorescent body layer 31 on the peripheral chip 3b can perform wavelength conversion also by excitation of the light emitted from the central chip 3a.

[0098] Next, with reference to FIGS. 8A to 8D, a manufacturing method of the semiconductor light emitting device of the second embodiment will be explained.

[0099] The process up to the removal of the substrate 5 is carried out as in the first embodiment.

[0100] After a substrate 5 has been removed, as shown in 8A, a sacrifice layer 41 is formed on the chip 3a selected from among the chips within the wafer.

[0101] When the sacrifice layer 41 is a resin having photosensitivity, after the sacrifice layer 41 has been formed over the whole face of the wafer, the sacrifice layer 41 is exposed selectively through the use of a photo-mask. After the exposure, the sacrifice layer 41 is removed selectively by development.

[0102] Alternatively, after an inorganic sacrifice layer 41 has been formed over the whole face of the wafer, resist is formed on the sacrifice layer 41. Then, by exposure and development of the resist, the resist is patterned. Then, through the use of the patterned resist as a mask, the sacrifice layer 41 is etched selectively.

[0103] For example, the sacrifice layer 41 is formed on the plurality of chips within the wafer every other chip in the one-dimensional alignment direction.

[0104] After the formation of the sacrifice layer 41, the fluorescent body layer 31 is formed on the wafer. As shown in 8B, the fluorescent body layer 31 fills a space between the sacrifice layer 41 and the sacrifice layer 41 and is formed on the chip 3b on which the sacrifice layer 41 is not formed.

[0105] By forming the sacrifice layer 41 so as to cause the cross section thereof to have a trapezoidal shape, the upper end opening of a space between the sacrifice layer 41 and the sacrifice layer 41 becomes wider than the bottom part and embedding properties of the fluorescent body layer 31 are improved.

[0106] After that, the fluorescent body layer 31 on the sacrifice layer 41 is removed by cutting work, for example, and the upper face of the sacrifice layer 41 is exposed. Then, as shown in FIG. 8C, the sacrifice layer 41 is removed selectively. The fluorescent body layer 31 is left on the chip 3b.

[0107] Then, as in the first embodiment, the wafer is cut at the position of a groove 6 and divided into pieces of the semiconductor light emitting devices. As shown in FIG. 8D, the semiconductor light emitting device is divided from the wafer in a unit including one central chip 3a and two peripheral chips 3b arranged symmetrically to each other sandwiching the central chip 3a.

[0108] As described above, the thicknesses of the fluorescent body layers 31 provided on the two peripheral chips 3b are the same as each other and the fluorescent body layer 31 is not provided on the central chip 3a.

[0109] Alternatively, as shown in FIG. 8E, the semiconductor light emitting device may have a structure in which the fluorescent body layer 31 is provided on the central chip 3a and the fluorescent body layers 31 are not provided on the peripheral chips 3b. Also in this structure of FIG. 8E, since the thickness of the fluorescent body layer 31 on the periphery is varied (zero thickness) symmetrically with respect to the center, a uniform color mixing effect and light distribution can be obtained when the semiconductor light emitting device is viewed from the light emitting face side.

[0110] By the process using the sacrifice layer 41, it is possible easily to form the flu-

orescent body layer 31 selectively in a wafer level.

[0111] (Third embodiment)

FIG. 9C is a schematic cross-sectional view of a semiconductor light emitting device of a third embodiment.

[0112] This semiconductor light emitting device, as the first embodiment, also includes one central chip 3a and two peripheral chips 3b arranged symmetrically to each other sandwiching the central chip 3a, for example. The configurations of the chip and a support body supporting the chip are the same as the configurations in the first embodiment.

[0113] Furthermore, the central chip 3a and the peripheral chips 3b are connected in parallel to a power supply, and, by adjusting power supplied from the power supply to each of the central chip 3a and the peripheral chips 3b, it is possible to adjust a ratio of light emission intensity between the central chip 3a and the peripheral chips 3b.

[0114] The thicknesses of the fluorescent body layers 31 provided on the two peripheral chips are the same as each other. Furthermore, the thickness of the fluorescent body layer 31 on the central chip 3a and the thickness of the fluorescent body layer 31 on the peripheral chips 3b are different from each other. In the third embodiment, the fluorescent body layer 31 is not provided on the central chip 3a and the thickness of the fluorescent body layer 31 on the central chip 3a is zero. Then, on the central chip 3a, a transparent resin layer 42 which is transparent to light emitted from the light emission layer is provided. By the transparent resin layer 42, the first face 15a of the central chip 3a can be protected.

[0115] Also in the third embodiment, by varying the thickness of the fluorescent body layer 31 between the central chip 3a and the peripheral chips 3b and also by adjusting input power for each of the central chip 3a and the peripheral chips 3b which are connected in parallel, it is possible to adjust the chromaticity of mixed light emitted from the semiconductor light emitting device.

[0116] Moreover, the fluorescent body layers 31 which are arranged symmetrically to each other with respect to the center and have the same thickness are provided on the peripheral. Accordingly, it is possible to obtain a uniform color mixing effect and light distribution when the semiconductor light emitting device is viewed from the fluorescent body layer 31 side.

[0117] Furthermore, when the thickness of the fluorescent body layer 31 is varied between the central chip 3a and the peripheral chip 3b, the thickness of the fluorescent body layer 31 on the central chip 3a is set to zero, that is, the fluorescent body layer 31 is not provided on the central chip 3a. Accordingly, the usage of the fluorescent body layer 31 can be reduced and cost reduction is realized.

[0118] Next, with reference to FIGS. 9A to 9C, a manufacturing method of the semi-

conductor light emitting device of the third embodiment will be explained.

[0119] The process up to the removal of the substrate 5 is carried out as in the first embodiment.

[0120] After the substrate 5 has been removed, as shown in 9A, the transparent resin layer 42 is formed on the chip 3a selected among the chips within the wafer.

[0121] When the transparent resin layer 42 is a resin having photosensitivity, after the transparent resin layer 42 has been formed over the whole face of the wafer, the transparent resin layer 42 is subjected to selective exposure by the use of a photomask. After the exposure, the transparent resin layer 42 is removed selectively by development.

[0122] Alternatively, after the transparent resin layer 42 has been formed over the whole face of the wafer, resist is formed on the transparent resin layer 42. Then, by exposure and development of the resist, the resist is patterned. After that, by the use of the patterned resist as a mask, the transparent resin layer 42 is etched selectively.

[0123] For example, the transparent resin layer 42 is formed on the plurality of chips within the wafer every other chip in the one-dimensional alignment direction.

[0124] After the formation of the transparent resin layer 42, the fluorescent body layer 31 is formed on the wafer. As shown in 9B, the fluorescent body layer 31 fills a space between the transparent resin layer 42 and the transparent resin layer 42 and is formed on the chip 3b on which the transparent resin layer 42 is not formed.

[0125] After that, as in the first embodiment, the wafer is cut at the position of a groove 6 and divided into pieces of the semiconductor light emitting devices. As shown in FIG. 9C, the semiconductor light emitting device is divided from the wafer in a unit including one central chip 3a and two peripheral chips 3b arranged symmetrically to each other sandwiching the central chip 3a.

[0126] As described above, the thicknesses of the fluorescent body layers 31 provided on the two peripheral chips 3b are the same as each other and on the central chip 3a, the fluorescent body layer 31 is not provided but the transparent resin layer 42 is provided.

[0127] Alternatively, as shown in FIG. 9D, the semiconductor light emitting device may have a structure in which the fluorescent body layer 31 is provided on the central chip 3a and the transparent resin layers 42 are provided on the peripheral chips 3b instead of the fluorescent body layers 31. Also in this structure of FIG. 9D, since the thickness of the fluorescent body layer 31 on the periphery is varied (zero thickness) symmetrically with respect to the center, a uniform color mixing effect and light distribution can be obtained when the semiconductor light emitting device is viewed from the light emitting face side.

[0128] (Fourth embodiment)

FIG. 11D is a schematic cross-sectional view of a semiconductor light emitting

device of a fourth embodiment.

[0129] This semiconductor light emitting device also includes one central chip 3a and two peripheral chips 3b and 3c arranged symmetrically to each other sandwiching the central chip 3a, for example. The configurations of the chip and a support body supporting the chip are the same as the configurations in the first embodiment.

[0130] Of the two peripheral chips 3b and 3c, a first fluorescent body layer 32 is provided on one peripheral chip 3b and a second fluorescent body layer 33 is provided on the other chip 3c.

[0131] The kinds of the first fluorescent body layer 32 and the second fluorescent body layer 33 are different from each other. The first fluorescent body layer 32 has a structure in which green phosphor particles, emitting green light when receiving excitation light from the chip, are dispersed in transparent resin. The second fluorescent body layer 33 has a structure in which red phosphor particles, emitting red light when receiving excitation light form the chip, are dispersed in transparent resin.

[0132] The thickness of the first fluorescent body layer 32 provided on the peripheral chip 3b and the thickness of the second fluorescent body layer 33 provided on the peripheral chip 3c are the same as each other. A fluorescent body layer is not provided on the central chip 3a and the thickness of the fluorescent body layer on the central chip 3a is zero.

[0133] The central chip 3a, the peripheral chip 3b, and the peripheral chip 3c have the same configuration and emit blue light. Consequently, according to the semiconductor light emitting device of the fourth embodiment, the blue light from each of the chips, the green light from the first fluorescent body layer 32, and the red light from the second fluorescent body layer 33 are mixed, and white color or light bulb color are obtained.

[0134] Furthermore, the central chip 3a, the peripheral chip 3b, and the peripheral chip 3c are connected in parallel to a power supply, and, by adjusting power supplied from the power supply to each of the chips, it is possible to adjust ratios of emission intensity among the chips, and it is possible to adjust the chromaticity of the mixed light emitted from the semiconductor light emitting device.

[0135] Here, from the central chip 3a, light is emitted also in a direction oblique to the first face 15a and the light can travel in the first fluorescent body layer 32 on the peripheral chip 3b and in the second fluorescent body layer 33 on the peripheral chip 3c. Accordingly, the first fluorescent body layer 32 and the second fluorescent body layer 33 can perform wavelength conversion also by excitation of the light emitted from the central chip 3a.

[0136] FIG. 16A shows a CIExy chromaticity diagram. The coordinates C show the chromaticity of the blue light emitted from the central chip 3a on which a fluorescent body layer is not provided. The coordinates D show the chromaticity of mixed light of the

emission light of the peripheral chip 3b and the emission light of the first fluorescent body layer 32 thereon. The coordinates E show the chromaticity of mixed light of the emission light of the peripheral chip 3c and the emission light of the second fluorescent body layer 33 thereon.

[0137] By adjusting input power for each of the central chip 3a, the peripheral chip 3b, and the peripheral chip 3c, it is possible to realize a chromaticity within a triangular range having the coordinates C, D, and E as apexes.

[0138] Next, with reference to FIGS. 10A to 11D, a manufacturing method of the semiconductor light emitting device of the fourth embodiment will be explained.

[0139] The process up to the removal of the substrate 5 is carried out as in the first embodiment.

[0140] After a substrate 5 has been removed, as shown in 10A, a first sacrifice layer 43 is formed on the chip selected among the chips within the wafer. In a partial cross section of the wafer shown in FIG 10A, the first sacrifice layer 43 is formed on the two chips 3a and 3c neighboring each other.

[0141] When the first sacrifice layer 43 is a resin having photosensitivity, after the first sacrifice layer 43 has been formed over the whole face of the wafer, the first sacrifice layer 43 is subjected to selective exposure through the use of a photo-mask. After the exposure, the first sacrifice layer 43 is removed selectively by development.

[0142] Alternatively, after an inorganic first sacrifice layer 43 has been formed over the whole face of the wafer, resist is formed on the first sacrifice layer 43. Then, by exposure and development of the resist, the resist is patterned. After that, through the use of the patterned resist as a mask, the first sacrifice layer 43 is etched selectively.

[0143] After the formation of the first sacrifice layer 43, as shown in FIG. 10B, the first fluorescent body layer 32 is formed on the wafer. The first fluorescent body layer 32 is formed on the chip 3b on which the first sacrifice layer 43 is not formed.

[0144] After that, the first fluorescent body layer 32 on the first sacrifice layer 43 is removed by cutting work, for example, and, as shown in FIG. 10C, the upper face of the first sacrifice layer 43 is exposed. Then, as shown in FIG. 10D, the first sacrifice layer 43 is removed selectively. The first fluorescent body layer 32 is left on the chip 3b.

[0145] Next, on one chip 3a of two neighboring chips 3a and 3c on which the first sacrifice layers 43 are removed, as shown in FIG. 10E, a second sacrifice layer 44 is formed. The second sacrifice layer 44 can be formed by the same method as the first sacrifice layer 43.

[0146] After the formation of the second sacrifice layer 44, as shown in FIG. 11A, the second fluorescent body layer 33 is formed on the wafer. The second fluorescent body layer 33 is formed on the chip 3c on which the first fluorescent body layer 32 is not formed or the second sacrifice layer 44 is not formed.

[0147] After that, the second fluorescent body layers 33 on the first fluorescent body layer 32 and the second sacrifice layer 44 are removed by cutting work, for example, and as shown in FIG. 11B, the upper face of the first fluorescent body layer 32 and the upper face of the second sacrifice layer 44 are exposed.

[0148] Then, as shown in FIG. 11C, the second sacrifice layer 44 is removed selectively. The first fluorescent body layer 32 is left on the chip 3b, and the second fluorescent body layer 33 is left on the chip 3c.

[0149] After that, as in the first embodiment, the wafer is cut at the position of a groove 6 and divided into pieces of the semiconductor light emitting devices. As shown in FIG. 11D, the semiconductor light emitting device is divided from the wafer in a unit including one central chip 3a and two peripheral chips 3b and 3c aligned symmetrically to each other sandwiching the central chip 3a.

[0150] By the process using the first sacrifice layer 43 and the second sacrifice layer 44, it is possible easily to form the structure including, in one package, the central chip 3a on which a fluorescent body layer is not provided, the peripheral chip 3b on which the first fluorescent body layer 32 is provided, and the peripheral chip 3c on which the second fluorescent body layer 33 of a kind different from the first fluorescent body layer 32 is provided, in a wafer level.

[0151] (Fifth embodiment)

FIG. 12C is a schematic cross-sectional view of a semiconductor light emitting device of a fifth embodiment.

[0152] This semiconductor light emitting device also includes one central chip 3a and two peripheral chips 3b and 3c arranged symmetrically to each other sandwiching the central chip 3a, for example. The configurations of the chip and a support body supporting the chip are the same as the configurations in the first embodiment.

[0153] Of the two peripheral chips 3b and 3c, the first fluorescent body layer 32 is provided on one peripheral chip 3b and the second fluorescent body layer 33 is provided on the other chip 3c. On the central chip 3a, a third fluorescent body layer 34 is provided.

[0154] The kinds of the first fluorescent body layer 32, the second fluorescent body layer 33, and the third fluorescent body layer 34 are different from one another. The first fluorescent body layer 32 has a structure in which green phosphor particles emitting green light when receiving excitation light from the chip, are dispersed in transparent resin. The second fluorescent body layer 33 has a structure in which red phosphor particles emitting red light when receiving excitation light form the chip, are dispersed in transparent resin. The third fluorescent body layer 34 has a structure in which blue phosphor particles emitting blue light when receiving excitation light from the chip, are dispersed in transparent resin.

[0155] The central chip 3a, the peripheral chip 3b, and the peripheral chip 3c have the same

configuration and emit ultraviolet light or near-ultraviolet light. The ultraviolet light or near-ultraviolet light emitted from the chips 3a and 3b is not a component directly constituting white light.

[0156] That is, according to the semiconductor light emitting device of the fifth embodiment, the green light from the first fluorescent body layer 32, the red light from the second fluorescent body layer 33 and the blue light from the third fluorescent body layer 34 are mixed, and white color or light bulb color is obtained.

[0157] Furthermore, the central chip 3a, the peripheral chip 3b, and the peripheral chip 3c are connected in parallel to a power supply, and, by adjusting power supplied from the power supply to each of the chips, it is possible to adjust ratios of light emission intensity among the chips, and it is possible to adjust the chromaticity of the mixed light emitted from the semiconductor light emitting device.

[0158] FIG. 16B shows a CIExy chromaticity diagram. The coordinates H show the chromaticity of the emission light (blue light) of the third single fluorescent body layer 34. The coordinates I show the chromaticity of the emission light (green light) of the first single fluorescent body layer 32. The coordinates J show the chromaticity of the emission light (red light) of the second single fluorescent body layer 33.

[0159] By adjusting input power for the central chip 3a, the peripheral chip 3b, and the peripheral chip 3c, it is possible to realize a chromaticity within a triangular range having the coordinates H, I, and J as apexes.

[0160] Next, with reference to FIGS. 12A to 12C, a manufacturing method of the semiconductor light emitting device of the fifth embodiment will be explained.

[0161] The process up to the removal of the second sacrifice layer 44 shown in FIG. 11C is carried out as in the fourth embodiment.

[0162] After the second sacrifice layer 44 has been removed, as shown in FIG. 12A, the third fluorescent body layer 34 is formed on the wafer. The third fluorescent body layer 34 is formed on the chip 3a on which the second sacrifice layer 44 is removed.

[0163] After that, the third fluorescent body layers 34 on the first fluorescent body layer 32 and the second fluorescent body layer 33 are removed by cutting work, for example, and as shown in FIG. 12B, the upper face of the first fluorescent body layer 32 and the upper face of the second fluorescent body layer 33 are exposed.

[0164] Then, the wafer is cut at the position of a groove 6 and divided into pieces of the semiconductor light emitting devices. As shown in FIG. 12C, the semiconductor light emitting device is divided from the wafer in a unit including one central chip 3a and two peripheral chips 3b and 3c arranged symmetrically to each other sandwiching the central chip 3a.

[0165] According to the fifth embodiment, by the process using the first sacrifice layer 43 and the second sacrifice layer 44, it is possible easily to form the structure including, in

one package, the peripheral chip 3b on which the first fluorescent body layer 32 is provided, the peripheral chip 3c on which the second fluorescent body layer 33 of a kind different from the first fluorescent body layer 32 is provided, and the central chip 3a on which the third fluorescent body layer 34 of a kind different from the first fluorescent body layer 32 and the second fluorescent body layer 33 is provided, in a wafer level.

[0166] (Sixth embodiment)

FIG. 13C is a schematic cross-sectional view of a semiconductor light emitting device of a sixth embodiment.

[0167] This semiconductor light emitting device is different from the semiconductor light emitting device of the fourth embodiment which is shown in FIG. 11D in the point that optical filter films 51 are formed on the upper face of the first fluorescent body layer 32 and the upper face of the second fluorescent body layers 33.

[0168] The optical filter film 51 is a dielectric multilayer film, for example, and has a reflectivity for the blue light emitted from the chips 3a and 3b. The optical filter film 51 has a permeability to the green light emitted from the first fluorescent body layer 32 and the red light emitted from the second fluorescent body layer 33a.

[0169] FIG. 16A shows a CIExy chromaticity diagram. The coordinates C show the chromaticity of the blue light emitted from the central chip 3a on which a fluorescent body layer is not provided. The coordinates F show the chromaticity of the emission light (green light) from the first fluorescent body layer (green fluorescent body layer) 32 on the upper face of which the optical filter film 51 is provided. The coordinates G show the chromaticity of the emission light (red light) from the second fluorescent body layer (red fluorescent body layer) 33 on the upper face of which the optical filter film 51 is provided.

[0170] According to the sixth embodiment, by adjusting input power for the central chip 3a, the peripheral chip 3b, and the peripheral chip 3c, it is possible to realize a chromaticity within a triangular range having the coordinates C, F, and G as apexes.

[0171] In the sixth embodiment, on the upper face of the green fluorescent body layer and the upper face of the red fluorescent body layer, the optical filter film 51 is provided reflecting the blue light from the chip. Accordingly, it is possible to expand the chromaticity adjustable range in the sixth embodiment more than in the fourth embodiment which can realize a chromaticity within the rectangular range having the coordinates C, D, and E as apexes.

[0172] Next, with reference to FIGS. 13A to 13C, a manufacturing method of the semiconductor light emitting device of the sixth embodiment will be explained.

[0173] The process up to the formation of the second fluorescent body layer 33 shown in FIG. 11B is carried out as in the fourth embodiment.

[0174] Then, after the second fluorescent body layer 33 has been formed, as shown in FIG 13A, the optical filter film 51 is formed on the upper face of the first fluorescent body layer 32, the upper face of the second sacrifice layer 44, and the upper face of the second fluorescent body layer 33 over the whole face of the wafer.

[0175] Next, as shown in FIG. 13B, the second sacrifice layer 44 is removed selectively. The optical filter film 51 on the upper face of the second sacrifice layer 44 is removed by lift-off together with the second sacrifice layer 44.

[0176] After that, the wafer is cut at the position of a groove 6 and divided into pieces of the semiconductor light emitting devices. As shown in FIG. 13C, the semiconductor light emitting device is divided from the wafer in a unit including one central chip 3a and two peripheral chips 3b and 3c arranged symmetrically to each other sandwiching the central chip 3a.

[0177] By the process using the first sacrifice layer 43 and the second sacrifice layer 44, it is possible easily to form the structure including, in one package, the central chip 3a on which a fluorescent body layer is not provided, the peripheral chip 3b on which the optical filter film 51 and the first fluorescent body layer 32 are provided, and the peripheral chip 3c on which the optical filter film 51 and the second fluorescent body layer 33 are provided, in a wafer level.

[0178] (Seventh embodiment)

FIG. 14B is a schematic cross-sectional view of a semiconductor light emitting device of a seventh embodiment.

[0179] This semiconductor light emitting device is different from the semiconductor light emitting device of the fourth embodiment which is shown in FIG. 11D in that a transparent resin layer 52 is provided on the central chip 3a. The transparent resin layer 52 is transparent to the light emitted from the chips 3a and 3b. By the transparent resin layer 52, the first face 15a of the central chip 3a can be protected.

[0180] Next, with reference to FIGS. 14A to 14B, a manufacturing method of the semiconductor light emitting device of the seventh embodiment will be explained.

[0181] The process up to the removal of second sacrifice layer 44 shown in FIG. 11C is carried out as in the fourth embodiment.

[0182] Then, on the chip 3a on which the second sacrifice layer 44 is removed, as shown in FIG. 14A, the transparent resin layer 52 is formed.

[0183] Then, the wafer is cut at the position of a groove 6 and divided into pieces of the semiconductor light emitting devices. As shown in FIG. 14B, the semiconductor light emitting device is divided from the wafer in a unit including one central chip 3a and two peripheral chips 3b and 3c arranged symmetrically to each other sandwiching the central chip 3a.

[0184] According to the seventh embodiment, by the process using the first sacrifice layer

43 and the second sacrifice layer 44, it is possible to easily form the structure at a wafer level, including, in one package, the peripheral chip 3b on which the first fluorescent body layer 32 is provided, the peripheral chip 3c on which the second fluorescent body layer 33 of a kind different from the first fluorescent body layer 32, and the central chip 3a on which the transparent resin layer 52 is provided.

[0185] In each of the above described embodiments, after removing the substrate to expose the first face 15 and before forming the fluorescent body layer, by forming an inorganic film such as a silicon nitride film over the whole face, the protection of the first face 15 and the improvement of the light extraction efficiency can be realized.

[0186] As the above described fluorescent body layer, a red fluorescent body layer, yellow fluorescent body layer, a green fluorescent body layer, or a blue fluorescent body layer to be illustrated below, can be used.

[0187] The red fluorescent body layer can contain, for example, a nitride-based fluorescent body $CaAlSiN_3$:Eu or a SiAlON-based fluorescent body.

[0188] When the SiAlON-based fluorescent body is used, in particular

$(M_{1-x}, R_x)_{a1}AlSi_{b1}O_{c1}N_{d1}$ .... composition formula (1)

(Here, M is at least one kind of metal element excluding Si and Al, and in particular, at least either one of Ca and Sr is desirable. R is a light emission center element and in particular, Eu is desirable. x, a1, b1, c1, and d1 satisfy the following relationship. x is larger than 0 and 1 or less, a1 is larger than 0.6 and less than 0.95, b1 is larger than 2 and less than 3.9, c1 is larger than 0.25 and less than 0.45, and d1 is larger than 4 and less than 5.7) can be used.

[0189] By using the SiAlON-based fluorescent body expressed by composition formula (1), it is possible to improve the temperature characteristics of the wavelength conversion efficiency and further improve the efficiency in a large current density region.

[0190] The yellow fluorescent body layer can contain, for example, a silicate-based fluorescent body $(Sr, Ca, Ba)_2SiO_4$:Eu.

[0191] The green fluorescent body layer can contain, for example, a halophosphoric acid-based fluorescent body $(Ba, Ca, Mg)_{10}(PO_4)_6Cl_2$:Eu or a SiAlON-based fluorescent body.

[0192] When the SiAlON-based fluorescent body is used, in particular,

$(M_{1-x}, R_x)_{a2}AlSi_{b2}O_{c2}N_{d2}$ .... composition formula (2)

(Here, M is at least one kind of metal element excluding Si and Al, and in particular, at least either one of Ca and Sr is desirable. R is a light emission center element and in particular, Eu is desirable. x, a2, b2, c2, and d2 satisfy the following relationship. x is larger than 0 and 1 or less, a2 is larger than 0.93 and less than 1.3, b2 is larger than 4.0 and less than 5.8, c2 is larger than 0.6 and less than 1, and d2 is larger than 6 and less than 11) can be used.

[0193] By using the SiAlON-based fluorescent body represented by composition formula (2), it is possible to improve the temperature characteristics of the wavelength conversion efficiency and further improve the efficiency in a large current density region.

[0194] The blue fluorescent body layer can contain, for example, an oxide-based fluorescent body $BaMgAl_{10}O_{17}$:Eu.

[0195] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the invention.

Claims

[Claim 1] A semiconductor light emitting device, comprising:
not less than three chips, each of the chips including a semiconductor layer having a first face, a second face formed on a side opposite to the first face, and a light emitting layer, a p-side electrode provided on the second face in a region having the light emitting layer, and an n-side electrode provided on the second face in a region without having the light emitting layer; and
fluorescent body layers of a same kind provided on the first faces of the chips,
the chips including:
a central chip centrally positioned in a plan view, and
at least two peripheral chips arranged symmetrically to each other sandwiching the central chip in the plan view,
a thickness of the fluorescent body layer on the first face being same among the peripheral chips, and
the fluorescent body layer on the first face of the central chip and the fluorescent body layers on the first faces of the peripheral chips having thicknesses different from each other.

[Claim 2] The device according to claim 1, further comprising:
a first insulating layer which is provided on the second face side and which has a first via leading to the p-side electrode, a second via leading to the n-side electrode, and a wiring face formed on a side opposite to the first face,
a p-side wiring part which is provided on the wiring face on the first insulating layer and which is electrically connected to the p-side electrode through the first via, and
an n-side wiring part which is provided on the wiring face and which is electrically connected to the n-side electrode through the second via.

[Claim 3] The device according to claim 2, wherein the first insulating layer covers a side face continuing from the first face of the chip.

[Claim 4] The device according to claim 2, further comprising a second insulating layer provided between the p-side wiring part and the n-side wiring part.

[Claim 5] The device according to claim 4, wherein the second insulating layer covers a periphery of the p-side wiring part and a periphery of the n-side wiring part.

[Claim 6] The device according to claim 2, wherein
the p-side wiring part has
a p-side wiring layer provided within the first via and on the wiring face and
a p-side metal pillar which is provided on the p-side wiring layer and has a thickness larger than the thickness of the p-side wiring layer, and
the n-side wiring part has
an n-side wiring layer provided within the second via and on the wiring face and
an n-side metal pillar which is provided on the n-side wiring layer and has a thickness larger than the thickness of the n-side wiring layer.

[Claim 7] A manufacturing method of a semiconductor light emitting device, comprising:
forming a sacrifice layer on a first face of a selected chip in a wafer having a plurality of chips each including a semiconductor layer having the first face, a second face formed on a side opposite thereto, and a light emitting layer, a p-side electrode provided on the second face in a region having the light emitting layer, and an n-side electrode provided on the second face in a region which does not have the light emitting layer;
forming a fluorescent body layer on the first face of the chip on which the sacrifice layer is not formed; and
removing the sacrifice layer and selectively leaving the fluorescent body layer on the wafer.

[Claim 8] The method according to claim 7, wherein the sacrifice layers are formed on the plurality of chips every other chip in a one-dimensional alignment direction.

[Claim 9] The method according to claim 8, wherein a semiconductor light emitting device is divided at a wafer level, from the wafer in a unit including the chip on which the sacrifice layer is removed and the fluorescent body layer is not formed on the first face, and the two chips on each of which the fluorescent body layer is formed on the first face, the two chips being arranged symmetrically to each other sandwiching the chip on which the fluorescent body layer is not formed.

[Claim 10] The method according to claim 8, wherein
a semiconductor light emitting device is divided from the wafer in a unit including the a chip on which the fluorescent body layer is formed on the first face, and the two chips on each of which the sacrifice layer

is removed and the fluorescent body layer is not formed on the first face, the two chips being arranged symmetrically to each other sandwiching the chip on which the fluorescent body layer is formed.

[Claim 11] The method according to claim 7, wherein
the forming the fluorescent body layer includes forming a first fluorescent body layer and forming a second fluorescent body layer of a kind different from the first fluorescent body layer,
the forming the sacrifice layer includes forming a first sacrifice layer and forming a second sacrifice layer,
the first sacrifice layer is formed on each of the two chips neighboring each other,
the first sacrifice layer is removed after the first fluorescent body layer has been formed on the first face on which the first sacrifice layer is not formed,
the second sacrifice layer is formed on one chip of the two neighboring chips on each of which the first sacrifice layer is removed, and the second fluorescent body layer is formed on the other chip, and
the second sacrifice layer is removed on the one chip after the second fluorescent body layer has been formed.

[Claim 12] The method according to claim 11, wherein
a semiconductor light emitting device is divided from the wafer in a unit including the chip on which the first fluorescent body layer and the second fluorescent body layer are not formed on the first face, the chip on which the first fluorescent body layer is formed on the first face, and the chip on which the second fluorescent body layer is formed on the first face, the latter two chips being arranged symmetrically to each other sandwiching the chip on which the first fluorescent body layer and the second fluorescent body layer are not formed.

[Claim 13] The method according to claim 11, further comprising, after removing the second sacrifice layer from on the one chip, forming a third fluorescent body layer of a kind different from the first fluorescent body layer and the second fluorescent body layer on the one chip.

[Claim 14] The method according to claim 13, wherein
a semiconductor light emitting device is divided from the wafer in a unit including the chip on which the first fluorescent body layer is formed on the first face, the chip on which the second fluorescent body layer is formed on the first face, and the chip on which the third fluorescent body layer is formed on the first face.

[Claim 15] A manufacturing method of a semiconductor light emitting device, comprising
forming a transparent resin layer transparent to light emitted form a light emitting layer on a first face of a selected chip in a wafer having a plurality of chips each including a semiconductor layer having the first face, a second face formed on a side opposite thereto, and the light emitting layer, a p-side electrode provided on the second face in a region which does not have the light emitting layer, and an n-side electrode provided on the second face in a region which does not have the light emitting layer; and
forming a fluorescent body layer on the first face of the chip on which the transparent resin layer is not formed.

[Claim 16] The method according to claim 15, wherein
the transparent resin layers are formed on the plurality of chips every other chip in a one-dimensional alignment direction.

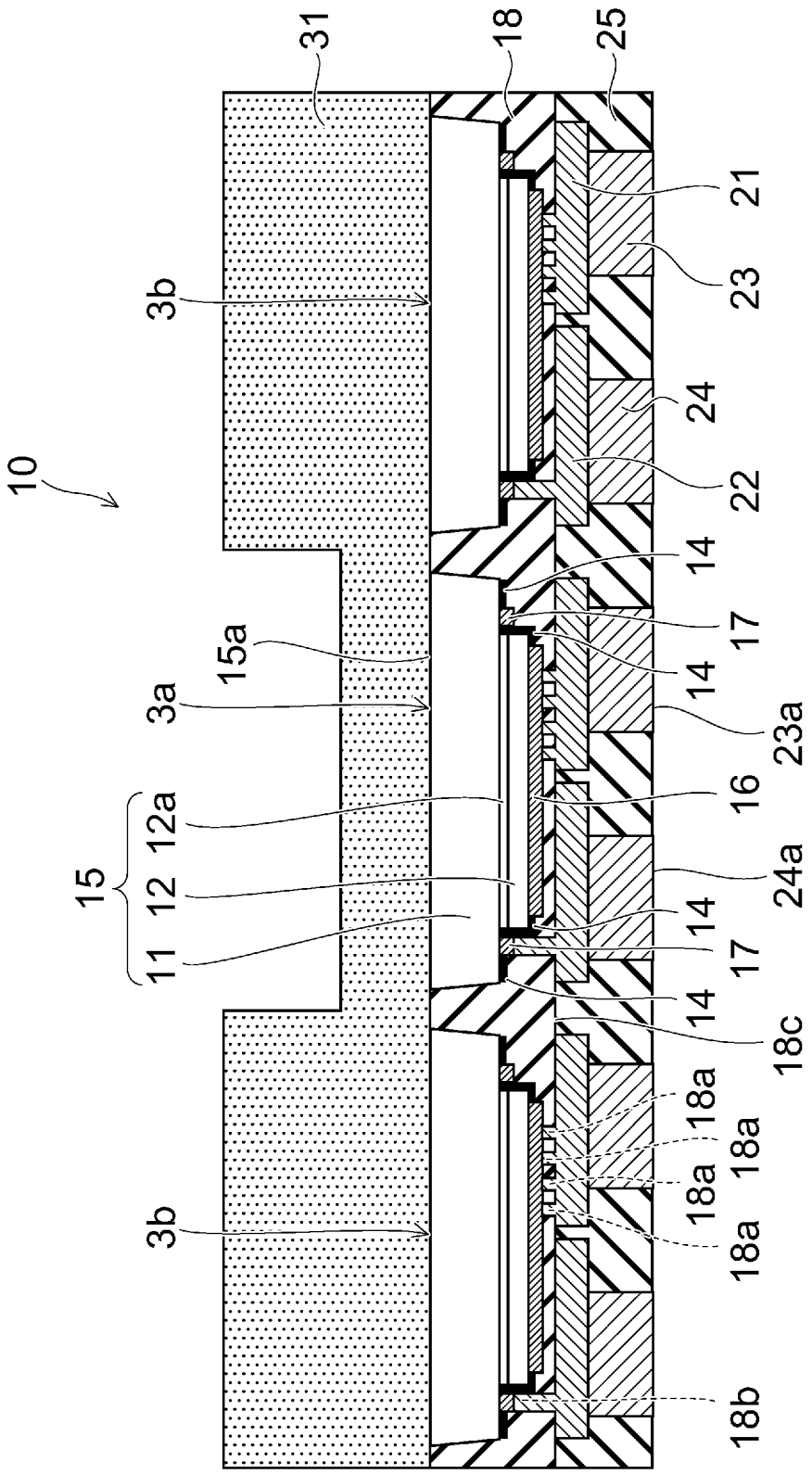
[Claim 17] The method according to claim 16, wherein a semiconductor light emitting device is divided from the wafer in a unit including the chip on which the transparent resin layer is formed on the first face and the two chips on each of which the fluorescent body layer is formed on the first face, the two chips being arranged symmetrically to each other sandwiching the chip on which the transparent resin layer is formed.

[Claim 18] The method according to claim 16, wherein a semiconductor light emitting device is divided from the wafer in a unit including a chip on which the fluorescent body layer is formed on the first face and two chips on each of which the transparent resin layer is formed on the first face, the two chips being arranged symmetrically to each other sandwiching the chip on which the fluorescent body layer is formed.

[Claim 19] The method according to claim 15, furthermore comprising
forming a sacrifice layer on each of the two chips neighboring each other before the fluorescent body layer is formed, wherein
the forming the fluorescent body layer includes forming a first fluorescent body layer and forming a second fluorescent body layer of a kind different from the first fluorescent body layer,
the sacrifice layer is removed after the first fluorescent body layer has been formed on the first face on which the sacrifice layer is not formed,
the transparent layer is formed on one chip of the neighboring two chips on each of which the sacrifice layer is removed and the second fluorescent body layer is formed on the other chip.

[Claim 20] The method according to claim 19, wherein
a semiconductor light emitting device is divided from the wafer in a unit including the chip on which the transparent resin layer is formed on the first face, the chip on which the first fluorescent body layer is formed on the first face, and the chip on which the second fluorescent body layer is formed on the first face, the latter two chips being arranged symmetrically to each other sandwiching the chip on which the transparent resin layer is formed.

[Fig. 1]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18
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21
23
3b
24
22
10
14
17
15a
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3a
23a
16
12a
15
12
24a
14
11
17
14
18c
18a
18a
18a
3b
18a
18b

FIG. 1

[Fig. 2]

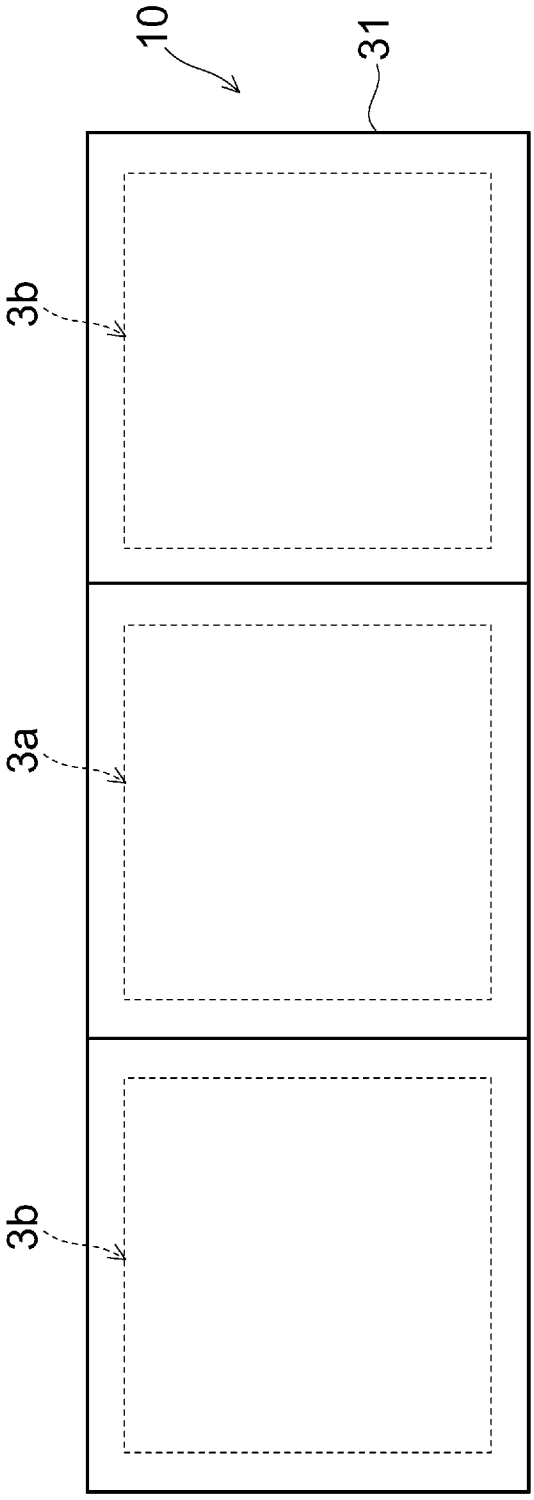


FIG. 2A

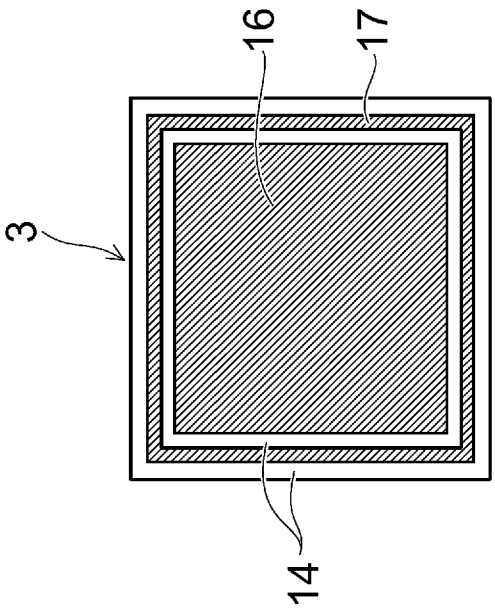


FIG. 2A

[Fig. 3]

FIG. 3A

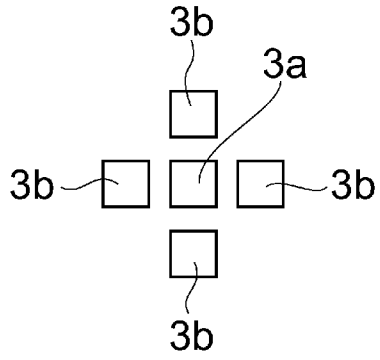


FIG. 3B

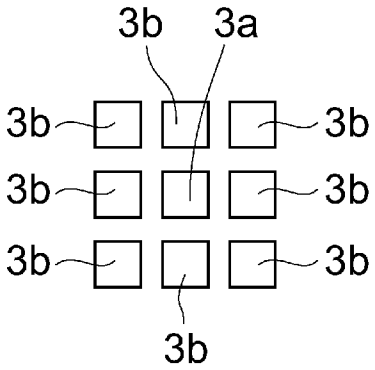
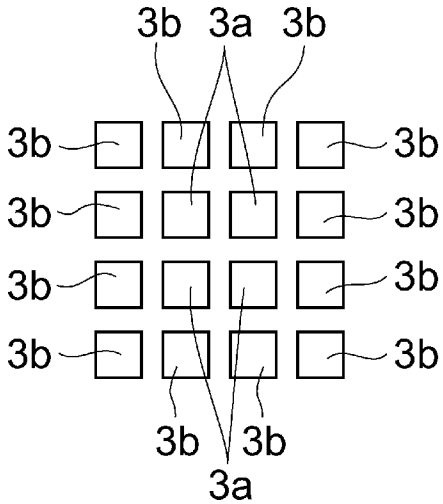


FIG. 3C



[Fig. 4]

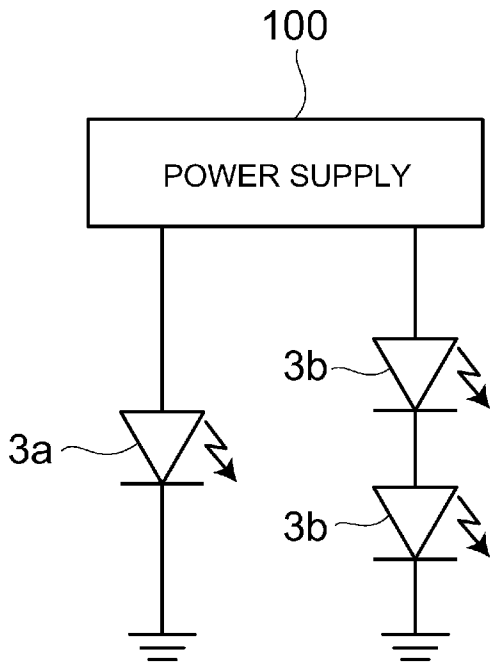


FIG. 4

[Fig. 5]

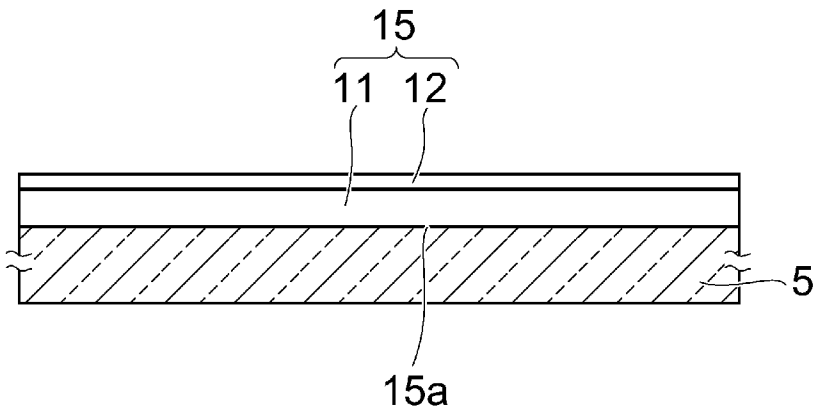


FIG. 5A

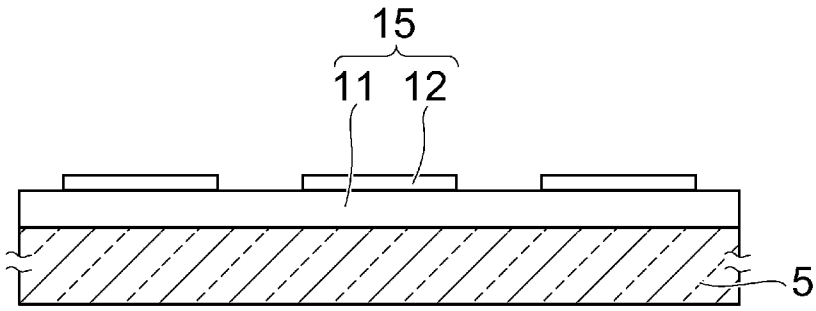


FIG. 5B

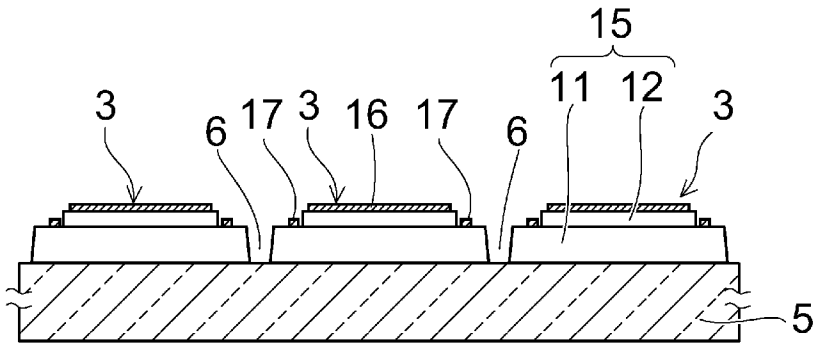


FIG. 5C

[Fig. 6]

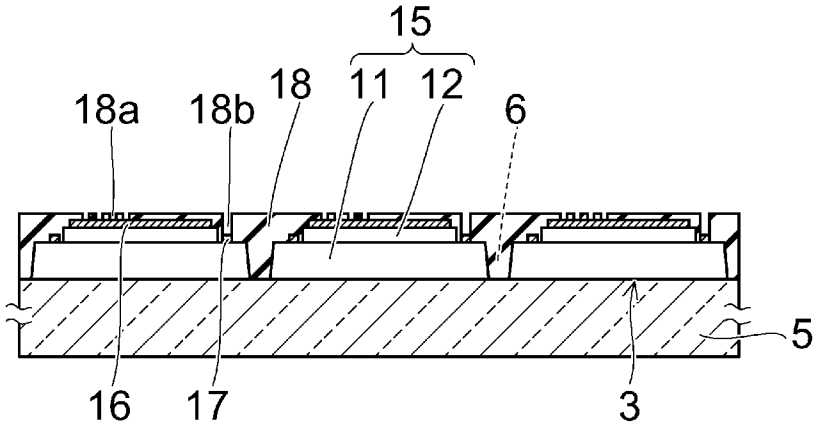


FIG. 6A

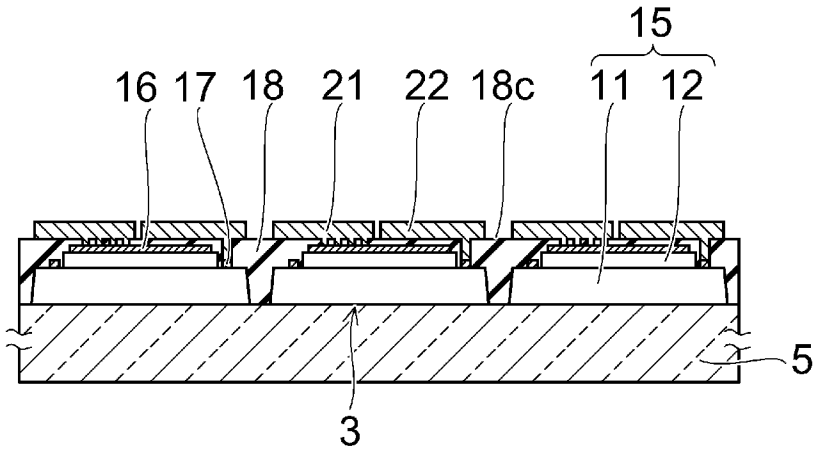


FIG. 6B

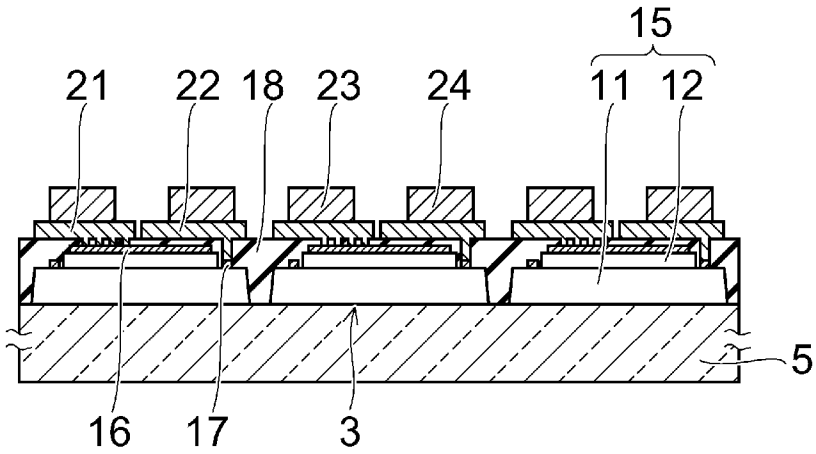


FIG. 6C

[Fig. 7]

FIG. 7A

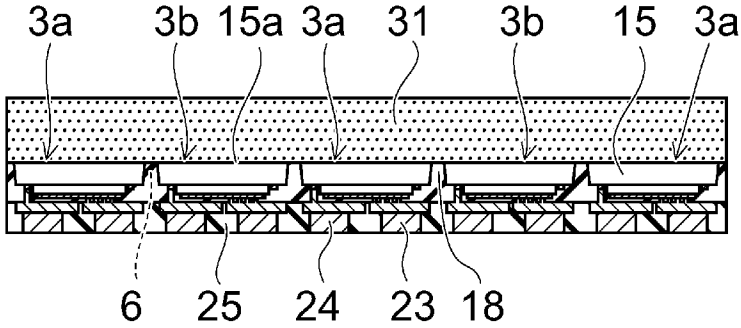


FIG. 7B

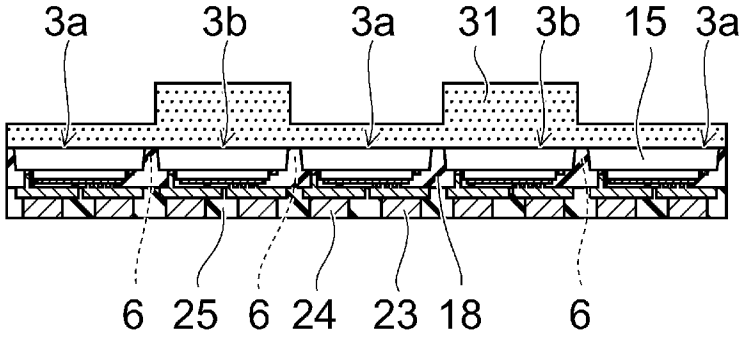


FIG. 7C

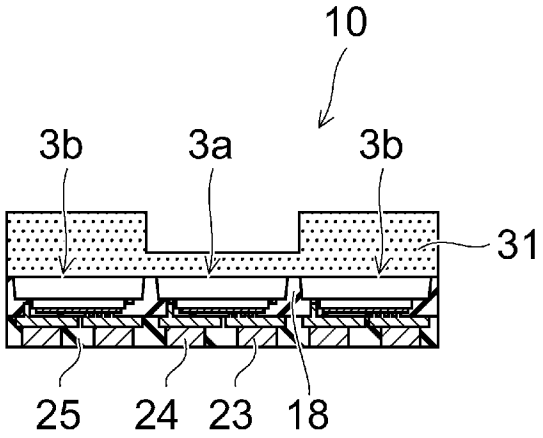
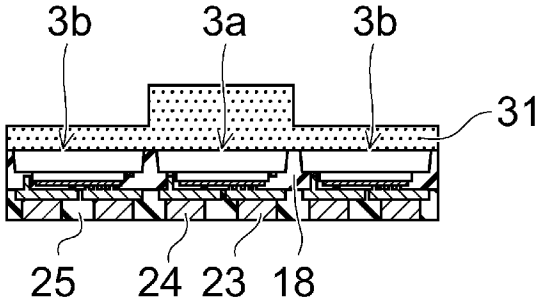


FIG. 7D



[Fig. 8]

FIG. 8A

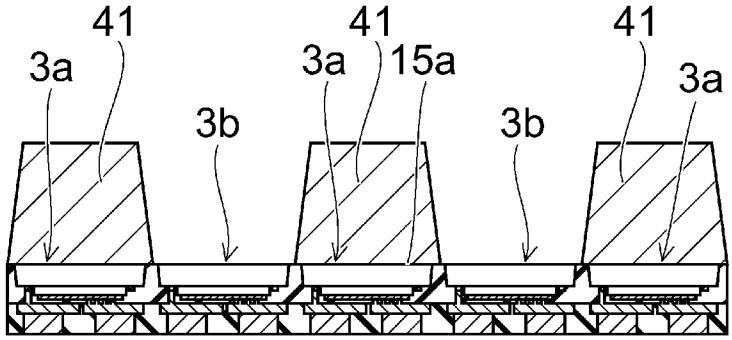


FIG. 8B

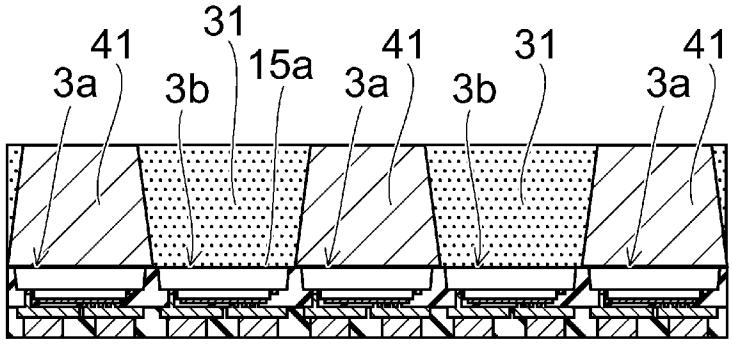


FIG. 8C

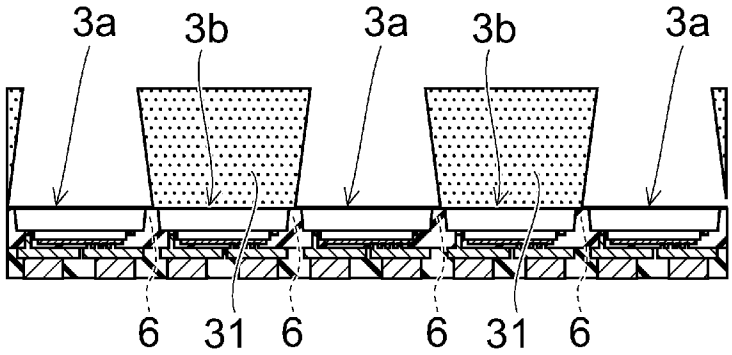


FIG. 8D

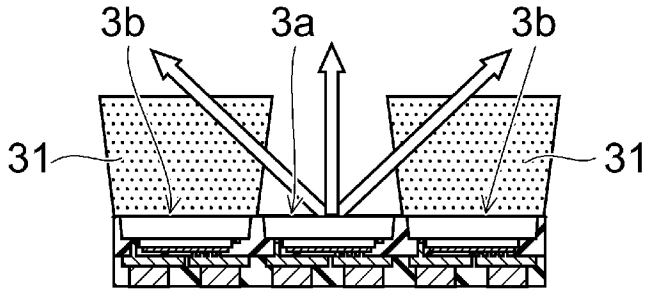
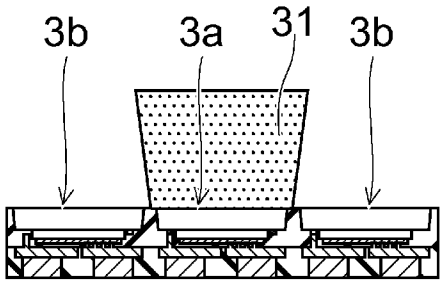


FIG. 8E



[Fig. 9]

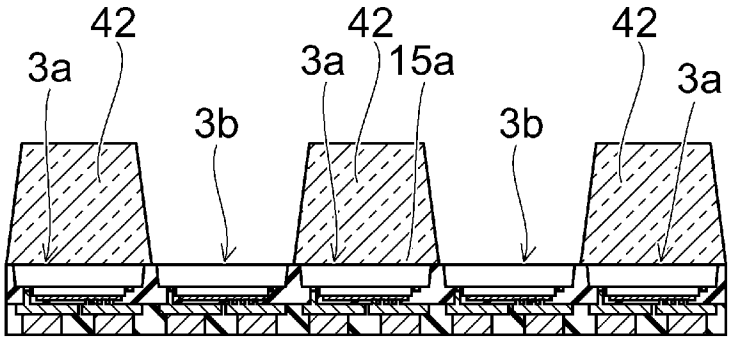


FIG. 9A

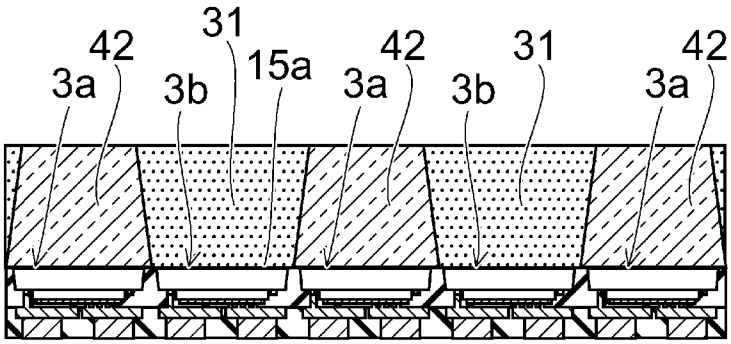


FIG. 9B

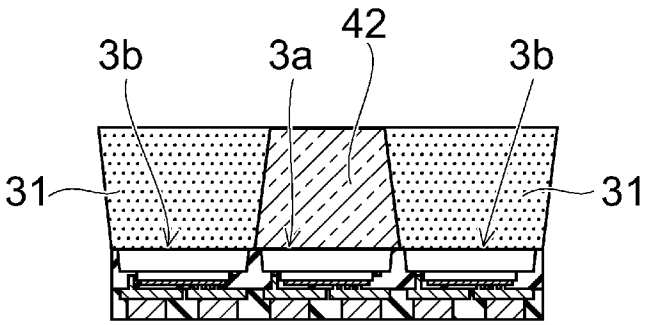


FIG. 9C

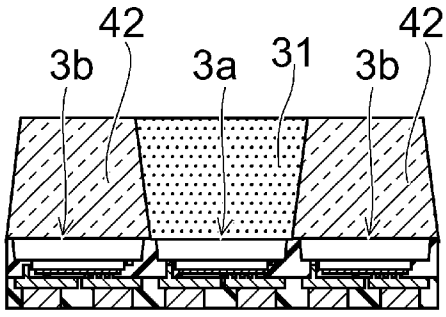


FIG. 9D

[Fig. 10]

FIG. 10A

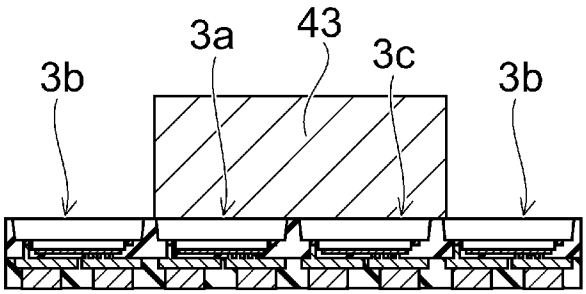


FIG. 10B

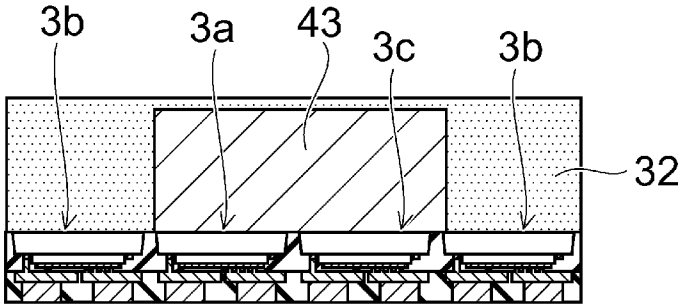


FIG. 10C

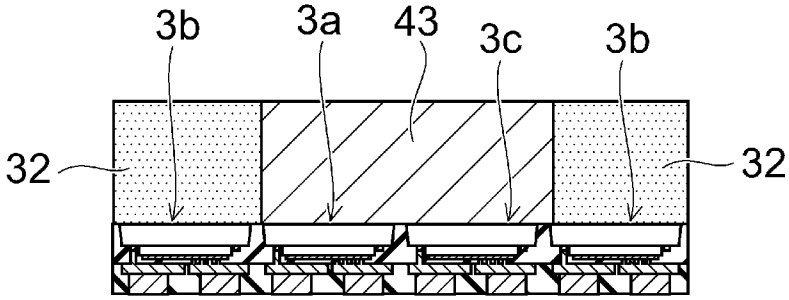


FIG. 10D

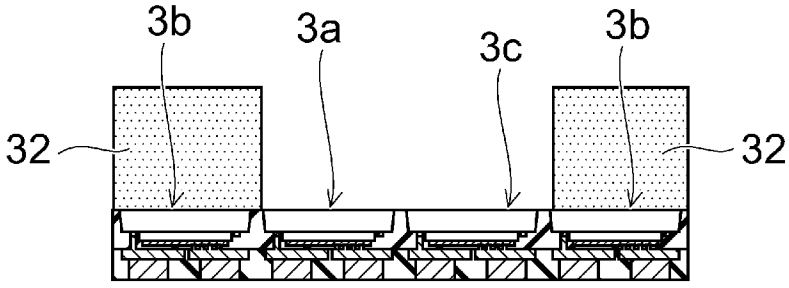
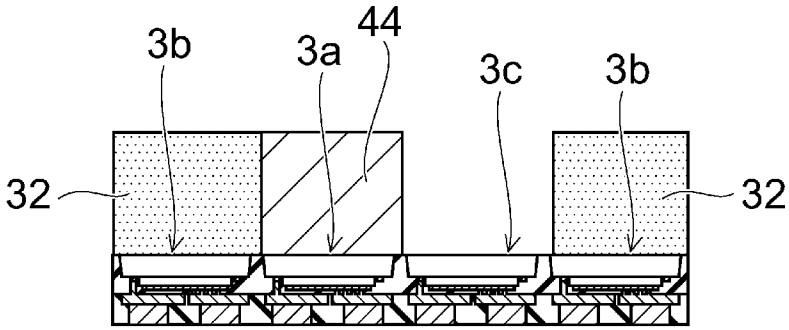


FIG. 10E



[Fig. 11]

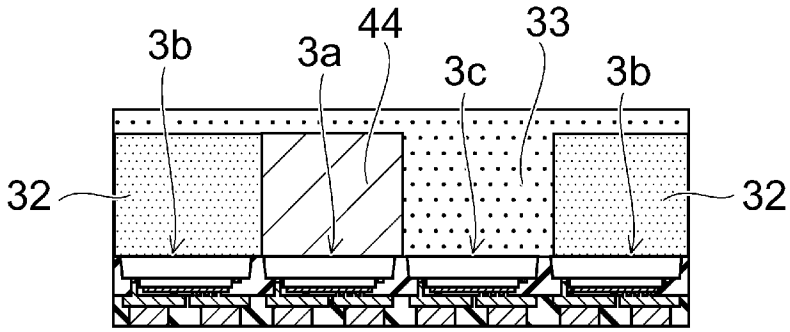


FIG. 11A

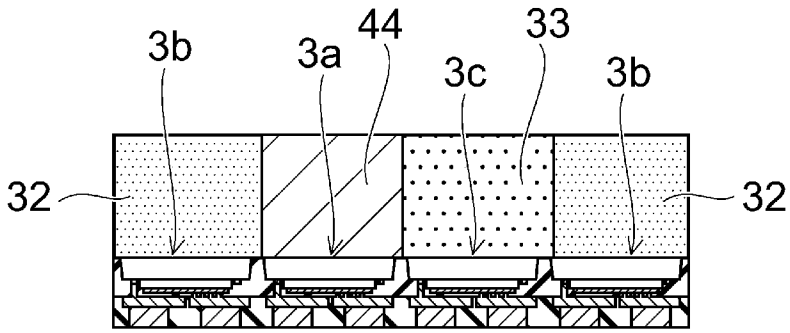


FIG. 11B

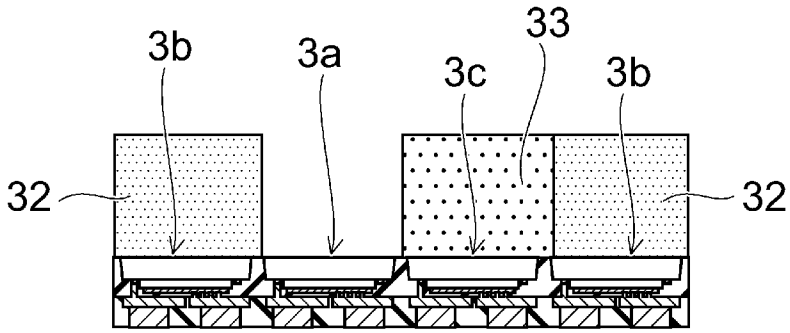


FIG. 11C

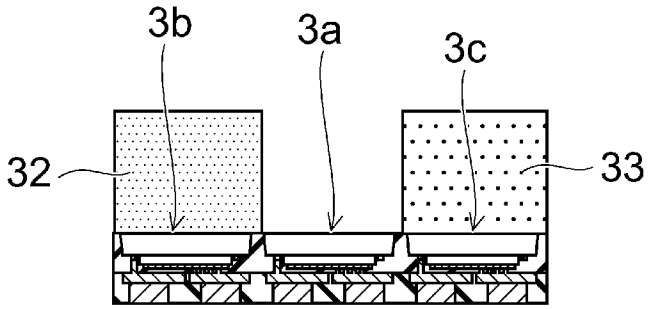


FIG. 11D

[Fig. 12]

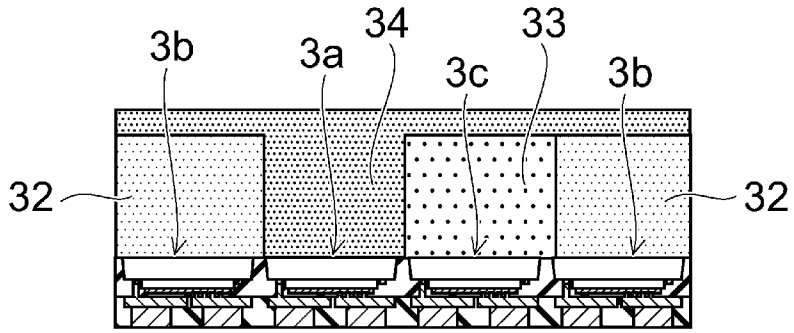


FIG. 12A

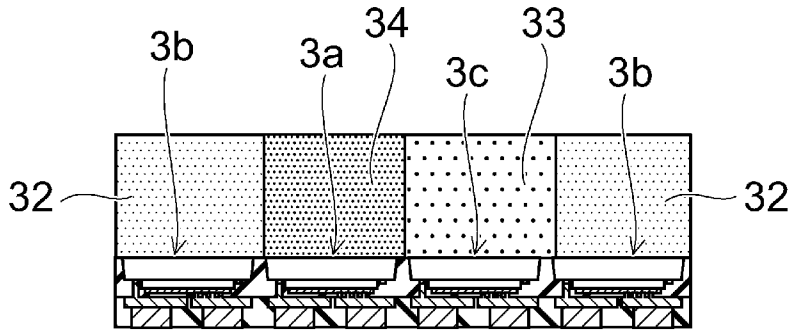


FIG. 12B

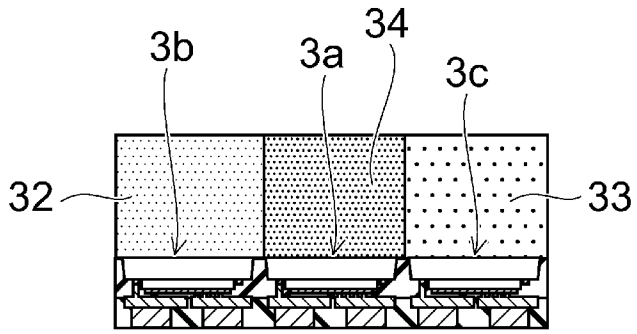


FIG. 12C

[Fig. 13]

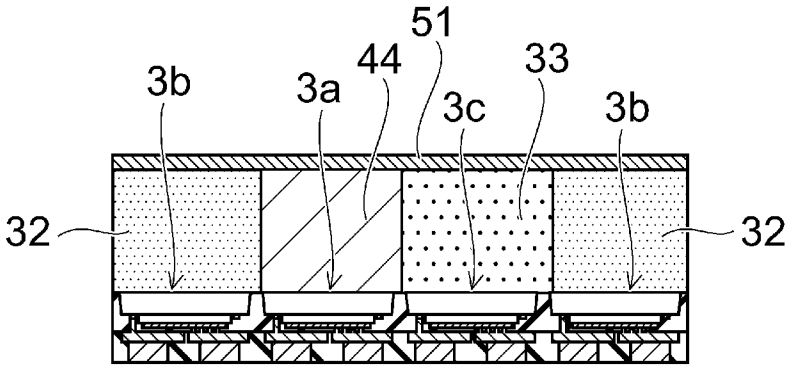


FIG. 13A

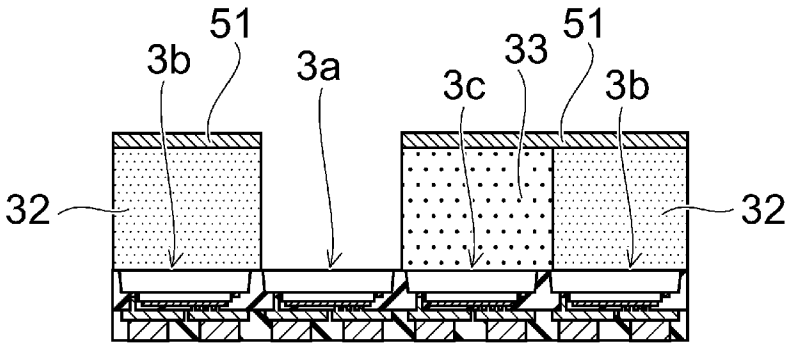


FIG. 13B

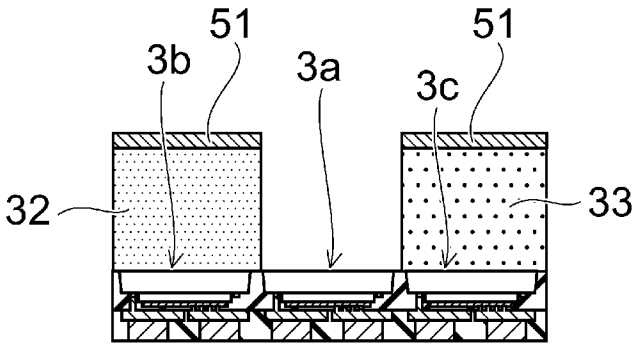


FIG. 13C

[Fig. 14]

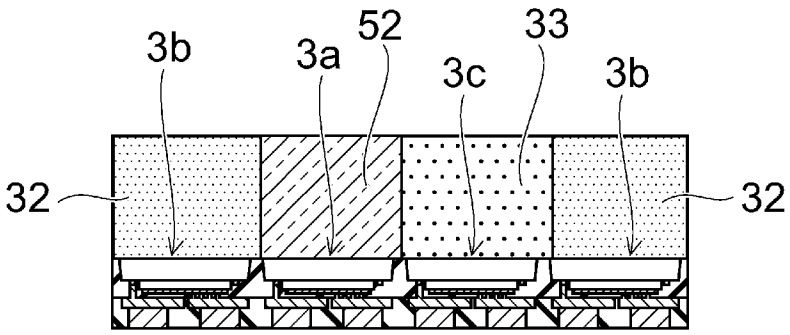


FIG. 14A

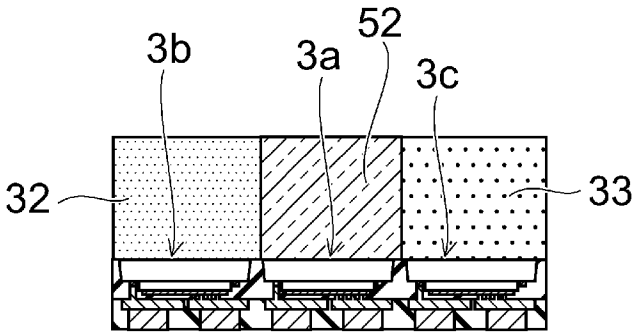


FIG. 14B

[Fig. 15]

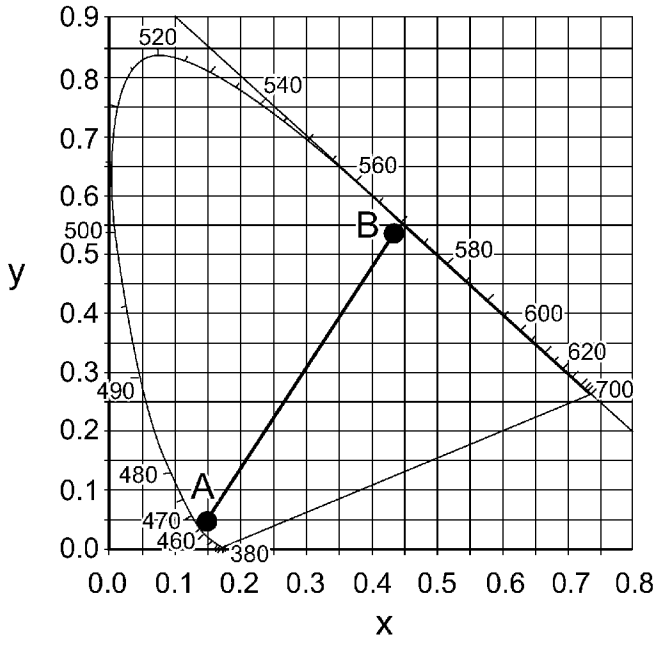


FIG. 15

[Fig. 16]

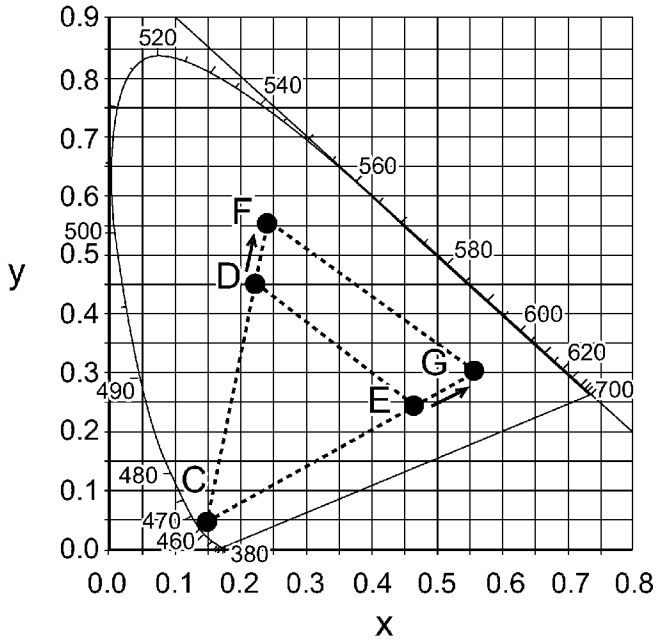


FIG. 16A

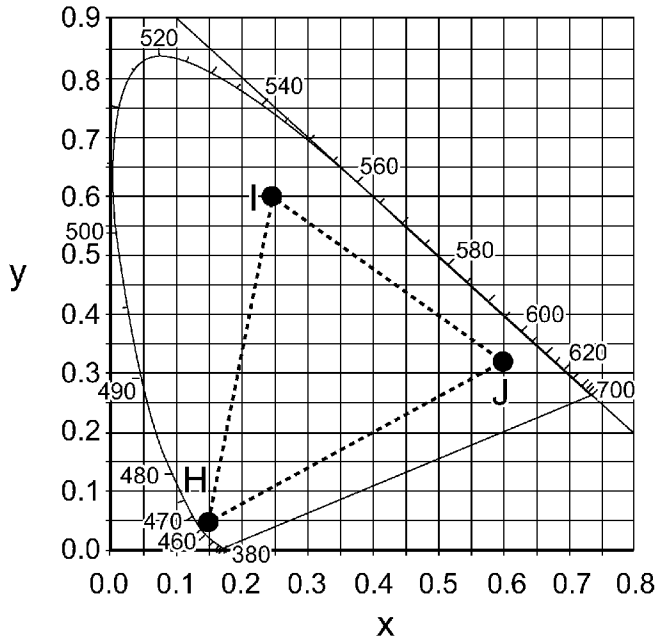


FIG. 16B

INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2012/001803

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/50 H01L25/075
ADD. H01L33/00 H05B33/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H05B F21K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/212305 A1 (HARADA MITSUNORI [JP]) 27 August 2009 (2009-08-27)	1
Y	abstract; figures 1,7,8 paragraphs [0052], [0058]	2-6
X	JP 2011 096739 A (PANASONIC ELEC WORKS CO LTD) 12 May 2011 (2011-05-12)	1
Y	abstract; figure 1 paragraph [0020]	2-6
Y	EP 2 197 051 A2 (TOSHIBA KK [JP]) 16 June 2010 (2010-06-16) paragraphs [0002], [0005], [0012] - [0022], [0048]; claim 13; figures 1A,1B,7B	2-6

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 October 2012	08/01/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Marani, Roberta

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/JP2012/001803

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009212305 A1	27-08-2009	CN 101520139 A	02-09-2009
		DE 102009010265 A1	03-09-2009
		JP 2009206246 A	10-09-2009
		US 2009212305 A1	27-08-2009
JP 2011096739 A	12-05-2011	NONE	
EP 2197051 A2	16-06-2010	EP 2197051 A2	16-06-2010
		JP 4724222 B2	13-07-2011
		JP 2010141176 A	24-06-2010
		TW 201031033 A	16-08-2010
		US 2010148198 A1	17-06-2010
		US 2012097972 A1	26-04-2012

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-6

A semiconductor light emitting device comprising at least three chips with fluorescent layers of different thicknesses arranged symmetrically. The chips comprise an insulating layer on the face opposite the fluorescent layer. The insulating layer having a first and second via for connecting the electrodes to respective wiring parts formed on the outer surface of the insulating layer.

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2. claims: 7-19

Method of manufacturing a semiconductor light emitting device comprising forming a sacrifice layer or a transparent resin layer on selected chips on a wafer and forming a fluorescent layer on the remaining chips.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2012/001803

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-6

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.