(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 December 2018 (27.12.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/236366 A1

(51) International Patent Classification:
H01L 43/08 (2006.01) *H01L 43/10* (2006.01)
H01L 43/02 (2006.01)

(21) International Application Number:
PCT/US2017/038472

(22) International Filing Date:
21 June 2017 (21.06.2017)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors; and

(71) Applicants: **MANIPATRUNI, Sasikanth** [IN/US]; 6993 NE Ronler Way, Apt 1817, Hillsboro, Oregon 97124 (US). **NIKONOV, Dmitri E.** [US/US]; 16569 SW Whitetail Lane, Beaverton, Oregon 97007 (US). **YOUNG, Ian A.** [US/US]; 3181 NW 114th Terrace, Portland, Oregon 97229 (US).

(74) Agent: **BRASK, Justin, K.** et al.; Schwabe, Williamson & Wyatt, 1211 SW 5th Ave., Suite 1900, Portland, OR 97204 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: COLOSSAL MAGNETORESISTANCE FOR MAGNETIC READ OUT

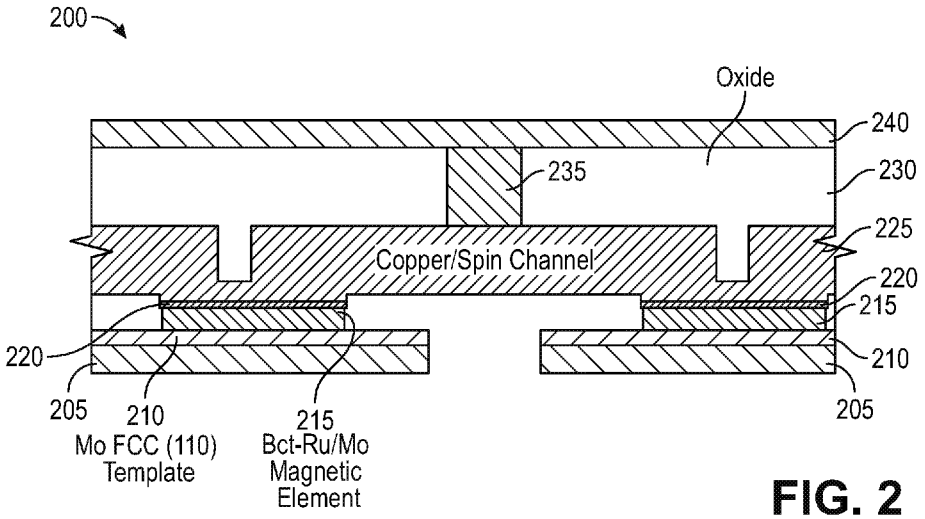


FIG. 2

(57) Abstract: Embodiments are generally directed to colossal magnetoresistance for magnetic read out utilizing Heusler alloys. An embodiment of a spin logic device includes a magnetic tunnel junction, which includes a stack including a plurality of layers, the stack including a ferromagnetic fixed layer, a ferromagnetic free layer, and a giant magnetoresistance layer between the ferromagnetic fixed layer and the first ferromagnetic free layer.

WO 2018/236366 A1

COLOSSAL MAGNETORESISTANCE FOR MAGNETIC READ OUT

TECHNICAL FIELD

Embodiments described herein generally relate to the field of electronic devices and, more particularly, colossal magnetoresistance for magnetic read out utilizing Heusler alloys.

BACKGROUND

With electronics approaching the nanometer scale, a scalable spintronic logic device that operates via spin-orbit transduction combined with magneto-electric switching has been developed as a technology to move beyond Complementary Metal Oxide Semiconductor (CMOS) computing. The Magneto-Electric Spin Orbit (MESO) logic enables the continued scaling of logic device to smaller scales. Spintronic logic can enable energy and computational efficiency by utilizing a new state variable for computation.

Present magnetic memory in the form of Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) technology utilizes magnetic tunnel junctions (MTJ) for switching and detection of the magnetic state. An MTJ consists of two ferromagnetic (FM) layers and a tunneling barrier (for example magnesium oxide, MgO) between the FM layers. The magnetic memory is read by the change of resistance for different relative magnetizations of FM layers, which is referred to as tunneling magnetoresistance (TMR).

However, this process and structure can create process problems including difficulty of control of the MgO thicknesses and uniformity; potential breakdown of the MgO layer; TMR degradation occurring after many switching cycles; and unfavorable scaling requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments described herein are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is an illustration of a giant magneto-resistance spin valve with colossal magneto-resistance material according to an embodiment;

Figure 2 is an illustration of a spin logic device with stacking of magnets below the spin channel according to an embodiment;

Figure 3 is an illustration of an operating mechanism for a ferroelectric metal-insulator transition Jahn-Teller device according to an embodiment;

Figure 4A, 4B, and 4C are illustrations of a strain induced metal-insulator transition non-volatile gate include Jahn-Teller materials according to an embodiment;

Figure 5A and 5B are illustrations of MTJ resistance with MTJ diameter;

Figure 6 is an illustration of an example of magnetoresistance for colossal magnetoresistive material for use in a device according to an embodiment;

Figure 7 is an illustration of spin torque switching utilizing certain materials for a spin logic device according to an embodiment;

Figure 8 is an illustration of the effect of use of high H_k and low M_s alloys on energy and delay of spin logic devices according to an embodiment;

Figure 9 is an illustration of energy and delay for spin logic devices according to an embodiment;

Figure 10 is an illustration of a system on chip including spin logic devices according to an embodiment;

Figure 11 is an illustration of a computing system including spin logic devices according to an embodiment; and

Figure 12 is an illustration of typical elements of a Heusler alloy.

DETAILED DESCRIPTION

Embodiments described herein are generally directed to colossal magneto-resistance for magnetic read out utilizing Heusler alloys.

For the purposes of this description:

"Giant magnetoresistance" or "GMR" refers to quantum mechanical magnetoresistance in thin-film structures composed of alternating ferromagnetic and non-magnetic conductive layers, providing significant change in electrical resistance depending on whether the magnetism of adjacent ferromagnetic layers are in parallel or antiparallel alignment.

"Colossal magnetoresistance" or "CMR" refers to a property of a materials that enables such materials to dramatically change their electrical resistance in the presence of a magnetic field. CMR materials include manganese-based perovskite oxides, Perovskite being a calcium titanium oxide mineral composed of calcium titanate ($CaTiO_3$).

"Heusler alloy" refers to ferromagnetic metal alloy based on a Heusler phase. A Heusler phase is an intermetallic with particular composition with particular composition and face-centered cubic crystal structure, and which are ferromagnetic as a result of the double-exchange mechanism between neighboring magnetic ions. A Heusler alloy in general is composed of metals that in their pure state are not ferromagnetic. As used herein, a Heusler alloy includes a full Heusler alloy (ferromagnetic metal alloy of the form X_2YZ), a half Heusler alloy (of the form XYZ), and an inverse Heusler alloy (of the form XYZX). An example of a Heusler alloy is Mn_3GeGa. **Figure 12** is an illustration of typical elements of a Heusler alloy.

"Jahn-Teller material" is a material with a geometric distortion of a non-linear molecular system, thereby reducing symmetry and energy. The Jahn-Teller effect is a geometric distortion in non-linear molecular systems that reduces the symmetry of the molecule or crystal. The reduced symmetry removes the degeneracy and reduces the energy of the molecule or the crystal. Jahn-Teller complexes include materials such as metal organic complexes, correlated oxide materials, and more recently fullerene based molecules. The effect can also be observed in tetrahedral complexes.

"Magneto-electric spin orbit logic device" or "MESO logic device" refers to a logic device that operates via spin-orbit transduction combined with magneto-electric switching, the MESO logic device utilizing magnetic state (or spin state) for logical operation. MESO devices may also be referred to in general as spin orbit logic (SOL) devices or spintronic devices.

STT-MRAM (Spin Transfer Torque – Magnetic Random Access Memory) utilizes spin transfer torque, spin transfer torque being the effect in which the orientation of a magnetic layer in a magnetic tunnel junction (MTJ) may be modified using a spin-polarized current.

A magnetic tunnel junction in general includes a first magnetic layer (a fixed magnetic layer) and a second layer (a free magnetic layer) of ferromagnetic (FM) material separated by a dielectric tunnel barrier, the dielectric tunnel layer being an ultrathin layer of insulator that allows electrons to tunnel through upon application of a bias voltage. The magnetic tunnel junction is a microelectronic element that may be a part of an integrated circuit including other types of microelectronic elements. The tunneling barrier commonly is magnesium oxide (MgO). When a bias is applied to the MTJ, electrons that are spin polarized by the magnetic layers may traverse the dielectric barrier through a tunneling process, wherein resistance to the tunneling is referred to as tunnel magnetoresistance (TMR). In operation, the MTJ device provides a low magnetoresistance when the magnetic moment of the free layer is parallel to the magnetic moment of the fixed layer and a high magnetoresistance when the magnetic moment of the free layer is oriented anti-parallel to the magnetic moment of the fixed layer. The tunneling current depends on the relative orientation of the magnetization of the two ferromagnetic layers, which may be changed by an applied magnetic field.

However, issues regarding the conventional MTJ technology include the following:

(1) Difficulty of control of the MgO thicknesses and uniformity to ensure the correct resistance and TMR;

(2) Potential breakdown of the MgO layer even at a modest bias voltage (such as 0.6 V);

(3) TMR degradation occurring after many switching cycles; and

(4) Unfavorable scaling requirements for RA product, which affects the spin efficiency and TMR.

In some embodiments, issues regarding conventional STT-MRAM technology are addressed by the implementation of GMR (Giant Magnetoresistance) switching devices in combination with CMR (Colossal Magnetoresistance) material.

In some embodiments, an MTJ comprises:

(a) A magnetic free layer and a magnetic fixed layer formed with CoFe (Cobalt Ferrite) in combination with magnetic Ru (Ruthenium) that is templated utilizing Mo (Molybdenum).

(b) Molybdenum is formed preferably in FCC <110> orientation and Ruthenium is formed in bct (body-centered-tetragonal) elongated or compressed tetragonal phase.

(c) The fixed layer may also be formed via combination of CoFe (Cobalt Ferrite) magnetic layer with Mo/Ru magnetic layers.

(d) A full stack for the MTJ comprises of:

Bottom Electrode/Mo/Ru/CoFe/MgO/CoFe/Ru/Mo/Top Electrode, for example in more detail of the structure

Ta/Ru/Ta/IrMn/Mo/Ru/CoFe(Fixedlayer)/MgO/CoFe(Freelayer)/Ru/Mo/Ru

In some embodiments, the magnetic properties of the MTJ can be further enhanced via use of magnetic super lattices:

Ta/Ru/Ta/IrMn/Mo/Ru/CoFe/[Mo/Ru/]$_n$CoFe/(Fixedlayer)/MgO/CoFe(Free layer)//[Mo/Ru/]n/CoFe/Ru

Figure 1 is an illustration of a giant magneto-resistance spin valve with colossal magneto-resistance material according to an embodiment. In some embodiments, a spin valve 100 includes a bottom electrode 105; a first ferromagnetic fixed layer 110; a GMR layer 115 typically comprising a non-magnetic metal, e.g. copper; ferromagnetic free layer 120, which may include Mn_3GeGa with effective anisotropy field $H_k > 7T$ (H_k = anisotropy field); a CMR layer 125, which may include 10 mOhm per centimeter, such as LaCaMnO (Lanthanum Calcium Manganese Oxide); a second ferromagnetic fixed layer 130; and a second electrode 135. In some embodiments, the spin valve is a portion of an integrated circuit including other microelectronic elements.

In some embodiments, the free layer 120 may include layers of TaN (Tantalum Nitride); $IrMn_3$ (Iridium Manganese); a second TaN layer; and a Mn_3GeGa (Manganese Germanium Gallium) layer. In some embodiments, Jahn-Teller materials are applied in computing and sensing operations.

In some embodiments, a structure for spin logic device/lateral spin valve includes the following:

(I) Magnetic contacts are formed with Jahn-Teller Magnetic Elements:

(1) Magnetic contacts are formed with high anisotropy (H_k) and low magnetic saturation (M_s) materials comprising of bct-Jahn-Teller materials.

(II) Engineered interface between the bct-Ru alloy and the spin channel:

(1) An engineered interface (such as, for example, Ag FCC) between the bct-Ru and the spin channel is formed utilizing atomistic crystalline matched layers. This component serves at least the following purposes:

(a) Provides a high mechanical barrier to stop or inhibit the inter-diffusion of the magnetic species with the spin channel.

(b) A template with the correct crystal orientation provides atomistic matching of the interfaces of the magnet with the channel.

(c) Maintains high spin injection at the interface.

(III) Electric contact to the magnets is formed with an engineered interface:

A second Mo interfacial layer is introduced for two purposes:

(a) Forming the electrical contact to the magnets. (b)Providing a template with the correct crystal orientation to seed the formation of the bct-Ru alloy.

(IV) An inverted structure for the spin logic is provided, the inverted structure provides the following:

(1) The inverted structure allows for placement of the magnetic contacts below the spin channel, wherein may be formed with an in-situ processing method. This processing method allows the following:

(a) The fabrication of bct-Ru alloy and the matching layer via the use of an in-situ processing flow.

(b) The templating of bct-Ru for an appropriate crystal structure.

(c) Easier formation of oxide insulation between the spin channels belonging to separate devices.

Figure 2 is an illustration of a spin logic device with stacking of magnets below the spin channel according to an embodiment. In some embodiments, The spin logic device, shown as lateral (non-local) spin valve, includes the following:

(a) A first copper (back end metal) layer 205;

(b) A Mo FCC <110> template 210;

(c) bct-Ru/Mo magnetic elements 215;

(d) Ag (FCC) (Silver) connections 220;

(e) A spin channel 220 shown as a copper, wherein a spin channel can be a channel

consisting of one or more of Copper, Silver, Aluminum, or Graphene or other 2D material (2D materials being crystalline materials consisting of a single layer of atoms);

(f) A via 235 surrounded by oxide layer 230; and

(g) A second copper layer 240.

In some embodiments, a structure for an FE-MIT (Ferroelectric Metal-Insulator Transition) memory element includes the following:

(a) A ferroelectric material stack to provide fixed charge concentration to set up a remnant electric field across a dielectric material;

(b) A dielectric capacitor comprised of Jahn-Teller distortion sensitive material; and

(c) Jahn-Teller distortion material in the dielectric capacitor, which responds to the attractive/repulsive force to cause a change in conductivity.

In some embodiments, structures using JT-AFM (Jahn-Teller Anti-Ferromagnetic) memory element include the following:

(a) Structures are of a SHE-MTJ (Spin Hall Effect Magnetic Tunnel Junction) formed by a JT-AFM (Exohedral C_{60}-based metallofullerenes, CsC_{60}) switched with Spin-Hall Effect; or

(b) A magnetic tunnel junction formed with free layers comprising of JT-AFM (CsC_{60}); or

(c) A magnetic tunnel junction formed with a pinned layer comprising of JT-AFM (CsC_{60}).

Figure 3 is an illustration of an operating mechanism for a ferroelectric metal-insulator transition Jahn-Teller device according to an embodiment. In some embodiments, a strain inducted metal-insulator transition utilizing Jahn-Teller materials include a stack including:

(a) Ta (Tantalum) 305;

(b) Ru (Ruthenium) 310;

(c) Ta 315;

(d) A ferroelectric pinned layer 320;

(e) Fix ferroelectric material 325;

(f) MIT-JTM (Metal-Insulator Transition Jahn-Teller Material) 330;

(g) HfO_2 (Hafnium Oxide) 335;

(h) Ta 340; and

(i) Ru 345.

In some embodiments, the MIT-JTM layer is:

Rb_2CsC_{60}, $Rb_xCs_{3-x}C_{60}$.

In some embodiments, the MIT-JTM layer is:

$NdNiO_3$, $La0.9Sr_{0.1}MnO_3$, $(Nd_{1-x}Prx)0.5Sr0.5MbO_3$.

Figure 4A, 4B, and 4C are illustrations of a strain induced metal-insulator transition non-volatile gate include Jahn-Teller materials according to an embodiment. In some embodiments, a gate includes Jahn-Teller materials, thereby generating a strain induced metal-insulator non-volatile gate. As illustrated in Figure 4, the gate includes metal 410 and an MIT (Metal-Insulator Transition) 430 including piezoelectric/ferroelectric materials 420. In some embodiments, the cross-section of the junction may be as illustrated in Figure 4B or 4C, which illustrate the strain induced metal-insulator transition.

Figure 5A and 5B are illustrations of magnetic tunnel junction resistance with magnetic tunnel junction diameter. The voltage drive required to the magnetic tunnel junction increases with the reduction in diameter, thereby leading to a loss of polarization. Figures 5A and 5B illustrate the unfavorable scaling requirements for RA products with conventional construction of MTJ devices.

Figure 6 is an illustration of an example of magnetoresistance for colossal magnetoresistive material for use in a device according to an embodiment. As illustrated in Figure 6, the magnetoresistance for the opposed (anti-parallel) state (610) providing the indicated resistance of R0 = 1.35 MΩ (megaohms) versus the parallel state (620) providing RH = 1.06 KΩ (kiloohms).

Figure 7 is an illustration of spin torque switching utilizing certain materials for a spin logic device according to an embodiment. The improvement in switching dynamics for a nanomagnet with reduced magnetic anisotropy (compared to 106 MA/m for CoFe) and improved H_k (10 kOe (kilo Oersteds) compared to 1 kOe) is illustrated in Figure 7. As illustrated in Figure 7, the switching time in nanoseconds for a spin current of a certain amount is significantly reduced in an embodiment incorporating a stack with Heusler alloys 710, with values in the range of M_s = 0.800 MA/cm^2 and H_k = 10,000 Oe, in comparison with materials with nominal PMA 720. In some implementations, a stack may have greater H_k values, with H_k reaching 60.000 Oe.

Figure 8 is an illustration of the effect of use of high anisotropy and low magnetic saturation alloys on energy and delay of spin logic devices according to an embodiment. In some embodiments, materials with H_k and low M_s are implemented in spin logic devices to improve energy-delay, i.e., to reduce energy at a constant delay or reduce delay at a constant energy. In some embodiments, the improvement in energy-delay arises from the ability to implement high H_k and low M_s magnetic materials using Jahn-Teller distortion in magnetic materials. In the illustration provided in Figure 8, M = 1MA/cm^2 and H_k = 2300 Oe.

Figure 9 is an illustration of energy and delay for spin logic devices according to an embodiment. As illustrated in Figure 9, devices with high Hk and low Ms alloys (PMA Improved Anisotropy) are compared to conventional material approaches for spin logic devices, with the improved anisotropy devices providing significantly improved energy delay in comparison with the conventional devices, as well as providing an improvement in energy delay in comparison with a 20 cm CMOS device.

Figure 10 is an illustration of a system on chip including spin logic devices according to an embodiment. In some embodiments, an integrated circuit such as a system on chip (SoC) 1000 includes one or more active components 1080 within the elements, including one or more spin logic devices 1085, a spin logic device including a stack including a plurality of layers, the stack including a ferromagnetic fixed layer and a ferromagnetic free layer, a giant magnetoresistance layer between the ferromagnetic fixed layer and the first ferromagnetic free layer, and a colossal magnetoresistance material layer adjacent to the ferromagnetic free layer; and a spin channel coupled with the stack.

In some embodiments, the SoC 1000 may further include, but is not limited to, the following:

(a) A central processing unit (CPU) or other processing element 1010 for the processing of data.

(b) A graphics processing unit (GPU) 1020 to create images for output to a display.

(c) Memory 1030, where memory may include random access memory (RAM) or other dynamic storage device or element as a main memory for storing information and instructions to be executed by the CPU 1010 and the GPU 1020. Main memory may include, but is not limited to, dynamic random access memory (DRAM). Memory 1030 may further include a non-volatile memory, such as flash memory, and a read only memory (ROM) or other static storage device for storing static information and instructions for the CPU 1010 and GPU 1020.

(d) A Northbridge 1040 to handle communications between the CPU and other component of the SoC. In some embodiments, the SoC 1000 may further include a Southbridge 1050 to handle I/O functions.

(e) A transmitter, receiver, or both 1060 for the transmission and reception of data via wireless communications, and one or more antennas for transmission or reception of wireless communication. Wireless communication includes, but is not limited to, Wi-Fi, Bluetooth™, near field communication, and other wireless communication standards. The one or more antennas include one or more dipole, monopole, or other antennas.

(f) One or more interfaces 1070, including USB (Universal Serial Bus), Firewire, Ethernet, or other interfaces.

Figure 11 is an illustration of a computing system including spin logic devices according to an embodiment. In this illustration, certain standard and well-known components that are not germane to the present description are not shown, and certain elements shown as separate elements may be combined.

In some embodiments, a computing system 1100 may include a processing means such as one or more processors 1110 coupled to one or more buses or interconnects, shown in general as bus 1105. The processors 1110 may comprise one or more physical processors and one or more logical processors. In some embodiments, the processors may include one or more general-purpose processors or special-purpose processors.

The bus 1105 is a communication means for transmission of data. The bus 1105 is illustrated as a single bus for simplicity, but may represent multiple different interconnects or buses and the component connections to such interconnects or buses may vary. The bus 1105 shown in Figure 11 is an abstraction that represents any one or more separate physical buses, point-to-point connections, or both connected by appropriate bridges, adapters, or controllers.

In some embodiments, the computing system 1100 further comprises a random access memory (RAM) or other dynamic storage device or element as a main memory 1115 for storing information and instructions to be executed by the processors 1110. Main memory 1115 may include, but is not limited to, dynamic random access memory (DRAM). In some embodiments, the main memory 1115 includes one or more memory devices having multiple memory dies, including stacked memory, the memory dies including multiple partitions.

The computing system 1100 also may comprise a non-volatile memory 1120; a storage device such as a solid-state drive (SSD) 1130; and a read only memory (ROM) 1135 or other static storage device for storing static information and instructions for the processors 1110.

In some embodiments, the computing system 1100 includes one or more transmitters or receivers 1140 coupled to the bus 1105. In some embodiments, the computing system 1100 may include one or more antennae 1144, such as dipole or monopole antennae, for the transmission and reception of data via wireless communication using a wireless transmitter, receiver, or both, and one or more ports 1142 for the transmission and reception of data via wired communications. Wireless communication includes, but is not limited to, Wi-Fi, Bluetooth™, near field communication, and other wireless communication standards.

In some embodiments, computing system 1100 includes one or more input devices 1150 for the input of data, including hard and soft buttons, a mouse or other pointing device, a keyboard, voice command system, or gesture recognition system.

In some embodiments, computing system 1100 includes an output display 1155, where the output display 1155 may include a liquid crystal display (LCD), projection device, or any

other display technology, for displaying information or content to a user. In some environments, the output display 1155 may include a touch-screen that is also utilized as at least a part of an input device 1150. Output display 1155 may further include audio output, including one or more speakers, audio output jacks, or other audio, and other output to the user.

The computing system 1100 may also comprise a battery or other power source 1160, which may include a solar cell, a fuel cell, a charged capacitor, near field inductive coupling, or other system or device for providing or generating power in the computing system 1100. The power provided by the power source 1160 may be distributed as required to elements of the computing system 1100.

In some embodiments, one or more components of the computing system 1100, such as the processors 1110, include MESO devices in accordance with one or more embodiments described herein.

In various implementations, the computing system 1100 may be a laptop, a netbook, a notebook, an Ultrabook™, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing system 1100 may be any other electronic device that processes data.

In some embodiments, a spin logic device includes a magnetic tunnel junction including a stack with a plurality of layers, the layers of the stack including the following: a first ferromagnetic fixed layer and a first ferromagnetic free layer, and a colossal magnetoresistance material layer between the first ferromagnetic fixed layer and the first ferromagnetic free layer.

In some embodiments, the layers of the stack further include a second fixed ferromagnetic layer; and a giant magnetoresistance layer between the second ferromagnetic fixed layer and the first ferromagnetic free layer.

In some embodiments, the device further includes a spin channel coupled with the stack. In some embodiments, the stack is fabricated below the spin channel. In some embodiments, the spin channel is composed of one or more of Copper (Co), Silver (Ag), Aluminum (Al), Graphene, or other 2D material.

In some embodiments, the colossal magnetoresistance material layer includes a Jahn-Teller material.

In some embodiments, one or more of the first ferromagnetic free layer and the first ferromagnetic fixed layer are formed with Cobalt Ferrite (CoFe) in combination with magnetic Ruthenium (Ru).

In some embodiments, the Ruthenium is templated with Molybdenum (Mo).

In some embodiments, the Molybdenum is formed in FCC <110> orientation.

In some embodiments, the Ruthenium is formed in bct (body-centered-tetragonal) elongated or compressed tetragonal phase.

In some embodiments, the stack of the magnetic tunnel junction further includes an engineering between the Ruthenium and the spin channel.

In some embodiments, an integrated circuit includes a plurality of microelectronic elements including one or more active components; wherein the one or more active components include a magnetic tunnel junction, the magnetic tunnel junction including a stack with a plurality of layers, the layers of the stack including the following: a first ferromagnetic fixed layer and a first ferromagnetic free layer; a colossal magnetoresistance material layer between the first ferromagnetic fixed layer and the first ferromagnetic free layer; a second fixed ferromagnetic layer; and a giant magnetoresistance layer between the second ferromagnetic fixed layer and the first ferromagnetic free layer.

In some embodiments, the integrated circuit further includes a spin channel coupled with the stack, wherein the stack is fabricated below the spin channel.

In some embodiments, the first ferromagnetic fixed layer and a first ferromagnetic free layer are formed with Cobalt Ferrite (CoFe) in combination with magnetic Ruthenium (Ru).

In some embodiments, the Ruthenium is templated with Molybdenum (Mo).

In some embodiments, the stack further includes a tunneling barrier of MgO (Magnesium Oxide), and the layers of the stack between a bottom electrode and a top electrode are: Mo/Ru/CoFe/MgO/CoFe/Ru/Mo.

In some embodiments, the colossal magnetoresistance material layer includes a Jahn-Teller material.

In some embodiments, the first ferromagnetic free layer includes the following layers: a first Tantalum Nitride (TaN) layer; an Iridium Manganese (IrMn3) layer; a second TaN layer; and a Manganese Germanium Gallium (Mn3GeGa) layer.

In some embodiments, a computing system includes a processor; a memory to store data for the processor; and a transmitter or receiver and antenna for transmitting or receiving data, wherein at least one element of the computing system includes a spin logic, the spin logic device including a magnetic tunnel junction including a stack with a plurality of layers, the layers of the stack including the following: a first ferromagnetic fixed layer and a first ferromagnetic free layer, and a colossal magnetoresistance material layer between the first ferromagnetic fixed layer and the first ferromagnetic free layer.

In some embodiments, the layers of the stack of the magnetic tunnel junction further

include: a second fixed ferromagnetic layer; and a giant magnetoresistance layer between the second ferromagnetic fixed layer and the first ferromagnetic free layer.

In some embodiments, the computing system further includes a spin channel coupled with the stack. In some embodiments, the stack is fabricated below the spin channel.

In some embodiments, the colossal magnetoresistance material layer includes a Jahn-Teller material.

In the description above, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the described embodiments. It will be apparent, however, to one skilled in the art that embodiments may be practiced without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form. There may be intermediate structure between illustrated components. The components described or illustrated herein may have additional inputs or outputs that are not illustrated or described.

Various embodiments may include various processes. These processes may be performed by hardware components or may be embodied in computer program or machine-executable instructions, which may be used to cause a general-purpose or special-purpose processor or logic circuits programmed with the instructions to perform the processes. Alternatively, the processes may be performed by a combination of hardware and software.

Portions of various embodiments may be provided as a computer program product, which may include a computer-readable medium having stored thereon computer program instructions, which may be used to program a computer (or other electronic devices) for execution by one or more processors to perform a process according to certain embodiments. The computer-readable medium may include, but is not limited to, magnetic disks, optical disks, read-only memory (ROM), random access memory (RAM), erasable programmable read-only memory (EPROM), electrically-erasable programmable read-only memory (EEPROM), magnetic or optical cards, flash memory, or other type of computer-readable medium suitable for storing electronic instructions. Moreover, embodiments may also be downloaded as a computer program product, wherein the program may be transferred from a remote computer to a requesting computer.

Many of the methods are described in their most basic form, but processes can be added to or deleted from any of the methods and information can be added or subtracted from any of the described messages without departing from the basic scope of the present embodiments. It will be apparent to those skilled in the art that many further modifications and adaptations can be made. The particular embodiments are not provided to limit the concept but to illustrate it. The

scope of the embodiments is not to be determined by the specific examples provided above but only by the claims below.

If it is said that an element "A" is coupled to or with element "B," element A may be directly coupled to element B or be indirectly coupled through, for example, element C. When the specification or claims state that a component, feature, structure, process, or characteristic A "causes" a component, feature, structure, process, or characteristic B, it means that "A" is at least a partial cause of "B" but that there may also be at least one other component, feature, structure, process, or characteristic that assists in causing "B." If the specification indicates that a component, feature, structure, process, or characteristic "may", "might", or "could" be included, that particular component, feature, structure, process, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, this does not mean there is only one of the described elements.

An embodiment is an implementation or example. Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. It should be appreciated that in the foregoing description of exemplary embodiments, various features are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various novel aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed embodiments requires more features than are expressly recited in each claim. Rather, as the following claims reflect, novel aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims are hereby expressly incorporated into this description, with each claim standing on its own as a separate embodiment.

CLAIMS

What is claimed is:

1. A spin logic device comprising:

a magnetic tunnel junction including a stack with a plurality of layers, the layers of the stack including the following:

a first ferromagnetic fixed layer and a first ferromagnetic free layer, and

a colossal magnetoresistance material layer between the first ferromagnetic fixed layer and the first ferromagnetic free layer.

2. The device of claim 1, wherein the layers of the stack further include:

a second fixed ferromagnetic layer; and

a giant magnetoresistance layer between the second ferromagnetic fixed layer and the first ferromagnetic free layer.

3. The device of claim 1, further comprising:

a spin channel coupled with the stack.

4. The device of claim 3, wherein the stack is fabricated below the spin channel.

5. The device of claim 3, wherein the spin channel is composed of one or more of Copper (Co), Silver (Ag), Aluminum (Al), Graphene, or other 2D material.

6. The device of claim 1, wherein the colossal magnetoresistance material layer includes a Jahn-Teller material.

7. The device of claim 1, wherein one or more of the first ferromagnetic free layer and the first ferromagnetic fixed layer are formed with Cobalt Ferrite (CoFe) in combination with magnetic Ruthenium (Ru).

8. The device of claim 7, wherein the Ruthenium is templated with Molybdenum (Mo).

9. The device of claim 8, wherein the Molybdenum is formed in FCC <110> orientation.

10. The device of claim 8, wherein the Ruthenium is formed in bct (body-centered-tetragonal) elongated or compressed tetragonal phase.

11. The device of claim 7, wherein the stack of the magnetic tunnel junction further includes an engineering between the Ruthenium and the spin channel.

12. An integrated circuit comprising:

a plurality of microelectronic elements including one or more active components;

wherein the one or more active components include a magnetic tunnel junction, the magnetic tunnel junction including a stack with a plurality of layers, the layers of the stack including the following:

a first ferromagnetic fixed layer and a first ferromagnetic free layer;

a colossal magnetoresistance material layer between the first ferromagnetic fixed layer and the first ferromagnetic free layer;

a second fixed ferromagnetic layer; and

a giant magnetoresistance layer between the second ferromagnetic fixed layer and the first ferromagnetic free layer.

13. The integrated circuit of claim 12, further comprising:

a spin channel coupled with the stack, wherein the stack is fabricated below the spin channel.

14. The integrated circuit of claim 12, wherein the first ferromagnetic fixed layer and a first ferromagnetic free layer are formed with Cobalt Ferrite (CoFe) in combination with magnetic Ruthenium (Ru).

15. The integrated circuit of claim 14, wherein the Ruthenium is templated with Molybdenum (Mo).

16. The integrated circuit of claim 15, wherein the stack further includes a tunneling barrier of MgO (Magnesium Oxide), and wherein the layers of the stack between a bottom electrode and a top electrode are:

Mo/Ru/CoFe/MgO/CoFe/Ru/Mo.

17. The integrated circuit of claim 12, wherein the colossal magnetoresistance material layer includes a Jahn-Teller material.

18. The integrated circuit of claim 12, wherein the first ferromagnetic free layer includes the following layers:

a first Tantalum Nitride (TaN) layer;

an Iridium Manganese ($IrMn_3$) layer;

a second TaN layer; and

a Manganese Germanium Gallium (Mn_3GeGa) layer.

19. A computing system comprising:

a processor;

a memory to store data for the processor; and

a transmitter or receiver and antenna for transmitting or receiving data;

wherein at least one element of the computing system includes a spin logic, the spin logic device including:

a magnetic tunnel junction including a stack with a plurality of layers, the layers of the stack including the following:

a first ferromagnetic fixed layer and a first ferromagnetic free layer, and

a colossal magnetoresistance material layer between the first ferromagnetic fixed layer and the first ferromagnetic free layer.

20. The computing system of claim 19, wherein the layers of the stack of the magnetic tunnel junction further include:

a second fixed ferromagnetic layer; and

a giant magnetoresistance layer between the second ferromagnetic fixed layer and the first ferromagnetic free layer.

21. The computing system of claim 19, further comprising:

a spin channel coupled with the stack.

22. The computing system of claim 21, wherein the stack is fabricated below the spin channel.

23. The computing system of claim 19, wherein the colossal magnetoresistance material layer includes a Jahn-Teller material.

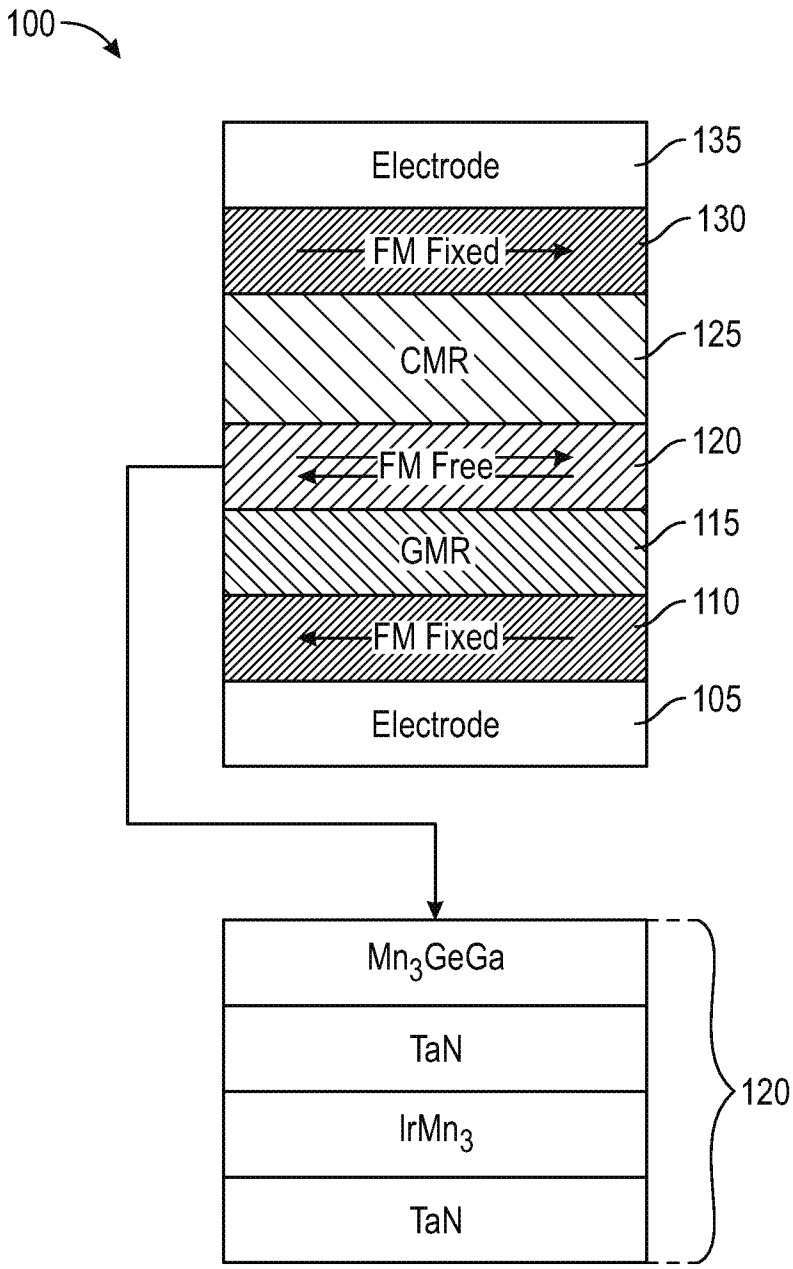

100
Electrode
135
FM Fixed
130
CMR
125
FM Free
120
GMR
115
FM Fixed
110
Electrode
105
Mn_3GeGa
TaN
$IrMn_3$
TaN
120

FIG. 1

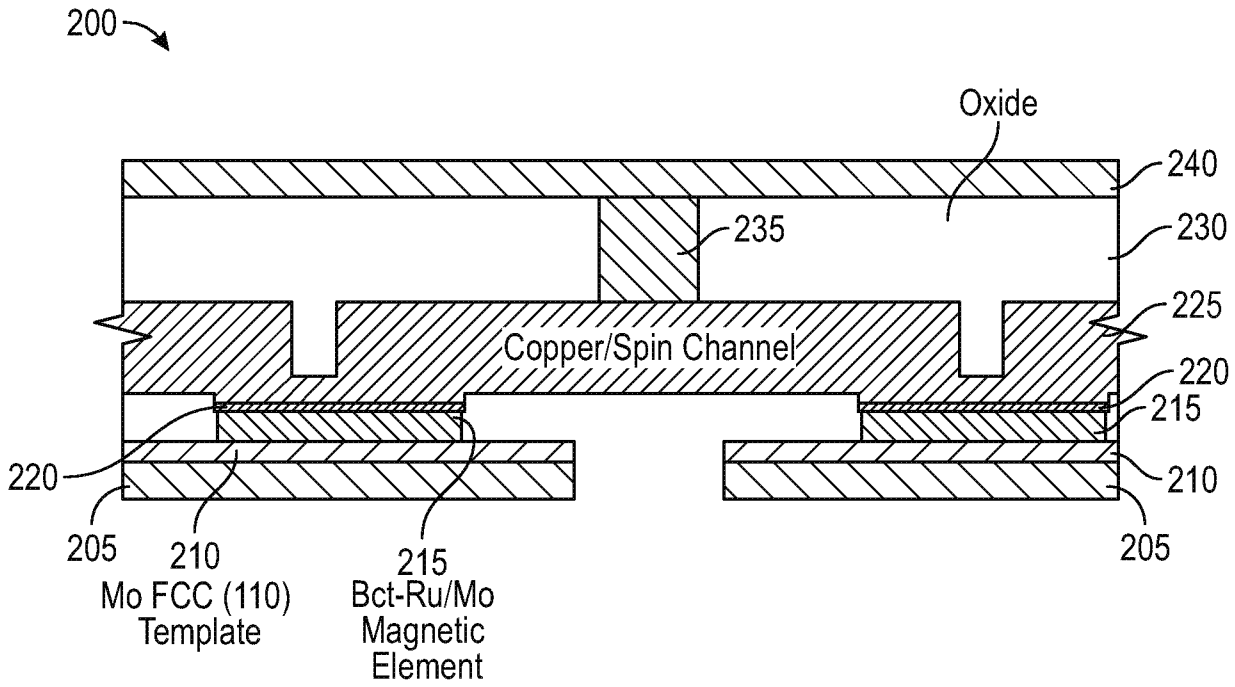
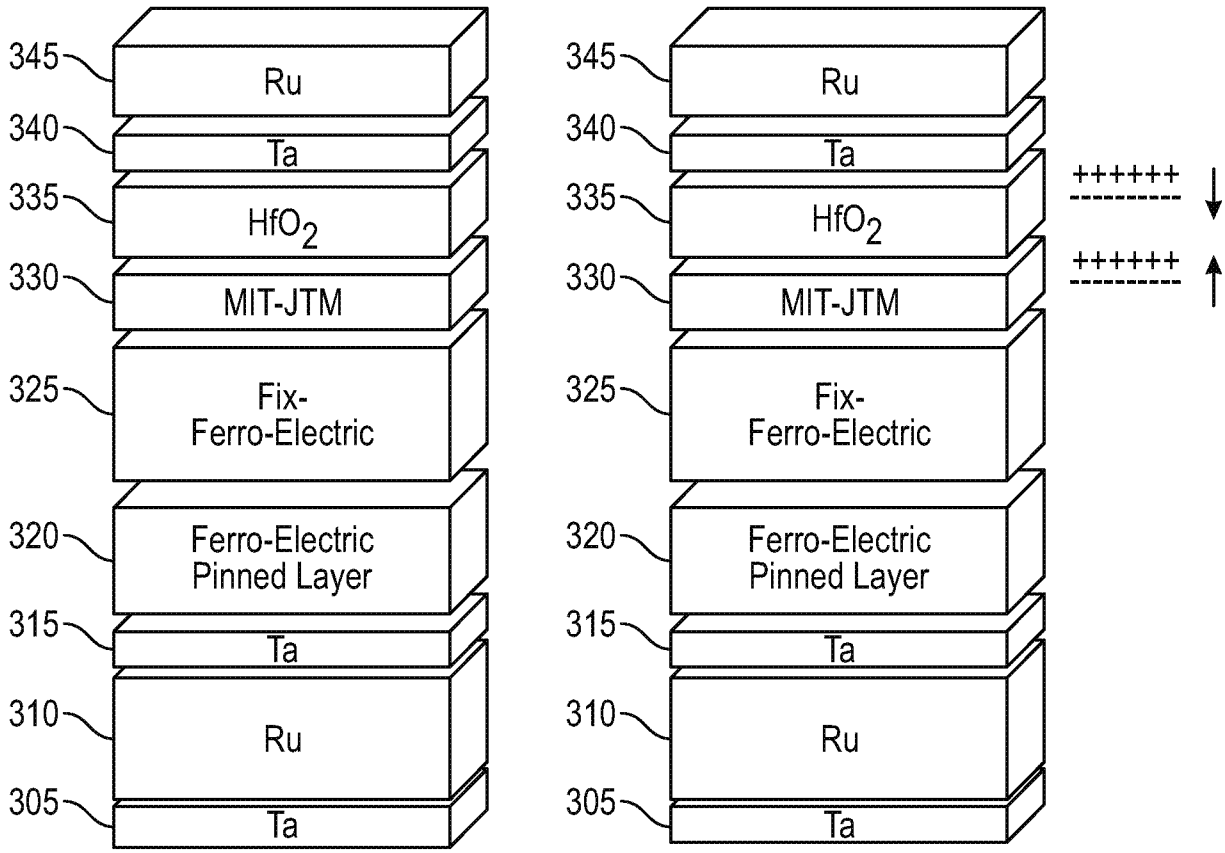

200
Oxide
240
235
230
225
Copper/Spin Channel
220
215
210
220
205
210
215
205
Mo FCC (110)
Template
Bct-Ru/Mo
Magnetic
Element

FIG. 2



MIT-JTM: Rb_2CsC_{60}, $Rb_xCs_{3-x}C_{60}$

MIT-JTM: $NdNiO_3$, $La_{0.9}Sr_{0.1}MnO_3$,
$(Nd_{1-x}Pr_x)_{0.5}Sr_{0.5}MnO_3$

FIG. 3

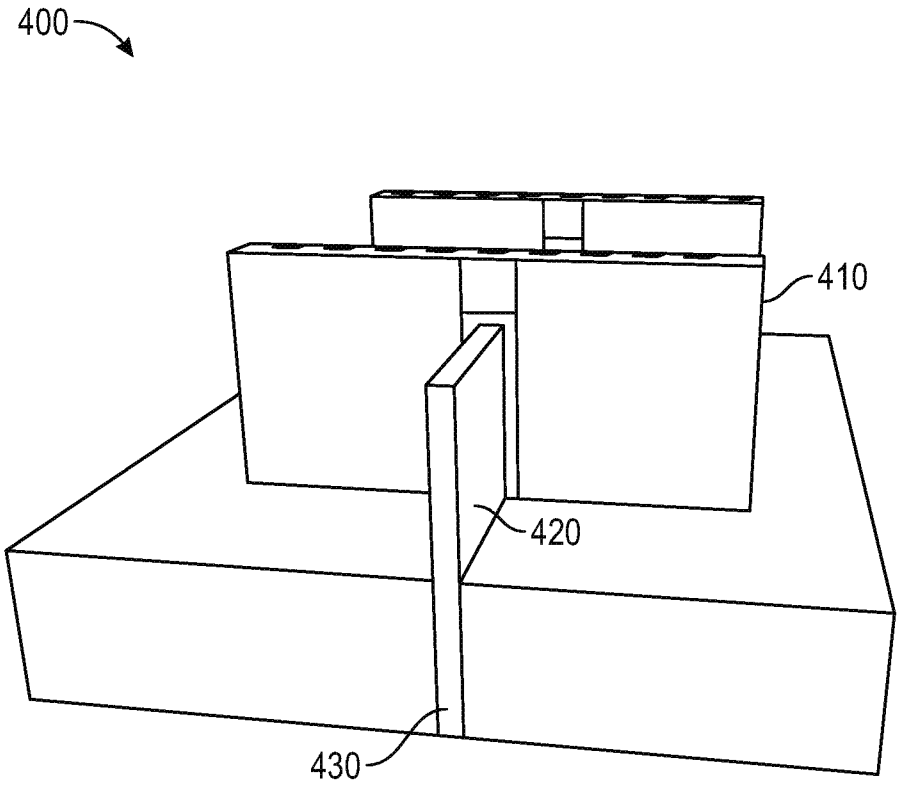


FIG. 4A

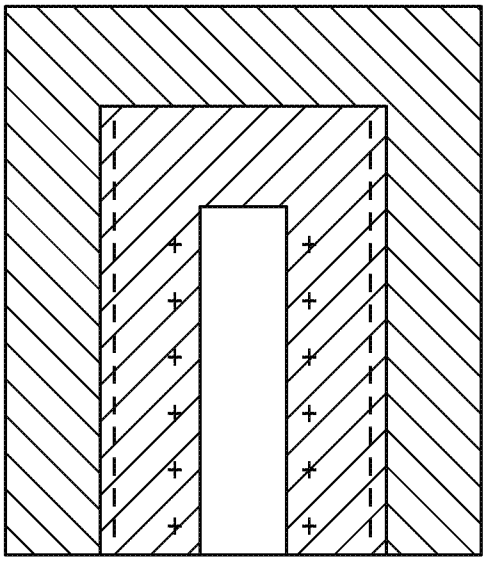


FIG. 4B

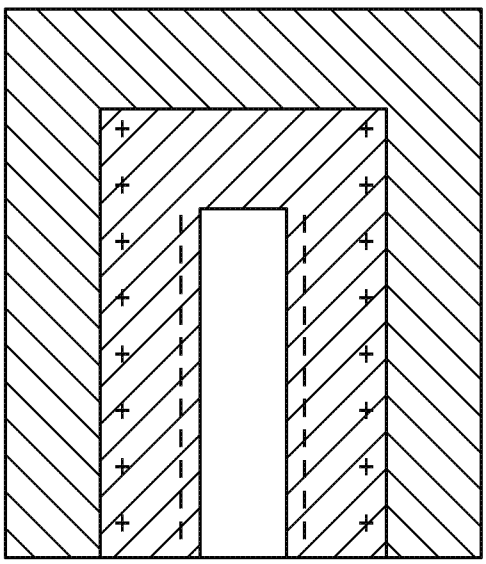


FIG. 4C

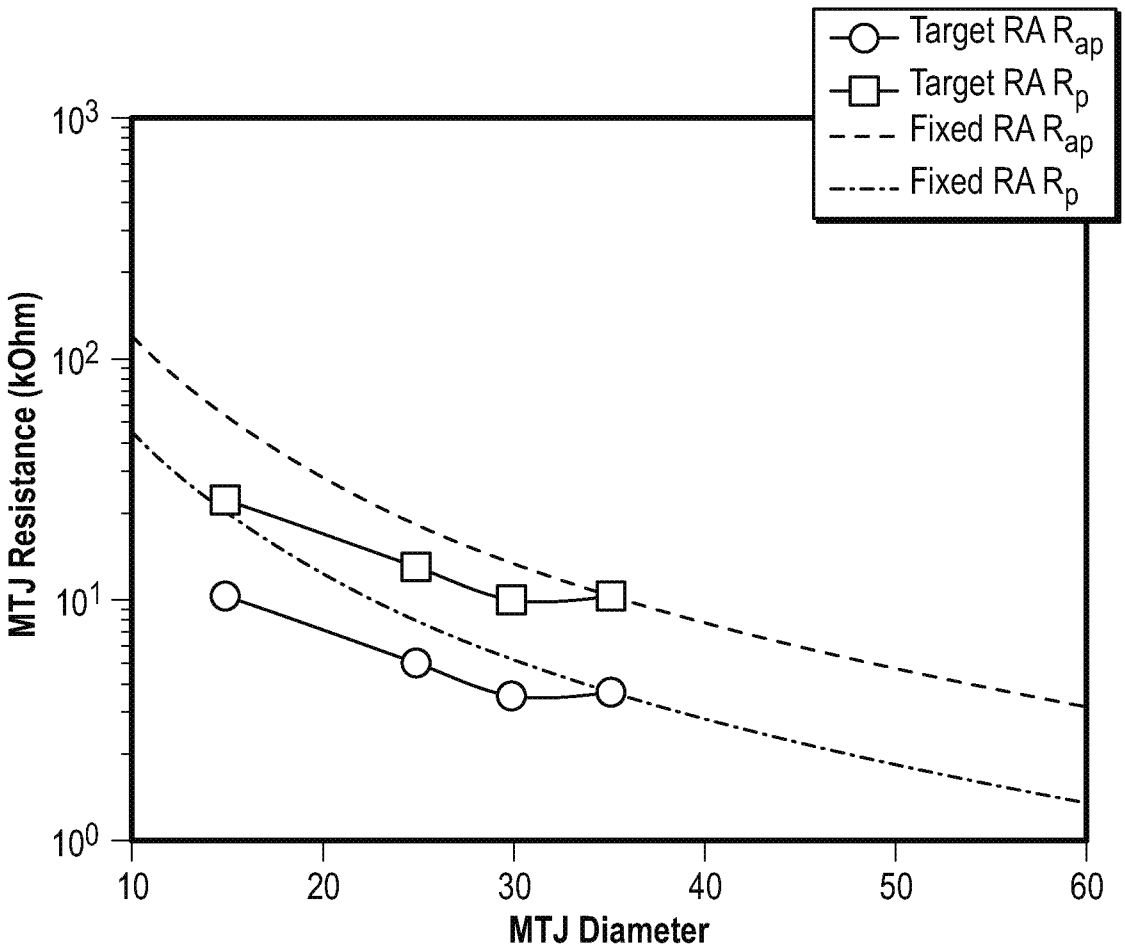

Target RA R_{ap}
Target RA R_p
Fixed RA R_{ap}
Fixed RA R_p
MTJ Resistance (kOhm)
10^3
10^2
10^1
10^0
10
20
30
40
50
60
MTJ Diameter

FIG. 5A

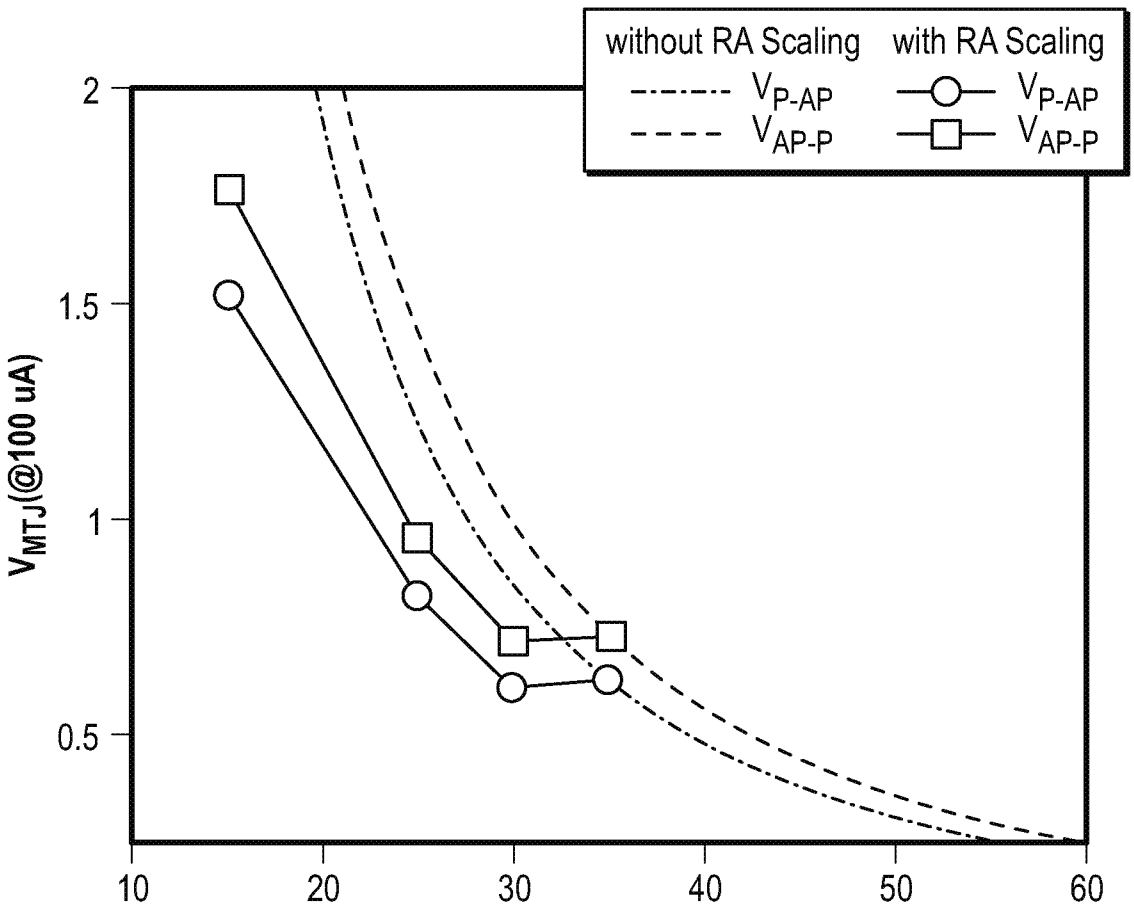

without RA Scaling
with RA Scaling
V_{P-AP}
V_{AP-P}
V_{P-AP}
V_{AP-P}
V_{MTJ}(@100 uA)
2
1.5
1
0.5
10
20
30
40
50
60

FIG. 5B

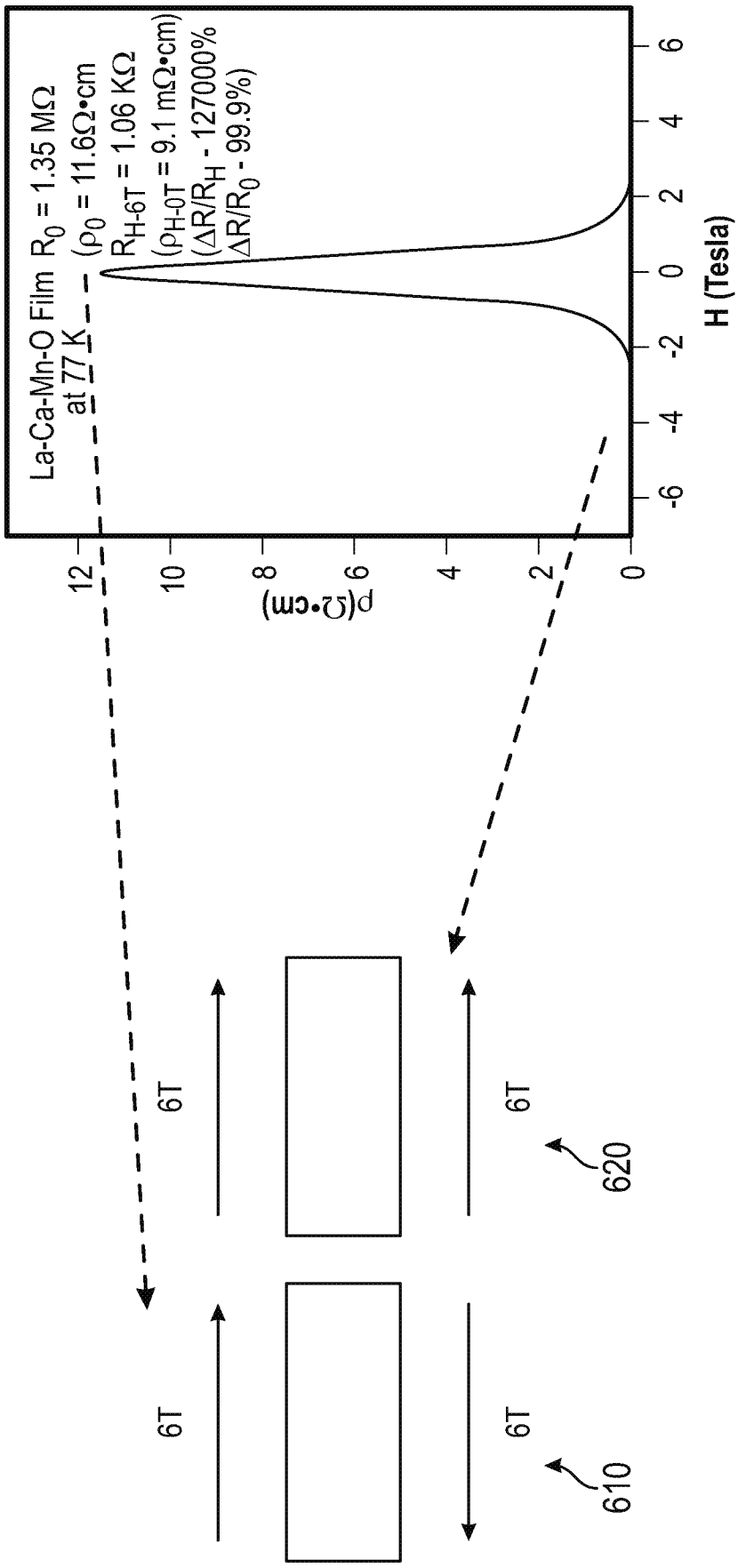

La-Ca-Mn-O Film R_0 = 1.35 MΩ
at 77 K (ρ_0 = 11.6Ω•cm
$R_{H\text{-}6T}$ = 1.06 KΩ
($\rho_{H\text{-}0T}$ = 9.1 mΩ•cm)
($\Delta R/R_H$ - 127000%
$\Delta R/R_0$ - 99.9%)
ρ(Ω•cm)
H (Tesla)
6T
6T
6T
6T
620
610

FIG. 6

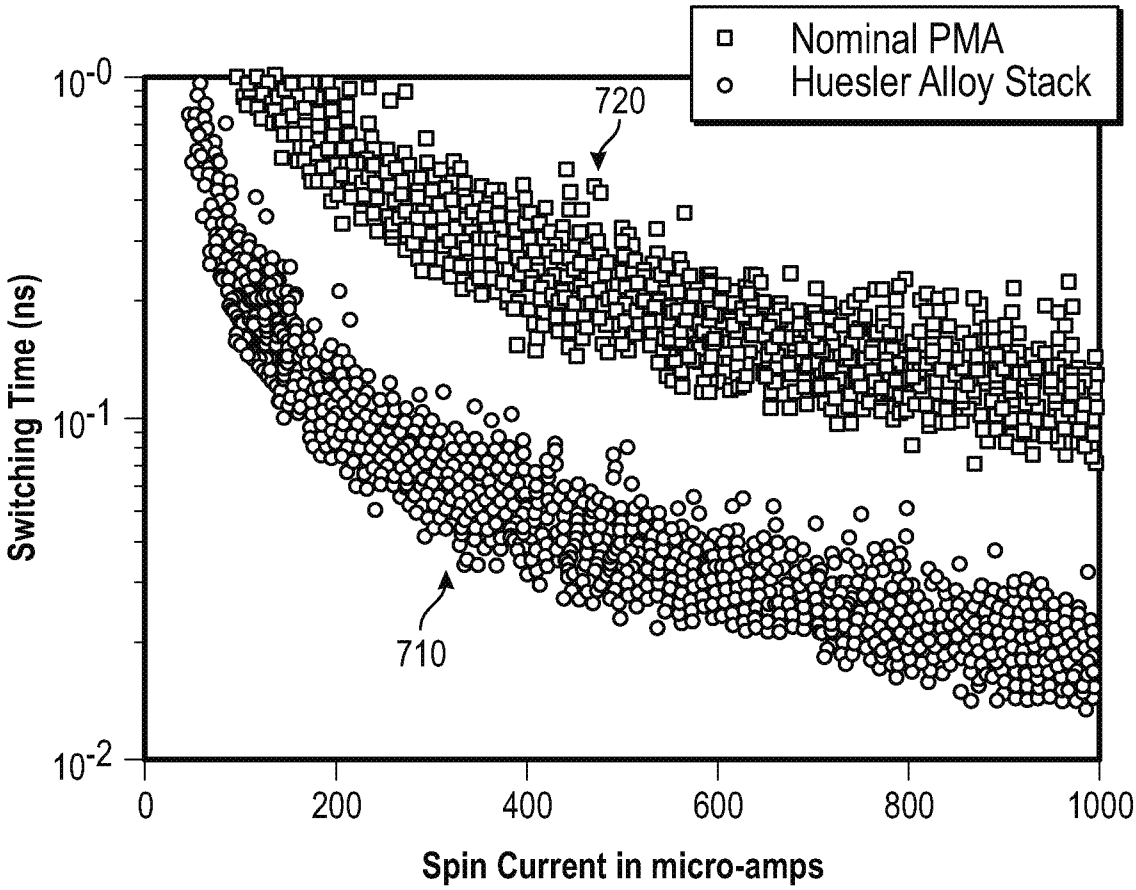

Nominal PMA
Huesler Alloy Stack
720
710
Switching Time (ns)
10-0
10-1
10-2
0
200
400
600
800
1000
Spin Current in micro-amps

FIG. 7

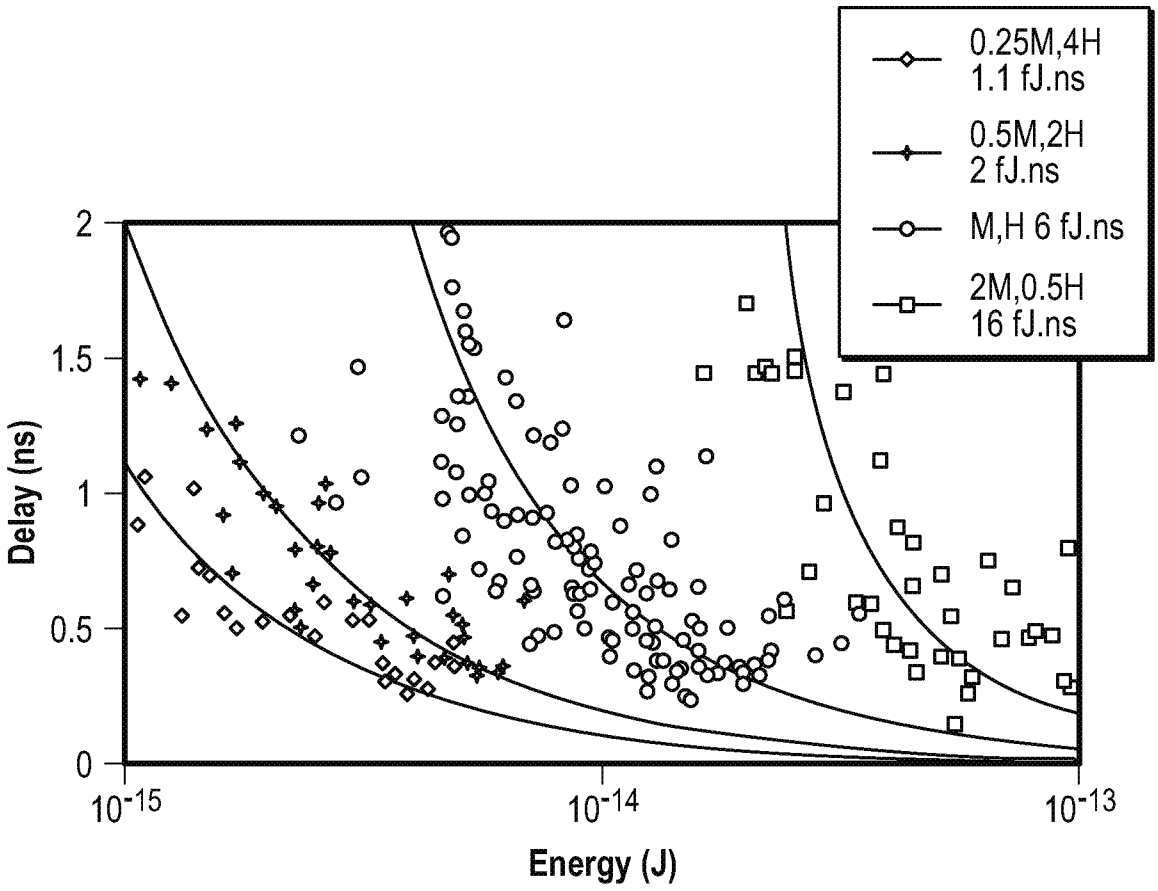

0.25M,4H
1.1 fJ.ns
0.5M,2H
2 fJ.ns
M,H 6 fJ.ns
2M,0.5H
16 fJ.ns
Delay (ns)
2
1.5
1
0.5
0
10-15
10-14
10-13
Energy (J)

FIG. 8

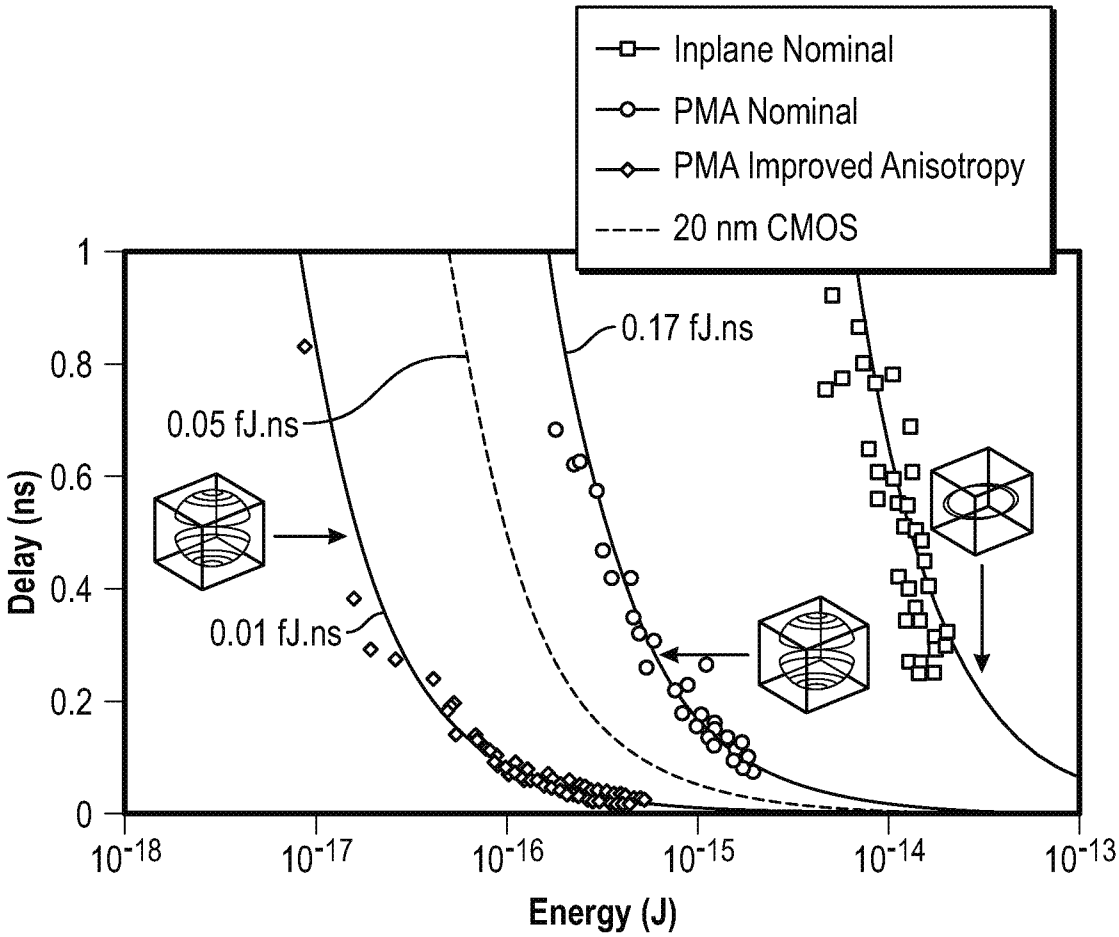

Inplane Nominal
PMA Nominal
PMA Improved Anisotropy
20 nm CMOS
0.17 fJ.ns
0.05 fJ.ns
0.01 fJ.ns
Delay (ns)
1
0.8
0.6
0.4
0.2
0
10-18
10-17
10-16
10-15
10-14
10-13
Energy (J)

FIG. 9

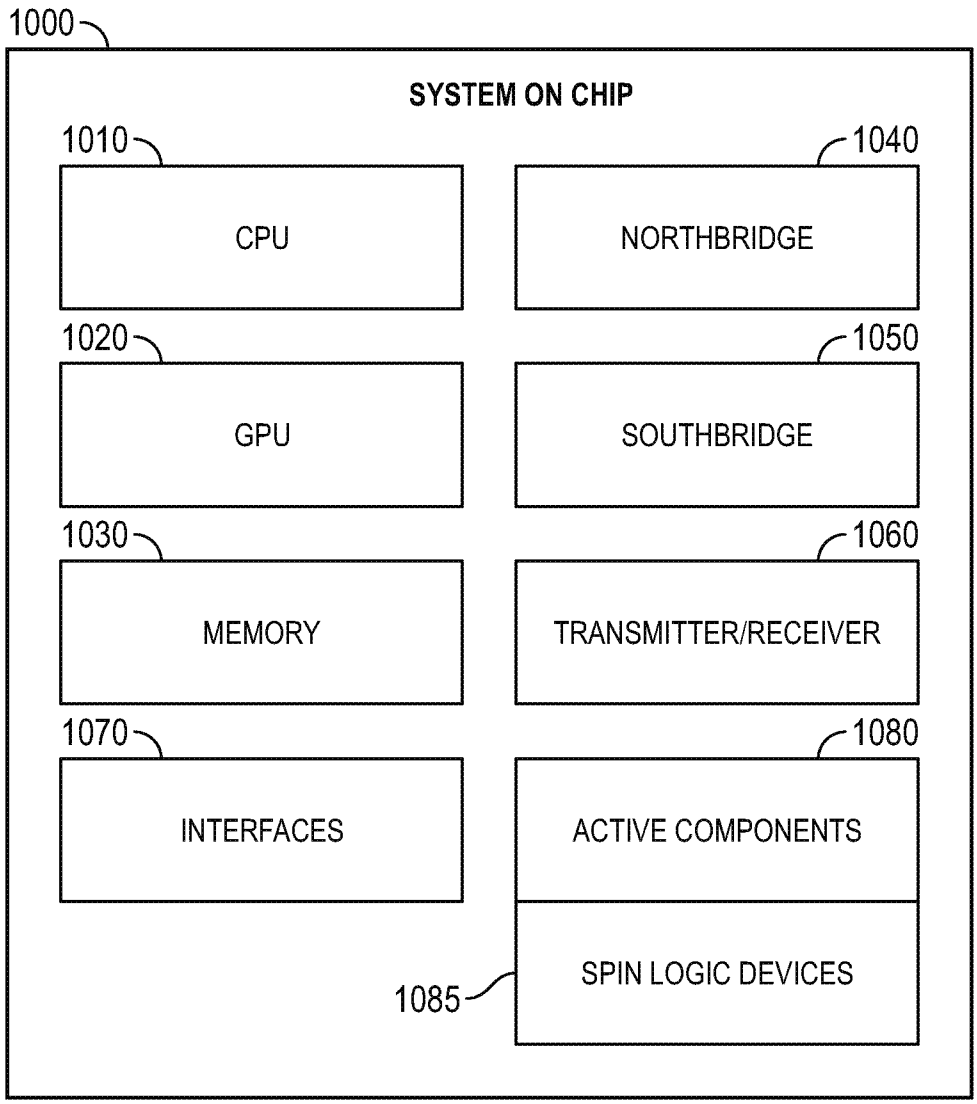

1000
SYSTEM ON CHIP
1010
CPU
1040
NORTHBRIDGE
1020
GPU
1050
SOUTHBRIDGE
1030
MEMORY
1060
TRANSMITTER/RECEIVER
1070
INTERFACES
1080
ACTIVE COMPONENTS
1085
SPIN LOGIC DEVICES

FIG. 10

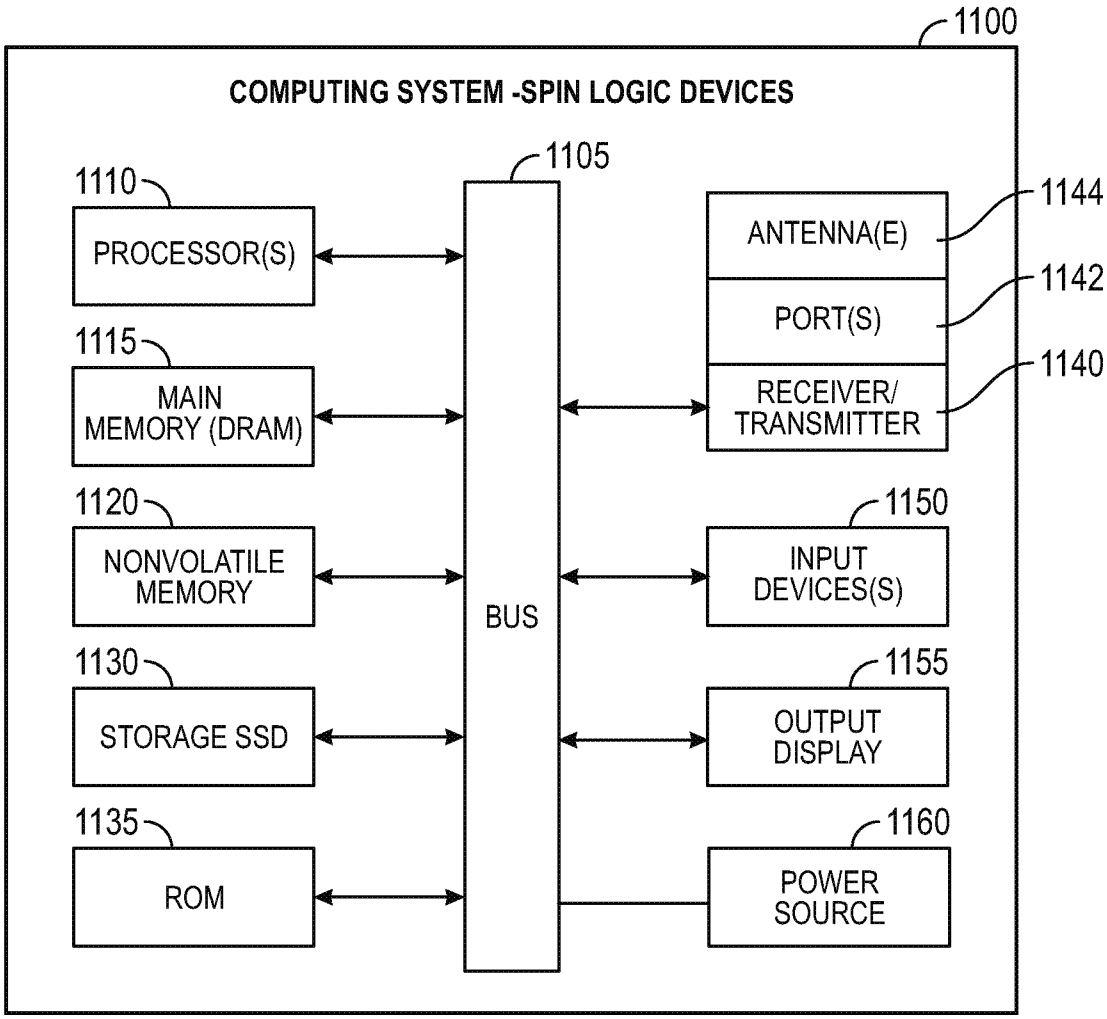
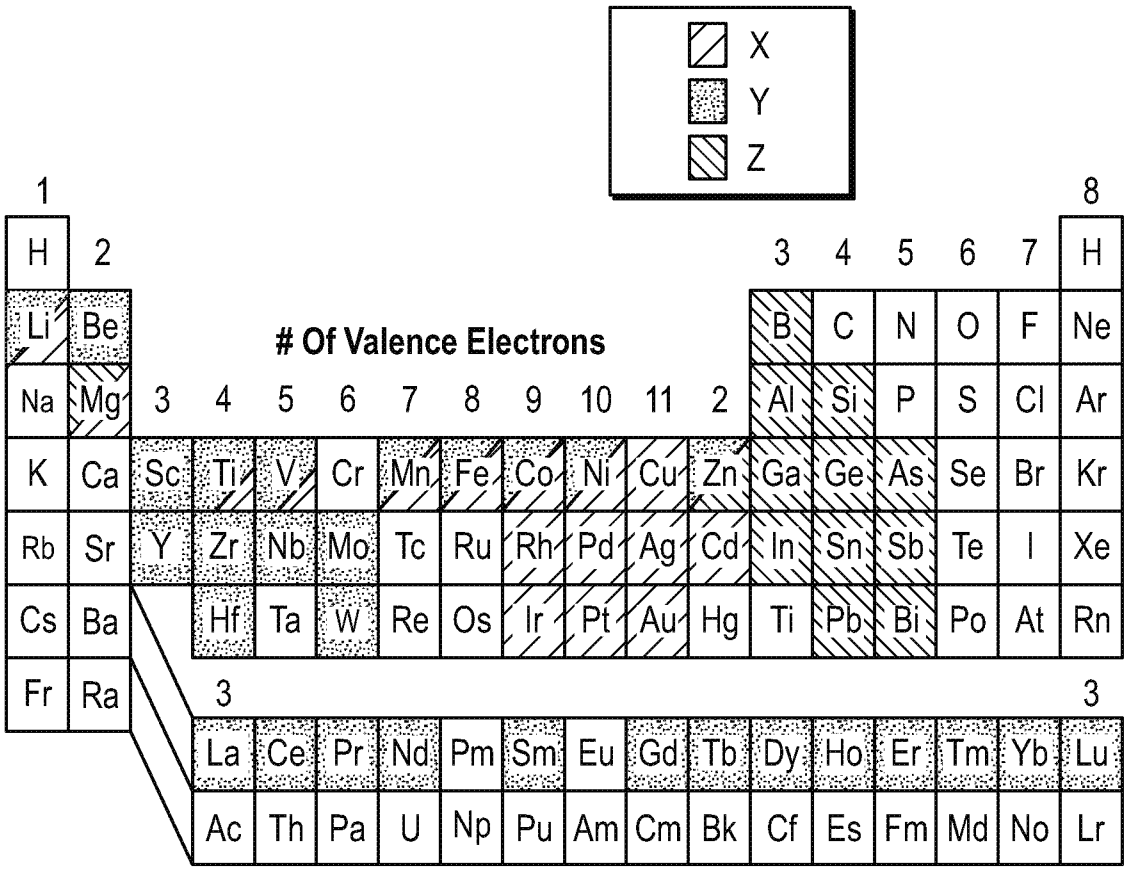

1100
COMPUTING SYSTEM -SPIN LOGIC DEVICES
1105
BUS
1110
PROCESSOR(S)
1115
MAIN MEMORY (DRAM)
1120
NONVOLATILE MEMORY
1130
STORAGE SSD
1135
ROM
1144
ANTENNA(E)
1142
PORT(S)
1140
RECEIVER/ TRANSMITTER
1150
INPUT DEVICES(S)
1155
OUTPUT DISPLAY
1160
POWER SOURCE

FIG. 11



Typical Elements for Half-Heusler XYZ and Full-Heulser Alloys X_2YZ:

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/038472

A. CLASSIFICATION OF SUBJECT MATTER

H01L 43/08(2006.01)i, H01L 43/02(2006.01)i, H01L 43/10(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 43/08; H01L 27/115; H01L 21/8246; G11C 11/16; H01L 27/105; H03K 19/16; G11C 11/00; H03K 17/80; H01L 43/02; H01L 43/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: magnetic tunnel junction, colossal magnetoresistance, giant magnetoresistance, spin channel, jahn-teller

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005-0195646 A1 (CHIAHUA HO et al.) 08 September 2005 See paragraphs [0008]-[0052], claim 1 and figures 7A-7B.	1-2,6-7,12,14,17
Y		3-5,8-11,13,15-16,19-23
A		18
Y	US 2015-0194963 A1 (SASIKANTH MANIPATRUNI et al.) 09 July 2015 See paragraphs [0036]-[0049], claim 1 and figure 10.	3-5,11,13,19-23
Y	US 2010-0244163 A1 (TADAOMI DAIBOU et al.) 30 September 2010 See paragraphs [0039]-[0043], [0060]-[0103], claim 1 and figure 2.	8-10,15-16
A	US 2016-0217842 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 28 July 2016 See paragraphs [0026]-[0028], claim 1 and figure 1A.	1-23
A	JP 2016-164944 A (BLUESPIN CO., LTD.) 08 September 2016 See paragraphs [0067]-[0078], claim 1 and figure 10.	1-23

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 February 2018 (20.02.2018)	**20 February 2018 (20.02.2018)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHIN, Sang Bum
Telephone No. +82-42-481-8398

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2017/038472

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005-0195646 A1	08/09/2005	US 7323732 B2	29/01/2008
US 2015-0194963 A1	09/07/2015	CN 104737318 A	24/06/2015
		CN 104737318 B	22/08/2017
		EP 2920827 A1	23/09/2015
		KR 10-1669800 B1	09/11/2016
		KR 10-2015-0055038 A	20/05/2015
		KR 10-2016-0127152 A	02/11/2016
		TW 2014-40434 A	16/10/2014
		TW 2016-31896 A	01/09/2016
		US 2014-0139265 A1	22/05/2014
		US 2015-0341036 A1	26/11/2015
		US 8988109 B2	24/03/2015
		US 9136848 B2	15/09/2015
		US 9379712 B2	28/06/2016
		WO 2014-078025 A1	22/05/2014
US 2010-0244163 A1	30/09/2010	JP 04745414 B2	10/08/2011
		JP 2010-238769 A	21/10/2010
		US 8686521 B2	01/04/2014
US 2016-0217842 A1	28/07/2016	CN 105826462 A	03/08/2016
		GB 2536768 A	28/09/2016
		US 9406365 B1	02/08/2016
JP 2016-164944 A	08/09/2016	CN 107210264 A	26/09/2017
		US 2016-0260771 A1	08/09/2016
		WO 2016-143157 A1	15/09/2016