Oct. 9, 1956 F. B. MAYNARD ET AL 2,766,376

ELECTRONIC ADDING TUBE FOR BINARY ADDITION SYSTEMS AND THE LIKE

Filed Aug. 24, 1955 2 Sheets-Sheet 1

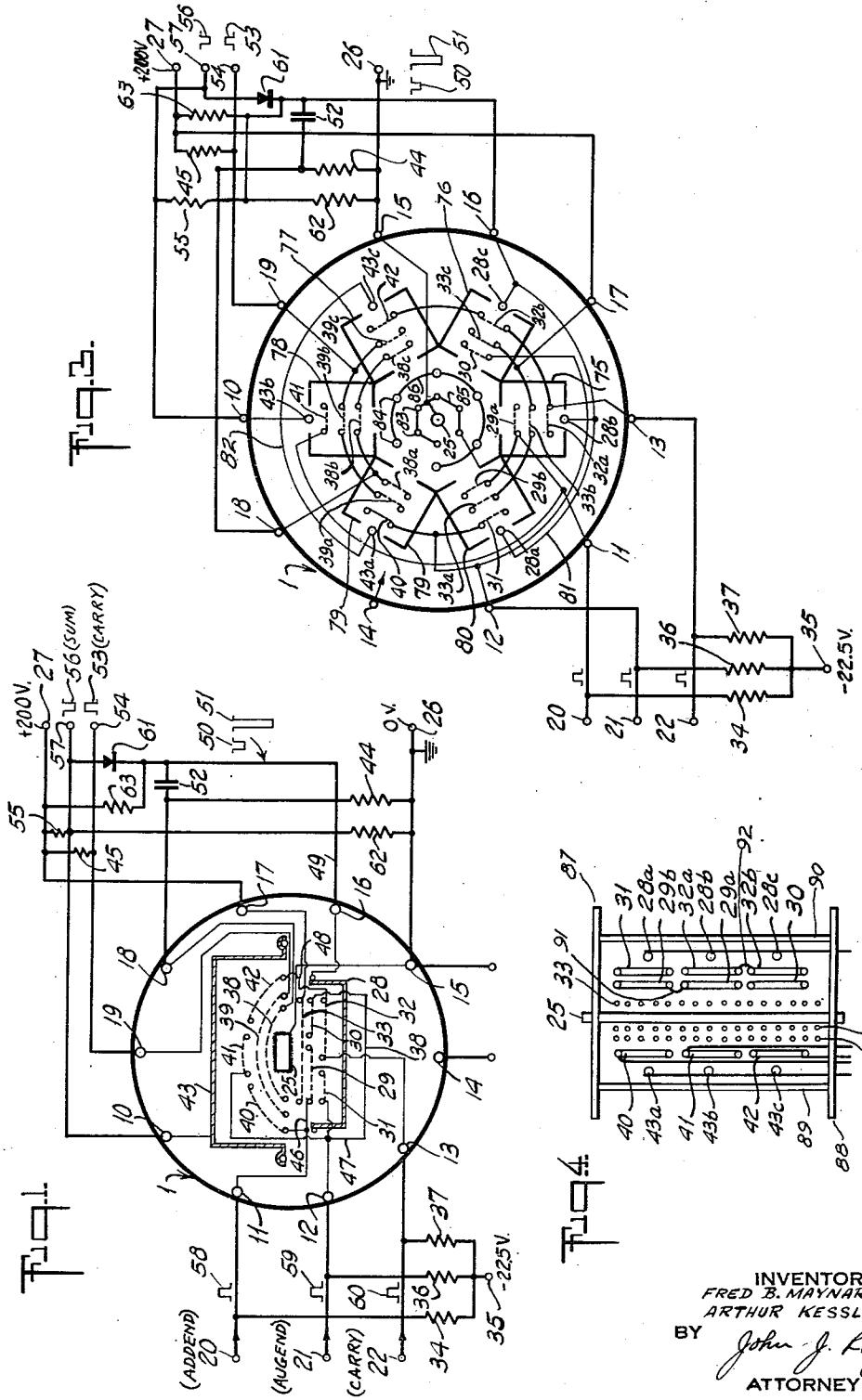

Fig. 1.

Fig. 4.

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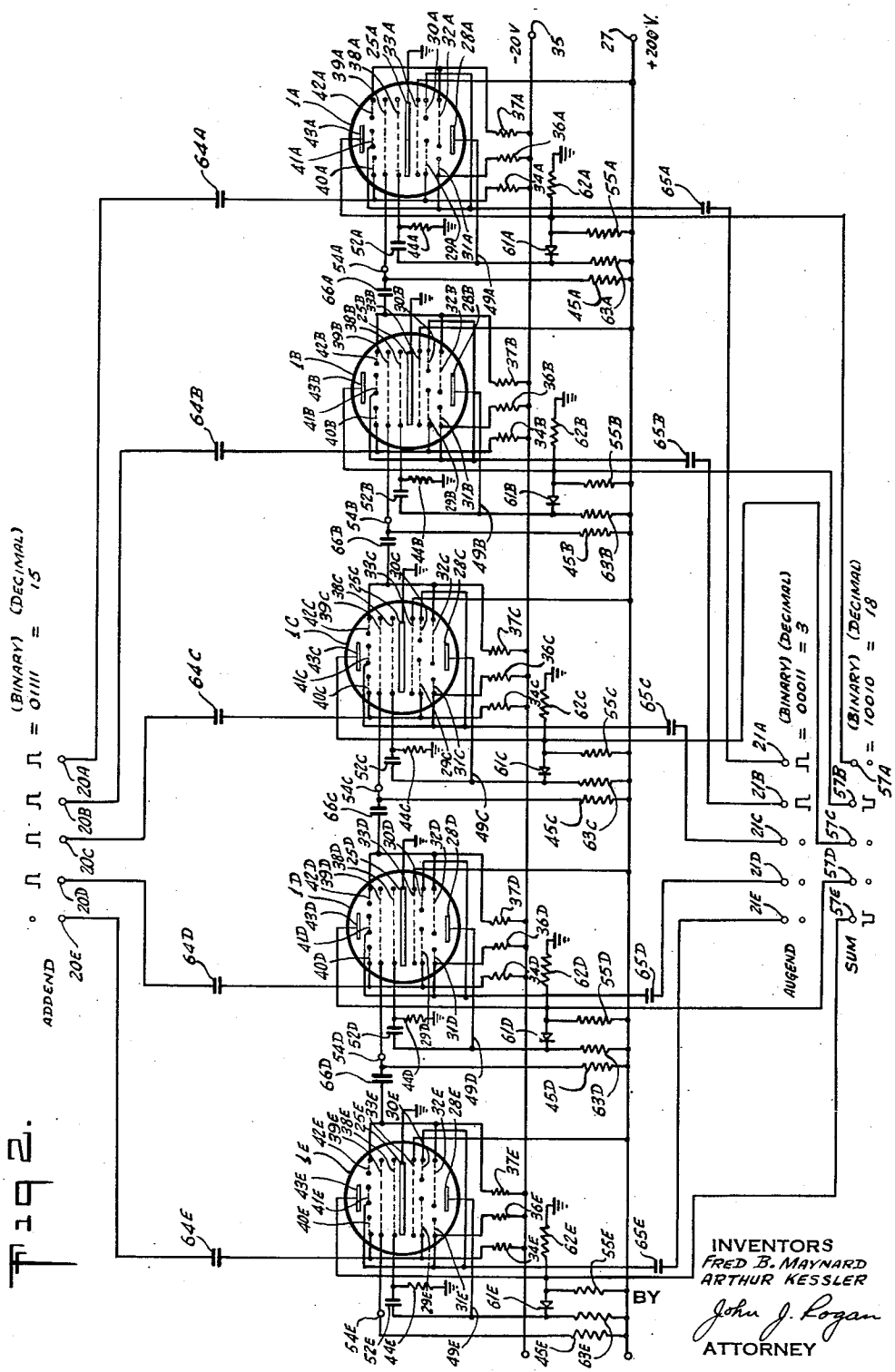

Fig. 2.

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ELECTRONIC ADDING TUBE FOR BINARY ADDITION SYSTEMS AND THE LIKE

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18 Claims. (Cl. 250—27)

This invention relates to electron tubes, and more especially it relates to novel multi-grid control tubes especially adapted for computation according to the binary code system.

A principal object of the invention is to provide a novel multi-grid tube of the variable gating kind, wherein the gating elements or grids are especially designed and arranged to produce output currents representing binary sum signals and binary carry signals corresponding to binary coded input signals to be added.

Another object is to provide a variable gating tube which is especially designed for carrying out the logical function of addition according to the binary addition system.

Another object is to provide novel variably controllable gating grid tubes where the sum and carry outputs derived from binary code input signals are generated by the tube and its output circuit directly from the said signals permitting the employment of a relatively simple output circuit.

A further object is to provide novel variable sectionalized gating grid tubes especially adapted for binary code adding systems either of the serial or parallel adding kind, and wherein there is produced a carry signal of such polarity, amplitude and pulse duration such that the said carry signal can be directly coupled from one stage to the next higher order stage in the case of parallel binary adding, or to the appropriate delay network in the case of serial binary adding.

A feature of the invention relates to a novel grid-controlled tube wherein a set of four grids are so arranged with respect to a common cathode and collector plate that collector currents of three different levels or magnitudes can be selectively produced in accordance with coded binary input signals representing binary addition input signals.

Another feature relates to a novel grid-controlled gating tube provided with two sections, one section comprising a series of gating grids which cooperate with a single output collector electrode to produce a stepped magnitude output signal, wherein one step represents binary sums without carry and another step represents a carry control signal. The second section of the tube includes another multi-grid grating arrangement which cooperates with the first section to produce in the output of the tube a special carry signal which can be fed directly to a similar tube in a series of such tubes for carrying out binary addition operations.

A further feature relates to a novel gating control multi-sectional electron tube having the grids of the various sections so interconnected that binary addition input signals applied to certain of the gating grids result in the selective production in the output of the tube of a signal representing a binary sum or a binary carry.

A further feature relates to an electron tube having a single electron emitting cathode which has mounted on opposite sides thereof two systems of gating control grids. One of the grid systems has the grids interconnected to

provide three different levels of electron collector current reaching a common collector electrode which levels correspond to input signals representing binary sums. The other grid section is also connected to the input signals and cooperates with the grids of the first set to produce selectively at the common output circuit of the tube a signal which represents either a binary sum or a binary carry condition.

A still further feature relates to an improved binary adding system employing tubes of the gated grid kind.

Other features and advantages not specifically enumerated will be apparent after a consideration of the following detailed description taken in conjunction with the attached drawings and the appended claims.

In the drawing,

Fig. 1 is a schematic diagram of an electron tube and associated circuits embodying principles of the invention;

Fig. 2 is a schematic wiring diagram of a binary adding system of the parallel adding kind employing a series of electron tubes according to the invention;

Fig. 3 is a schematic diagram of a modification of the tube of Fig. 1;

Fig. 4 is an elevational view of an electrode mount such as schematically shown in Fig. 1.

Referring to Fig. 1, the designation numeral **1** represents the evacuated enclosing bulb or envelope of an electron tube according to the invention and wherein the various electrodes are mounted. Such bulbs and means for supporting the electrodes therein are well known in the art and for simplicity in the drawing are omitted therefrom. Likewise, in order to simplify the explanation, the tube of Fig. 1 is shown as connected to a binary coded wire system having only three coded input wires. Accordingly, the tube as shown is provided with a series of ten lead-in wires or contact prongs numbered **10–19**, which may be sealed for example in a circular array through the base wall or header of the tube. The pins **11**, **12** and **13** represent binary code signal input connections which are connected respectively to the terminals **20**, **21**, **22** of any well known source of current impulses representing binary digits to be added. As is well known in the binary coded wire system, the absence of a pulse on any wire represents the binary digit 0. The positive or negative pulse represents the binary system digit 1. As is well known in the art of binary addition, binary coded numbers can be added to produce a binary sum, the binary numbers that are being added being referred to in the art as addend and augend. It becomes important, therefore, in such systems when combining addends and augends to derive in a common output circuit two voltage conditions, one representing the binary sum and the other representing a carry condition. In Fig. 1 the addend pulses can be applied to terminal **20**, the augend pulses to terminal **21**, and the carry pulses to terminal **22**. In accordance with one feature of the invention, when input pulses are applied simultaneously to the terminals **20**, **21**, **22**, a special large impulse is generated in the tube and its associated output circuit, which large impulse is referred to herein as the inhibitor signal, the purpose and function of which will be described hereinbelow.

The electrode system in the tube **1** comprises an electron emitting cathode **25** which is preferably of the well known indirectly heated kind, consisting for example of a tubular elongated metal sleeve, whose external surface is coated with electron emissive material. A suitable heater wire (not shown) is insulatingly supported within the sleeve to raise it to electron emitting temperature. The heater wire has its ends connected to pins **14**, **15**, and the cathode sleeve also is connected to pin **15**. The pin **15** is connected to the grounded or 0 voltage terminal **26** of any suitable direct current power

supply (not shown). A suitable high positive potential tap, for example 200 volts D. C., of the power supply is connected to terminal 27 for purposes to be described.

Located on one side of the cathode is a collector plate 28 which is adapted to receive electron emission from the adjacent side of cathode 25. In accordance with the invention, the quantity or number of electrons collected by plate 28 can be selectively made of three different levels or magnitudes under control of a series of gating control grids 29, 30, 31, 32 located between the cathode 25 and the collector 28. An additional accelerating grid 33 is located between the cathode 25 and grids 29, 30. The dimensional relations between the size of the cathode 25 and the various grids and plates cooperating therewith is essentially schematic in the showing of Fig. 1. However, the arrangement is such that when no binary pulses are applied to the terminals 20, 21, and 22, the electrons from the cathode 25 are completely gated off, that is, no substantial quantity reaches the collector 28. The grids 29 and 30 may be substantially coplanar, and the lateral electron passing width of the grid 29 is approximately twice the lateral electron passing width of the grid 30, so that when grid 29 alone is gated on, it permits approximately twice as much electron current to flow therethrough as compared with the amount of electron current through grid 30 when grid 30 alone is gated on. Similarly, grid 32, which may be coplanar with grid 31, when it is gated on, permits approximately twice the amount of electron current to reach the collector 28 as compared with the amount of electron current reaching that plate when grid 31 alone is gated on. The accelerator grid 33 is substantially coextensive with both grids 29, 30 and with grids 31, 32. It will be understood, of course, that while the showing of Fig. 1 is schematic, it is intended that the grids and the cathode are elongated in a direction perpendicular to the plane of the drawing.

The accelerator grid 33 is connected directly to the 200 volt terminal 27 of the power supply. However, even with this positive bias on the accelerator grid, it does not permit current to flow to the collector 28 from the cathode 25 unless two or more of the gating grids are supplied with positive binary pulses. The grid 29 is connected to pin 11 and thence through a biasing resistor 34 to a direct current supply terminal 35, for example of negative 22.5 volts so that the grid 29 is normally, that is in the absence of positive binary pulses impressed thereon, gated off. The gating grid 31 is connected to pin 12 and thence through a biasing resistor 36 to the negative terminal 35, likewise biasing grid 31 to gating off condition in the absence of positive binary pulses impressed thereon. Similarly, the gating grid 32 is connected to pin 13 and through resistor 37 to the negative biasing terminal 35 to bias grid 32 to gating off condition in the absence of positive binary pulses at terminal 22. It should be observed that the gating grid 30 is connected by a wire 38 to the grid 31 and also to pin 12, the purpose of which connection will be described hereinbelow.

From the foregoing it will be seen that if a positive binary coded pulse is applied to terminal 20 alone, substantially no electron current is collected by the plate 28. If binary pulses, such as addend and augend pulses, are simultaneously applied respectively to terminals 20, 21, electron current will reach the collector 28, the amount of this electron current being determined by the actual angular control width of the gating grid 31. The amount of electron current reaching the collector 28, being determined by the grid 31, will be approximately one-third the total possible electron current from the cathode 25 to the collector 28. In other words, the collector 28 can receive electrons from the cathode to produce a signal only when two input terminals are simultaneously energized by positive pulses, and even then only one-third of the maximum electron current is collected. If positive pulses are applied simultaneously to terminals 20, 21 and 22, the amount of current collected by electrode 28 will be approximately three times that obtainable when only two input terminals are positively energized. In other words, there are three possible signal states at the collector 28, namely zero current, maximum current, and approximately one-third maximum current.

Also associated with cathode 25, but on the opposite side from grids 29—32, is a second grid system including grids 38—42. Cooperating with these latter grids is another collector plate 43. Grid 38 is referred to herein as the inhibitor grid and when biased to plate current flow permits the maximum of electron emission to reach the collector 43 from the side of the cathode facing that collector. Grid 38 is connected to pin 18 and through resistor 44 to the zero voltage terminal 26, thus normally biasing grid 38 to plate current cut-off. The next grid 39, which is substantially angularly coextensive with grid 38, serves a dual purpose and thereby constitutes one of the novel features of this invention. Grid 39 is connected to pin 19 and thence through load resistor 45 to the positive 200 volt direct current terminal 27. Grid 39 serves as an accelerator grid and as a screen grid between cathode 25 and the three equi-angular grids 40, 41 and 42. Grid 40 is connected directly to input terminal 20; grid 41 to input terminal 21; grid 42 to input terminal 22. In order to reduce the number of contact pins, these latter connections can be made by connecting grid 40 through a short metal strap 46 to grid 29; also by connecting grid 41 by a short metal strap 47 to grid 30; and grid 42 by short metal strap 48 to grid 32.

As pointed out hereinabove, the grid system 29—32 forms a so-called dual coincidence gating section between the cathode 25 and collector 28. Thus, if one grid, for example grid 29, is opened, that is biased to plate current flow, the electrons from the cathode are stopped by grids 31 and 32 and the collector 28 does not receive any electrons from the cathode. A signal is produced at collector 28 and on conductor 49, therefore, only when two input terminals, for example terminals 20 and 21, are simultaneously energized by respective positive pulses. However, even under that condition, only about one-third of the electron transit volume from the side of the cathode facing collector 28 is open which, therefore, results in the application of a negative pulse 50 to the conductor 49. If at the same time that positive pulses are applied to terminals 20, 21, a positive pulse is also applied to terminal 22, then there is produced at the collector plate 28 and on the conductor 49 a negative pulse 51 of approximately three times the amplitude of pulse 50.

When either of the negative pulses 50, 51 is present on conductor 49, it is fed across capacitor 52 to the inhibitor grid 38 which causes that grid to be driven to plate current cut-off. This cut-off action causes substantially all electron flow to cease to grid 39 and that grid 39 therefore swings to a strong positive potential as indicated by the pulse 53 at the carry terminal 54. This positive carry pulse 53 results from the fact that the current flow through the load resistor 45, which is connected to grid 39, is stopped, and terminal 54, therefore, swings up to the 200 volt potential of terminal 27. Summarizing the above, a carry signal 53 is produced only when any two or all of the input terminals 20, 21, 22 are simultaneously energized, but not if only one such terminal is energized. Also, the large negative pulse 51 is produced only when the three input terminals 20, 21, 22 are simultaneously energized by positive pulses. The function of the large negative signal pulse 51 will be described hereinbelow.

Considering in further detail the grid system constituted of grids 38 to 42, since grids 40, 41 and 42 are normally at cut-off, no electrons reach collector 43, but since grids 38 and 39 are both normally at non-cut-off, electrons are always ready to flow in the space between grid 39 and the grids 40, 41 and 42. When a positive input pulse at any

input terminal occurs, for example at terminal 20, electrons can flow from cathode 25 through grids 38, 39 and 40 to the collector 43, producing through load resistor 35 a negative pulse 56 which appears on the sum terminal 57. If input terminals 20 and 21 are simultaneously energized by respective positive pulses, electrons can start to flow through grids 40 and 41. However, since the action above described, resulting from any double coincidence input pulses, causes the generation of a negative pulse 50 on conductor 49 and, therefore, on grid 48, the supply of electrons to collector 43 is cut off. Therefore, essentially the sum signal 56 appears at terminal 57 only, when only one of the input terminals is energized.

The tube above described is, therefore, capable of carrying out the well known logical operations of binary addition. As is well known, binary numbers are represented in each digital place by either a 0 or a 1, and never by anything else. The addition of two binary numbers requires, for each digital place, except the first, the adding of three signals, two of which are known as the addend and augend respectively, and the third being a carry signal from the next lower order place. In actual use, the input signals may be positive pulses 58, 59, 60, for example of 20 volts amplitude. Since the input grids 29, 30, 31 are normally biased to plate current cut-off, for example minus 20 volts, these positive input pulses will open their respective grids. In some cases it may be advantageous to have the input pulses larger or more positive-going than the applied negative bias, so that the respective grids are driven somewhat positive.

As stated above, one of the novel features of the present invention is the derivation of the carry pulse 53. It should be observed that this carry pulse is positive and can be made precisely like the addend and augend input pulses. Thus, the carry pulse can be made of such polarity and amplitude that it can be fed directly into one of the inputs of the next higher order tube similar to the tube of Fig. 1, without the use of any intermediate components. The section of the tube represented by elements 25, 38 and 39 can be designed as an amplifying triode so that the carry signal does not degenerate but is rather amplified at every successive position. Since, with respect to grids 40, 41 and 42, grid 39 constitutes a virtual cathode by space charge action, when one of the grids 40, 41, 42 is opened, the space charge flows away from the grid 39 which may cause grid 39 to go slightly positive. However, this effect can be kept so small as to be substantially negligible.

With a double coincidence, however, for example with positive pulses simultaneously on grids 40, 41, the space charge flow away from grid 49 causes it to go substantially positive at once. Since the same action causes the generation of an inhibitor pulse 50 on conductor 49, causing grid 38 to swing negatively, grid 39 will go positive to its full extent. However, the pulse generated on conductor 49 will not arrive at grid 38 instantaneously, but is delayed slightly because of charging capacitances and other effects. The immediate positive swing of grid 39, resulting from the opening of grids 40, 41, causes a substantial positive migration of the potential of grid 39 ahead of the inhibitor pulse. This results in a substantially faster rise time for the carry pulse 53. This is a great advantage in a binary parallel adder such as is disclosed in Fig. 2, since the carry pulse must in some additions travel laterally in all tubes to give the required sum and any lateness of the carry pulses tends to degenerate substantially the sum outputs.

The foregoing description of the operation of Fig. 1 has been completely applicable to the logic of binary addition with respect to sum and carry outputs except where the binary addition requires the production of a sum and carry signal simultaneously. In other words, the triple coincidence of input pulses on the terminals 20, 21, 22. As described above, the carry signal is produced by the inhibitor pulse 50 which cuts off grid 38. This, however, makes it impossible to produce a sum output at terminal 57. However, the large negative pulse 51 produced on conductor 49 by this same action is derived on the sum output terminal 57 by the action of a diode 61 and the voltage divider constituted of resistors 55 and 62. The potential on collector 43 is maintained at, for example, 20 volts less than that of the 200 volt terminal 27, by means of the voltage divider 55, 62. The collector 28 is meanwhile held at the full 200 volt potential by resistor 63. This places diode 61 in a non-conductive condition unless the potential of collector 28 is reduced to less than 180 volts. Thus, if the double coincidence inhibitor pulse 50 is, for example, minus 20 volts, it will not appear on the sum output terminal 57 being blocked by the diode 61. In the case of triple coincidence on the terminals 20, 21, 22, the negative voltage pulse 51 under the above assumptions is approximately minus 60 volts, and it overrides the blocking action of the diode 61, thus placing a negative 40 volt pulse 56 on the sum output terminal 57, which is the desired result. In order to clarify the operation of the arrangement shown in Fig. 1, the following table sets forth the various conditions above described in tubular form.

Summary of logic for binary addition

0 represents no signal, and the binary digit 0.
+ represents positive pulse and the binary digit 1.
— represents negative pulse and the binary digit 1, or an inhibitor signal.

Input Positions			Intermediate Outputs			Final Outputs	
G_A	G_B	G_C	19	10	16	Sum	Carry
0	0	0	0	0	0	0	0
+	0	0	0	—	0	—	0
0	+	0	0	—	0	—	0
0	0	+	0	—	0	—	0
+	+	0	+	0	—	0	+
0	+	+	+	0	—	0	+
+	0	+	+	0	—	0	+
+	+	+	+	0	— * (Inhibitor)	—	+

*The large pulse (51) is developed at this point.

It will be understood that the showing of the tube in Fig. 1 is essentially schematic and that various structural modifications may be made in the electrode conformation and locations to achieve the desired binary controls. Some of these modifications are illustrated in Figs. 3 and 4 of the drawing and will be described hereinbelow. Thus, the cathode 25 may be centrally located or even two cathodes may be used with the two grid systems (29—32; and 38—42) cooperating respectively with the top and bottom halves of the cathode, in which event the grids and plates may be full grids and plates surrounding their respective operations of the cathode instead of half grids and plates as shown in Fig. 1. Furthermore, the grids may be planar, that is straight instead of curved, and the multiple grid sections may be arranged in a variety of ways.

Referring to Fig. 2, there is shown in schematic form a binary adding system of the parallel adding kind. Merely for illustration, the system is shown as employing five binary input channels each including a respective tube 1A–1E, each of which may be identical with the tube 1 of Fig. 1. The input and output circuits of each of the tubes of Fig. 2 are also identical with the input and output circuits of the tube of Fig. 1. Merely for convenience, the elements of Fig. 2, which are functionally the same as those of Fig. 1, carry the same designation numerals with the appropriate letter suffix. Since the connections from each addend input terminal and from each augend input terminal and the connections to the sum output terminals and carry terminals of the tubes are alike, a detailed description is only necessary for one tube in the set, for example tube 1A. For purposes of explanation, it will be assumed that the decimal digit 15, which is the addend, is to be added to the decimal digit 3, which is the augend. Under that assump-

tion, the binary code for the addend digit is represented by the presence of simultaneous pulses on the terminals 20A–20D and with no pulse on terminal 20E. The augend is represented by a positive pulse on terminals 21A and 21B and no pulse on 21C, 21D, and 21E. Since there is no carry signal at the input to the first tube 1A, the grid 32A is biased to plate current cut-off through resistor 37A. It will be observed that the input addend pulse at terminal 20A is applied to the grids 29A and 40A through a suitable condenser 64A. Likewise, the augend pulse at terminal 21A is applied through condenser 65A to grids 31A, 30A, and 41A. As a result of this double pulse coincidence, the positive carry pulse alone is produced at terminal 54A, but no sum pulse is produced at terminal 57A for the reasons described above in connection with Fig. 1.

This carry pulse at terminal 54A is applied through condenser 66A to the grids 42B and 33B of tube 1B. Since, under the above assumptions, there are also present addend and augend pulses at tube 1B by reason of the pulses at terminals 20B and 21B, there is therefore a triple coincidence at tube 1B. Therefore, the large amplitude negative pulse corresponding to pulse 51 (Fig. 1) appears on conductor 49B, and by reason of the above described action of the diode 61B, there is produced a sum pulse at the terminal 57B. Of course, at the same time there is produced a positive carry pulse at terminal 54B which is applied through condenser 66B to the corresponding grids of the next tube 1C. Similarly, since there are only two coincidence pulses on tube 1B because of the absence of an augend pulse, only a positive carry pulse is produced at the output of tube 1C which is applied through condenser 66C to tube 1D. For similar reasons there is applied to the input of tube 1E only a carry pulse since no augend pulse is applied at terminal 21D. Tube 1E will now receive at its input only the carry pulse from tube 1D, and by reason of the absence of addend and augend pulses at tube 1E, only a single negative sum pulse appears at terminal 57E. Thus, there are produced simultaneous pulses only on terminals 57B and 57E which, therefore, represent the decimal sum 18. It will be understood, of course, that the system may employ any number of input wires and corresponding coded binary pulses, depending on the magnitude of the decimal digits to be added.

Fig. 3 shows a modification of the tube which is schematically shown in Fig. 1. The parts of Fig. 3 which perform the same functions as those of Fig. 1 bear the same designation numerals. Thus, the enclosing bulb or tube 1 has a central emitting cathode 25. Cathode 25 is symmetrically surrounded by six field-free enclosures designated 75–80, each consisting of a substantially box-like metal compartment, each compartment having parallel side walls and having front and rear walls. Each front and rear wall has a respective opening in radial alignment with the cathode 25. Located centrally with respect to each rear opening is a corresponding rod-like anode or electron collector, designated respectively 28*a*, 28*b*, 28*c*, and 43*a*, 43*b*, 43*c*. Collectors 28*a*, 28*b*, 28*c* are interconnected by a jumper wire 81 so that they function exactly the same as the collector electrode 28 of Fig. 1. Likewise, the collector rods 43*a*, 43*b*, 43*c* are interconnected by a jumper wire 82 so that they function exactly the same as the collector electrode 43 of Fig. 1. Preferably, the electrons from the cathode 25 are formed into six radial beams, each arranged to pass into the corresponding one of the six compartments 75–80. For this purpose cathode 25 may be surrounded by two sets of radially aligned metal rods 83, 84. The set of six rods 83 are interconnected by respective jumper wires 85. Likewise, the set of rods 84 are connected by jumper wires 86.

Located within each of the compartments 75–80 is a set of three grids. These grids are interconnected by respective jumper wires as shown, so that they function exactly the same as the corresponding grids 29, 30, 31, 32, 33, and 38, 39, 40, 41, 42 of Fig. 1. In order to simplify the explanation, the corresponding grids in Figs. 1 and 3 have the same designation numerals, but in Fig. 3 the numerals have appropriate letter suffixes. Thus, grids 29*a*, 29*b*, are directly connected to constitute the full equivalent of grid 29 (Fig. 1) and are connected to input terminal 11. The grid 30, which is identical with the corresponding grid 30 of Fig. 1, is connected to grids 31 and 40, which also are identical with the corresponding grids 31 and 40 of Fig. 1, and these three interconnected grids are connected to terminal 12. Grids 33*a*, 33*b*, 33*c*, are connected together and, therefore, function the same as grid 33 of Fig. 1, and are connected to the corresponding terminal 13. Grids 38*a*, 38*b*, 38*c* are connected together and function the same as grid 38 of Fig. 1 and are connected to terminal 18. Likewise, grids 38*a*, 38*b*, 38*c* are connected together and function the same as grid 39 of Fig. 1 and are connected to terminal 19.

The external circuit elements of Fig. 3 and their connection to the respective tube terminals 10—19 are identical with those of Fig. 1. It is believed, therefore, that the operation of the tube of Fig. 3 will be clear from the foregoing explanation of Fig. 1.

Fig. 4 shows a still further modification of the electrode arrangement schematically shown in Fig. 1. In this arrangement the cathode and the various grids and collector electrodes are supported in any suitable manner between a pair of mica insulator discs 87, 88 which may be held in spaced relation by suitable side rods 89, 90. If desired, the rods 89, 90 may be replaced by rectangular metal sheets which may act as baffles to prevent stray electrons from reaching the collectors. Since the various electrodes of Fig. 4 function in exactly the same manner as the corresponding electrodes of Fig. 1, they bear the same designation numerals. However, it should be observed that the collector electrode 28 of Fig. 1 is replaced by three separate rod-like collectors 28*a*, 28*b*, 28*c*, which are interconnected by a jumper wire to constitute in effect a single collector. Likewise, the collector electrode 43 is constituted of three separate rod-like collectors 43*a*, 43*b*, 43*c*, which are interconnected by a jumper wire to constitute in effect a single collector similar to collector 43. Located on one side of the cathode 25 is the grid 33, while located on the opposite side of the cathode are the separate grids 38, 39. These grids 33, 38, and 39 may be constituted each of a planar grid construction, whose plane extends substantially perpendicular to the sheet of drawings.

Instead of making the grids 29, 30, 31, 32 of different arcuate length, each of these grids may be made of identical construction consisting of well known side rod supports around which are wound fine wire grid turns. The side rods for these respective grids extend perpendicular to the plane of the sheet of drawings. In order to accomplish the three different magnitudes for the collector currents above mentioned, grid 29*a* is connected to grid 29*b* by a short jumper wire 91, thus in effect constituting a grid which has twice the width of the grid 30, insofar as permitting passage of electrons from the cathode to the collectors 28*a*, 28*b*, 28*c*, is concerned. Likewise, the grids 32*a*, 32*b* are connected by a short jumper wire 92, thus in effect constituting grids 32*a*, 32*b* a single grid having substantially twice the electron passage control as the associated grid 31. It is believed, therefore, that the manner of operation of the electrode system of Fig. 4 will be clear from the foregoing description of Fig. 1. Merely for clarity in the drawing, the enclosing bulb 1 for the electrode mount is omitted in Fig. 4.

Various changes and modifications may be made in the disclosed embodiments without departing from the spirit and scope of the invention. While Fig. 2 shows a tube according to the invention as embodied in a binary adding system of the parallel adding kind, it will be obvious to

those familiar with the binary adding art that the tubes can be equally well used in a binary adding system of the well known serial adding kind.

What is claimed is:

1. Electron tube apparatus, comprising an evacuated bulb containing two discrete electrode systems; the first system including an electron emitter, an electron collector, a first pair of gating grid means, a second pair of gating grid means, said second pair being located between the first pair and said first collector, the grid means of the first pair being of respectively different electron gating area, the grid means of the second pair also being of respectively different electron gating area, lead-in means for all said grids for applying respective gating voltages thereto and thereby selectively gating three distinct magnitudes of electron current to said collector electrode; the second electrode system including an electron emitter, an electron collector, and an inhibitor grid; and means interconnecting said inhibitor grid to said first collector to gate off electron emission to said second collector when the first collector receives the highest magnitude of said three electron magnitudes.

2. Electron tube apparatus according to claim 1, in which one of the grid means of each of said pairs has approximately twice the effective gating area as the other grid means of its pair.

3. Electron tube apparatus according to claim 2, in which one of the grid means of each of said pairs has approximately twice the effective gating area of the other grid means of its pair and the larger gating area grid of each pair overlaps the smaller gating area grid of the other pair of a portion of the larger gating area of said other pair.

4. Electron tube apparatus, comprising an evacuated bulb containing two discrete electrode systems; one system including an electron emitter, electron collector means and a plurality of gating control grid means between the emitter and collector, said grid means being arranged in successive sets between the emitter and collector with the grid means in each set having different electron gating areas, whereby said collector means receives three different magnitudes of electron flow in accordance with respective gating voltages applied to said grid means; the second system also including an electron emitter, a collector, and an inhibitor grid between the emitter and collector; and means connecting the first collector to said inhibitor grid to gate off the second collector when the highest one of said three magnitudes of electron flow reaches said first collector.

5. An electron tube especially designed for binary addition systems, having a set of three input terminals to be energized respectively by addend, augend, and carry pulses, a pair of binary addition output terminals one of which is a binary sum terminal and the other a binary carry terminal, an electron emitting cathode, a pair of discrete electrode systems cooperating with said cathode each system including electron collector means to receive emission from said cathode, respective gating control grid systems between the cathode and each collector, each grid system including a plurality of gating control grids, means connecting the gating control grids of each system and said collector electrodes to said input and output terminals to cause the sum pulse to be produced at said sum terminal when augend and addend pulses are applied to said augend and addend input terminals and for simultaneously applying a carry pulse to said carry output terminal when augend, addend, and carry pulses are applied simultaneously to said three input terminals.

6. An electron tube according to claim 5, in which the gating control grid system between the cathode and first collector includes two grid areas each area located successively between the cathode and the first collector and each area including a pair of grids one of which has a larger gating area than the other grid of the pair, and means connecting the said grid areas to said augend, addend, and carry input terminals whereby the first collector receives three distinct magnitudes of electron current in accordance with the application of gating pulses to one, two, or all three of said input terminals.

7. An electron tube according to claim 6, in which the gating control grid system between the cathode and second collector includes in succession an inhibtor grid and three substantially equal area gating grids, means connecting said three equal area gating grids respectively to said addend, augend, and carry input terminals, and means connecting said inhibitor grid to the first collector to develop a positive carry pulse at said carry output terminal when said first collector receives the highest of said three magnitudes of electron current.

8. Electron tube apparatus especially designed for binary addition, comprising an electron emitter, discrete electron collector means cooperating with said emitter, a first gating control grid system located between the emitter and the first collector, a second gating control grid system located between the emitter and the second collector, the first system including a first set of substantially coplanar grids to provide two separate gating controls of respectively different areas, said first system also including a second set of substantially coplanar grids also providing two separate gating openings of respectively different areas, the gating openings of the two sets overlapping whereby the first collector receives three different magnitudes of electron current in accordance with the particular combination of grids in said first set which are energized by addend, augend, or carry input pulses.

9. Electron tube apparatus according to claim 8, in which the said second gating control grid system between the emitter and the second collector includes a set of three gating grids of substantially equal gating area, an inhibitor grid located between the said three grids and the emitter; and an additional grid located between said inhibitor grid and said three gating grids, said inhibtor grid being interconnected with the first collector to gate off said second collector and thereby to develop at said additional grid a positive carry pulse when the said first collector receives the highest of said three electron magnitudes.

10. Electron tube apparatus according to claim 9, in which said additional grid is connected to a positive direct current terminal through a load resistor across which said positive pulse is developed, and said inhibitor grid is coupled to the first collector and also to said load resistor through a normally non-conductive rectifier and circuit connections to render said rectifier conductive only when the largest of said three electron magnitudes is received by said first collector.

11. An electron tube especially designed for binary addition, comprising an evacuated envelope containing an emitter, an electron collector cooperating with said emitter, a first pair of gating grids located adjacent the emitter and between the emitter and said collector, a grid of said first pair having approximately twice the gating area of the other grid of that pair, a second pair of gating grids located between the first pair and said collector, the second grid of said second pair having approximately twice the gating area of the first grid of said second pair, the first grid of the first pair being in gating alignment with the first grid of the second pair and partially overlapping the second grid of the second pair, the second grid of the first pair being in gating alignment with the second grid of the second pair.

12. An electron tube according to claim 11, in which a second collector electrode is provided for said emitter, a set of three substantially equal gating area grids between the emitter and said second collector and adjacent the second collector, and an inhibitor grid in gating alignment with all of said three equal area grids and located between said three equal area grids and said emitter.

13. An electron tube according to claim 12, in which an additional positively biased accelerating grid is located

between said inhibitor grid and said three equal area gating grids.

14. An electron tube according to claim 13, in which the first grid of said first pair is directly connected to the first of said three equal area gating grids, the second grid of said first pair is directly connected to the first grid of said second pair and to the second of said three equal area gating grids, the second grid of said second pair being directly connected to the third of said three equal area gating grids, a set of three input terminals to be energized respectively by addend, augend, and carry pulses, and means connecting said three input terminals respectively to each one of said three equal area gating grids.

15. An electron tube according to claim 14, in which a binary sum terminal and a binary carry output terminal are provided for said tube, means connecting said sum terminal to said second collector, and means connecting said carry output terminal to said additional grid.

16. An electron tube especially designed for binary addition, comprising a central cathode, six sets of similar grids with three grids in each set, the grid sets being symmetrically arranged around the cathode, first electron collector means in radial alignment with three of said grid sets, second electron collector means in radial alignment with the remaining three sets of grids, a set of three input

terminals to receive addend, augend, and carry pulses, an output sum terminal, an output carry terminal, and means interconnecting said grids with said input terminals to produce a sum signal at said sum terminal when addend and augend pulses are applied to said input terminals and simultaneously produce at said carry output terminal a signal when addend, augend and carry signals are applied to said three input terminals.

17. An electron tube according to claim 16, in which, in the absence of input pulses to said input terminals, both said collector means are at cut off, and means to apply positive input pulses to said three input terminals to produce a negative sum pulse at said sum output terminal when only addend and augend pulses are applied to the input terminals, and to produce a positive carry pulse at said carry output terminal when addend, augend, and carry pulses are simultaneously applied to said three input terminals.

18. An electron tube according to claim 16, in which said cathode is provided with electrode means to form the electrons into six discrete beams each in radial alignment with a corresponding set of three grids and each set of three grids is located within a respective field-free enclosure.

No references cited.