June 27, 1961 R. E. STOFFELS 2,990,451

TELEGRAPH CHARACTER COUNTER

Filed Dec. 15, 1958 3 Sheets-Sheet 1

FIG. 1

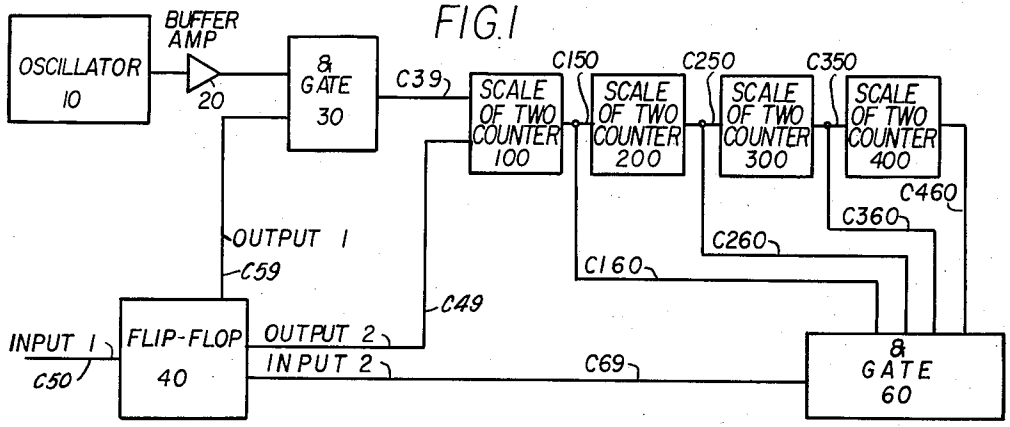
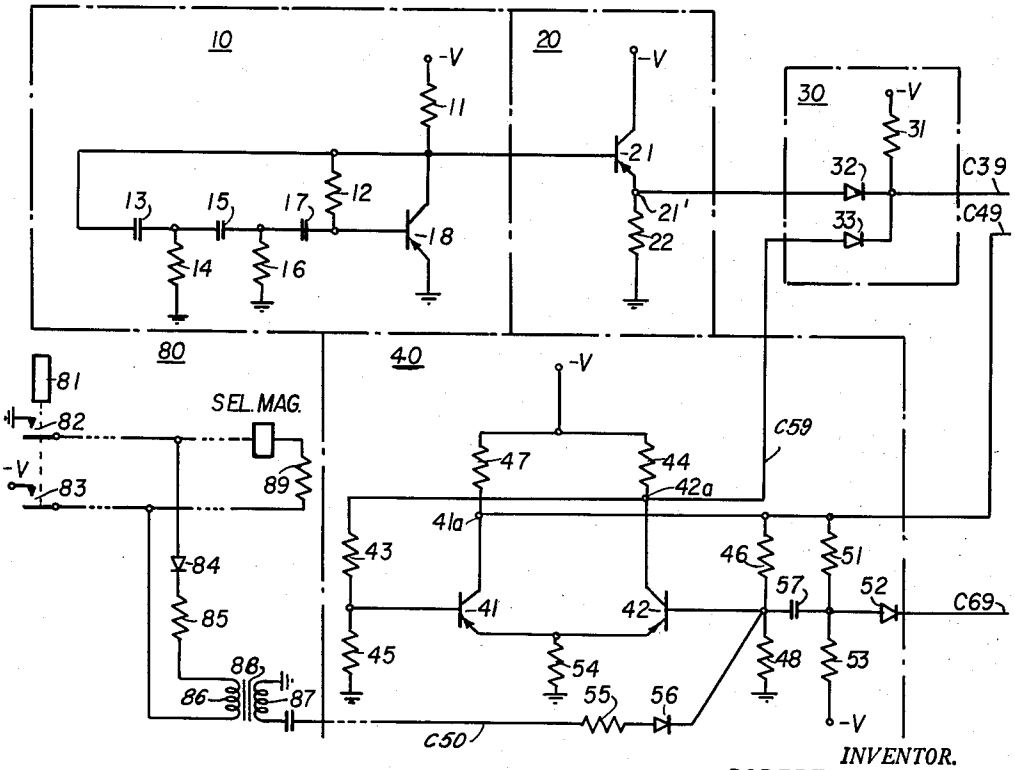


FIG. 2



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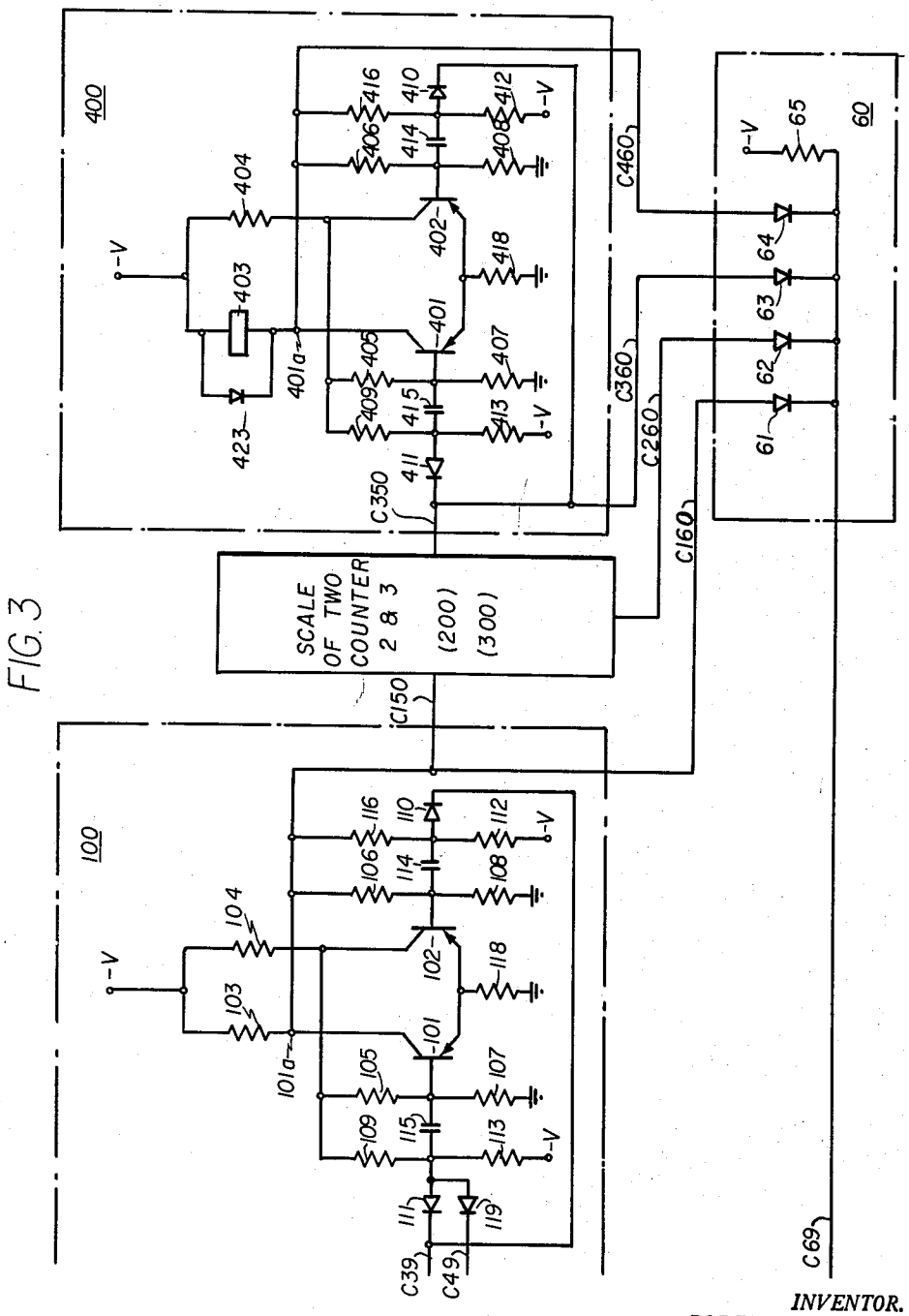


FIG. 3

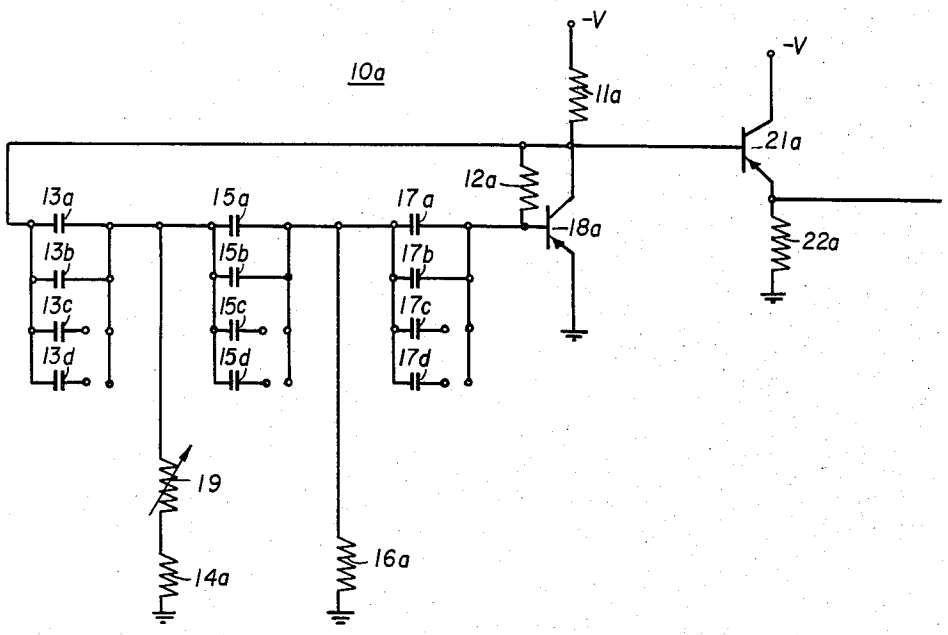
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FIG. 4



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TELEGRAPH CHARACTER COUNTER

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8 Claims. (Cl. 178—15)

This invention relates to telegraph receivers and more particularly to counting chains for use in conjunction therewith for registering the number of separate characters received in a telegraph message.

A telegraph message of the type sometimes referred to as "start-stop," consists of a number of code combinations or characters. Each character consists of an equal number of code elements or signals permutatively arranged. Each code element or signal consists of a space condition signified by a pulse of current or a mark condition signified by an open line condition or absence of pulse. The usual code utilizes either five or six of these signals to comprise a character. Each character is immediately preceded by a start pulse in the form of a space condition and each character is immediately succeeded by a stop pulse in the form of a mark condition.

The present invention is provided to respond to and provide an indication after the occurrence of each start pulse, in effect counting start pulses. Further mark or space pulses received during the counting cycle will have no effect on the counting chain until the cycle is completed. The cycle length therefore should be the equivalent in time of a message character. This timing can be achieved by the user of proper circuit components.

The present circuit would generally have no effect on the normal receipt of the message information which could be performed in any one of a number of known ways. The circuit as shown could be used to respond to service information transmitted along with a regular information message. For this purpose the output relay shown herein could be the motor magnet of a rotary switch, a peg count meter or any form of relay.

It is therefore an object of the invention to provide a circuit for counting start pulses in a telegraph message.

It is a further object of the invention to provide a counting chain which is triggered into a cycle by a first pulse and is thereby blinded to all subsequent pulses while the cycle continues.

A further object consists of the use of a transistorized binary counting chain which operates an electromagnetic relay in its output stage.

Another object is to provide a multi-stage counting chain, each stage having a diode gate output circuit, the complete operation of which places the chain in readiness to start a new cycle.

In the drawings:

FIG. 1 shows a schematic block diagram of the invention while FIGS. 2 and 3 jointly constitute a more detailed circuit diagram. FIG. 4 shows a second embodiment of an oscillator to provide various time constants which could be required.

In FIG. 1 is shown a control flip-flop **40** having two input leads and two output leads. The first input lead **C50** is the signal input from the telegraph receiver such as **80** and the other input lead **C69** is a recycling input from the counting chain output gate **60**. The first output lead **C59** is connected to "and" gate **30** to trigger the counting circuit into operation on receipt of a start pulse. Oscillator **10** and its amplifier **20** provide timed pulses through gate **30** during its open period and these pulses are counted by the four stage binary counter which includes counter stages **100**, **200**, **300**, and **400**. At the conclusion of the counting cycle, gate **60** is opened and an output pulse is transmitted past the output gate to recycle the counting chain, and to condition the control

flip-flop **40** for the next start pulse. Once during each cycle an output signal is given to an external circuit.

In FIG. 2, is shown control flip-flop **40** which is a bistable transistor device having an odd numbered transistor **41** and an even numbered transistor **42**. These transistors have a common emitter connection to ground through resistor **54**. Each of these transistors **41** and **42** has its base connected into a voltage divider and its collector connected into the voltage divider which is connected to the base of the other transistor. Thus, the voltage divider comprising resistors **44**, **43**, **45** has a connection to the base of odd transistor **41** and a connection to the collector of transistor **42**. The voltage divider comprising resistors **47**, **46**, **48** has a connection to the base of transistor **42** and a connection to the collector of transistor **41**. Each of these voltage dividers is connected at one end to a negative voltage sourch which is preferably a —15 volt source, and at the other end to a ground connection. The collector of each of these transistors also has an output lead connection; these being lead **C59** of FIG. 1 from the collector of even transistor **42** and lead **C49** from the collector of odd transistor **41**.

Output lead **C59** of the control flip-flop **40** is connected to diode **33** in gate **30**. This "and" gate **30** is made up of an output circuit and two diodes, one diode **33** as mentioned and the other **32**. The other diode **32** is connected to receive the output of oscillator **10** from amplifier **20**. Both of these diodes are poled so that when no current flows through them, the individual diodes are in the blocking state and the gate itself is considered open. With the gate open, a negative pulse is transmitted through the output circuit of the gate.

The oscillator **10** of FIG. 2 is composed of a transistor **18** coupled to a resistive-capacitive network. The emitter of transistor **18** is connected directly to ground. The collector circuit is biased through resistor **11** from the negative voltage source. The collector to base connection includes a series-parallel network including a first parallel path through resistor **12**. A second path includes a number of capacitors **13**, **15** and **17** and resistors such as **14** and **16** in a double T connection to provide a pulsating voltage to the oscillator transistor **18**.

FIG. 4 shows a variation in the oscillator of the circuit. Oscillator **10*a*** includes a possible paralleling of capacitors and the addition of a variable resistor **19** in the resistance-capacitance network. These variations in oscillator **10*a*** are provided so that the speed of oscillation can be adjusted for any telegraph speeds including 60, 75 or 100 words per minute which are the speeds currently in use. The capacitors **13*c***, **13*d***, **15*c***, **15*d***, **17*c***, and **17*d*** are shown in a manner having adjustable straps which could be completed to place these capacitors into the R-C network feeding the base of transistor **18*a***. The values and numbers of capacitors would be dependent on the telegraph reception speed required.

Referring back to FIG. 2 and oscillator **10**, the collector of oscillator transistor **18** is connected directly to the base of amplifying transistor **21**. The emitter of transistor **21** is connected through resistor **22** to ground and also is connected to the "and" gate diode **32**. The collector of transistor **21** is biased directly by the negative voltage.

The output of gate **30** which takes the form of a negative pulse through resistor **31** is connected to the input of first stage counter **100**. Counter stage **100** is composed of a binary flip-flop somewhat similar to control flip-flop **40** and is made up of two transistors **101** and **102**. Transistor **101** (the odd numbered transistor) and transistor **102** (the even numbered transistor) have a common emitter connection to ground through resistor **118**, a base connection into separate voltage dividers and separate collector connections into the voltage divider

connected to the base of the other transistor of the stage. The first of these voltage dividers includes resistors **104**, **105** and **107** and has a connection to the base of odd transistor **101** and a connection to the collector of even transistor **102**. The second voltage divider comprising resistors **103**, **106** and **108** has a connection to the collector of even transistor **102**. The second voltage divider comprising resistors **103**, **106** and **108** has a connection to the base of even transistor **102** and a connection to the collector of odd transistor **101**.

The inputs to counter stage **100**, are leads C39 and C49. Lead C39, which is the output lead of gate **30**, has a multiple connection to rectifiers **110** and **111** which lead to bases of transistors **102** and **101** respectively through capacitors **114** and **115** respectively. A second input, lead C49 provides a connection from the collector of transistor **41** at multiple connection point **41***a* to rectifier **119** which in turn is connected to capacitor **115**.

The output lead of counter stage **100** in the form of a connection from the collector of the odd numbered transistor has two paths. One path using lead C160 is connected to rectifier **61** of "and" gate **60**. The other path on lead C150 provides the input to the second counter stage **200** to feed pulses to that stage as lead C39 feeds pulses to the first stage **100**. The stage **200** and third stage **300** are identical to the first counter stage **100** and have been shown simply as a rectangular box. The fourth stage is identical to the other stages except that a resistor in the voltage divider connected to the collector of the odd numbered transistor **401** has been replaced by an electro-magnetic relay **403**. This relay can be the motor magnet of a stepping switch, a peg count meter relay or any relay having a suitable external registering or responsive circuit.

The operation of the network is as follows: In the normal condition transistors **42**, **101**, **202**, **302**, and **402** are biased conductive. When a start pulse is received on input lead C50 in the form of a ground pulse, this ground is transmitted through resistor **55** and rectifier **56** to the base of conducting transistor **42**. The voltage at the base of transistor **42** is raised by this ground pulse to the cut-off value to cause transistor **42** to stop conducting. Transistor **41** then becomes conductive. With transistor **41** conducting, the voltage at point **42***a* assumes a negative value and this negative voltage effectively blocks the first rectifier **33** of "and" gate **30**.

The resistance-capacitance network of oscillator **10** causes transistor **18** to periodically become conductive and then be shut off. When transistor **18** is shut off, a negative bias is transmitted through resistor **11** to the base of amplifier transistor **21** which then conducts. Conduction of transistor **21** causes a negative voltage at points **21'** which then tends to block the second rectifier **32** of "and" gate **30**. With both rectifiers blocked, the negative voltage at resistor **31** is transmitted through the open gate to the first counter stage **100**. As mentioned, transistor **101** in stage **100** is normally conductive which causes rectifier **111** to be essentially blocked, and thus the negative bias from open gate **30** is transmitted through rectifier **110** to the base of non-conducting transistor **102**. Transistor **102** then is triggered conductive and transistor **101** is driven to its cut-off point. When transistor **101** is cut-off, the voltage at point **101***a* is changed from an essentially ground potential (with transistor **101** conducting) to a negative voltage (with transistor **102** conducting).

This negative voltage at point **101***a* is then transmitted on lead C150 to the second stage counter **200** (not shown) to cause the odd numbered transistor **201** of the second stage to conduct. The oscillator **10** continues to transmit timed pulses which block rectifier **32** and open the gate **30** periodically to pulse the four stage binary chain in the usual binary manner following the method described for stage **100**. During the last half of the sixteen step cycle, transistor **401** is conducting. While transistor **401** is conducting, relay **403** operates and remains operated to record the passage of a single cycle, the cycle length of which is equivalent to the length of a single telegraph character.

After the final step of the sixteen count cycle, the even numbered transistor in each stage **102** (**202**, **302** not shown) and **402** is conducting. At this time point **101***a* and its equivalent points **201***a*, **301***a* and **401***a* in the remaining stages are at essentially the negative source voltage which tends to block rectifiers **61**, **62**, **63** and **64**. Gate **60** then is opened to allow a negative pulse to be sent through resistor **65** on lead C69 to the control flip-flop **40** through rectifier **52**. This negative pulse is then fed to the base of transistor **42** of the bistable control flip-flop **40** to trigger transistor **42** conductive and cause transistor **41** to be cut-off. Point **41***a* in the collector circuit of odd numbered transistor **41** assumes a negative voltage thus initiating a negative pulse on lead C49 through rectifier **119** to the base of transistor **101**. Transistor **101** will then conduct and cause transistor **102** to be cut-off, returning the circuit to its normal state of awaiting the next start pulse. This last step in the operative cycle should occur as the final or stop pulse of a character is received.

When the counting chain is in its operating timing cycle, control flip-flop **40** is in the off-normal state, with transistor **41** conducting. This control flip-flop is then blocked to all incoming telegraph signal pulses on lead C50. All negative pulses on lead C50 will be blocked by the high reverse resistance of rectifier **56**. Positive pulses on lead C50 will have no effect on the control flip-flop since the effect of a positive pulse at the base of the transistor **42** is to cut-off transistor **42**, and transistor has already been cut-off by the start pulse. Thus, it requires a negative pulse from gate **60** to change the state of transistor **42** at this time. At the end of the timing cycle, the negative pulse on lead C69 as described resets control flip-flop **40** to the normal state awaiting a further start pulse.

FIG. 2 shows a possible embodiment of an input device to the telegraph receiver. This input device contains a pulse transformer **88** which in the preferred embodiment is a ferrite core type transformer as explained on pages 253–271 of "Pulse and Digital Circuits" by J. Millman and H. Taub, McGraw-Hill, 1956. A transformer of this type combines small physical size with the necessary qualities of pulse transmission. A space-mark telegraph message in the form of a square wave signal would be impressed on the primary **86** and a wave form of greater amplitude and shorter duration would appear at the secondary **87**. These wave forms would be both positive and negative, showing an output voltage whenever the input signal was changed.

The operation of receiver **80** is as follows: Relay **81** is a conventional polar relay. During a mark period such as that of the usual line condition, contacts **82** and **83** of the polar relay are open. On the start pulse, the polar relay **81** is closed, closing contacts **82** and **83**. Ground through contact **82** is transmitted through rectifier **84**, resistor **85** and the primary **86** of pulse transformer **88** to contact **83** and negative battery. This causes a positive pulse to be transmitted on lead C50 to the counter input and could also be transmitted to the normal receiver circuits. The next pulse on lead C50 would occur when contacts **82** and **83** are opened. This would occur at the beginning of a mark pulse. Thus when the received mark signal follows a space signal, a negative pulse would be transmitted from the secondary **87** of transformer **88**. All changes in the type of received signal affect the signal transformer to provide a steeply rising potential gradient output.

What is claimed is:

1. In a telegraph system, a receiver for receiving intelligence characters in the form of code symbols comprising permutations of mark signals and space signals,

a character counter comprising: a multistage counting chain having a cycle length equal to the reception time of the complete character gating means; an oscillator connected to and periodically providing impulses to said gating means; first means initiated by the start of a character rendering itself non-receptive to further signals, and operating said gating means coincident with the impulses from said oscillator to trigger said counting chain into operation; and second means operated responsive to the completion of a cycle to render said first means receptive to the start of a subsequent character.

2. In a telegraph system as claimed in claim 1 wherein said counting chain comprises a plurality of binary counting stages connected in tandem, each stage including a two transistor bistable flip-flop, said plurality of stages responsive to the periodic impulses provided by said oscillator to said gating means to count said impulses in a binary manner.

3. A character counter for a telegraph system adapted to receive a plurality of characters each composed of a permutation of marked signals and space signals comprising: bistable signal receiving means having first and second stable states, on reception of the start of a character operated to said first stable state; gating means; a pulse source; a multistage counting chain having a cycle length equal to the reception time of a complete character, said signal receiving means while in said first stable state operating said gating means coincident with said operating pulses supplied by said pulse source to said gating means to operate said counting chain blocking means initially operated by said signal receiving means while in the first stable state to prevent reception of further signals by said signal receiving means, said counting chain on completion of a cycle operating said signal receiving means to said second stable state to permit reception of subsequent signals.

4. A character counter for a telegraph system adapted to receive a plurality of characters each composed of a permutation of mark signals and space signals, comprising a plurality of bistable circuits, said bistable circuits each having a first stable state and a second stable state, a first one of said bistable circuit operated to its first stable state in response to a first space signal of a character, means associated with said first bistable circuit for rendering said first bistable circuit non-responsive to further signals in the first stable state said remaining bistable circuits connected to said first bistable circuit in tandem, a gate circuit, an oscillator operated coincident with the operation of said first bistable circuit to its first stable state to operate said gate circuit, said gate circuit operated to supply pulses for pulsing the remaining of the plurality of bistable circuits, said remaining bistable circuits comprising a counting chain for counting pulses after said first bistable circuit is in its second stable state, recording actuating means in said chain rendered operative once during the counting cycle of said chain to register the receipt of a character, and means responsive to the conclusion of said chain cycle for returning said first bistable circuit to its first stable state.

5. In a receiver as claimed in claim 3, said signal receiving circuit comprising a first and a second transistor connected to form a bistable flip-flop circuit, said first transistor responsive to the receipt of a space signal to become conductive, said first transistor once conductive non-responsive to further space signals, and a rectifier poled to block all mark signals from said first transistor.

6. In a telegraph receiver for receiving a series of characters, each character comprising a number of code signals, each of said characters having a like time duration; means for counting characters in a series comprising: a control circuit, a first and a second transistor in said control circuit, said control circuit normally in an inoperative state with said first transistor conducting, means for transmitting the first signal in a character to said second transistor to cause said second transistor to become conductive, said control circuit in the operative state when said second transistor is conductive, first coincidence means prepared for operation by the conduction of said second transistor, means for initiating a sequence of timed impulses, said prepared first coincidence means on receiving said impulses transmitting output pulses, a multistage binary counting chain operated responsive to the application of said sequence of timed impulses to the first stage of said chain to count said impulses, second coincidence means responsive to a predetermined number being reached by said counting chain to initiate a recycling pulse, circuit means for transmitting said recycling pulse to said first and second transistors to render said first transistor conductive and said second transistor non-conductive, and further circuit means responsive to the rendering of said first transistor conductive to stop said counting chain.

7. In a telegraph receiver for receiving a series of characters, each character of which comprises a like number of code signals of either of two types, the first and last of the signals in a character of predetermined one of said types with the intervening signals randomly of either type, each of said characters having like time duration, a control circuit, a first and a second transistor in said control circuit, said control circuit normally in an inoperative state with said first transistor conducting, means for transmitting the first signal in a character to said second transistor to cause said second transistor to become conductive and cause said first transistor to become non-conductive, said control circuit in the operative state with said second transistor conducting, means operative on conduction of said second transistor to maintain said control circut in the operative state, a first "and" gate having a plurality of input paths, a first of said input paths blocked in response to said second transistor becoming conductive, means for initiating a sequence of timed impulses for periodically blocking the second input of said first "and" gate, said first "and" gate operative by simultaneous blocking of said first and second inputs to transmit periodic output pulses, a counting chain having a predetermined cycle length of duration equal to the time duration of a character, said counting chain comprising a plurality of binary stages connected in tandem, said chain responsive to the output pulses from said first "and" gate conducted to the first stage of said chain to sequentially change the state of said stages to thereby count through a counting cycle, means in the final stage of said plurality of stages operative on the change of state of said last stage to register the passage of a cycle, a second "and" gate responsive to a cycle completion to transmit an output pulse to said control circuit to render said first transistor conductive and said second transistor non-conductive, said first input to the first "and" gate opened on conduction of said first transistor to maintain said first "and" gate inoperative, said second transistor thereby rendered receptive to the next received signal of the type of said first signal in a character.

8. In a receiver as claimed in claim 7, each of said stages comprising a substantially identical pair of transistors connected in flip-flop circuit configuration, said stages connected in tandem, each of said stages having an output path, said second "and" gate comprising rectifiers in each of said stage output paths, each of said rectifiers poled to become blocked on conduction of the first of said pair of transistors in the stage to which the path containing the rectifier is connected, said second "and" gate operative to indicate the completion of a cycle when all the rectifiers in said second "and" gate are blocked coincidentally.

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