

[54] **CHARACTER GENERATOR FOR PRODUCING CHARACTERS ON THE SCREEN OF A CATHODE-RAY TUBE**

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[57] **ABSTRACT**

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Mar. 5, 1970 France 7007946

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[51] Int. Cl. G06f 3/14

[58] Field of Search 340/324 A

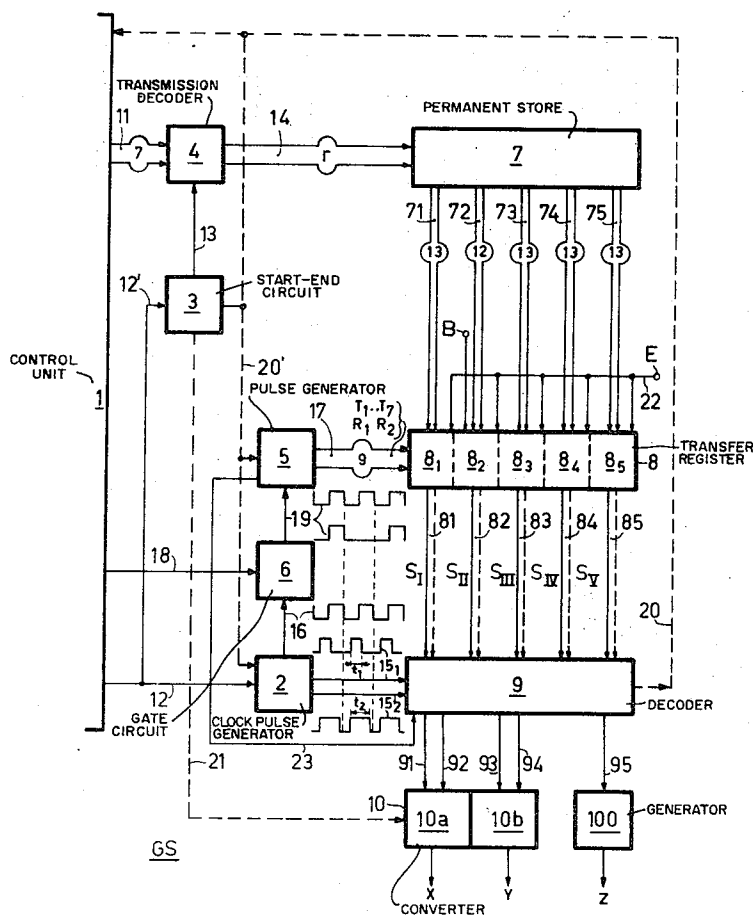
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Ultra-rapid character generator for use with a cathode-ray tube operating on straight line segments and equipped with a permanent store from which by means of a store word address a character codeword is passed to a transfer register, which transfers the relevant character codeword sequentially in a number of relevant groups of 5 bits to a decoder, 3 bits determining 8 line segment directions, 1 bit determining a single or double line segment length and 1 bit determining the display or non-display.

9 Claims, 11 Drawing Figures



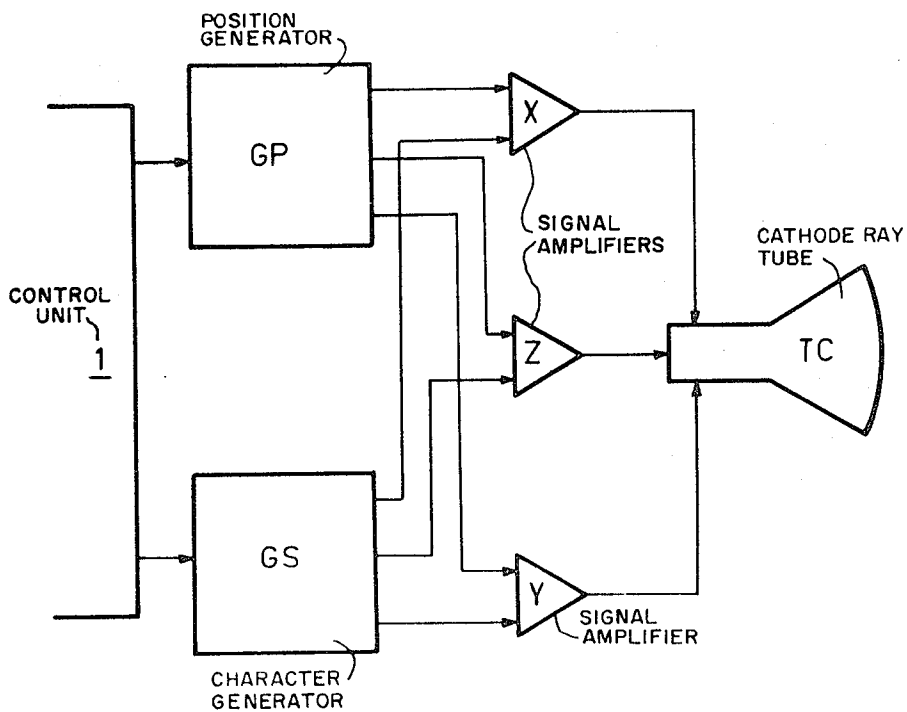
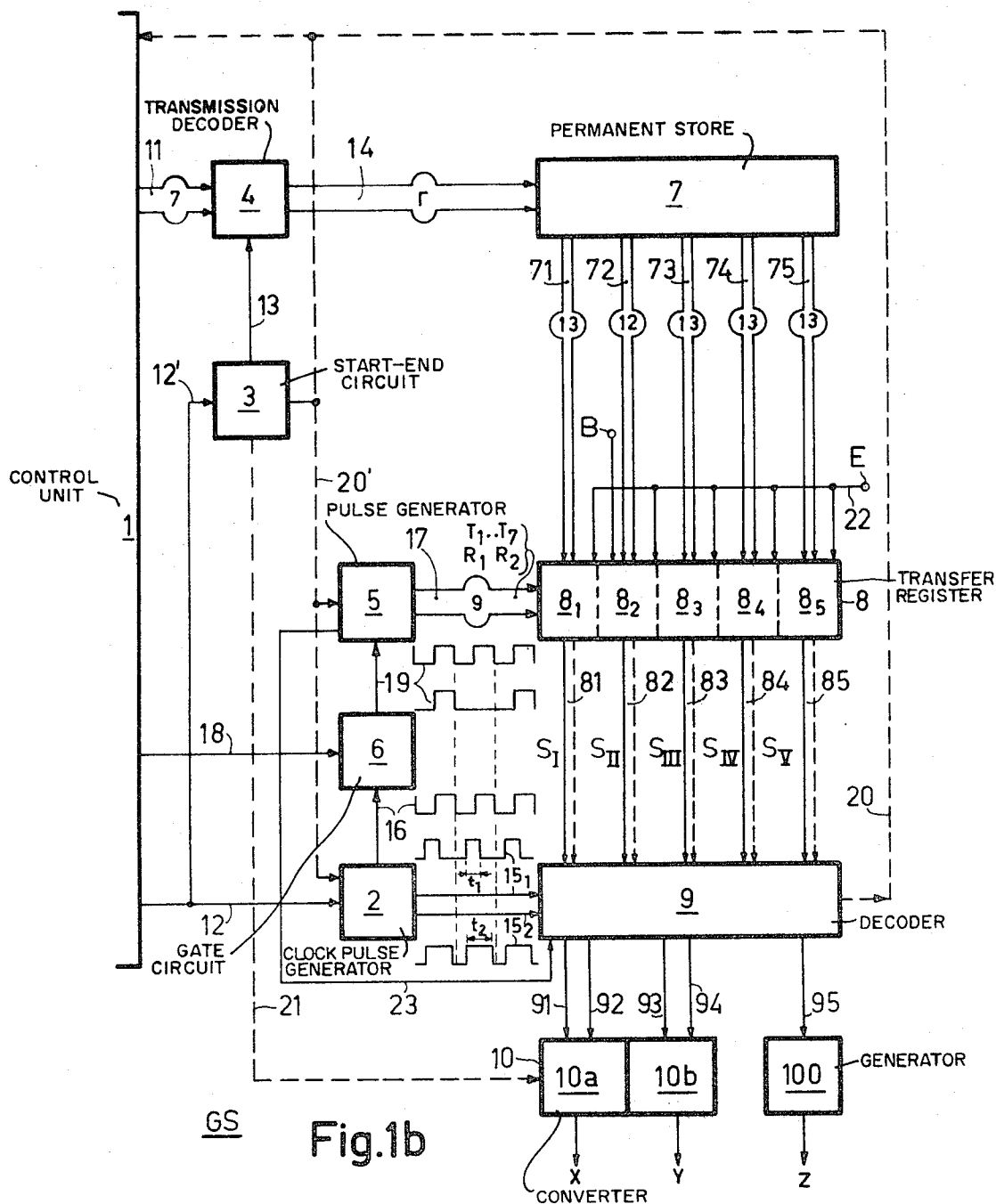


Fig.1a

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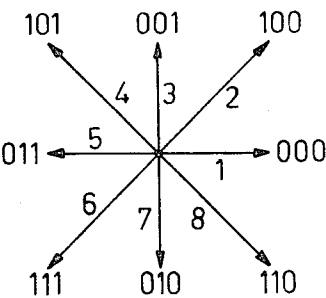


Fig. 2

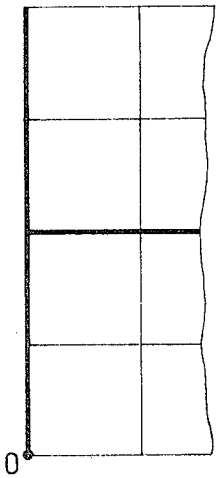
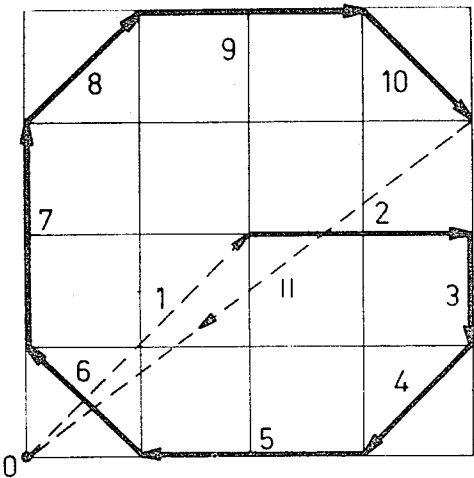


Fig. 3

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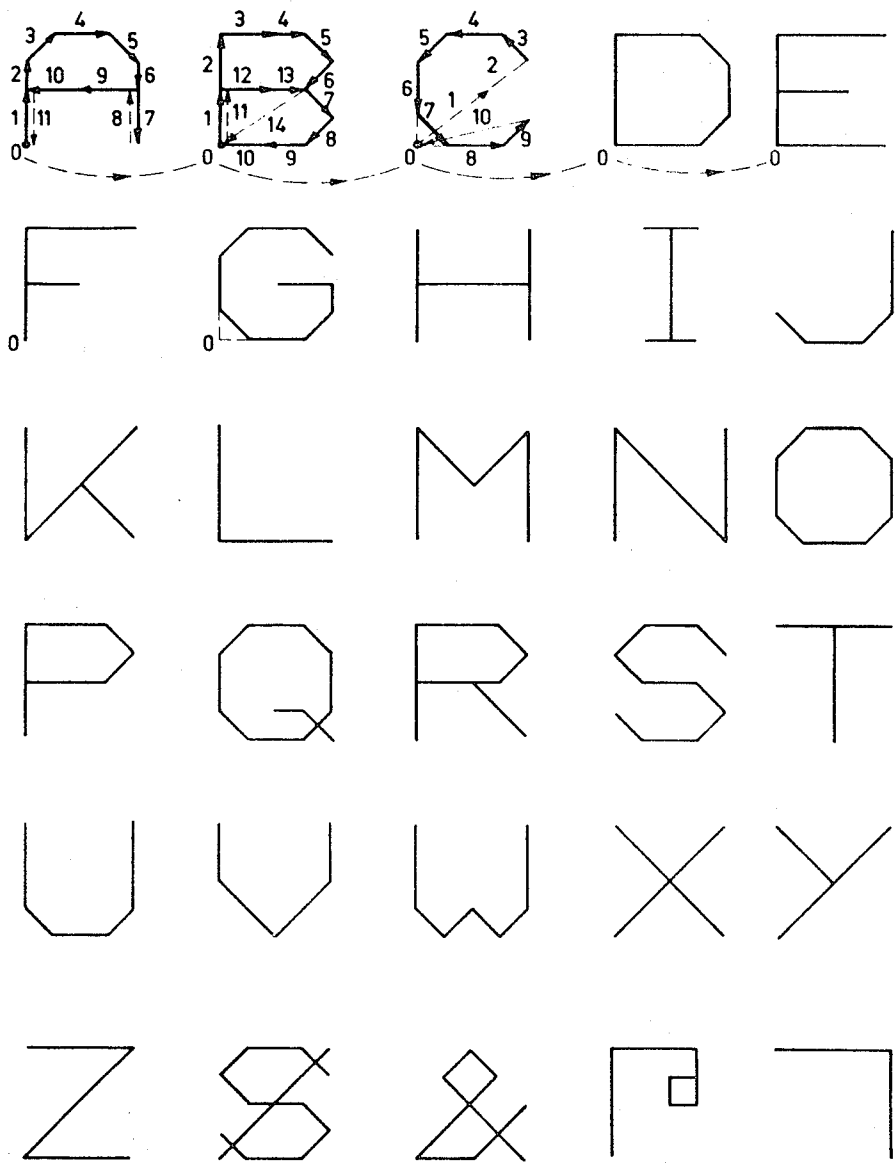
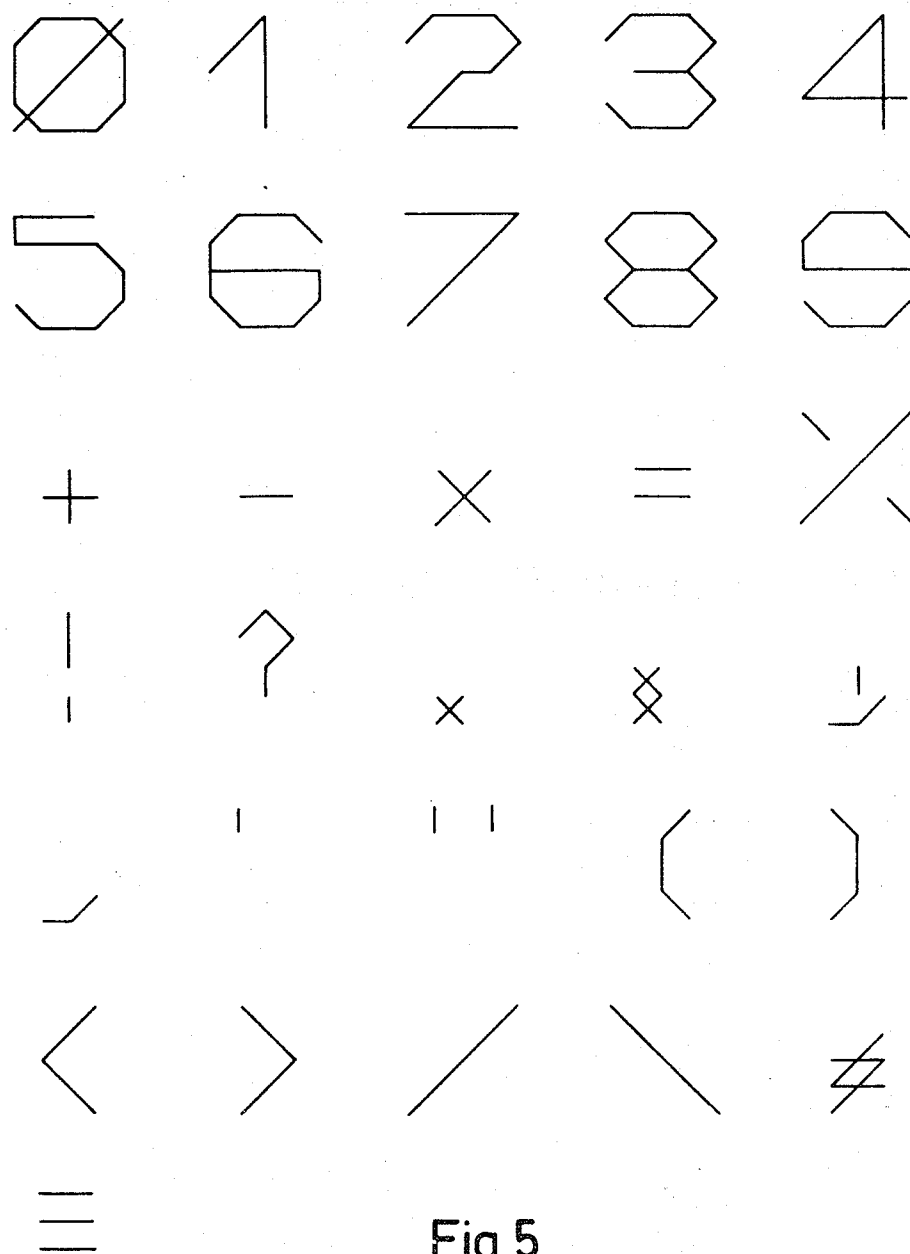


Fig.4

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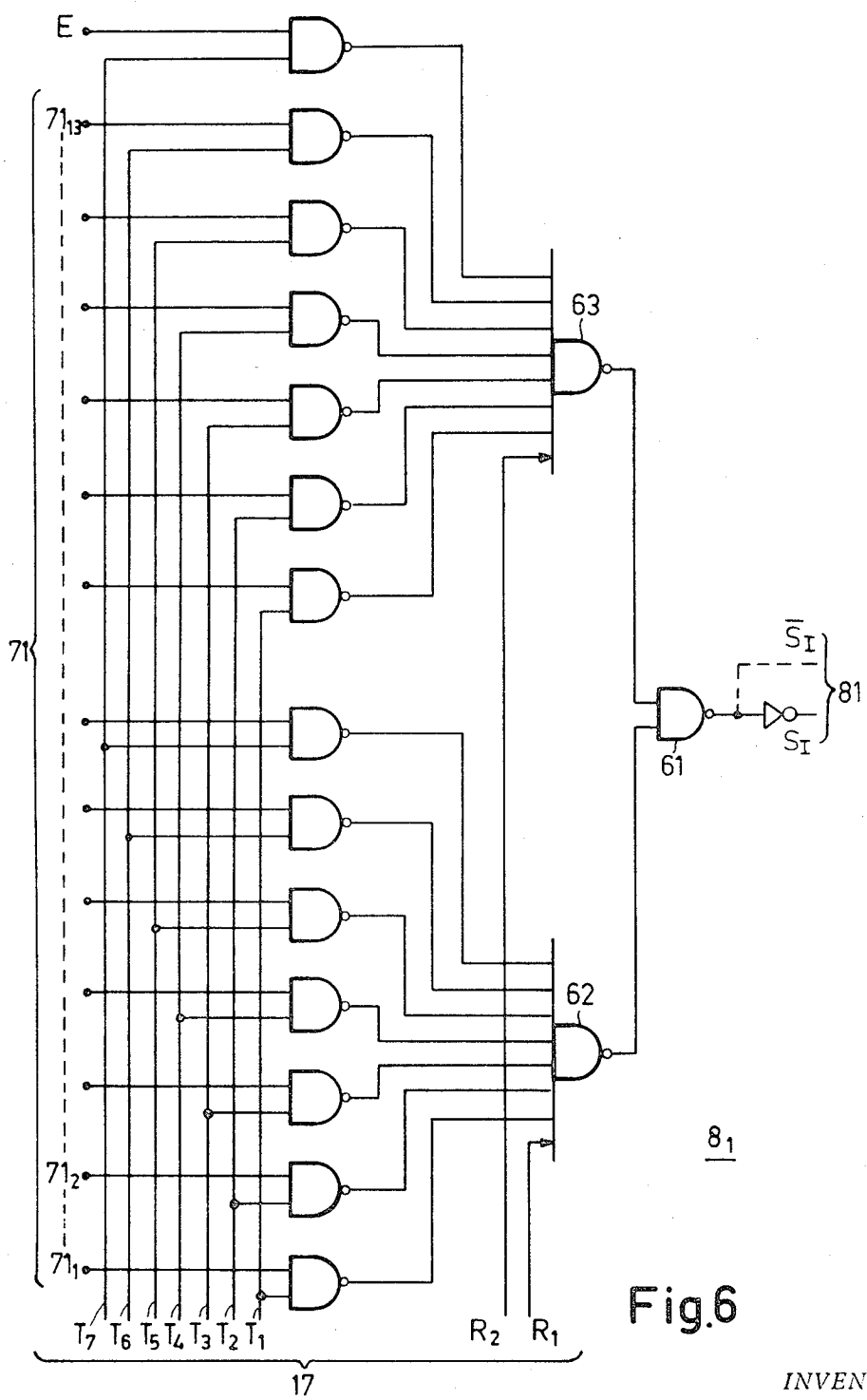


Fig.6

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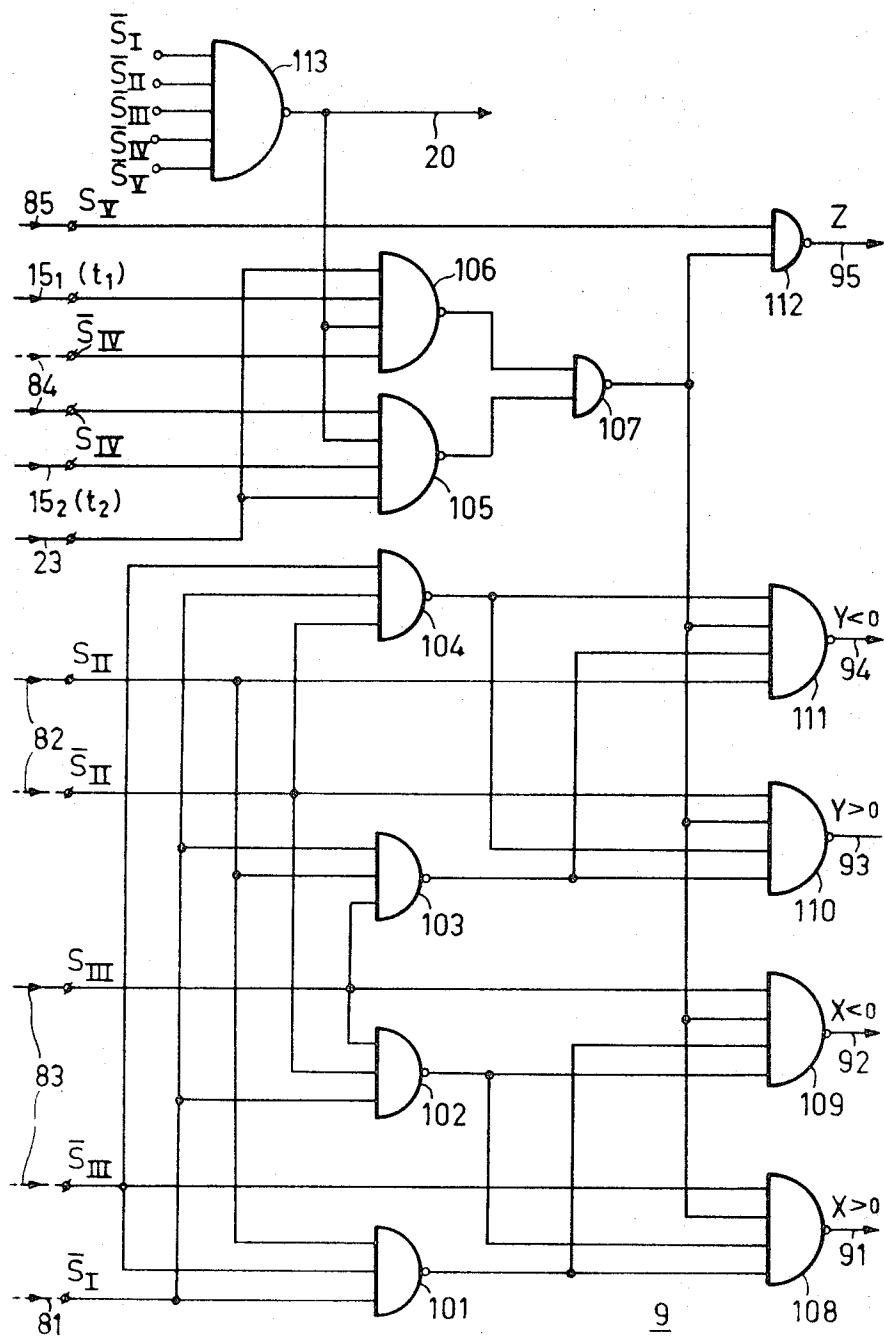
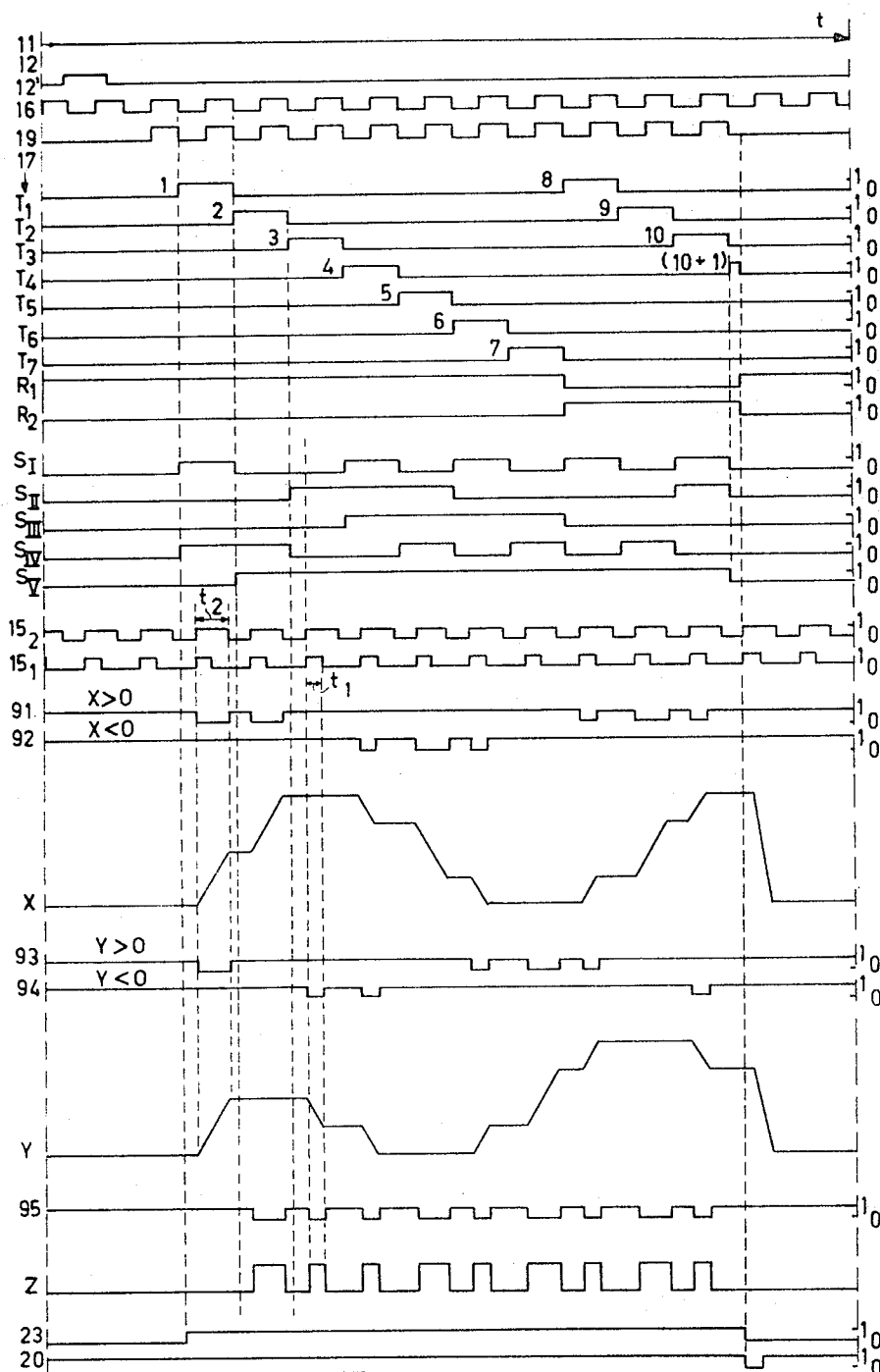


Fig.7

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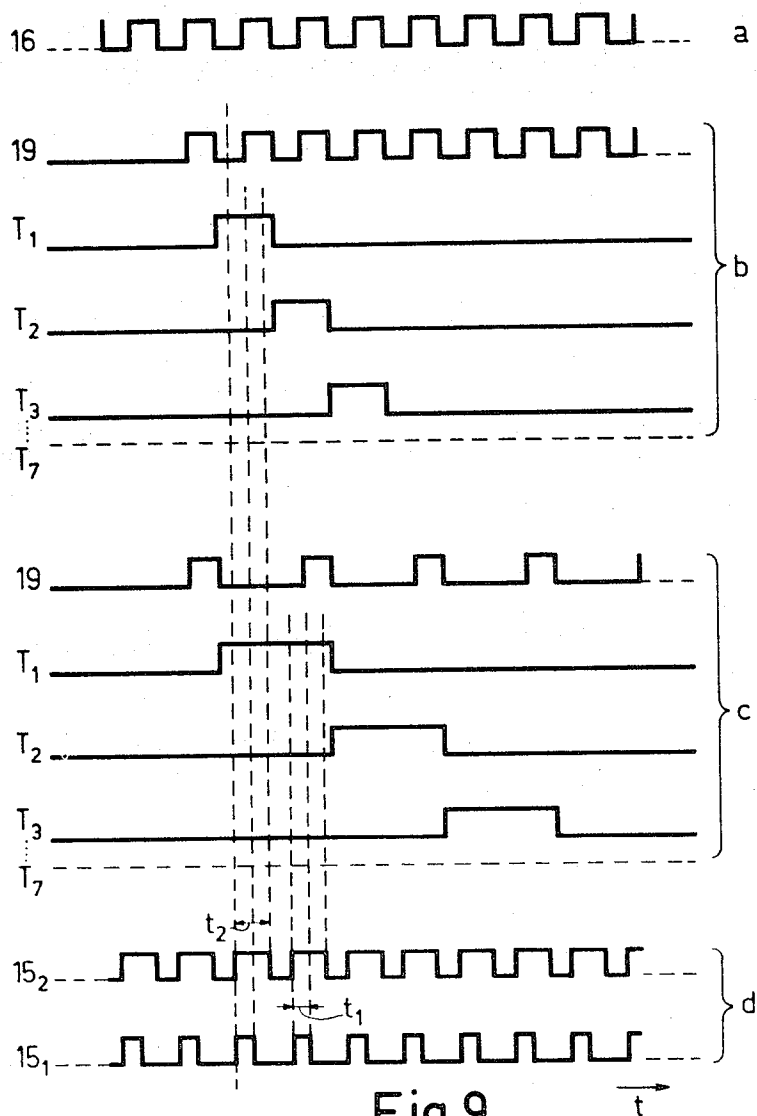


Fig.9

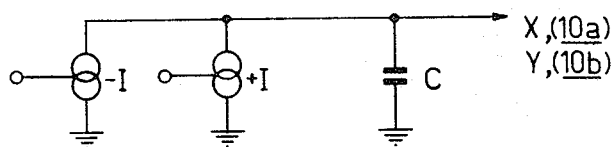


Fig.10

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CHARACTER GENERATOR FOR PRODUCING CHARACTERS ON THE SCREEN OF A CATHODE-RAY TUBE

The invention relates to a character generator for producing characters on the screen of a cathode-ray tube, said characters being formed by straight line segments, the character generator comprising a permanent memory store with the segment information in a code word of n groups of bits, one group per segment, and a pulse generator for producing phase-shifted pulses having a gating function, by means of which the segment information is supplied sequentially, group after group, on one hand through a transfer register, to a digital-analogue converter for providing deflection signals for the cathode-ray tube and on the other hand to the tube for the display or non-display of the segment.

Such a generator or device for generating characters formed by straight line segments is described in the article "Variable Symbol Cathode-Ray tube Generator" in "Electronic Engineering," October 1968, pages 553 to 559.

In this article it is described that every character or symbol to be displayed may be formed by 16 groups of 15 bits, that is to say, 15 groups for 15 straight line segments of a given length and one group for supplying a signal for indicating the end of the character (character- or symbol-end signal). The permanent store is scanned by consecutive pulses as many times as there are potential segments for the display of each symbol. However, this method is not appropriate for a quick display of a symbol because the obtainment of all instructions for the formation of a word from the permanent store requires fifteen scans of the store for each symbol, that is to say, one scan for each group of 5 bits, whereas a character may well be formed by considerably fewer segments than 15. By way of example the character B formed by 12 segments is given.

In the known generator a dynamic analysis of the store is carried out, whereas it appears to be preferable to carry out a static scan and to reduce the dynamic analysis to the level of the transfer register, which provides, in addition, time saving in the transmission of information required for the display of a character.

The known generator involves an access delay time and a scanning time of a vector or line segment of comparatively great length with respect to the time required for the display of the vector. Moreover, the display rate of a character and the price of the apparatus are two intimated related aspects due to the usually increasing complexity of the electronic equipment required for the simultaneous display of a great number of symbols. The ultra-rapid generator according to the invention provides a simple, economic solution of said problem.

The known generator does not permit of magnifying the symbols to be formed in all directions in a simple manner without variation of the brightness of said symbols.

The character generator according to the invention avoids these disadvantages. This generator is used for providing a device permitting a high-rate display of symbols to be transmitted, the time required for the transmission being of the order of $0.08 \mu\text{sec}$ per segment instead of $25 \mu\text{sec}$ as indicated in said article, so

that the time of occupation of the separate control-unit (computer or the like) is minimized.

According to the invention the character generator is characterized in that it comprises a decoder which decodes the segment information given for each character in its own code word by groups of five bits, three bits determining one of eight line segment directions, one bit determining a single or a double line-segment length and one bit determining display or non-display of the line segment on the screen of the cathode-ray tube, said decoder being connected between the transfer register and the digital-analogue converter and the cathode-ray tube.

As compared with the known generator with the segment code in five bits described a similar result is found to be obtainable by using four items of information instead of five. A five-bit code can thus comprise one bit providing an additional information, for example, an information relating to the single or the double length of a segment. This particular mode of coding is used in the generator according to the invention so that a greater variety of symbols can be displayed by a smaller number of segments.

It is found that in the generator according to the invention the maximum number of straight line segments required for the display of the most complicated symbol is equal to 14 instead of 16. Consequently, this means that the storage word occupies a smaller length ($70 = 14 \times 5$ instead of $80 = 16 \times 5$).

This is a saving of the number of elements and in mounting operations so that the cost price of the assembly is reduced.

The particular coding in accordance with the invention permits of utilizing the full capacity of a store of 64 bits of the commercially available type. Such an occupation of the store is an economic advantage, which can be attained by reducing the maximum length of a storage word to 64 bits, instead of 70 bits. This is achieved by connecting six inputs of the transfer register beyond the store through external wiring to two biased terminals, the first terminal providing the second bit of the first group of each of the characters and the second terminal providing, in a group of five bits, the 14th group which corresponds to the character-end signal if the character is formed by a maximum number of 13 segments.

The invention will now be described more fully with reference to the drawing.

FIG. 1a shows the character generator according to the invention associated with a position generator providing a sequence of starting points of characters and symbols on the display screen of a cathode-ray tube of a peripheral display system connected to an external control-unit, for example, a computer or the like.

FIG. 1b illustrates the basic diagram of the ultra-rapid character generator embodying the invention.

FIG. 2 illustrates the relationship between the direction and the sense of 8 vectors and their coding by 3 bits, which are the first bits of each group of 5 bits, which determine the display of each character segment.

FIG. 3 illustrates the rhombis unity pattern having sides of 4×4 , in which all symbols are displayed with the aid of the 8 vectors of FIG. 2. In FIG. 3 the more solid lines form the capital G and moreover a portion of the next character H. This Figure illustrates clearly

the return to the origin after the "character-end" signal.

FIGS. 4 and 5 show by way of example a few characters that can be displayed without exceeding the limit number 13 of segments per character. FIG. 4 shows the 26 characters of the alphabet in bold letters and, in addition, 4 further symbols. FIG. 4 illustrates the transition from one origin to a next origin, said transition being performed by means of the position generator of FIG. 1 independently of the ultra-rapid character generator embodying the invention. FIG. 5 illustrates the digits 0 to 9 and 21 other characters and symbols.

FIG. 6 illustrates the circuit-diagram of one stage of a transfer register of FIG. 1b. the transfer register is formed by five of these stages.

FIG. 7 illustrates the circuit-diagram of the decoder of FIG. 1b.

FIG. 8 illustrates a time diagram indicating the time division, on the one hand, of the various operations required for storage in a store, for the analysis of the transfer register and on the other hand, the display and the termination of the display of the characters (shown in FIG. 8 for the display of the character G).

FIG. 9 is a diagram of the pulses obtained at the outputs of a clock-pulse generator and of a pulse generator producing shifted pulses for said transfer register with respect to the output pulses of a gate circuit operating as a magnifying member, which determines the size of the displayed character or symbol.

FIG. 10 illustrates the principle of a digital-analogous converter employed herein.

Herein the terms "symbol" or "character" are used for denoting a letter or any other representation, whilst the term "bit" is used for denoting a binary information.

FIG. 1a illustrates the independence of the operation of a character generator GS embodying the invention of a position generator GP for positioning the beginning of the symbols. The generators GS and GP controlled by a control-unit 1 are connected to the deflection signal amplifiers X and Y and to a video-signal amplifier Z of a cathode-ray tube TC.

For the display of a character or a symbol the control-unit 1 determines the position of the light spot at the desired starting place on the screen of the cathode-ray tube TC through the position generator GP and subsequently supplies to the character generator GS the code of the symbol and, in addition, the information of the size of said symbol and then supplies the symbol starting pulse. The signals produced by the generator GS are then applied to the inputs of the amplifiers X, Y and Z.

For the following description of the operation of the ultra-rapid character generator it is stated that the transition from the origin of one symbol to the origin of the next symbol does not fall within the scope of the invention and that these consecutive transitions are performed in synchronism with the display of each symbol by means of a given control-programme supplied by the control-unit 1.

FIG. 1b illustrates schematically the principle of an ultra-rapid character generator GS embodying the invention. The control-unit 1 is connected to a clock-pulse generator 2, which produces synchronizing pulses of a time period t_1 and of a time period $t_2 = 2t_1$, transmitted via the lines 15₁ and 15₂ and connected to a circuit 3, which generates the starting signal and also the

signal corresponding to the termination of a symbol display. The clock-pulse generator 2 and the "starting-ending" circuit 3 are connected to the external control-unit 1 via lines 12 and 12', which have to supply to the generator GS the symbol starting signal from the control-unit 1.

A transmission decoder 4 is provided between the control-unit 1 and a permanent store 7 and ensures that a coded group of bits determining the symbol to be displayed is decoded to a storage word address. A multi-core cable 11 connects the control-unit 1 to the transmission decoder 4. The number of cores of the cable 11 depends upon the code used by the control-unit. In the case of the international code ASC II comprising 7 bits permitting a coding of 128 characters, the cable 11 comprises 7 cores in parallel connection which link the control-unit 1 to the decoder 4. A cable 14 having r parallel cores connects r outputs of the decoder 4 to r inputs of a permanent store 7, that is to say one input for each stored word. The number r thus corresponds to the number of words stored, one for each symbol. The permanent store 7 comprises a number r of words equal to the number of symbols to be displayed.

A line 13 connects an output of the beginning-ending circuit 3 to a further input of the transmission decoder 4. Thus the line 13 supplies to this decoder the scan sequence for the store 7 with the corresponding address and provides the control from the beginning of the display of the symbol after the circuit 3 has received the symbol starting pulse from the control-unit 1.

The display of each character segment requires one group of 5 binary information signals and in the case of a character formed by 13 segments an additional group of 5 bits occurs for generating the signal corresponding to the end of the character. Thus a length of 70 bits of the character code word is obtained, which is required for the display of any symbol. This is not desirable because the commercially available apparatus is adapted to standard word lengths of 64 or 128 bits.

According to the invention the cable connects the permanent store 7 to a transfer register 8, whilst in two steps said word length of 70 bits is reduced to a word length of 64 bits, so that the store 7 can be a 64-bit codeword length store.

In a first step four cables 71, 73, 74, 75 comprising 13 cores ensure the sequential rate of transmission of the first, the third, the fourth and the fifth bit, respectively, of each of the groups determining the consecutive segments of a character, whilst a cable 72 comprising 12 cores is provided with an additional core for connecting a terminal B external of the store having a given voltage to register 8. In a second step, a core 22 connects in the same manner the register 8 to a terminal E located outside the store 7, which terminal has the same voltage as the terminal B. This core 22 permits the formation of the 14th group of 5 bits, which is coded so that it generates the character-end pulse when the number of n -segments forming the symbol is equal to 13. If the number n is lower than 13, which depends upon the character itself, said character-end pulse is produced by the $(n + 1)^{\text{th}}$ group of 5 bits in the store 7.

The transfer register 8 is connected between the store 7 and a decoder 9 and is connected by cable 17 having 9 cores to a pulse generator 5, which controls the transmission of each group of 5 information bits transmitted by the cables 71, 72, 73, 74 and 75 across

the transfer register 8 to said decoder 9, the register 8 being formed by 5 identical stages 8₁, 8₂, 8₃, 8₄ and 8₅ operating in parallel.

Since each of said stages 8₁ through 8₅ is connected via 14 cores, each core providing the transmission of the bit of the same ordinal number in each of the 14 potential groups of 5 bits, the decoder 9 receives the information in a group of 5 bits. The transfer register 8 is connected via double lines 81, 82, 83, 84 and 85 to the decoder 9, whose outputs are connected via lines 91, 92, 93 and 94 to deflection signal generators 10a and 10b of a digital-analogue converter 10 and via a line 95 to the video-signal generator 100. The information supplied by the transfer register 8 via the lines 81 to 85 is transmitted, after conversion in synchronism with one of the synchronizing pulses of a duration t_1 , t_2 , transmitted via one of the lines 15₁, 15₂ connecting the clock-pulse generator 2 to the decoder 9 and after conversion into control-pulses with the value 0 or 1 of the fourth bit of the group of 5 information pulses, to, on the one hand, the generators 10a and 10b of said digital analogue converter 10 for generating an analogue signal for the amplifier X and Y respectively and on the other hand, the generator 100, which supplies to the amplifier Z pulses controlling the ignition of the Wehnelt electrode of the cathode-ray tube TC of FIG. 1a.

The decoder 9 comprises, in addition, a device for producing the character-end signal which is transmitted via a line 20 to the control-unit 1. The character-end signal sets back to the initial state the assembly of elements of the generator GS via lines 20' and 21, i.e., via the line 20' the circuit 3 and the generators 2 and 5 and via the line 21 the converter 10 across the circuit 3. Via a line 23 the pulse generator 5 supplies a release pulse to the decoder 9 for releasing it for the time in which the character information is available via the transfer register 8.

The operation of the digital-analogue converter 10 in the character generator GS, the circuit-diagram of which is illustrated in FIG. 10 is based on the charge and discharge of a capacitor C with a constant current value $+i$ or $-i$. Such a converter may be used for generating positive and negative voltages having, in absolute value, the same steepness.

Finally a gate circuit 6 provides an omnidirectional enlargement of a character. The circuit 6 is directly controlled via a line 18 by the unit 1 and is connected on the one hand to the clock pulse generator 2 via a line 16 and on the other hand to the generator 5 via a line 19, said generator supplying a sequence of pulses to the transfer register 8.

FIG. 2 illustrates the coding of the 8 unity vectors by means of the first 3 bits of each group of 5 bits.

In accordance with the invention the display can start from the beginning of any character only in one of the three directions: the horizontal direction having the code 000, the diagonal direction having the code 100 and the vertical direction having the code 001. It is apparent that in these three code values the second bit is the same, that is to say 0. This mode of coding in accordance with the invention permits of supplying the second bit of the first group of each character beyond the store 7 via an external connection (terminal B).

The following Table I indicates by way of example the coding of a character (letter G of FIG. 3). The numbers 1 to 10 of the left-hand column of this Table indicate the order of succession in time for writing the

ten vectors used for the character, whilst the number 11 corresponds to the command "character-end."

Table I indicates the value of "n" of the character to be displayed: for the character G (11 groups) the value n is 100. The Table also indicates the (n+1)th group of 5 bits generating the character-end signal, said group of 00000 providing zero-setting of the various circuits of the system; the Table shows the case of the character-end signal for a symbol of $n = 13$ (characters B or S).

Table also indicates the places of the bits originating from said terminals B and E of FIG. 1b.

TABLE I

		Ordinal nr. of the bit in the group				
		Sense-direction			Duration 0=1X 1=2X	Brightness 0=extinguished 1=excited
Number of the group (n)		I	II	III	IV	V
n=13 (characters B and S)	1.....	1	(B)0	0	1	0
	2.....	0	0	0	1	1
	3.....	0	1	0	0	1
	4.....	1	1	1	0	1
	5.....	0	1	1	1	1
	6.....	1	0	1	0	1
	7.....	0	0	1	1	1
	8.....	1	0	0	0	1
	9.....	0	0	0	1	1
	10(n).....	1	1	0	0	1
	11(n+1).....	0	0	0	0	0
n<13 (n=10 character G)	11.....					
	12.....					
	13(n).....					
	(E) 14(n+1).....	0	0	0	0	0

In this application the term "group" of 5 bits indicates the static effect in the case of a word stored in the permanent store 7 and the term "sequence" is used to indicate a dynamic effect, for example, in the case of duration of treatment of a group of 5 bits.

In said mode of segment coding the symbols can be determined independently of each other, so that the number of symbols or characters may exceed 256 (2⁸), the system using this mode being thus changed only as far as the corresponding number of storage codewords is added.

The Table illustrating the coding of a character G shows the special nature of the coded sequence transferred by the register 8 to the segment decoder 9 (formed by 00000), which generates the character-end signal.

This character-end signal is produced immediately after the transmission of the n groups of 5 bits of the stored word, which corresponds to any symbol, n being any integral number lying between 2 and 13. This (n+1)th group of 5 bits either obtained from the permanent store when the stored codeword comprises fewer than 13 groups as in the case of the character G or from beyond said store 7 via the additional line 22 with 5 parallel-connected inputs to the transfer register 8 (FIG. 1b).

The particular relationship existing in accordance with the invention between each combination of the first three bits of a group of 5 bits determining the display of a segment of a symbol by means of the analogue values of the voltages controlling the horizontal and vertical deflections (X) and (Y), respectively, of the electron beam in the cathode-ray tube TC is as follows:

In the code of the said 3 bits, the values of these bits are:

0 for bit 3, when $X > 0$ and 1 for bit 3, when $X < 0$;
0 for the bit 2, when $Y > 0$ and 1 for bit 2 when $Y < 0$.

Bit 1 assumes the value 0, when either X or Y , are zero, whereas it assumes the value 1 when X and Y are equal to each other (inclined vectors).

By these rules the vectors 2, 4, 6 and 8 (FIG. 2) are completely coded. It is apparent, however, that for the vectors 1 and 5 the second bit is not yet used and the third bit is not used for the vectors 3 and 7. It is then applied that for $X > 0$ the second bit has the value 0 and for $X < 0$ this bit has the value 1. The values of the third bits of the remaining vectors 3 and 7 are determined by the rule: $Y > 0$ this bit assumes the value 1 and $Y < 0$, it assumes the value 0.

FIGS. 4 and 5, illustrating a few digits, characters and symbols obtainable by the character generator GS embodying the invention, permit a statement of the aesthetic value thereof. By way of example the sequence of the straight line segments is given for the first three symbols of FIG. 4. As is shown in FIGS. 4 and 5, the cable 14 of FIG. 1b comprises $r = 61$ cores for the 61 characters and the store 7 comprises 64 word addresses.

FIG. 6 illustrates one embodiment (8₁) of one of the five stages 8₁ to 8₅ of the transfer register 8 for the transfer of the first bit of each group of 5 bits by means of two electronic subassemblies having each 8 Nand-gates.

14 inputs of lines 71₁, 71₂, . . . 71₁₃ and terminal E are arranged in two groups of 7 inputs each and are connected to inputs of two groups of 7 Nand-gates, whereas the other inputs of said two groups of gates are connected to 7 lines T₁ to T₇. The 7 gate outputs of one group are connected to 7 inputs of a Nand-gate 62 or 63, respectively the 8th input of which is connected to a line R₁ or R₂, respectively. The outputs of the gates 62 and 63 are connected to two inputs of a Nand-gate 61, the output of which directly forms an output S_i and an output \overline{S}_i via an inverter. This output S_i and its complementary output \overline{S}_i indicated by a double line, supply in order of succession the information of the first bit 1 of each of the 14 groups of 5 bits.

An identical diagram is used for processing the next four bits II, III, IV and V, which indicate as indices the order of the bit in each of the groups 1 through 14 in accordance with the Table I above. For the stage 8₂ it applies than an input 72₂ corresponding with the input 71₂ of stage 8₁ is connected to terminal B of FIG. 1b. The 5 outputs of the stages, i.e., \overline{S}_I , S_I(81), \overline{S}_{II} , S_{II}(82) . . . \overline{S}_V , S_V(85), are connected to the corresponding inputs of the decoder 9 of FIGS. 1 and 7.

FIG. 7 shows one embodiment of the decoder 9 and illustrates the synchronism between the signals X, Y and Z and in the decoding stage, the influence of the length information, that is to say, of the fourth bit at the inputs for the synchronizing pulses of durations t_1 , t_2 and at the input \overline{S}_{IV} (S_{IV}), which selects between the durations t_1 and t_2 .

FIG. 7 shows for the decoder 9 the main connections in accordance with the invention to the transfer register 8 (lines 81 to 85), to the clock-pulse generator 2 (lines 15₁ and 15₂) and to the pulse generator 5 (line 23 of FIG. 1b).

The input \overline{S}_I corresponds to one of the lines 81 of FIG. 1b, the inputs S_{II} and \overline{S}_{II} correspond to the lines 82, the inputs S_{III} and \overline{S}_{III} correspond to the lines 83, the inputs S_{IV} and \overline{S}_{IV} correspond to the lines 84 and the input S_V corresponds to one of the lines 85, which in common connect the transfer register 8 to the decoder 9.

In addition, the input for the pulses of the duration t_1 corresponds to the line 15₁ of FIG. 1b and the input for the pulses of the duration t_2 corresponds to the line 15₂ from the clock-pulse generator 2, which provides the synchronous operation.

Via the line 23 the pulse generator 5 supplies a release pulse to the decoder 9.

Moreover a 5-input Nand-gate 113, connected to inputs \overline{S}_I . . . S_V forms the device supplying the character-end signal via the line 20.

The decoder 9 comprises furthermore 12 Nand-gates 101 to 112, FIG. 7 showing the following input connections:

Gate	Gate
101: \overline{S}_I , S _{II} , \overline{S}_{III}	108: \overline{S}_{III} , 101, 102, 107
102: S _I , \overline{S}_{II} , S _{III}	109: S _{III} , 101, 102, 107
103: S _I , S _{II} , S _{III}	110: S _{II} , 103, 104, 107
104: S _I , S _{II} , S _{III}	111: S _{II} , 103, 104, 107
105: S _{IV} , 15 ₂ , 23, 113	
106: S _{IV} , 15 ₁ , 23, 113	112: S _V , 107
107: 105, 106	

With reference to the coding described above it follows that:

The gates 101 and 102 decode the signal $X = 0$ with code $S_I = 0$, that is to say, $S_I = 1$ so that with $S_{II} = 1$, $S_{III} = 0$ gate 101, and with $S_{II} = 0$, $S_{III} = 1$ gate 102, indicates the logical 0, and the gates 108 and 109 are blocked.

The gate 108 decodes the signal $X > 0$, when $S_{III} = 0$, (that is to say, when $\overline{S}_{III} = 1$).

The gate 109 decodes the signal $X < 0$, when $S_{III} = 1$.

The output signals of the gates 108 and 109 depend upon, and are synchronized by, the output signals of the gate 107.

The Nand-gates 103, 104, 110 and 111 have identical functions for Y.

The gate 105 passes the pulse of the duration t_2 (15₂), when $S_{IV} = 1$ and if line 23 and the gate 113 provide the logical 1. In the same manner gate 106 selects pulse t_1 , when $S_{IV} = 0$, i.e. when $\overline{S}_{IV} = 1$. The gate 107 ensures the passage of the pulse emanating from gate 105 or 106.

The gate 112 performs the video-signal synchronization Z with the aid of the gate 107 (as for signals X and Y when $S_V = 1$).

As aforementioned, in accordance with the invention, coding of the 3 bits determining the vectorial direction permits of reducing the length of the stored word from 70 to 64 represented bits for normal use.

Moreover, in decoding the combination of the meaning of the first three bits of a group of five bits determining the direction and the value of the segment with the length information represented by the fourth bit provides the possibility of materially reducing the number of the logical integrated circuits required for decoding.

The use of a reduced number of elementary circuits reduces the cost price of the assembly, whilst the information transmission is accelerated; the system accord-

ing to the invention is thus simplified and its performance is improved.

This novel decoder 9 results from the said adjustments characteristic of the generator GS embodying the invention, in which an assembly of integrated circuits reduced to 12 Nand-gates forms the decoding part which provides the vectorial information $X < 0$; $X > 0$; $Y < 0$; $Y > 0$ and $X = 0$ or $Y = 0$ for each sequence and at the same time also the single or the double time period associated with said information and which passes in synchronism the value of the fifth bit controlling the ignition or extinction of the Wehnelt electrode, whilst said vectorial information controls the deflections along the X- and Y-axes of the electron beam in the cathode-ray tube TC via the digital-analogue converter 10 (FIG. 1b).

The time diagram shown in FIG. 8 illustrates the manner of operation of the various electronic circuits forming the ultra-rapid generator GS embodying the invention as a function of time during the display of a symbol on the display screen.

The waveforms of FIG. 8 illustrate in detail the signals appearing at the corresponding cables and lines of FIGS. 1, 6 and 7.

The lines 11, 12 and 12' indicate the instants of reception of the code ASC II with 7 bits supplied in parallel by the control-unit 1 to the transmission decoder 4 (line 11) the instant being directly followed by the symbol- or character-starting pulse to the clock-pulse generator 2 and the "character-starting and -ending" circuit 3 (lines 12 and 12').

Line 16 indicates the pulse emanating from the clock-pulse generator 2 via the gate circuit 6 to the pulse generator 5, which supplies sequential, i.e., phase-shifted pulses. The line 19 shows the character-size pulses transmitted by the gate circuit 6 operating as a magnifying member, to the generator 5.

In the case shown by way of example for the display of the character G of normal size the gate circuit 6 passes 11 unchanged clock pulses to the line 19. The clock pulse generator 2 operates, for example, with a frequency of 12.5 MHz.

The lines T_1 to T_7 and R_1 and R_2 show relatively shifted pulses transmitted by said generator 5, operating as a time base, to register 8 via the cable 17 having 9 parallel-connected cores, whilst R_1 passes the first 7 groups of 5 bits and R_2 passes the further groups of 5 bits (FIG. 6).

The signals $S_1 \dots S_V$, corresponding to the lines 81 to 85, provide the simultaneously occurring bits I to V of consecutive groups in accordance with the foregoing Table indicating the coding of the character G, the order of succession being determined by the transfer register 8.

The pulses of the durations t_1 and t_2 correspond to the single or the double duration of the pulses produced by the clock pulse generator 2, which are separately transmitted in parallel to the segment decoder 9 via the lines 15₂ and 15₁. The time ratio of these pulses corresponds to the length ratio of the various displayed segments of the same symbol (single or double).

The line X shows the analogue signal X, which is formed by the signal generator 10a from the digital pulses of the lines 91 and 92, which provide, through the logical circuits in the decoder 9, the decoding of the respective values $X > 0$ and $X < 0$.

In the same way the lines 93 ($Y > 0$), 94 ($Y < 0$) and

Y indicate the analogue signal Y processed in the same manner.

The segment decoder 9 selects the pulse of the duration t_1 or the pulse of the duration t_2 so that the display time depends upon the value of the fourth bit of the group of 5 bits determining one segment. The choice of t_1 ($S_{IV} = 0$) or t_2 ($S_{IV} = 1$) is illustrated on the lines X, Y and Z of the time diagram of FIG. 8.

The lines 95 and Z represent the decoded ignition and extinction signals for the Wehnelt electrode (line 95) and the corresponding ignition pulses.

Line 20 indicates a character-end pulse and line 23 the decoder release pulse, the leading edge of which corresponds with that of the first pulse on the line T_1 , whereas the trailing edge is given by the character-end pulse.

FIG. 9 illustrates by a pulse diagram the operation of the gate circuit 6, operating as a magnifying member and arranged between the clock pulse generator 2 and the pulse generator 5 producing phase-shifted pulses.

At a in FIG. 9 line 16 indicates the synchronizing pulses of the system transmitted by the clock pulse generator 2, whereas at b and at c the lines 19 $T_1, T_2, T_3, \dots, T_7$ indicate the pulses passed by the gate circuit 6 to the generator 5 (line 19) with the correspondingly produced phase-shifted pulses at the lines T_1, T_2 , etc.

As before, the lines 15₂ and 15₁ indicate at d the double duration of the t_2 pulses as compared with the t_1 pulses, which determine the length of the segment to be displayed.

At the level of the decoder 9, which receives sequentially the groups of bits and in parallel the group of 5 bits in accordance with the display of each segment, the pulse of duration t_1 or the pulse of duration t_2 is chosen in accordance with the value of the fourth bit, of each of said groups for controlling the time required for displaying one segment. The output of the decoder 9 thus provides the 5 said signals at the lines 91 to 95 for a duration t_1 or for a duration t_2 in accordance with the length of the displayed segment. In this example the time t_1 corresponds to a unit length and the time t_2 to twice the length. It follows that the lines drawn at b in FIG. 9 correspond with those of FIG. 8. Apart from the single (t_1) length or twice the length (t_2) of a segment, it follows from c and d of FIG. 9 that per group of 5 bits instead of one display of the segment (b and d in FIG. 9) two displays are obtained. Consequently, all segments have double the length.

Further lengthening of the pulses on the lines T_1 to T_7 permits a further overall magnification by a factor p.

The industrial results and advantages of the ultra-rapid character generator suitable for use in a peripheral display system in accordance with the invention may be recapitulated as follows:

1. Quick action: display time required for not too complicated a symbol of 7 segments: 0.8 μ sec at a clock pulse frequency of 12.5 MHz, any time lag being assumed to take 3 segment periods.

2. Reliable operation: for the major part operation in digital logics, suppression of interferences; it is essential for the conversion of digital signals into analogue signals to be performed at the latest possible instant.

3. Readily readable characters and symbols: owing to the aesthetical shape of each character, to the con-

stancy of the brightness and to the precision of each character.

4. Economic operation: the character generator permits of displaying an optimum number of characters with the use of a minimum number of electronic elements.

5. Readily controllable: a single knob provides the sharpness of the displayed symbols and characters by a phase control in synchronism with the clock pulses.

6. The generator is equipped with an image magnifying member allowing an overall variation from the unit value 1 of the symbol size to a value $p \times 1$, the factor p being an integral number at least equal to 2. The unit size of a symbol displayed on the screen is preferably written in a pattern of squares (width 4 mm and height 5 mm). The height and width vary, of course, with the application of the deflection-signal amplifiers X and Y employed.

In operation the character generator GS is controlled by the control of the relative values of the times t_1 and t_2 corresponding to the relation $t_2 = 2t_1$ and by the control of the time phases for obtaining synchronism with the signals from the transfer register. The synchronism suppresses all errors due to the variations in characteristics of the logical circuits employed in the whole assembly.

The two functions $X > 0$ or $X < 0$ and $Y > 0$ or $Y < 0$ must not appear simultaneously.

The signal values $X = 0$ or $Y = 0$ are obtained in the absence of $X > 0$ or $X < 0$ and of $Y > 0$ or $Y < 0$.

All logical circuits of the generator GS are compatible with DTL integrated circuits (diode-transistor-logics) and the TTL integrated circuits (transistor-transistor-logics).

As a matter of course, it is possible to design a character generator GS for reducing the characters from the size of a first character occupying approximately the whole available surface of the screen; in this case the display changes to characters of smaller dimensions by carrying out an overall diminution by $1/p$, the factor p corresponding to a whole number.

It should be noted that the clock pulse generator 2, which provides two different time intervals t_1 and t_2 , may be replaced by two separate generators, which are switched on alternately in accordance with the segment length to be displayed.

It is also possible to design a generator producing configurations of any size, provided the Figures are formed by straight line segments, the unit surfaces of the segments of the configurations being adjacent each other without interstices or with an overlap obtainable by a simple programme of the position generator GP, which determines the consecutive starting points of said unit surfaces in co-operation with the computer.

What is claimed is:

1. A character generator for producing characters on the screen of a cathode-ray tube, said characters being formed by straight line segments, the character generator comprising a permanent memory store with the segment information in a codeword of groups of bits, one group per segment, a pulse generator for producing phase-shifted pulses having a gating function, whereby pulses of the segment information are supplied sequentially, group after group, on the one hand through a transfer register to a digital-analogue converter for providing deflection signals for the cathode-ray tube, and on the other hand to said cathode ray tube for the display or non-display of the segment, the character gen-

erator further comprising a decoder for decoding the segment information given for each character in its own codeword with groups of five bits, three bits determining one of eight line segment directions, one bit determining a single or double line segment length and one bit determining the display or non-display of the line segment on the screen of the cathode-ray tube, said decoder being connected between the transfer register and the digital-analogue converter and the cathode-ray tube.

2. A character generator as claimed in claim 1 wherein the permanent memory store is of the type in which each character has its own word address, and wherein outputs carrying the character information in one codeword are fed to the transfer register, said transfer register being connected to said pulse generator providing the phase-shifted gate pulses, the character generator being synchronized with a clock pulse generator connected to the pulse generator and to the decoder.

3. A character generator as claimed in claim 1 wherein each of the code-words of the characters supplied by the store have a group of bits for the first segment comprising four bits and all further groups comprise five bits each, two of the bits in the first group of four bits determine the direction of the segment, the transfer register itself supplying beyond the store, by means of a biased terminal, the failing bit which is the same for each codeword, to the decoder.

4. A character generator as claimed in claim 2 wherein between the clock pulse generator and the pulse generator providing the phase-shifted gate pulses for the transfer register, a gate circuit is provided which operates as a character magnifying member in accordance with the passage or nonpassage of consecutive clock pulses.

5. A character generator as claimed in claim 2 wherein the clock pulse generator supplies pulses through two lines to the decoder, pulses having a duration t_1 in one line thereof and pulses having a duration $t_2 = 2t_1$ in the other line thereof.

6. A character generator as claimed in claim 5 characterized in that the decoder comprises multi-input gates coupled with the transfer register and connected to each other, the outputs of the decoder being formed by outputs of gates of which one input of each gate is connected to one input on further gates for synchronization purposes, said inputs being coupled with outputs of further gates, to inputs of which are applied the fourth bits information of the transfer register and the pulses of the durations t_1 and t_2 of the clock pulse generator.

7. A character generator as claimed in claim 1, wherein the decoder comprises a gate of five inputs, to which five information outputs of the transfer register are connected, said gate supplying a character-end signal in the case of 0-information.

8. A character generator as claimed in claim 7 when using a store having character information in the form of a store codeword having an n number of groups presenting a maximum permissible total number of bits, the transfer register is provided with a group of inputs connected to a biased terminal supplying the 0-information beyond the store for the $(n + 1)$ th group.

9. A character generator as claimed in claim 8 wherein the store is of the type having a maximum length codeword of 64 bits, whilst the transfer register supplies 14 groups of 5 bits at its 5 outputs.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3755805 Dated August 28, 1973

Inventor(s) PIERRE DANDREL and JEAN-FRANCOIS MOREAU

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

- Column 3, line 14, "the" should be --The--
Column 6, line 11, after "Table" insert --I--
Column 6, line 46, "The Table" should be --Table I--
Column 7, line 44, " $\overline{S_I}$ " should be -- $\overline{S_I}$ --
Column 7, line 53, " $\overline{S_I}$, S_I (81)" should be -- $\overline{S_I}$, S_I (81) --
" $\overline{S_{II}}$, S_{II} (82)" should be -- $\overline{S_{II}}$, $\overline{S_{II}}$ (82) --
Column 7, line 54, " $\overline{S_V}$ S_V (85)" should be -- $\overline{S_V}$ $\overline{S_V}$ (85)--
Column 7, line 61, " $\overline{S_{IV}}$ (S_{IV})" should be -- $\overline{S_{IV}}$ ($\overline{S_{IV}}$) --
Column 8, line 2, " S'_{II} and S_{II} " should be -- $\overline{S_{II}}$ and $\overline{S_{II}}$ --
Column 8, line 3, " S_{III} and S_{III} " should be -- $\overline{S_{III}}$ and $\overline{S_{III}}$ --
Column 8, line 56, "of reducing" should be --the reduction of--
Column 10, line 23, " T_2 T_2 " should be -- $\overline{T_2}$, $\overline{T_2}$ -- .

Signed and sealed this 19th day of March 1974.

(SEAL)

Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

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