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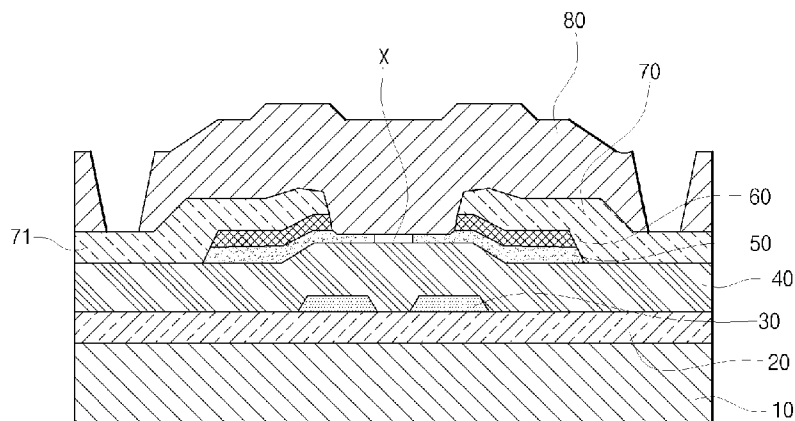
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(54) Title: MANUFACTURING METHOD OF INVERSE STAGGERED POLY-SI TFT WITH CENTER OFF-SET

[Fig. 3]



(57) Abstract: Disclosed herein is a method for manufacturing a poly-Si TFT with a center offset structure, including (1) preparing a buffer layer on a substrate, (2) preparing a gate electrode with a center offset structure on the buffer layer, (3) forming a gate insulating film on the gate electrode, (4) forming an active layer on the gate insulating film, (5) depositing an n+ amorphous silicon based ohmic contact layer over the active layer, (6) placing source/drain electrodes on the n+ amorphous silicon based ohmic contact layer, and (7) forming a passivation film as a protective layer on the source/drain electrodes. According to the disclosed method, an offset pattern is formed in the center of a gate constituting the TFT to form an offset region in the middle of an active layer channel, so that complicated processes for fabrication of the TFT may be simplified and leakage current may be noticeably inhibited.



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Description

MANUFACTURING METHOD OF INVERSE STAGGERED POLY-SI TFT WITH CENTER OFF-SET

Technical Field

- [1] The present invention relates to fabrication of thin film transistors (TFTs) and, more particularly, a method for manufacturing a TFT, including formation of an offset pattern in the center of a gate constituting the TFT in order to form an offset region in the middle of the active layer channel, so that complicated processes for fabrication of the TFT are simplified and leakage current is considerably reduced.

Background Art

- [2] TFTs may be generally classified into four types based on an order in which an active layer, a gate insulating layer, source/drain electrodes and a gate electrode are manufactured. More particularly, a staggered type TFT includes a gate electrode and source/drain electrodes arranged by interposing an active layer while a coplanar type TFT includes both a gate electrode and source/drain electrodes located at the same side of an active layer. The staggered type TFT is fabricated by forming source/drain electrodes on a substrate and laminating an active layer, an insulating layer and a gate electrode thereon in sequential order. In this regard, the insulating layer is generally formed on the active layer by a plasma process, often causing defects on semiconductor interfaces. On the other hand, the coplanar type TFT is fabricated by arranging source/drain electrodes, an insulating layer and a gate electrode on an active layer in sequential order. Similar to the staggered type TFT, such coplanar type TFT encounters interfacial defects occurring during formation of the insulating layer and, in addition, has another problem in that the interfacial defects are extended due to an etching process required for lamination of an electrode on the active layer. For this reason, the coplanar type TFT is not substantially used for manufacture of amorphous silicon TFTs.
- [3] Alternatively, inverse staggered type and inverse coplanar type TFTs are also well known, which are fabricated by reversing the processes for fabrication of the staggered type TFT and the coplanar type TFT, respectively. Especially, the inverse staggered type TFT is mostly applied to manufacture of amorphous silicon TFTs.
- [4] The disclosed TFT may include a TFT based on amorphous silicon or polycrystalline silicon and a TFT based on compound semiconductors, depending on materials for the active layer.
- [5] In order to reduce considerable leakage current in a conventional polycrystalline silicon TFT (poly-Si TFT), an offset structure has been proposed. An offset region has

a high resistance area so as to reduce an electric field formed between a channel and the source/drain. As a result, the leakage current is decreased in view of a transfer curve of the poly-Si TFT.

- [6] FIG. 1 is a cross-sectional view illustrating a process for fabrication of a poly-Si TFT with a coplanar structure having an offset 5. In particular, a silicon oxide film is formed on an insulated substrate 10, which serves as a buffer layer 8 to block diffusion of impurities from the substrate caused by crystallization. Amorphous silicon as an active layer 11 is deposited thereon. Crystallizing the amorphous silicon may form the polycrystalline silicon. As a gate insulating film 9, another silicon oxide film is formed and a gate electrode 1 is formed and patterned above the gate insulating film 9. In order to form the offset 5, a doping barrier 4 sufficient to cover the gate electrode 1 is used. After implanting ions into the remaining part except an area covered by the doping barrier 4 to prepare an ohmic contact area 7, a source 2 and a drain 3 are patterned and prepared, followed by depositing a protective layer 6 on the active layer 11 so as to protect the fabricated device from external gas or moisture.
- [7] FIG. 2 is a plan view illustrating a poly-Si TFT with a coplanar structure having an offset structure 5.
- [8] As for the structure shown in FIG. 2, an offset region is formed by preliminarily patterning a doping barrier 4 with a larger size than the pattern of the gate 1, before ion implantation. Therefore, the foregoing coplanar type TFT entails problems of requiring photolithography as well as an additional expense for fabrication of a mask.
- [9] Moreover, since the offset 5 is limited to sub-micron scale, a process margin such as alignment error caused during processing may be drastically decreased. Due to process complexity and/or reliability, the above disclosed coplanar type TFT is not broadly employed in various applications, in spite of enhanced electrical properties thereof.
- [10] The conventional process for manufacturing TFTs as described above may require photolithography using five (5) masks. Since the photolithography demands more complicated and precise processes including, for example, masking, photosensitive film coating, exposing and/or developing, an increase in number of individual processes may result in a complicated process, increased tact time and/or increased failure of products due to frequent repetition of processes. Accordingly, there may be a strong requirement for reduction in number of masks as well as decreased leakage current occurring during fabrication of TFTs.

Disclosure of Invention

Technical Problem

- [11] Therefore, the present invention is directed to solve conventional problems described above and an object of the present invention is to provide a method for manufacturing

a TFT including formation of an offset pattern in the center of a gate constituting the TFT in order to form an offset region in the middle of the active layer channel, so that complicated processes for fabrication of the TFT are simplified and leakage current is considerably reduced.

Technical Solution

- [12] In order to decrease leakage current and accomplish the above object of the present invention, a center offset is formed in the middle of a channel by patterning a gate. Such a structure may not require addition of a mask, thereby stably inhibiting leakage current without increasing production costs.
- [13] More particularly, the present invention provides a method for manufacturing TFTs by a simple process with reduced leakage current, wherein an offset is formed in the center of a gate when the gate is formed in a poly-Si TFT having an inverse-staggered structure. In this manufacturing method, since an offset region is placed in the center of the gate pattern, no additional processes are required. Also, the patterned offset region may not be affected by further processes, thus embodying external merits thereof. Therefore, the present invention may provide a poly-Si TFT having an inverse staggered structure manufactured using a center offset in order to enable remarkably stable control of leakage current.

Advantageous Effects

- [14] According to the method for manufacturing a TFT of the present invention, an offset pattern is formed in the center of a gate constituting the TFT to form an offset region in the middle of an active layer channel, so that complicated processes for fabrication of the TFT may be simplified and leakage current may be noticeably inhibited.
- [15] The above and other objects, features and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

Brief Description of Drawings

- [16] FIGS. 1 and 2 are a cross-sectional view and a plan view illustrating a poly crystal TFT with an offset structure according to a conventional technology;
- [17] FIGS. 3 and 4 are a cross-sectional view and a plan view illustrating an inverse staggered poly crystal TFT manufactured using a center offset according to the present invention;
- [18] FIGS. 5 to 7 show a method for fabrication of an active layer according to an exemplary embodiment of the present invention;
- [19] FIG. 8 illustrates transfer curves of a general poly-Si TFT; and
- [20] FIG. 9 illustrates transfer curves of an inverse staggered poly-Si TFT manufactured using a center offset according to the present invention.

Best Mode for Carrying out the Invention

- [21] The present invention provides a method for manufacturing a poly-Si TFT with a center offset structure, comprising: (1) preparing a buffer layer on a substrate; (2) preparing a gate electrode with a center offset structure on the buffer layer; (3) forming a gate insulating film on the gate electrode; (4) forming an active layer on the gate insulating film; (5) depositing an n⁺ amorphous silicon based ohmic contact layer over the active layer; (6) placing source/drain electrodes on the n⁺ amorphous silicon based ohmic contact layer; and (7) forming a passivation film as a protective layer on the source/drain electrodes. The inventive method may omit addition of a mask required for photolithography and may stably inhibit leakage current without increasing production costs.
- [22] The step (5) in the above manufacturing method of the poly-Si TFT with the center offset structure may comprise directly depositing an amorphous silicon thin film on an n⁺ zone.
- [23] The step (2) in the above manufacturing method of the poly-Si TFT with the center offset structure may comprise using a pattern of the gate electrode to form the center offset structure with a thickness of 0.1 to 5 μm .
- [24] The step (3) in the above manufacturing method of the poly-Si TFT with the center offset structure may comprise using a silicon oxide film to form the gate insulating film.
- [25] As for the manufacturing method of the poly-Si TFT with the center offset structure described above, the active layer may be formed using polycrystalline silicon which has an average metal planar density ranging from 10^{12} to $10^{15}/\text{cm}^2$.
- [26] As for the manufacturing method of the poly-Si TFT with the center offset structure described above, the metal in the polycrystalline silicon may be nickel.
- [27] Moreover, as for the manufacturing method of the poly-Si TFT with the center offset structure described above, a center offset region X in the active layer may not be doped with impurities.

Mode for the Invention

- [28] Hereinafter, a detailed description will be given of technical configurations and functional effects of the present invention.
- [29] According to the present invention, a poly-Si TFT with an inverse staggered structure may be manufactured in place of conventional poly-Si TFTs with coplanar structures.
- [30] Referring to FIGS. 3 and 4, FIG. 3 is a cross-sectional view illustrating an inverse staggered poly crystal TFT manufactured using a center offset according to the present invention, while FIG. 4 is a plan view illustrating a gate electrode and a center offset region of the TFT shown in FIG. 3.

- [31] As to manufacture of the TFT illustrated in the above figures, a buffer layer 20 is prepared above an insulated substrate 10. The buffer layer 20 may be formed using a silicon oxide film having a thickness of 200nm. Then, a gate electrode 30 is deposited on the buffer layer 20. The gate electrode 30 may be formed by depositing MoW to a thickness of 70nm and, in particular, may be patterned in order to form a center offset region X. The pattern of the gate electrode may produce a center offset structure, which preferably has a length of 0.1 to 5 μ m.
- [32] Next, a gate insulating film 40 is prepared over the gate electrode 30. Here, the gate insulating film may comprise a silicon oxide film. Continuously, an active layer 50 is placed on the gate insulating film 40 and an ohmic contact layer 60 is formed on top of the active layer 50. Then, source/drain electrodes 71 and 70 are placed on the ohmic contact layer 60 and a passivation layer 80 is prepared over the source/drain electrodes. The ohmic contact layer may be formed by directly depositing an n⁺ amorphous silicon based ohmic contact layer on the active layer.
- [33] The active layer 50 may generally comprise a poly-Si thin film and, in particular, the poly-Si thin film may be obtained by two different methods, that is, direct deposition of a poly-Si thin film and formation of a poly-Si thin film after crystallizing amorphous silicon into polycrystalline silicon.
- [34] The direct deposition of the poly-Si thin film may be conducted as follows: depositing a silicon oxide film to a thickness of 200nm as the gate insulating film 40 over the gate electrode 30; depositing a polycrystalline silicon layer to a thickness of 100nm as the active layer 50 on the deposited silicon oxide film; and then depositing phosphorous-doped amorphous silicon to a thickness of 50nm thereon to form the ohmic contact layer 60. Next, after dry etching the active layer 50, Cr is deposited to a thickness of 100nm to form the source/drain electrodes, followed by patterning the electrodes. Back Channel Etching (BCE) is performed using the pattern of the source/drain electrodes 71 and 70 in order to etch the phosphorus doped amorphous silicon constituting the ohmic contact layer 60 around a channel. The exposed active layer 50 is protected using the passivation layer 80 prepared by depositing a silicon nitride film to a thickness of 400nm. As a result, an inverse staggered poly-Si TFT may be manufactured.
- [35] As to fabrication of an active layer, an alternative method for preparation of a poly-Si thin film by crystallizing amorphous silicon into polycrystalline silicon, in place of the direct deposition, will be described in detail with reference to FIGS. 5 to 7.
- [36] Referring to FIG. 5, the gate 30 having a center offset pattern X is formed on the insulated substrate 10 having the buffer layer 20. A silicon oxide film as a gate insulating film 40 is deposited to a thickness of 200nm on a gate 30, amorphous silicon as an active layer 50a is deposited to a thickness of 100nm on top of the silicon oxide

film 40, and then, a silicon nitride film as a cover layer C is deposited to a thickness of 50nm over the amorphous silicon based active layer 50a. The deposited amorphous silicon may have a thickness of 30 to 100 μ m.

- [37] Following this, metal-induced crystallization using the cover layer C is performed to change the amorphous silicon 50a into polycrystalline silicon 50b. Briefly, heat treatment after metal deposition may crystallize amorphous silicon into polycrystalline silicon. Then, the cover layer C is removed as shown in FIG. 6.
- [38] After removing the cover layer C, the phosphorus doped amorphous silicon as an ohmic contact layer 60a is deposited to a thickness of 50nm, as shown in FIG. 7, followed by dry etching the same so as to form an active layer 50b. The source/drain electrodes are formed by depositing Cr to a thickness of 100nm and then patterning the deposited film. The deposited phosphorus-doped amorphous silicon 60a as the ohmic contact layer around a channel is dry-etched through BCE. In order to protect the exposed active layer, a passivation layer is prepared by depositing a silicon nitride film to a thickness of 400nm. As a result, a TFT having a center offset region according to the present invention as shown in FIG. 3 may be manufactured through the foregoing processes.
- [39] According to the manufacturing process of the present invention, deposition of polycrystalline silicon may be performed at a temperature in the range of 300 to 400°C and the polycrystalline silicon may have a mean metal planar density ranging from 10^{12} to $10^{15}/\text{cm}^2$. In this case, a metal fraction of the polycrystalline silicon may be nickel. The center offset region may not be doped with other impurities such as phosphorus or boron.
- [40] Although the present invention may form an offset in the middle of a channel using a pattern of a gate metal, such process for formation of offset is not included in additional processes according to the manufacturing method of the present invention.
- [41] A center offset region is correctly defined depending on gate patterning designs, thus completely solving a problem of varied offset region depending on different processes. The TFT manufactured in the present invention may desirably decrease leakage current which is a significant problem in a substrate for an active matrix organic light-emitting device (AMOLED) and/or an active matrix liquid crystal display (AMLCD).
- [42] Referring to FIG. 8, I-V characteristics of an inverse staggered poly-Si TFT without an offset are illustrated. It can be seen that undesirable leakage current is increased as a gate voltage increases in a negative direction.
- [43] Referring to FIG. 9, I-V characteristics of an inverse staggered poly-Si TFT with a center offset according to the present invention are illustrated. Compared to FIG. 8, it can be seen that leakage current is not increased even when gate voltage increases in a negative direction.

- [44] Although the present invention have been described in detail with reference to the foregoing exemplary embodiments, these exemplary embodiments are proposed for illustrative purpose only and those skilled in the art will appreciate that various modifications and variations are possible without departing from the scope and spirit of the invention. Accordingly, the scope of the present invention is not limited to the disclosed embodiments but may be defined only by the appended claims and their equivalents.

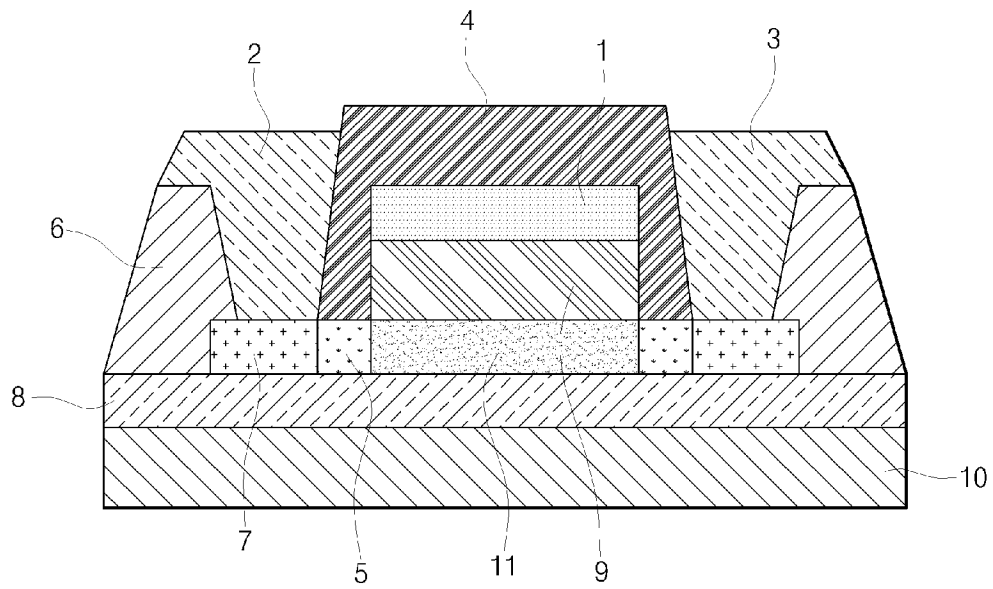
Industrial Applicability

- [45] As for a poly-Si TFT with an inverse staggered structure according to the present invention, a center offset is formed in the center of a gate so as to improve leakage current by a simple process. The present invention adopts a structure of positioning an offset region in the center of a gate pattern, thus not requiring additional processes. In addition, since the offset region is patterned, it may not be affected by further processes, thus embodying external merits thereof. Accordingly, the present invention may be favorably utilized in manufacture of a poly-Si TFT with an inverse staggered structure using a center offset to enable remarkably stable control of leakage current.

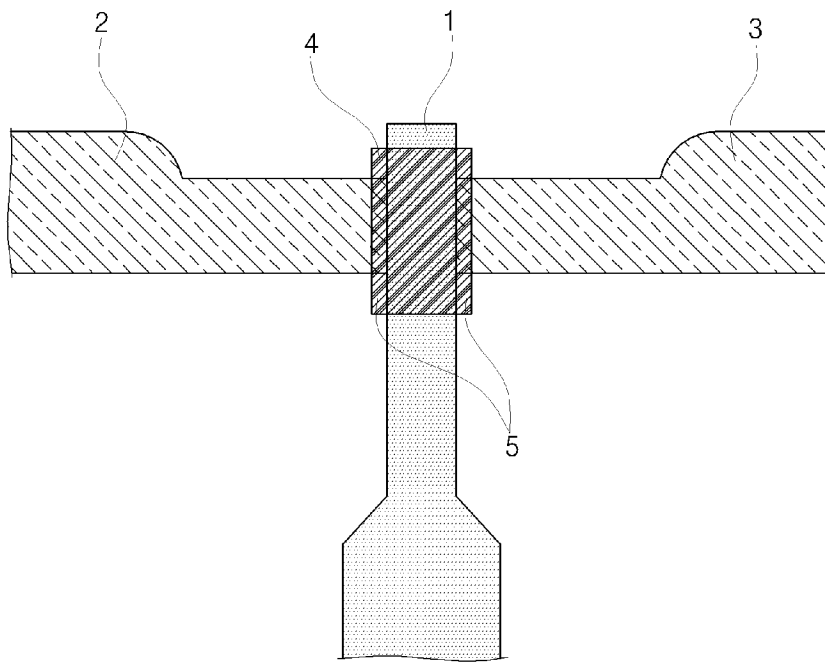
Claims

- [1] A method for manufacturing a poly-Si TFT with a center offset structure, comprising:
- (1) preparing a buffer layer on a substrate;
 - (2) preparing a gate electrode with a center offset structure on the buffer layer;
 - (3) forming a gate insulating film on the gate electrode;
 - (4) forming an active layer on the gate insulating film;
 - (5) depositing an n+ amorphous silicon based ohmic contact layer over the active layer;
 - (6) placing source/drain electrodes on the n+ amorphous silicon based ohmic contact layer; and
 - (7) forming a passivation film as a protective layer on the source/drain electrodes.
- [2] The method for manufacturing the poly-Si TFT according to claim 1, wherein the process (5) comprises directly depositing an amorphous silicon thin film on an n⁺ zone.
- [3] The method for manufacturing the poly-Si TFT according to claim 1 or 2, wherein the process (2) comprises using a pattern of the gate electrode to form the center offset structure with a thickness of 0.1 to 5 μm .
- [4] The method for manufacturing the poly-Si TFT according to claim 1 or 2, wherein the process (3) comprises using a silicon oxide film to form the gate insulating film.
- [5] The method for manufacturing the poly-Si TFT according to claim 1 or 2, wherein the active layer is formed using polycrystalline silicon which has an average metal planar density ranging from 10^{12} to $10^{15}/\text{cm}^2$.
- [6] The method for manufacturing the poly-Si TFT according to claim 5, wherein the metal in the polycrystalline silicon is nickel.
- [7] The method for manufacturing the poly-Si TFT according to claim 1 or 2, wherein a center offset region X in the active layer is not doped with impurities.

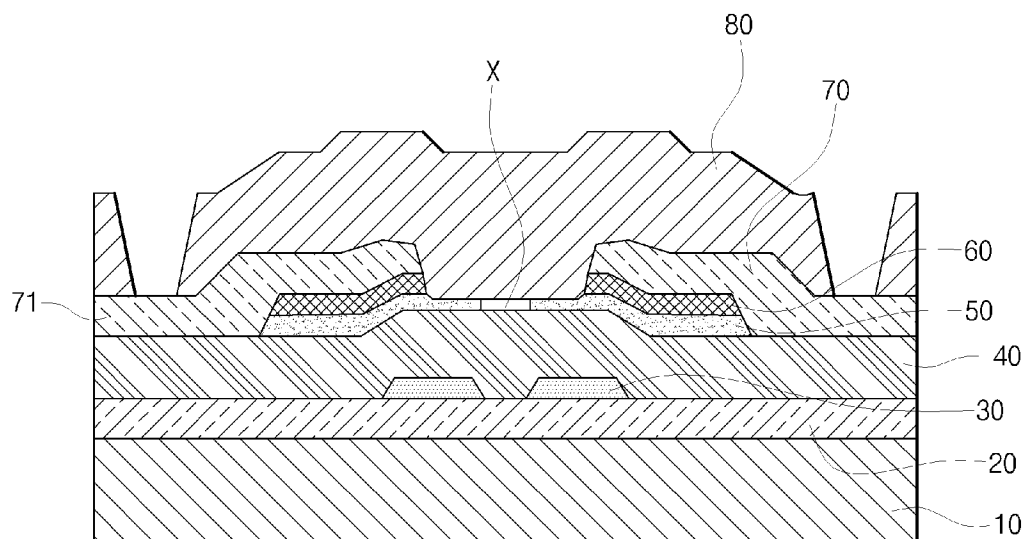
[Fig. 1]



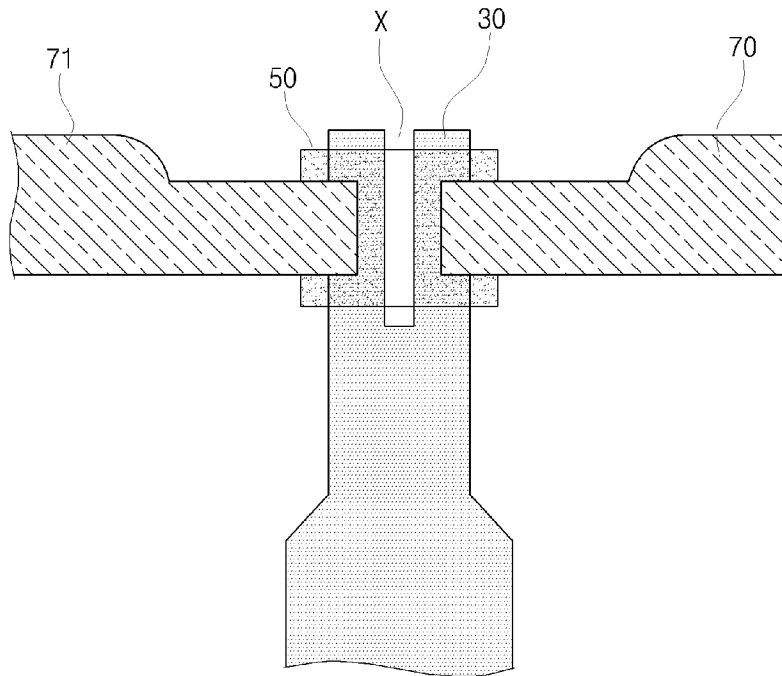
[Fig. 2]



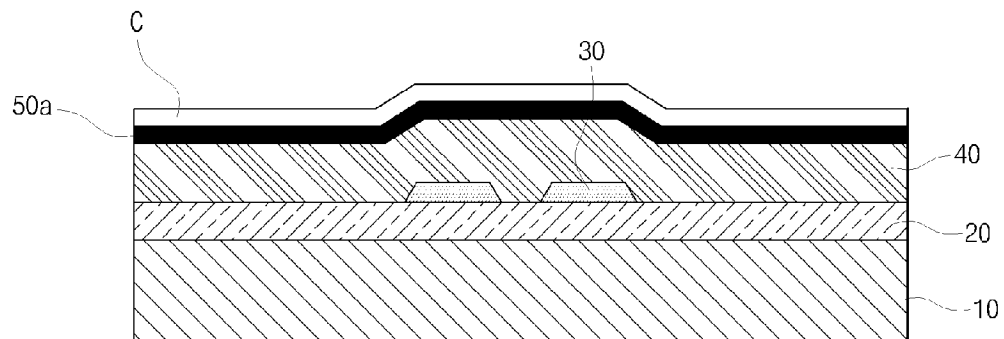
[Fig. 3]



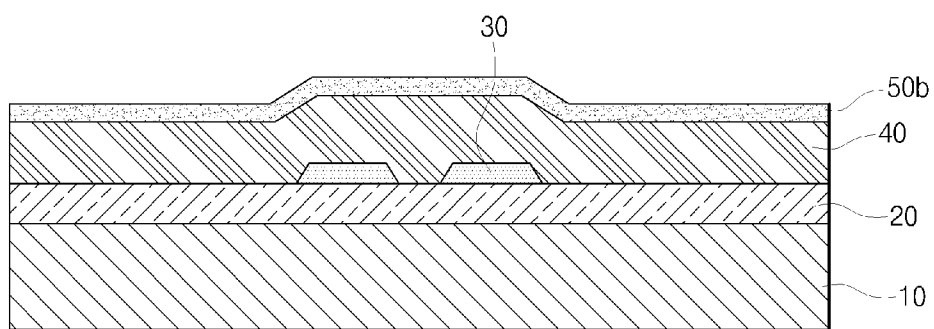
[Fig. 4]



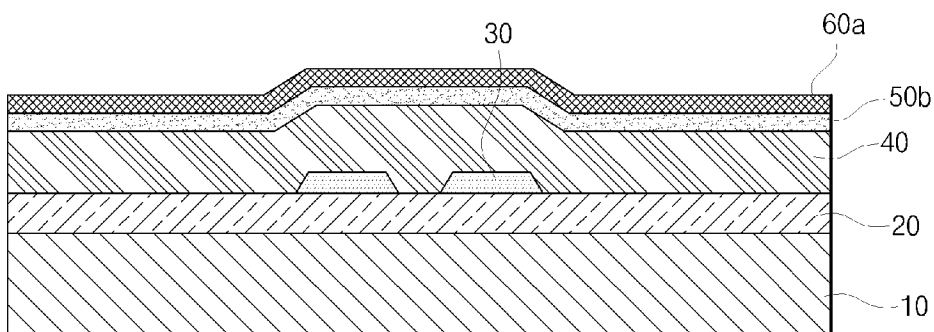
[Fig. 5]



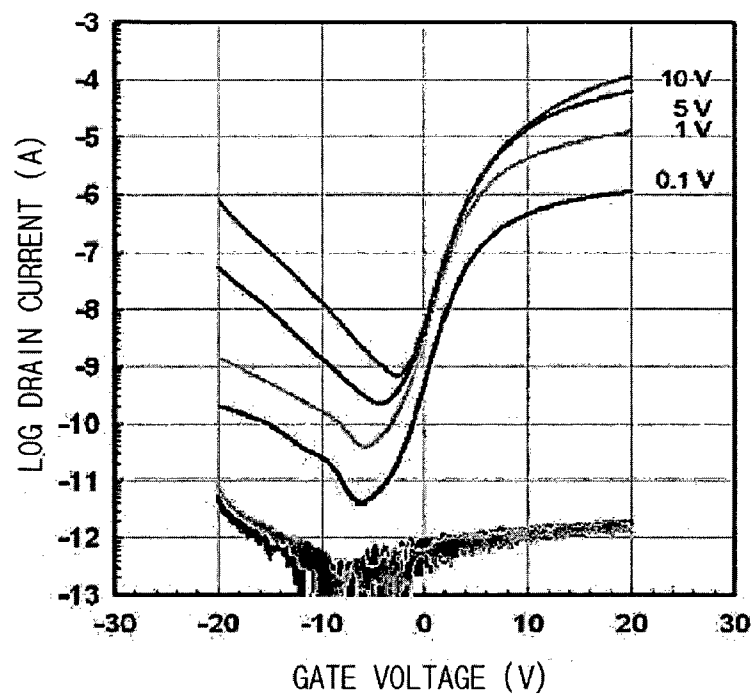
[Fig. 6]



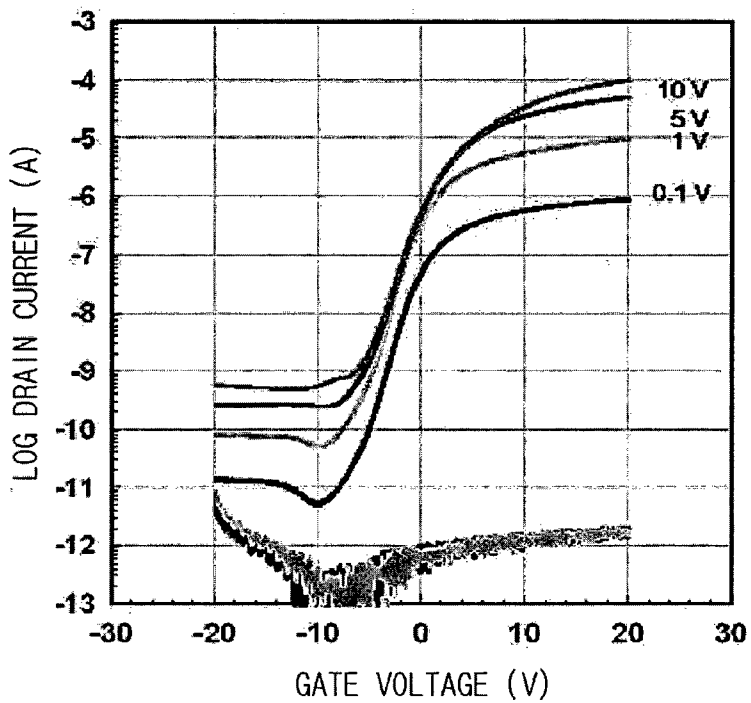
[Fig. 7]



[Fig.8]



[Fig.9]



A. CLASSIFICATION OF SUBJECT MATTER***H01L 29/78(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; G02F 1/136; G02F 1/1368; H01L 27/12; H01L 29/784; H01L 29/786

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models since 1975.

Japanese utility models and applications for utility models since 1975.

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: insulating , amorphous, buffer, passivation, TFT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 10-2006-0045688 A (NEC LCD TECHNOLOGIES, LTD.) 17 May 2006 See abstract, figures 5, 6, page 5, line 36-page 6, line 24 and claims 11-17	1-7
Y	KR 10-0161892 B1 (LG SEMICONDUCTOR CO., LTD.) 26 August 1998 See abstract, figure 2 and claim 1	1-7
A	JP 05-110095 A (SEIKO EPSON CORPOPRTION) 30 April 1993 See abstract, figures 1-5 and claims 1-6	1-7
A	US 6825893 B2 (CHOI BYEONG-DAE) 30 November 2004 See abstract, figures 1-11 and claims 1-8	1-7



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

22 DECEMBER 2009 (22.12.2009)

Date of mailing of the international search report

28 DECEMBER 2009 (28.12.2009)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2009/002255

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