A multi mode mobile computing device is disclosed. In a particular embodiment, the device includes a communication processor configured to facilitate wireless voice and data communication when the device is in a communication mode and an application processor configured to execute at least one computing application when the device is in a computing mode. The device further includes a configuration module configured to switch from the computing mode to the communication mode in response to user input of at least part of a telephone number.
Phone Mode?

Yes

App. Proc. Deenergized

No

A. P. Acts as Master; C.P. Treated as Peripheral

C.P. in Master Control of PLB and Necessary Peripheral

FIG. 3
MULTI MODE MOBILE COMPUTING DEVICE

I. CROSS REFERENCE TO RELATED APPLICATIONS


II. FIELD

[0002] The present disclosure relates generally to multi mode mobile computing devices such as wireless telephones that can also undertake ancillary computer functions.

III. DESCRIPTION OF RELATED ART

[0003] Multi mode mobile computing devices have been proposed which have multiple capabilities. For example, mobile telephones might be expected to undertake personal computing tasks now undertaken by notebook computers, in addition to their communication functions.

[0004] As recognized herein, multiple processors might be required to support multiple modes of operation. As also recognized herein, using the same internal operation independent of the operational mode means that a main processor typically functions as a master device that controls peripheral devices and that treats the other device processors (e.g., a telephone modem processor) as peripherals. Such a design requires that the main processor be active in all modes, including, e.g., the main processor needs to be active in the telephone mode, in which the modem processor is active, simply to provide the modem processor access to device hardware (e.g., a data display, non volatile storage, audio input/output) that is controlled by the main processor. In other words the main processor is mediating on behalf of the modem processor, because the hardware architecture does not allow the modem processor direct access to some of the hardware resources in the device.

[0005] As understood herein, it would be advantageous to minimize when possible, the use of hardware intermediaries (such as the main processor in the example above) to allow power efficient execution of tasks, to conserve the battery. Furthermore, requiring a single main processor to always function as a device master means that software and software changes that might apply only to a modem processor are coordinated or otherwise integrated with the main processor as well, complicating software management. In particular, the large base of software presently available for cellular phone type devices, which functions on the modem processor cannot be used unchanged in a device in which the modem processor is a peripheral to a main application processor.

IV. SUMMARY

[0006] In a particular embodiment, a multi mode mobile computing device that can also undertake ancillary computer functions is disclosed. The device includes a housing holding a battery and a communication processor that may be embodied in a module configured to facilitate wireless communication using the device. The communication processor module is supported on the housing and is powered by the battery. An application processor that may be embodied in a module is configured to execute applications is also supported on the housing and powered by the battery. A module in this description means a collection of hardware, assembled of discrete components or within an integrated circuit package, which performs a function through coordinated use of its hardware components. In a particular embodiment, a communication processor module includes a communications processor core in addition to other hardware resources that function as peripherals of the communications processor. Qualcomm’s MSM 3300, 5100, 5500 with an ARM processor core are examples of communications processor modules. An application processor module includes an application processor core together with assisting hardware. Qualcomm’s MSP1000 or IBM’s 405GP, which have ARM and PowerPC processor cores, are examples of application processor modules.

[0007] One particular advantage provided by at least one of the disclosed embodiments is that the device has a communication mode and a computing mode, and when the device is in the communication mode, a core of the application processor is not energized to conserve the battery. Accordingly, the application processor core is energized when the device is in the computing mode.

[0008] Another particular advantage provided by at least one of the disclosed embodiments is that the device allows the reuse of a large base legacy of application software by architecting the hardware so that it appears to the legacy software as it would in current single processor devices.

[0009] The present invention can allow the reuse of this large base legacy of application software by architecting the hardware so that it appears to the legacy software as it would in current single processor devices.

[0010] The communication processor module is associated with a memory bus that communicates with one or more memory devices and the application processor module is associated with a processor local bus (PLB). The preferred memory bus communicates with the PLB through hardware interfaces between the communication processor module and the application processor module. More specifically, the preferred memory bus communicates with a PLB bridge processor to facilitate the communication processor functioning as a master of the PLB. The communication processor can thereby access peripheral hardware associated with the PLB.

[0011] In another particular embodiment, a multi mode mobile computing device includes a housing holding a battery and a communication processor configured to facilitate wireless communication using the device. The communication processor is supported on the housing and is powered by the battery. An application processor is configured to execute applications, and the application processor is supported on the housing and powered by the battery. The device has at least a communication mode and a computing mode, and when the device is in the communication mode, the communication processor functions as a master processor.

[0012] In another particular embodiment, a method of operating a multi mode mobile computing device includes providing an application processor and a communication processor in a housing. The method also includes selectively establishing one of the processors as a master processor based on a mode of operation.

[0013] While the description of the invention is presented in the context of distinct communication and application processor modules, it is recognized that this is only done for clarity of exposition. In particular it is envisaged that the communication and application processor modules could be realized on the same integrated circuit module, whether this be through a multi-chip-module packaging technique or
through the design of the entire circuit as a single chip with both (application and communications) processor cores on it.

[0014] Other aspects, advantages, and features of the present disclosure will become apparent after review of the entire application, including the following sections: Brief Description of the Drawings, Detailed Description, and the Claims.

V. BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 is a block diagram of a particular illustrative embodiment of a multi mode mobile computing device;

[0016] FIG. 2 is a block diagram of a particular illustrative embodiment of a low power dual processor architecture for multi mode mobile computing devices; and

[0017] FIG. 3 is a flow diagram of a particular embodiment of a method for operating a multi mode mobile device in a computing mode and communication mode.

VI. DETAILED DESCRIPTION

[0018] Referring to FIG. 1, a mobile multi mode computing device is shown, generally designated 10. In a particular embodiment, the device 10 can be used to undertake wireless voice and/or data communication as well as personal computing application-based functions, such as but not limited to word processing. The device 10 includes a preferably lightweight portable housing 12 that holds the components discussed herein. A battery 14 can be engaged with the housing 12 to provide a source of power to the components disclosed below. The battery 14 preferably is rechargeable in accordance with portable computing principles known in the art, but when the device 10 is not connected to an electrical outlet, the battery 14 is the sole source of power to the components of the device 10.

[0019] A mode selector 16 can be provided on the housing 12. The mode selector 16 can be a user-manipulable input device to select the operational mode of the device 10, e.g., communication or computing. The mode selector 16 can be implemented in any number of ways, e.g., it can be a switch, or a portion of a touchscreen display that is used in conjunction with appropriate software to select the mode, or other equivalent input structure. The mode selector 16 can be automatically implemented by software responsive to the user’s activities, e.g., if the user starts to dial a number the mode selector can be software that automatically configures the device 10 in the communication mode.

[0020] Referring to FIG. 2, the device 10 includes a communication processor 18, preferably a type of processor referred to as a mobile system modem (MSM) that can access synchronous dynamic random access memory (SDRAM) 20 over, e.g., a 16/32 bit bus 22 and that can be implemented in a communication processor module. Also, the communication processor 18 can be active, as for instance, a 16 bit memory interface bus 24, MSM flash memory 26 and MSM static random access memory (SRAM) 28. Communication-related applications, such as the present assignee’s “BREW” applications, can be stored in one or more of the memories 20, 26, 28 for execution thereof by the communication processor 18.

[0021] As also shown in FIG. 2, the communication processor 18 accesses wireless communication circuitry 30 to effect wireless communication in accordance with means known in the art. In other words, the communication processor 18, associated memories 20, 26, and 28, and circuitry 30 establish a wireless voice and/or data communication portion, generally designated 32.

[0022] In an illustrative embodiment, the communication portion 32, also referred to as a mobile station (“MS”), is a mobile telephone-type device made by Kyocera, Samsung, or other manufacturer that uses Code Division Multiple Access (CDMA) principles and CDMA over-the-air (OTA) communication air interface protocols such as defined in, but not limited to, IS-95A, IS-95B, WCDMA, IS-2000, and others to communicate with wireless infrastructure, although the present invention applies to any wireless communication device.

[0023] For instance, the wireless communication systems to which the present invention can apply, in amplification to those noted above, include GSM, Personal Communications Service (PCS) and cellular systems, such as Analog Advanced Mobile Phone System (AMPS) and the following digital systems: CDMA, Time Division Multiple Access (TDMA), and hybrid systems that use both TDMA and CDMA technologies. A CDMA cellular system is described in the Telecommunications Industry Association/Electronic Industries Association (TIA/EIA) Standard IS-95. Combined AMPS and CDMA systems are described in TIA/EIA Standard IS-98. Other communications systems are described in the International Mobile Telecommunications System 2000/Universal Mobile Telecommunications Systems (IMT-2000/UM), standards covering what are referred to as wideband CDMA (WCDMA), cdma2000 (such as cdma2000 1x or 3x standards, for example) or TD-SCDMA.

[0024] A main processor 34 that can be embodied in a module holds an application processor core 36, which in one illustrative embodiment can be an IBM 405 LIP processor or equivalent. While FIG. 2 shows that the processors 18, 36 can be on separate chips from each other, it is to be appreciated that they can also be disposed on the same chip.

[0025] The application processor core 36 accesses one or more software applications that can be stored in various memories to execute the applications. For example, the application processor core 36 can access an SRAM/Flash memory 38 over, e.g., a 16-bit memory bus 40, and it can also access an SDRAM memory 42 (where software applications typically will be preferentially stored) over a preferably 32-bit bus 44.

[0026] FIG. 2 also illustrates that the application processor core 36 accesses a processor local bus (PLB) 46. In an illustrative embodiment, the PLB bus 46 can be a 64-bit bus. Various supporting devices and peripherals are accessed by the application processor core 36 using the PLB 46 in accordance with principles known in the art. For example, the PLB 46 (and, hence, application processor core 36) can be connected to a SDRAM controller 48 for controlling the SDRAM memory 42. Also, the PLB 46 can communicate with a personal computer memory card interface architecture (PCMCIA) interface or other storage interface 50. Moreover, the PLB 46 (and, hence, application processor core 36) can be connected to a liquid crystal display (LCD) controller 52, which drives an LCD display that can be provided on the housing of the device 10.

[0027] In addition to the components discussed above, the application processor 34 which bears the application processor core 36 can also hold an on-chip peripheral bus (OPB) 54 which in one non-limiting embodiment can be a 32 bit bus. The OPB 54 is connected to the PLB 46 through a PLB/OPB bridge device 56. The bridge device 56 can translate 32 bit
data to 64 bit data and vice versa. Various peripheral devices can communicate with the OPB 54. By way of non-limiting examples, a touch panel interface 58 can be connected to the OPB 54. Also, other storage interfaces 60 can be connected to the OPB 54. Further non-limiting examples of peripheral devices that can be connected to the OPB 54 include a USB, a UART, an interrupt (UC), and an AC97 device.

In a particular embodiment, the communication processor 18 can also communicate with the PLB 46 over its memory interface 24. As shown in FIG. 2, the memory interface 24 of the communication processor 18 is connected to the PLB 46 by a PLB bridge processor 62. In one illustrative embodiment, the PLB bridge processor 62 is implemented in hardware by a logic device, such as, e.g., a processor. In this way, the communication processor 18 can access the devices connected to the PLB 46. If desired, the functions of the PLB bridge processor 62 can be implemented by, e.g., a dedicated portion of the communication processor 18.

FIG. 3 shows the logic that is executed by the PLB bridge processor 62 to negotiate which processor 18, 36 controls the peripherals shown in FIG. 2. At decision diamond 64 it is determined whether the device 10 is in the communication mode as indicated by, e.g., the mode selector 16 or other user activity discussed above. If not, meaning that the device 10 is in the computing mode, the logic flows to block 66, wherein the PLB bridge processor 62 designates the application processor core 36 to be the master processor in control of the PLB 46 and OPB 54. In this mode, the communication processor 18 can be treated by the application processor core 36 as a peripheral device.

On the other hand, if the device 10 is in the communication mode, the logic moves from decision diamond 64 to block 68, wherein at least the application processor core 36 of the application processor 34 is deenergized. That is, in the communication mode, according to present principles the application processor core 36 is deenergized. Consequently, the communication processor 18 is assigned (by, e.g., the PLB bridge processor 62) the role of master processor at block 70, controlling the peripheral devices connected to the PLB 46 and OPB 54.

Those of skill would further appreciate that the various illustrative logical blocks, configurations, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, configurations, modules, circuits, steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in combination of the two. A software module may reside in random access memory (RAM), flash memory, read-only memory (ROM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable program-mable read-only memory (EEPROM), registers, hard disk, a removable disk, a compact disc read-only memory (CD-ROM), or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an application-specific integrated circuit (ASIC). The ASIC may reside in a computing device or a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a computing device or user terminal.

The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the disclosed embodiments. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the principles defined herein may be applied to other embodiments without departing from the scope of the disclosure. Thus, the present disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope possible consistent with the principles and novel features as defined by the following claims.

what is claimed is:

1. A multi mode mobile device configured to switch between a communication mode and a computing mode, the device comprising:
   a communication processor configured to facilitate wireless voice and data communication when the device is in the communication mode;
   an application processor configured to execute at least one computing application when the device is in the computing mode; and
   a configuration module configured to switch from the computing mode to the communication mode in response to user input of at least part of a telephone number.

2. The device of claim 1, wherein the application processor functions as a master processor and the communication processor functions as a peripheral processor when the device is in the computing mode.

3. The device of claim 2, wherein the application processor is deenergized when the device is in the communication mode to enable the communication processor to function as the master processor.

4. The device of claim 2, wherein the application processor is associated with a processor local bus (PLB), the device further comprising a PLB bridge processor configured to enable the communication processor to function as the master processor when the device is in the communication mode and to enable the communication processor to function as a peripheral processor when the device is in the computing mode.

5. The device of claim 4, wherein the communication processor is associated with a memory bus communicating with one or more memory devices, and wherein the PLB bridge processor is configured to bridge the memory bus to the PLB.

6. The device of claim 5, further comprising at least one peripheral hardware component connected to the PLB.

7. The device of claim 6, wherein the communication processor is further configured to access the at least one peripheral hardware component when the device is in the communication mode.
8. The device of claim 7, wherein the at least one peripheral hardware component includes at least one of a touch panel controller and a storage interface.

9. A multi mode mobile device configured to switch between a communication mode and a computing mode, the device comprising:
application processing means for executing at least one computing application when the device is in the computing mode;
communication processing means for facilitating wireless voice and data communication when the device is in the communication mode; and
means for switching the device from the computing mode to the communication mode in response to user input of at least part of telephone number.

10. The device of claim 9, wherein the application processing means functions as a master processor and the communication processing means functions as a peripheral processor when the device is in the computing mode.

11. The device of claim 10, wherein the application processing means is deenergized when the device is in the communication mode to enable the communication processing means to function as the master processor.

12. The device of claim 11, wherein the application processing means is associated with a processor local bus (PLB), the device further comprising a PLB bridge processing means for enabling the communication processing means to function as the master processor and the communication processing means to function as a peripheral processor when the device is in the computing mode.

13. The device of claim 12, wherein the communication processing means is associated with a memory bus communicating with one or more memory devices, and wherein the PLB bridge processing means comprises means for bridging the memory bus to the PLB.

14. The device of claim 13, further comprising at least one peripheral hardware component coupled to the PLB.

15. A method for operating a multi mode mobile device in a computing mode and a communication mode, the method comprising:
executing at least one computing application by an application processor in the computing mode;
switching from the computing mode to the communication mode in response to user input including at least a part of a telephone number; and
facilitating wireless voice and data communication using a communication processor in the communication mode.

16. The method of claim 15, wherein the application processor functions as a master processor and the communication processor functions as a peripheral processor when the device is in the computing mode.

17. The method of claim 16, wherein the application processor is deenergized when the device is in the communication mode to enable the communication processor to function as the master processor when the device is in the communication mode.

18. The method of claim 17, wherein the application processor is associated with a processor local bus (PLB), the method further comprising using a PLB bridge processor to enable the communication processor to function as the master processor and the communication processor to function as a peripheral processor when the device is in the computing mode.

19. The method of claim 18, wherein the communication processor is associated with a memory bus communicating with one or more memory devices, the method further comprising using the PLB bridge processor to bridge the memory bus to the PLB.

20. The method of claim 19, further comprising using the communication processor to access the at least one peripheral hardware component when the device is in the communication mode.

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