(54) Title: INEXACT ADDRESSABLE DIGITAL MEMORY

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(57) Abstract: A memory configuration for use in a computer system, the memory comprising a plurality of address decoders each of which is allocated an identifier having a predetermined number of bits, each bit having first and second selectable states, and a data memory having a plurality of word lines of predetermined length, each of the said address decoders being activatable to select one of the plurality of word lines, and the address decoders comprising means to receive an input address having a predetermined number of bits and means to compare the identifier of an address decoder with the input address wherein the memory further comprises means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier.

Published:

— with international search report
— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

(88) Date of publication of the international search report:

31 December 2003

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# INTERNATIONAL SEARCH REPORT

**A. CLASSIFICATION OF SUBJECT MATTER**
- IPC 7 G11C8/40 G06F12/02 G06F15/18

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**
- Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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<td>WO 90 04830 A (UNIV SPACE RES ASS) 3 May 1990 (1990-05-03) cited in the application page 24, line 1 - page 27, line 25; figure 1</td>
<td>1,15,16, 21</td>
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<td>US 5 829 009 A (FRAZIER GARY A) 27 October 1998 (1998-10-27) column 3, line 1-24; figure 2</td>
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Date of the actual completion of the international search: 16 October 2003

Date of mailing of the international search report: 28/10/2003

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