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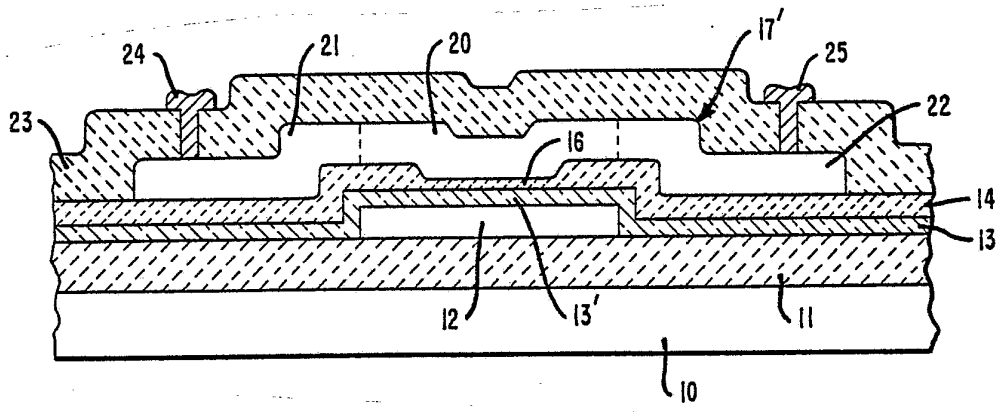

(57) Abstract

A nonvolatile memory device includes a substrate (10) provided with an insulator layer (11). A conductive gate (12) is located on the insulator layer (11) and has provided thereon a silicon nitride layer (13, 13') and a silicon dioxide layer (14) having a relatively thin central portion (16). Overlying the silicon dioxide layer is a recrystallized polysilicon layer (17') including a channel region (20) and source and drain regions (21, 22) having boundaries aligned with the boundaries of the gate (12). The device is manufactured by forming the layers successively, the thin oxide (16) being formed by oxidation of the underlying nitride (13') after removal of the thick oxide in the central portion above the gate (12). The polysilicon layer (17') is recrystallized by subjecting it to laser radiation prior to forming the source and drain regions (21, 22).

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NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

Technical Field

This invention relates to nonvolatile semiconductor memory devices.

The invention also relates to a method of making a nonvolatile semiconductor memory device.

Background Art

Metal-nitride-oxide-semiconductor (MNOS) memory devices and their silicon gate counterpart (SNOS) devices are well-known non-volatile memory devices capable of storing charges in a thin memory oxide sandwiched between the nitride film and the semiconductor substrate. (Hereafter, MNOS includes SNOS). An MNOS transistor and a method of making same are disclosed in U.S. Patent Specification No. 3,719,866. The conventional process of fabricating a SNOS device typically involves the use of monocrystalline silicon starting material and after forming thick silicon dioxide regions which electrically isolate adjacent devices on the semiconductor chip (typically, by localized oxidation of silicon process) a thin (of the order of about 25 Angstroms) memory oxide film is grown over the gate region by thermal oxidation of the silicon substrate. Another technique of forming the memory oxide is by chemical vapor deposition. Immediately after forming the memory oxide a relatively thick (of the order of 400 Angstroms) silicon nitride is deposited on the oxide film by, for example, low pressure chemical vapor deposition (LPCVD) followed by metal/polysilicon gate formation on the nitride layer.

In the above conventional SNOS process when the memory oxide is formed by thermal oxidation of the silicon substrate, the oxide is invariably not stoichiometric SiO_2 but contains free silicon. Presence of

free silicon in the memory oxide deleteriously affects the charge retention characteristic of the memory device. Another disadvantage of forming the memory oxide by thermal oxidation of the silicon substrate is that it is difficult to control the oxide thickness due to high rate of silicon oxidation even at relatively low temperatures. Likewise, when the memory oxide is formed by CVD, the ultra-thin nature (typically 4-5 atoms thick) of the memory oxide necessitates very careful control of the oxide deposition. In addition, both these memory oxide forming techniques present serious difficulties in forming a uniform oxide free of pin holes and other defects. In other words, the prior art technique of forming the SNOS device memory oxide is disadvantageous due to lack of oxide integrity and/or the oxide thickness uncertainty. Since the thickness of the memory oxide determines the retention and speed of the device, uncertainty in memory oxide thickness introduces uncertainties in the device characteristics. Yet another disadvantage of the conventional SNOS scheme is the requirement of using a substrate of monolithic silicon material having only single crystals and which has relatively good electrical conductivity, high purity, etc. in order to achieve the necessary high performance (by high operational speed, etc.) of the memory device built thereon. All of these requirements add to the cost of the integrated circuit chip.

Disclosure of the Invention

According to one aspect of the present invention, there is provided a nonvolatile semiconductor memory device, characterized by: a substrate; a conductive gate overlying a portion of said substrate; a gate insulator layer overlying said gate and an adjacent portion of said substrate, said gate insulator layer having a relatively thin memory portion

overlying a central portion of said gate and a relatively thick non-memory portion overlying the remaining portion of said gate; and a conductive silicon layer overlying said gate insulator layer.

It will be appreciated that a nonvolatile memory device in accordance with the invention has the advantage of avoiding the need for a monolithic single crystal silicon substrate.

According to another aspect of the present invention, there is provided a method of making a nonvolatile semiconductor memory device, characterized by the steps of: providing a substrate; forming a conductive gate on said substrate; forming a dielectric layer on said gate and an adjacent portion of said substrate, said dielectric layer having a relatively thin memory section overlying a central portion of said gate and a relatively thick non-memory portion overlying the remaining portion of said gate; forming a doped polysilicon layer on said dielectric layer; and converting said polysilicon layer into recrystallized silicon.

One embodiment of the present invention comprises a nonvolatile memory trigate field effect transistor fabricated in laser-beam recrystallized silicon-on-insulator. The device comprises a thick insulating layer formed on a silicon/non-silicon substrate and having a conductive polysilicon gate electrode thereon. Overlying the gate is a multiple dielectric layer (e.g., nitride-oxynitride-oxide or nitride-oxide) consisting of a relatively thin memory section and relatively thick non-memory sections abutting the memory section and serving as the memory device gate insulator. Overlying the gate insulator is a relatively thick doped and laser-beam recrystallized silicon layer having source and drain formed in alignment with the gate and the region between the source and drain serving as the channel. This memory

transistor has excellent charge retention, superior to the conventional SNOS transistors and offers high density design capability. Furthermore, the device is highly reliable, accurately reproducible and economically viable.

One example of the fabrication method of the above memory transistor is as follows. Starting from a low expansivity substrate material (there is no requirement that the substrate be silicon) a thick insulating layer such as silicon dioxide or silicon nitride is formed thereon. Then, a highly doped polysilicon gate is formed followed by deposition of a nitride layer over the gate and the insulating layer not covered by the gate. Next, a relatively thick silicon dioxide layer is formed over the nitride. Thereafter, the thick oxide overlying a central (memory) section of the gate is removed thereby exposing the nitride thereunder. The structure is then subjected to an oxidation step to convert in a controlled and slow manner the upper surface of the exposed nitride into a thin oxide layer. The thin oxide and nitride layers thus formed serve as the memory dielectric layers for the device. Thereafter, a relatively thick doped polysilicon layer is formed over the entire structure and it is subjected to a laser-beam anneal step to form recrystallized silicon. (Prior to laser anneal an encapsulant anti-reflective coating of nitride may be formed on the polysilicon layer.) The recrystallized silicon layer is then patterned into the transistor active area followed by masking the channel region with an implantation mask and forming source and drain regions therein.

Brief Description of the Drawings

One embodiment of the invention will now be described with reference to the accompanying drawings, in which:

Figs. 1-6 are cross-sectional representations of the sequential steps of fabricating a nonvolatile field effect transistor.

Best Mode for Carrying Out the Invention

Table I is an outline of the process sequence for forming a laser-beam recrystallized SOI nonvolatile silicon trigate n-FET memory device. It should be noted that many of the techniques for implementing the various steps of the fabrication method are well-known in the art and may be implemented in a number of different ways which are readily apparent to those of ordinary skill in the art.

The thickness and other dimensions shown in the figures are selected for clarity of illustration and not to be interpreted in a limiting sense. The dimensions can be larger or smaller depending upon the operating environment in which the device is going to be used.

TABLE I

PROCESS FLOWCHART FOR LASER-BEAM RECRYSTALLIZED SOI NONVOLATILE MEMORY DEVICE

1. Starting material: e.g., a high temperature glass
2. Isolation oxide formation (Fig. 1) (Optional)
3. Doped polysilicon gate formation (Fig. 1)
4. Memory nitride deposition (Fig. 2)
5. Thick LPCVD oxide formation over the nitride (Fig. 2)
6. Removal of LPCVD oxide over the memory section (Fig. 2)
7. Memory oxide formation over the nitride in the memory section (Fig. 3)
8. Polysilicon layer formation (Fig. 3)

9. Implantation of polysilicon layer with p-type (e.g. boron) ions (Fig. 3)
10. Anti-reflective nitride cap formation over polysilicon (Fig. 4)
11. Laser-beam recrystallization of polysilicon layer (Fig. 4)
12. Removal of nitride cap (Fig. 5)
13. Patterning recrystallized silicon into the device active area (Fig. 5)
14. Formation of implant mask over the recrystallized silicon layer in alignment with the gate (Fig. 5)
15. Implantation of n-type (e.g., phosphorus) ions in the unmasked recrystallized silicon forming source and drain (Fig. 5)
16. Removal of implant mask (Fig. 6)
17. Formation of low temperature oxide (Fig. 6)
18. Formation of contact holes and metallization (Fig. 6)

The starting material i.e., the substrate is a wafer of a material having a low coefficient of thermal expansion comparable to that of materials such as silicon dioxide and silicon nitride. In other words, the expansivity of the substrate material should not only be low but should match the expansivities of various material layers that will be formed on the substrate lest these various overlying layers are prone to cracking. Suitable substrate materials are silicon, high temperature glasses, aluminum oxide and ceramics. In the figures, the substrate 10 represents only a small undivided part of the wafer. After appropriate cleaning, a thick layer 11 of insulating material such as silicon dioxide or silicon nitride is formed on the substrate 10 (step 2). Typical thickness of insulator layer 11 is about 10,000 Angstroms (1 micron). If layer 11 is oxide, it may be formed by chemical vapor deposition or in the case where the

substrate 10 is silicon, by a high temperature (about 1,000 degrees C) oxidation of the silicon. Layer 11 is called the isolation oxide and it electrically isolates/insulates the memory device from the substrate 10 and the peripheral circuitry. Layer 11 may be omitted if the substrate 10 is a high temperature glass material since in this case the substrate itself is capable of providing the necessary electrical isolation of the devices thereon. A polysilicon layer (hereafter, polysilicon I) of about 3,000 Angstroms is then formed, by a conventional process, such as LPCVD, over the entire surface of layer 11. Another technique of forming polysilicon I layer is by forming a thicker (of thickness of about 3,500 Angstroms) polysilicon layer over the oxide 11 and then oxidizing the nascent polysilicon I at a temperature of about 1000 degrees C for a period of time. During this oxidation step, an oxide layer is formed on the polysilicon I by consumption of a surface layer of polysilicon I. Thereafter, the oxide on polysilicon I is etched off by conventional techniques. The polysilicon I layer formed in this manner will be free of surface asperities and spikes which could cause leakage currents and premature breakdown of the overlying gate dielectric layers (to be formed). The final thickness of polysilicon I formed in this manner is about 3,000 Angstroms.

Next, the polysilicon I layer is delineated and patterned into a polysilicon gate electrode 12 by conventional photolithographic and etching techniques. Gate electrode 12 is then doped, for example, by implanting with phosphorus ions of energy about 100 keV and dose 1.4 X 10^{16} ions per square cm (step 3).

Referring now to Fig. 2, after forming the polysilicon gate 12, a silicon nitride layer 13 (about 400 Angstroms thick) is deposited (step 4) on the gate 12 and the isolation oxide 11 not covered by gate 12

by conventional LPCVD at a temperature of about 750 degrees C and a pressure of about 400 millitorr.

Thereafter, referring to Fig. 2, a relatively thick (of thickness in the range 700-800 Angstroms) silicon dioxide layer 14 is formed over the nitride 13 (step 5). An exemplary technique of forming the oxide 14 is by LPCVD at a pressure of about 300 millitorr and a low temperature of about 420 degrees C using a reactant gas mixture of silane and oxygen.

Next, referring to Fig. 2, the LPCVD oxide layer 14 overlying the nitride and corresponding to a central section 15-15 of the gate 12 is removed (step 6) by using conventional photolithographic and etching techniques thereby, exposing the portion designated by numeral 13' of the nitride 13.

Next, as shown in Fig. 3, a thin (of thickness 10-40 Angstroms) oxide 16 is formed (step 7) over the exposed nitride portion 13'. The thin oxide 16 and the nitride portion 13' thereunder constitute the memory section of the gate insulator 14/16-13/13'. The thick oxide 16 and the nitride 13 therebeneath and overlying the gate 12 constitute the non-memory sections of the gate insulator 14/16-13/13'. One technique of forming the memory oxide 16 is by CVD. Another technique of forming the oxide 16 is by conversion treatment of the exposed nitride 13'. This is achieved by oxidizing the exposed nitride portion 13', for example, at a temperature of about 1,000 degrees C in wet oxygen for a period of about 30 minutes, thereby converting the upper portion of the exposed nitride 13' into an oxide layer 16 of about 20 Angstroms thickness. Both these techniques of forming the memory oxide will yield a highly stoichiometric SiO_2 unlike the memory oxide formed in the conventional SNOS process by oxidation of the silicon substrate which yields a composite layer of silicon-rich oxide

and a non-stoichiometric SiO_2. Forming memory oxide 16 by the conversion treatment technique is preferable to the CVD technique since it provides a much better control of the oxide 16 thickness than the CVD technique. Further, the conversion treatment technique of forming the oxide results in an ultra-thin transition layer of silicon oxynitride (not shown) sandwiched between the exposed nitride 13' and oxide 16 which is highly desirable as a memory dielectric layer. Another benefit of the conversion treatment technique is that during this step (step 7) the thick (non-memory) oxide 14 over the remainder (i.e. unexposed portion) of the nitride 13 will be densified.

Immediately after forming the memory oxide layer 16 as shown in Fig. 3, a second polysilicon layer 17 (hereafter, polysilicon II) of thickness about 4,500-5,000 Angstroms is formed over the memory oxide 16 and the thick oxide 14 by a conventional technique such as LPCVD (step 8). Forming the polysilicon immediately is essential for minimizing impurities on the memory oxide 16. Polysilicon II layer 17 is then doped lightly by ion implantation technique using, for example, boron ions of energy 35 keV and dose about (1-20) X 10^{12} ions per square cm (step 9). This doping provides the necessary conductivity for the polysilicon II layer 17 for forming a channel in correspondence with the underlying gate electrode 12.

Thereafter, as shown in Fig. 4, the polysilicon II layer 17 is capped with a nitride layer 18 of thickness of about 400-450 Angstroms and formed by a conventional process such as LPCVD (step 10). The nitride 18 is necessary for providing an anti-reflective coating over the polysilicon II layer 17 during the process step (step 11) of laser-beam recrystallization of polysilicon II layer 17 which ensues next.

Then, the polysilicon II layer 17 is exposed to a laser beam (step 11) to transform this layer from

a polycrystalline silicon material into a material having single crystal islands. One example of the laser-beam recrystallization technique is mounting the wafer on a chuck heated to a temperature of about 500 degrees C and using a continuous wave argon laser of spot size 45 microns, step size (i.e., displacement in the Y-direction) of 20 microns, beam power of about 4.5 watts and scanning the wafer (in the X-direction) at a speed of about 200 cm/sec. During the laser-beam recrystallization step, the high intensity of the laser beam will cause localized (i.e., non-uniform) heating of the polysilicon II layer 17 to a temperature exceeding about 1400 degrees C and will convert localized regions of polysilicon II layer 17 from a solid to molten state. Upon cooling, these regions will recrystallize into a matrix of crystallites having various crystal orientations. The polysilicon II layer 17 recrystallized in this manner will be of device-quality material and will hereinafter be referred to as recrystallized silicon layer 17. During this laser beam recrystallization step, the polysilicon gate 12, due to its proximity to the polysilicon II layer 17 (note, the gate 12 is separated from layer 17 by only about 400-450 Angstroms thick memory insulator 13'-16 and about 700-850 Angstroms thick non-memory insulator 13-14) may also be recrystallized. However, laser recrystallization of polysilicon gate 12 will have no deleterious effect on the device performance.

Other techniques of transforming the polysilicon II layer 17 (Fig. 4) into recrystallized device-quality silicon which can be advantageously used in place of the laser beam include the e-beam, graphite strip heater and quartz lamp techniques.

Next, the nitride cap 18 is removed using concentrated hydrofluoric acid (step 12). Then, the recrystallized silicon II layer 17 is patterned by

conventional photolithographic and etching techniques into the configuration 17' shown in Fig. 5 (step 13). The configuration 17' constitutes the active area of the field effect transistor that will be formed thereon.

Thereafter, as shown in Fig. 5, an implant mask 19 is formed over the recrystallized silicon layer 17' in correspondence with the gate 12 (step 14). One suitable implant mask is a layer of photoresist material formed over the entire structure and delineated into the configuration shown in Fig. 5 by conventional techniques. Another suitable implant mask is a layer of silicon dioxide. To form an oxide implant mask, a layer of undoped silicon dioxide of thickness about 9,000-10,000 Angstroms is formed over the structure and then patterned by conventional photolithographic and etching techniques into the configuration shown in Fig. 5. Regardless of whether a photoresist or oxide implant mask is used, the implant mask 19 needs to be perfectly aligned with the gate 12. In other words, the implant mask 19 is formed to protect the channel region 20 from being doped during the source-drain implantation step (step 15) that follows next. This critical alignment is necessary also to ensure that the source and drain are aligned with the gate.

After forming the implant mask 19, referring to Fig. 5, the structure is subjected to an n-type ion implantation step to form the source 21 and drain 22 in the recrystallized silicon layer 17' (step 15). The implantation step 15 typically is accomplished by using phosphorus ions of energy about 80-100 keV and dose about 1×10^{16} ions per square cm.

Referring to Figs. 5 and 6, the next step of the fabrication process is removal of the implant mask 19 (step 16) and forming a thick (typically about 9,000-10,000 Angstroms thickness) low temperature

oxide (LTO) layer 23 at a temperature of about 420 degrees C (step 17). The LTO 23 is then densified at a temperature of about 900 degrees C in a nitrogen environment. During this densification step, activation of the n-type ions introduced in the source and drain regions 21 and 22, respectively, is also achieved. Thereafter, contact holes are etched in the LTO 23 in correspondence with the source 21 and drain 22 and gate 12 (step 18). These contact areas are then enhanced to ensure good ohmic contact between the next-to-be-formed metal layer and these various elements 12, 21 and 22 of the memory device. The contact enhancement step typically involves phosphorus oxychloride ($POCl_3$) deposition and thermal diffusion such that the phosphorus ions from the $POCl_3$ layer diffuse into the various contact areas.

Thereafter, a layer of metal such as aluminum is formed over the structure. The metal is next delineated and thereafter alloyed into the areas of silicon with which it is in contact. Two such contacts 24 and 25 are shown in Fig. 6 which make electrical contact with source 21 and drain 22, respectively. The remainder of the process steps such as forming a passivation layer are well-known in the art and it is deemed unnecessary to describe them herein.

Having described a process of forming the laser-beam recrystallized SOI silicon gate field effect transistor, the operation of this memory element will now be traced. Referring to Fig. 6, in operation, for example, when a large (typically about 20-25 volts) positive polarizing potential of pulse width 1-100 milliseconds is applied between the gate 12 and the overlying recrystallized silicon i.e., the channel region 20 (the source 21 and drain 22 being maintained at ground potential), electrons from the recrystallized silicon region 20 will tunnel though the memory oxide 16 in the gate region and are

trapped at the oxide 16-nitride 13' interface, in any oxynitride present, and possibly in the nitride 13' bulk. The electrons so trapped will remain there even after removal of the polarizing potential and constitute the nonvolatile memory of the transistor. To erase this memory, a large (20-25 volts, 1-100 ms pulse duration) negative polarizing potential is applied to the gate 12 with respect to the recrystallized silicon region 20 whereupon the electrons trapped in the gate dielectric layers 13' and 16 will return to the silicon region 20 by back tunneling. It has been found that the trigate structure of the gate dielectric is essential for the erase operation. Without this structure the device will not erase once it has been written.

It is clear from the foregoing description of the operation of the memory device, the present laser-beam recrystallized SOI field effect transistor is quite similar in its mode of operation to the conventional SNOS FET. Consequently, the present device will be suitable for conveniently taking the place of conventional SNOS FET device without the requirement of any circuit modification.

By using the present process nonvolatile memory devices of excellent retention can be realized. Since the memory oxide 16 formed by thermal oxidation of the nitride 13' (all references to Fig. 6) it is of uniform thickness and of stoichiometric SiO_2 quality. Since the memory oxide 16 can be formed in a precisely controlled manner this process yields consistently reliable devices. Another advantage is that this process provides self-isolated devices on a chip since the recrystallized silicon 17' (Fig. 6), which essentially takes the place of the monolithic single crystal silicon substrate in conventional SNOS devices, is patterned into individual device active areas without physical connection between one device active area and

an adjacent one. This self-isolation scheme not only reduces the number of device fabrication steps but saves valuable chip real estate.

Although the description of this invention has been confined to a laser beam recrystallized SOI nonvolatile silicon gate n-FET and a process of making the same, this invention is suitable for fabricating its counterpart p-FET. Another modification which is within the realm of this invention is use, in place of the silicon gate, a gate made of a metal or refractory metal silicide.

Another modification is a common-gate, vertically stacked nonvolatile memory device pair formed in a piggy-back configuration. In this version of the present invention first the SNOS structure is formed, for example, on a p-type silicon substrate. Then, steps 4 through 18 (Table I) are accomplished to form a SOI structure thereon. In this configuration the single silicon gate serves as the common gate for the SNOS device and the SOI device.

CLAIMS:

1. A nonvolatile semiconductor memory device, characterized by: a substrate (10, 11); a conductive gate (12) overlying a portion of said substrate (10, 11); a gate insulator layer (13, 14) overlying said gate and an adjacent portion of said substrate (10, 11), said gate insulator layer (13, 14) having a relatively thin memory portion (13', 16) overlying a central portion of said gate (12) and a relatively thick non-memory portion overlying the remaining portion of said gate (12); and a conductive silicon layer (17') overlying said gate insulator layer (13, 14).

2. A nonvolatile semiconductor memory device according to claim 1, characterized in that said conductive silicon layer (17') is formed of recrystallized polysilicon.

3. A nonvolatile semiconductor memory device according to claim 1, characterized in that said gate (12) is formed of polysilicon.

4. A nonvolatile semiconductor memory device according to claim 1, characterized in that said conductive silicon layer includes a channel region (20) of a first conductivity type located between spaced-apart source and drain regions (21, 22) of a second conductivity type, said gate (12) being aligned with said channel region (20), whereby said device forms a nonvolatile field effect transistor.

5. A nonvolatile semiconductor memory device according to claim 4, characterized in that said first and second conductivity types are p-type and n-type respectively.

6. A nonvolatile semiconductor memory device according to claim 1, characterized in that said gate insulator layer includes a silicon nitride layer (13') having a uniform thickness and a silicon dioxide layer (14, 16) which has a relatively thin portion (16) overlying said central portion of said gate (12), said relatively thin portion (16) permitting charge transfer therethrough, and a relatively thick portion (14) overlying the remaining portion of said gate (12), said relatively thick portion (14) inhibiting charge transfer therethrough.

7. A nonvolatile semiconductor memory device according to claim 6, characterized by a thin silicon oxynitride layer permitting charge transfer therethrough and located between said silicon nitride layer (13') and the relatively thin portion (16) of said silicon dioxide layer.

8. A method of making a nonvolatile semiconductor memory device, characterized by the steps of: providing a substrate (10, 11); forming a conductive gate (12) on said substrate (10, 11); forming a dielectric layer (13, 14) on said gate and an adjacent portion of said substrate (10, 11), said dielectric layer (13, 14) having a relatively thin memory section (13', 16) overlying a central portion of said gate and a relatively thick non-memory portion overlying the remaining portion of said gate (12); forming a doped polysilicon layer (17') on said dielectric layer (13, 14); and converting said polysilicon layer into recrystallized silicon.

9. A method according to claim 8, characterized by the step of forming source and drain regions (21, 22) in the recrystallized silicon layer

(17'), said source and drain regions (21, 22) being separated by a channel region (20) in the recrystallized silicon.

10. A method according to claim 9, characterized in that said step of forming a dielectric layer includes the steps of forming a silicon nitride layer (13) overlying said gate (12) and an adjacent portion of said substrate (10, 11); forming a relatively thick silicon dioxide layer (14) on said silicon nitride layer (13), removing said relatively thick silicon dioxide layer (14) corresponding to a central portion of said gate (12); and thermally oxidizing the thereby exposed surface of said silicon nitride layer (13') to form a relatively thin silicon oxynitride-silicon dioxide dual layer on the exposed portion of the silicon nitride layer (13').

11. A method according to claim 8, characterized in that said substrate includes an insulator layer (11), said gate (12) being formed on said insulator layer (11).

FIG. 1

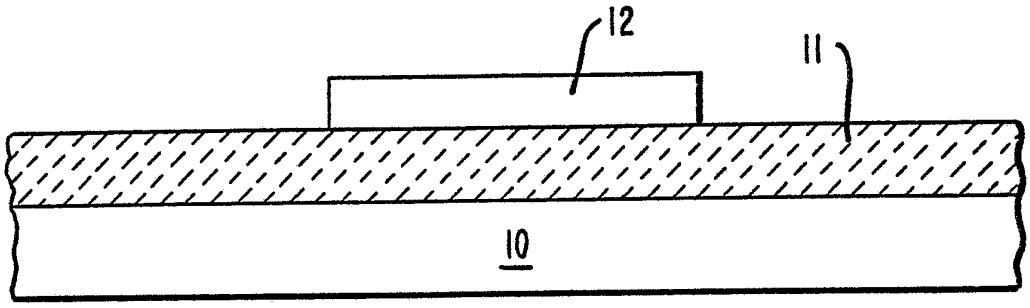


FIG. 2

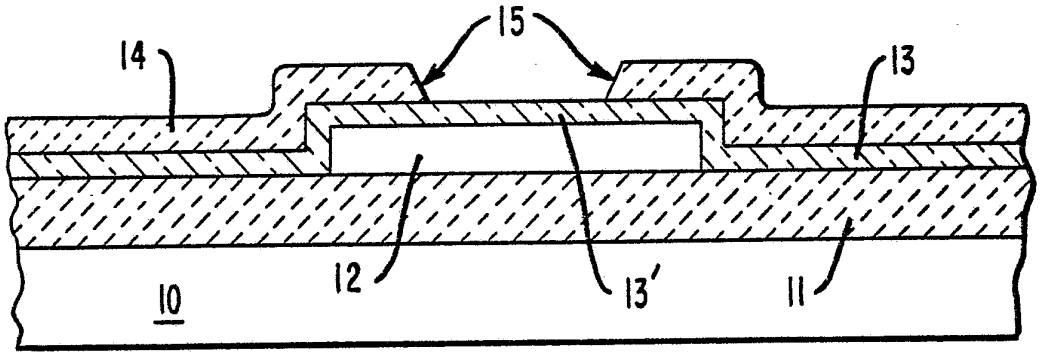
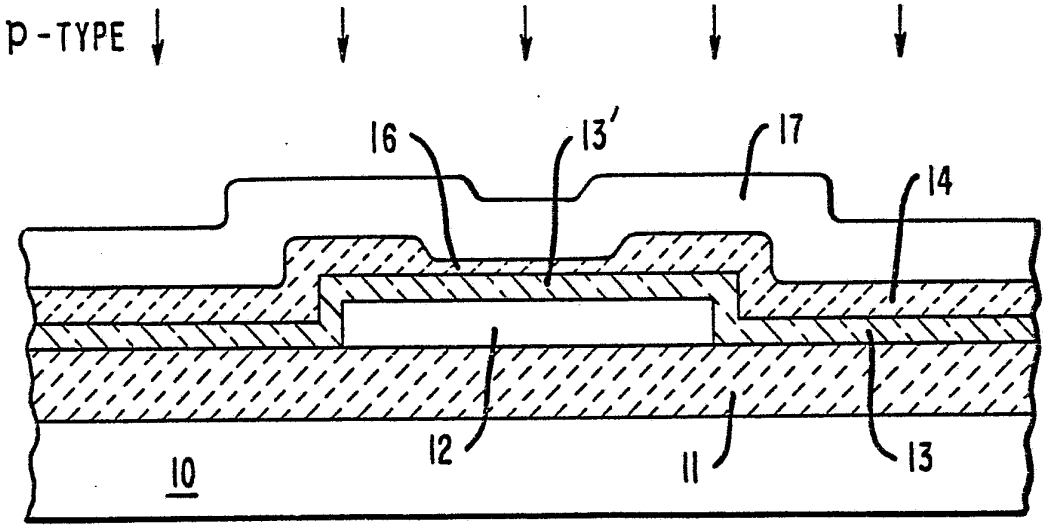


FIG. 3



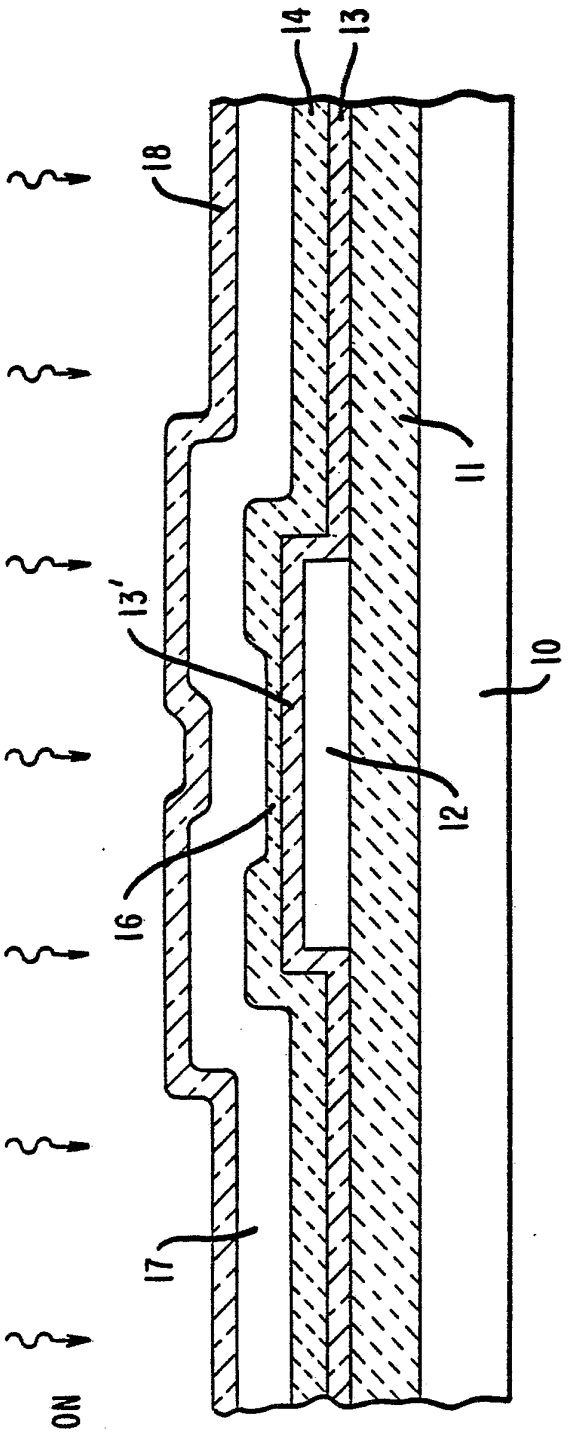


FIG. 4

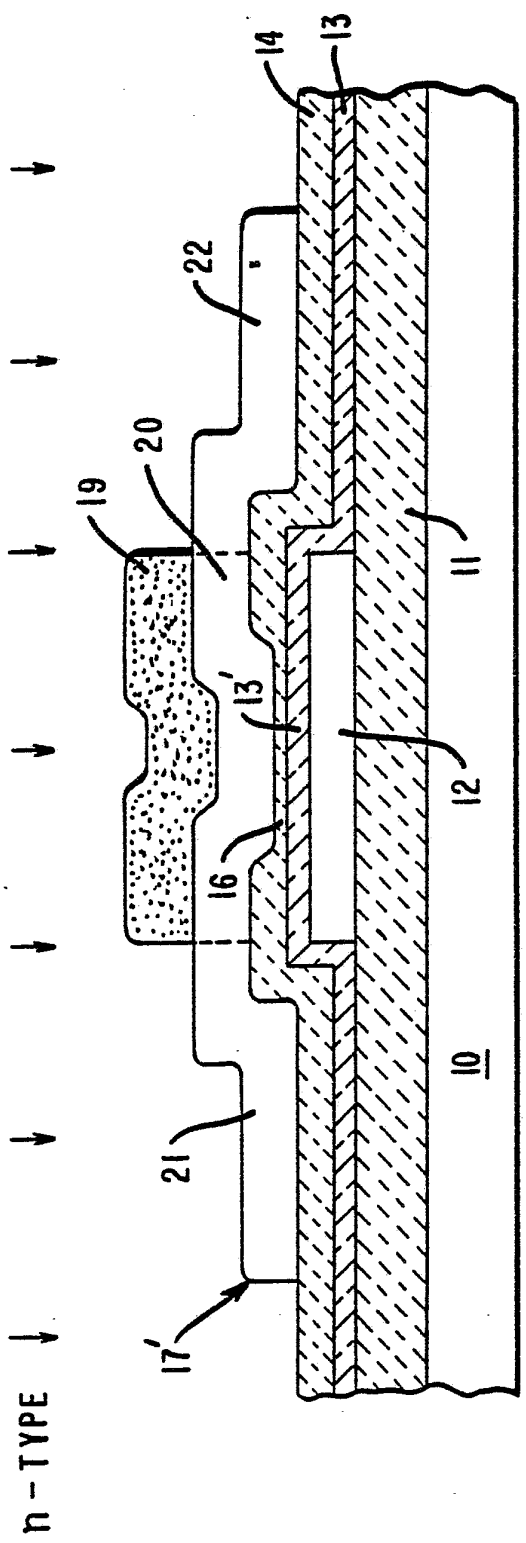


FIG. 5

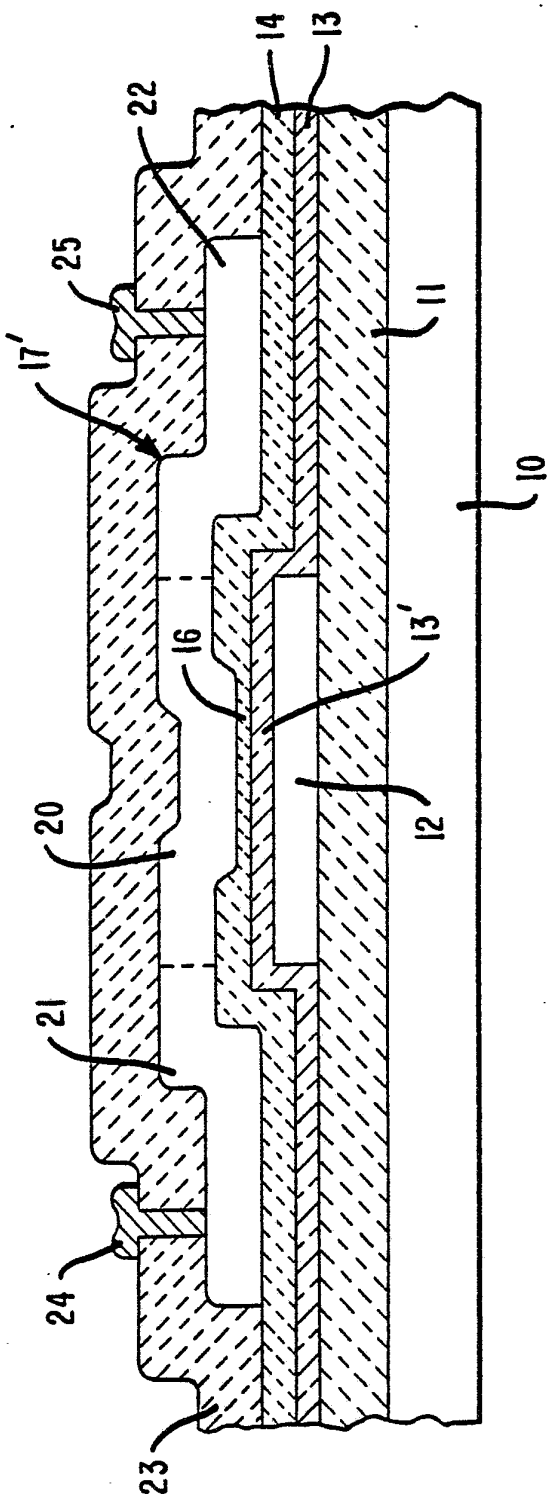


FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 84/00638

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[3]: G 11 C 11/34; H 01 L 29/60 // H 01 L 21/268

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC[3]	H 01 L; G 11 C

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	Patent Abstracts of Japan, vol. 6, no. 230, 6 November 1982 (Tokyo, JP) page E142 & JP, A, 57132365 (TOKYO SHIBAURA DENKI K.K.)	1
A	see abstract and figures 4 and 5	3-5
Y	US, A, 4096509 (THE UNITED STATES OF AMERICA AS REPRESENTED BY THE SECRETARY OF THE AIR FORCE) 20 June 1978 see claims 1-3; column 3, lines 1-17; figures 4-7	1
A		6-7,10
A	GB, A, 2064866 (THE GENERAL ELECTRIC COMPANY LTD.) 17 June 1981 see claims 1-3,5,7,12,13; page 1, lines 57-80; figure 5	1,2,8,9,11
A	IEEE Transactions on Electron Devices, vol. ED-24, no. 5, May 1977 (New York, US) P.C.Y. Chen: "Threshold-alterable Si Gate MOS devices", pages 584-586,	10 ./.

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
7th August 1984	04 SEP 1984
International Searching Authority [1]	**Signature of Authorized Officer [20]**
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

Form PCT/ISA/210 (second sheet) (October 1981)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No [18]
	see page 584, right-hand column, last paragraph; page 585, left-hand column, paragraph 1; figure 1B	
A	Japanese Journal of Applied Physics, vol. 18, no. 9, September 1979 (Tokyo, JP) H. Nakayama et al.: "Effects of nitride deposition conditions on characteristics of an MNOS nonvolatile memory transistor", pages 1773-1779, see page 1777, right-hand column	1

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 84/00638 (SA 7106)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 21/08/84

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4096509	20/06/78	None	
GB-A- 2064866	17/06/81	None	