

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
28 February 2002 (28.02.2002)

PCT

(10) International Publication Number
WO 02/17490 A2

(51) International Patent Classification⁷: **H03K 3/00**

(21) International Application Number: PCT/US01/26420

(22) International Filing Date: 23 August 2001 (23.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/645,226 24 August 2000 (24.08.2000) US

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(81) Designated States (*national*): CA, JP.

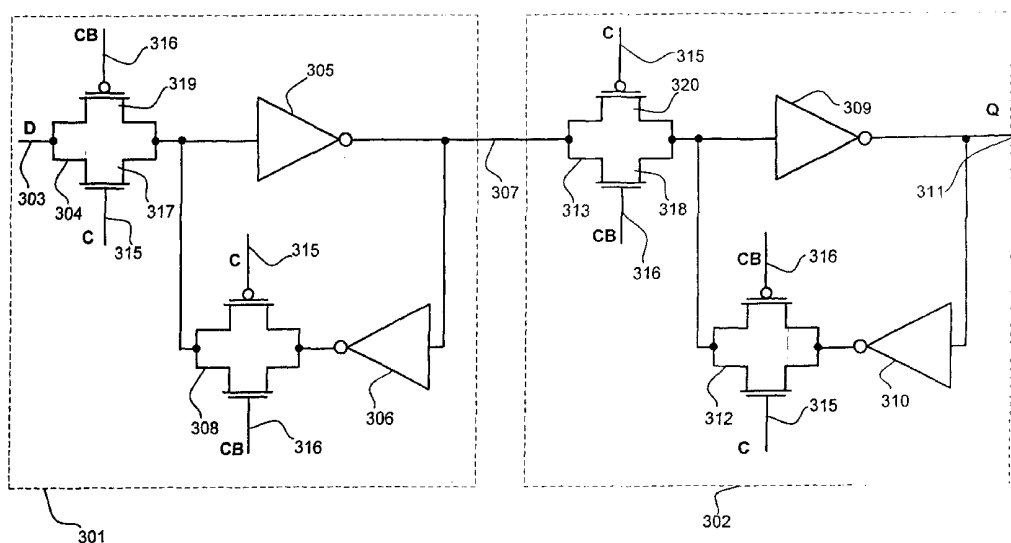
(84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYNCHRONIZING CIRCUIT FOR COMPLEMENTARY SIGNALS



(57) Abstract: A synchronization circuit is disclosed that helps synchronize true and complement input signals over a wide range of environmental and process conditions. This is preferably accomplished by synchronizing the input signals with active elements, wherein the active elements slow down the leading input signal and/or speeding up the lagging input signal to produce a synchronized output signal. Two or more of these synchronizing circuits may be used to provide synchronized complementary output signals, if desired.



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SYNCHRONIZING CIRCUIT FOR COMPLEMENTARY SIGNALS

Background of the Invention

The present invention generally relates to electronic digital circuits, and more particularly, to digital circuits that produce synchronized output signals.

5 Some digital circuits accept both true and complement signal as inputs. One such circuit is a conventional CMOS flip-flop circuit. Other circuits include, for example, differentially driven circuits, Complementary Pass-Transistor Logic (CPL) circuits, Dual-Pass-Transistor Logic (DPL) circuits, and others. The performance of such circuits can depend on the skew between the true and complement input signals.

10 Typically, a reduction in the skew or an increase in the synchronization between the true and complement signals may increase the performance of the circuit.

Figure 1 is a schematic diagram of a conventional positive edge triggered master-slave flip-flop. The flip-flop includes a master latch 301 and a slave latch 302. The output of the master latch 301 is coupled to the input of the slave latch 302. Both

15 the master latch 301 and the slave latch 302 receive true and complement clock signals. Because the master-slave flip-flop of Figure 1 is positive edge triggered, the master latch 301 is transparent and the slave latch 302 is latched when the clock signal 315 is high (and the complement clock signal 316 is low), and the master latch 301 is latched and the slave latch 302 is transparent when the clock signal 315 is low (and the

20 complement clock signal 316 is high).

The master latch 301 includes a pair of inverters 305 and 306. The output of the first inverter 305 is connected to the input of the second inverter 306 and also to the data input terminal 307 of the slave latch 302. The input of the first inverter 305 is coupled to the data input terminal 303 of the master latch 301 through transmission gate 304.

25 The output of the second inverter 306 is coupled to the input of the first inverter 305 via transmission gate 308.

Transmission gate 304 connects the data input terminal 303 of the master latch 301 to the input of the first inverter 305 when the clock signal 315 is high (and the complement clock signal 316 is low). When transmission gate 304 is closed,

30 transmission gate 308 is open, and vice versa. As such, transmission gate 308 isolates the output of inverter 306 from the input of inverter 305 when transmission gate 304 is closed. This eliminates the need for the signal entering the master latch 301 on input terminal 303 to overdrive the output of inverter 306, thereby reducing the setup time of

master latch 301. In this state, the master latch 301 is transparent, allowing the data input signal 303 to set the state of the cross-coupled inverters 305 and 306.

When the clock signal 315 transitions low (and thus the complement clock signal 316 transitions high), transmission gate 304 disconnects the data input terminal 303 from the input of the first inverter 305. Likewise, transmission gate 308 connects the output of inverter 306 to the input of inverter 305. In this state, the master latch 301 is latched, allowing the cross-coupled inverters 305 and 306 to store the state previously set by the data input signal 303.

Like the master latch 301, the slave latch 302 may also include a pair of cross-coupled inverters 309 and 310, as well as isolating transmission gates 312 and 313. Transmission gate 313 connects the input terminal 307 of the slave latch 302 to the input of the first inverter 309 when the clock signal 315 is low (and the complement clock signal 316 is high). When transmission gate 313 is closed, transmission gate 312 is open, and vice versa. As such, transmission gate 312 isolates the output of inverter 310 from the input of inverter 309 when transmission gate 313 is closed. This eliminates the need for the signal entering the slave latch 302 on input terminal 307 to overdrive the output of inverter 310, thereby reducing the setup time of slave latch 302. In this state, the slave latch 302 is transparent, allowing the data input signal 307 to set the state of the cross-coupled inverters 309 and 310.

When the clock signal 315 transitions low (and the complement clock signal 316 transitions high), transmission gate 313 disconnects the data input signal 307 of the slave latch 302 from the input of the first inverter 309. Likewise, transmission gate 312 connects the output of inverter 310 to the input of inverter 309. In this state, the slave latch 302 is latched, allowing the cross-coupled inverters 309 and 310 to store the state previously set by the data input signal 307.

During operation, the clock signal 315 may initially be high and the complement clock signal 316 may be low. At this time, the master latch 301 is transparent, allowing the data input signal 303 to enter the master latch 301 and set the state of the cross-coupled inverters 305 and 306. The slave latch 302 is in a latched state, preventing the output signal 307 of the master latch 301 from reaching the cross-coupled inverters 309 and 310 of the slave latch 302.

When the clock signal 315 falls (and the complement clock signal 316 rises), the transmission gate 304 disconnects the data input signal 303 from the pair of cross-coupled inverters 305 and 306. At about the same time, transmission gate 308 closes,

connecting the output of inverter 308 to the input of inverter 305. The pair of cross-coupled inverters 305 and 306 maintain or store the data state set during the setup period. Also, transmission gate 313 of the slave latch 302 closes, and transmission gate 312 opens. Thus, the data stored in the cross-coupled inverters 305 and 306 is allowed
5 to set the state of inverters 309 and 310. The clock-to-Q time for the master-slave flip-flop is defined as the time from the falling edge of the clock signal 315 (the rising edge of the complement clock signal 316) to when the data stored in the master latch 301 is available on the slave output terminal 311.

Typically, the data input signal 303 must be stable for a sufficient period of time
10 before the clock signal 315 falls. This time period is typically referred to as the setup time of the master-slave flip-flop. For the master-slave flip-flop shown in Figure 1, the setup time corresponds to about two gate delays, including the delay through the transmission gate 304 and the first inverter 305.

When the complementary control (e.g., clock) signals for transmission gates
15 304, 308, 312, and 313 are unsynchronized, both the setup time and clock-to-Q time may increase, thereby reducing the performance of the circuit. As indicated above, the setup time corresponds to the delay through the transmission gate 304 and the first inverter 305. The clock-to-Q time corresponds to the delay through the transmission gate 313 and inverter 309. Both of these paths include the delay through one
20 transmission gate.

With unsynchronized clock signals, the delay through the transmission gates may be dependent on the state of the signal that is transmitted. For example, the n-channel transistors 317 and 318 of transmission gates 304 and 313, respectively, tend to
25 transmit low signals more efficiently than high signals. Likewise, the p-channel transistors 319 and 320 of transmission gates 304 and 313 tend to transmit high signals more efficiently than low signals. As such, the signal reaching the transmission gate will not be transmitted efficiently until its favored transistor is turned on and saturated. Because both the setup time and clock-to-Q time are dependent on the delay through a transmission gate, the performance of the flip-flop may be dependent on the data state
30 of the flip-flop.

To reduce this dependency, various attempts have been made to produce synchronized complementary control signals. One such circuit is shown in Figure 2. The circuit of Figure 2 creates a true control signal and a complement control signal by inverting and buffering an input control signal a different number of times. Referring

specifically to Figure 2, input signal C enters the circuit at terminal 410. Inverter 412 inverts the input signal C to create CB, which is simultaneously passed to inverters 414 and 416. Following inversion by inverters 414 and 416, the signals are again inverted by inverters 418 and 420. Inverter 418 provides complement output signal CB 428.
5 Inverter 420 also provides a complement output signal CB, which is then inverted by inverter 424 to produce output signal C 426.

To provide some level of synchronization between the true and complement signals 426 and 428, a capacitor is inserted into the 'fast' path, i.e., the path that carries the signal that is subject to one less gate delay. In the example shown, capacitor 422 is
10 connected to the output of inverter 414. The capacitor 422 is preferably sized to provide about one gate delay to the output of inverter 414 in an attempt to synchronize signals C 426 and CB 428.

A limitation of the synchronizing circuit shown in Figure 2 is that the value of the capacitor 422 that is used to delay the 'fast' path by one gate delay does not track
15 the change in gate delay due to various environmental and process conditions such as temperature, supply voltage, transistor parameter variations, etc.

Another approach for providing synchronized complementary control signals is shown in Figure 3. The circuit of Figure 3 provides an input control signal, and creates a complement control signal by inverting and buffering the input control signal. A true
20 control signal is created by passing the input control signal through a pass-gate. Referring specifically to Figure 3, input signal CK_{in} enters the circuit at terminal 450. The input signal CK_{in} is simultaneously passed to the input of inverter 452 and to the input of pass gate 454. Inverter 452 inverts the input signal CK_{in} to create the complement control signal CKB 470. The pass gate 454 passes the input signal CK_{in} to
25 create the true control signal CK 472.

The pass gate 454 has a p-channel transistor 460 and an n-channel transistor 462 connected in a conventional pass gate configuration. The gate of the p-channel transistor 460 is tied to VDD, and the gate of the n-channel transistor 462 is tied to ground. Accordingly, both the p-channel transistor 460 and the n-channel transistor 462
30 are always "on". The purpose of the p-channel transistor 460 and the n-channel transistor 462 is to provide some resistance and/or capacitance in series with the true control signal CK. Like the capacitor of Figure 2, the resistance and/or capacitance provided by pass gate 454 tends to slow down the 'fast' path, i.e., the path that carries the signal that is subject to one less gate delay. This provides some level of

synchronization between the true and complement control signals 470 and 472. One such circuit is shown in Razavi et al., "A 13.4-GHz CMOS Frequency Divider", IEEE International Solid-State Circuits Conference, 1994.

5 A limitation of the synchronizing circuit shown in Figure 3 is that the resistance and/or capacitance provided by the pass gate 454 may not track the change in gate delay of inverter 452 over various environmental and process conditions such as temperature, supply voltage, transistor parameter variations, etc. Thus, the degree of synchronization between the true and complement control signals 470 and 472 may vary over such parameters. What would be desirable, therefore, is a synchronization circuit that helps
10 synchronizes true and complement signals over a wider range of environmental and process conditions.

Summary of the Invention

The present invention overcomes many disadvantages of the prior art by providing a synchronization circuit that helps synchronize true and complement input
15 signals over a wider range of environmental and process conditions. This is preferably accomplished by providing a circuit that receives unsynchronized complementary input signals and slows down the leading input signal and speeds up the lagging input signal. By slowing down the leading input signal and speeding up the lagging input signal, the circuit provides complementary output signals that are more synchronized. And
20 advantage of this approach is that the synchronizing circuit can provide synchronization over a wider range of environmental and process conditions.

The leading input signal is preferably slowed down by providing a mechanism for impeding the transition of the output signal until the lagging input signal arrives. One way of accomplishing this is to provide a switching element such as a source
25 follower that is controlled by the lagging input signal. The switching element is connected so as to promote the present state of the output signal until the lagging input signal arrives. Once the lagging input signal arrives, the switching element preferably turns off, and another switching element switches turns on to promote the transition of the output signal when the lagging input signal arrives. This latter switching element
30 preferably speeds up the transition once the lagging input signal arrives. Thus, the transition of the output signal is impeded until the lagging input signal arrives, and then is promoted once the lagging input signal arrives.

It is contemplated that the leading input signal may be used to further promote the transition of the output signal once the lagging input signal arrives by providing a

mechanism for beginning the transition of the output signal before the lagging input signal arrives. This can be accomplished by, for example, providing a switching element that is controlled by the leading input signal. Because the transition of the output signal is already begun, the time required to finish the transition of the output signal once the lagging input signal arrives may be reduced.

In one illustrative embodiment of the present invention, the synchronization circuit includes a conventional CMOS inverter, with two feedback transistors connected as "source followers". One input signal is provided to the input of the conventional inverter, and the other input signal is provided to the gate terminals of the source followers. The circuit operates in such a fashion that two complementary input signals coming in at different times are output as a solitary output signal. The output signal transitions at a time that is slowed relative to the leading input signal and is sped up relative to the lagging input signal. This basic synchronization circuit may be combined with another synchronization circuit to enable the creation of two complementary output signals that are substantially synchronized.

To provide further synchronization, the synchronization circuits of the present invention may be cascaded together. In one embodiment, two synchronization circuits are used to provide complementary output signals that are substantially synchronized. The synchronized complementary output signals are then provided as inputs to a second stage of synchronization circuits for further synchronization. Any number of synchronization stages can be provided to achieve the desired level of synchronization.

It is also contemplated that the synchronization circuits of the present invention may be configured to provide a logic function. They may allow various unsynchronized complementary input signals to be logically combined or gated, as well as synchronized for later use.

Brief Description of the Drawings

Figure 1 is a schematic diagram of a typical prior art flip-flop circuit;

Figure 2 is a schematic diagram of a synchronization circuit according to the prior art;

Figure 3 is a schematic diagram of another synchronization circuit according to the prior art;

Figure 4 is a schematic diagram of an illustrative embodiment of a synchronization circuit in accordance with the present invention;

Figure 5 is a schematic diagram of the same synchronization circuit if Figure 4, with the input signals reversed;

Figure 6 is a schematic diagram of two stages of synchronization circuits cascaded together to provide further synchronization;

5 Figure 7 is a graph showing simulated voltages for the C and CB signals of Figure 6 versus time;

Figure 8 is a graph showing simulated voltages for the C1 and C1B signals of Figure 6 versus time;

Figure 9 is a graph showing simulated voltages for the C2 and C2B signals of Figure 6 versus time;

Figure 10 is a schematic diagram of a synchronizing NAND logic gate according to the present invention; and

Figure 11 is a schematic diagram of a synchronizing AND logic gate according to the present invention.

15 Detailed Description of the Preferred Embodiments

Figure 4 is a schematic diagram of an illustrative embodiment of the present invention. This circuit, shown generally at 510, accepts two input signals, A and its complement $\bar{A}$ at terminals 512 and 514, respectively. Input signal A is connected to the gate terminals of PMOS transistor 516 and NMOS transistor 518. In the illustrative embodiment, PMOS transistor 516 and NMOS transistor 518 are coupled together to form a standard CMOS inverter, with the input of the inverter coupled to input signal A and the output of the inverter providing the output of the synchronization circuit.

To help provide synchronization, NMOS transistor 520 and PMOS transistor 522 are provided as source followers. NMOS transistor 520 is coupled in parallel with PMOS transistor 516, and PMOS transistor 522 is coupled in parallel with NMOS transistor 518. Complement input signal $\bar{A}$ is connected to the gate terminals of NMOS transistor 520 and PMOS transistor 522. The technology-independent logic gate equivalent of the circuit 510 is shown by 526.

To describe the operation of this circuit, first assume that input signal A is low and complement input signal $\bar{A}$ is high. In this state, the output signal 524 is high, NMOS transistor 518 is "OFF", PMOS transistor 516 is "ON", NMOS transistor 520 is "OFF", and PMOS transistor 522 is "OFF". Also assume that input signal A leads input signal AB. That is, when input signal A transitions high, both input signals A and $\bar{A}$

are high until input signal $\overline{A}$ transitions low. In this state, NMOS transistor 518 is “ON” and PMOS transistor 516 is “OFF”. NMOS transistor 518 begins to pull output signal 524 low. However, as the output signal 524 is pulled low, NMOS transistor 520 turns “ON” helping to maintain the output signal 524 in the high state, albeit about one threshold voltage below VDD. Thus, the transition of the output signal 524 from high to low is at least partially inhibited by NMOS transistor 520, which slows the transition of output signal 524.

Once input signal $\overline{A}$ transitions low, however, NMOS transistor 520 turns “OFF”, and PMOS transistor 522 turns “ON”. Thus, PMOS transistor 522 then promotes the transition of the output signal 524, which speeds up the transition of the output signal 524 once input signal $\overline{A}$ transitions low. Because the voltage of the output signal 524 is already about one threshold below VDD, the transition of the output signal 524 is even further sped up.

Under the same initial conditions (i.e., A is low and $\overline{A}$ is high), now assume that input signal A lags input signal AB. That is, when input signal $\overline{A}$ transitions low, both input signals A and $\overline{A}$ are low until input signal A transitions high. In this state, NMOS transistor 518 is “OFF”, PMOS transistor 516 is “ON”, NMOS transistor 520 is “OFF” and PMOS transistor 522 is “ON”. Accordingly, PMOS transistor 522 begins to pull output signal 524 low. However, PMOS transistor 516 is “ON”, which helps maintain the output signal 524 in the high state, albeit about one threshold voltage below VDD. Thus, the transition of the output signal 524 from high to low is at least partially inhibited by PMOS transistor 516, which slows the transition of output signal 524.

Once input signal A transitions high, however, PMOS transistor 516 turns “OFF”, and NMOS transistor 518 turns “ON”. Thus, NMOS transistor 518 promotes the transition of the output signal 524 once input signal A transitions high, which speeds up the transition of the output signal 524 once input signal A transitions high. In addition, and because the voltage of the output signal 524 is already about one threshold below VDD, the transition of the output signal 524 is even further sped up.

Now assume that input signal A is high and complement input signal $\overline{A}$ is low. In this state, the output signal 524 is low, NMOS transistor 518 is “ON”, PMOS transistor 516 is “OFF”, NMOS transistor 520 is “OFF”, and PMOS transistor 522 is “OFF”. Now, also assume that input signal A leads input signal AB. That is, when

input signal A transitions low, both input signals A and $\overline{A}$ are low. In this state, NMOS transistor 518 is "OFF" and PMOS transistor 516 is "ON". PMOS transistor 516 then begins to pull output signal 524 high. However, as the output signal 524 is pulled high, PMOS transistor 522 turns "ON" helping to maintain the output signal 524 in the low state, albeit about one threshold voltage above ground. Thus, the transition of the output signal 524 from low to high is at least partially inhibited by PMOS transistor 522, which slows the transition of output signal 524.

Once input signal $\overline{A}$ transitions high, however, NMOS transistor 520 turns "ON", and PMOS transistor 522 turns "OFF". Thus, NMOS transistor 520 promotes the transition of the output signal 524 once input signal $\overline{A}$ transitions high. Because the voltage of the output signal 524 is already about one threshold voltage above ground, the transition of the output signal 524 is even further sped up.

Finally, and under the same initial conditions (i.e., A is high and $\overline{A}$ is low), assume that input signal A lags input signal $\overline{A}$. That is, when input signal $\overline{A}$ transitions high, both input signals A and $\overline{A}$ are high. In this state, NMOS transistor 518 is "ON", PMOS transistor 516 is "OFF", NMOS transistor 520 is "ON" and PMOS transistor 522 is "OFF". NMOS transistor 520 then begins to pull output signal 524 high. However, NMOS transistor 518 is also "ON", which helps maintain the output signal 524 in the low state, albeit about one threshold voltage above ground. Thus, the transition of the output signal 524 from low to high is at least partially inhibited by NMOS transistor 518, which slows the transition of output signal 524. Once input signal A transitions low, however, PMOS transistor 516 turns "ON", and NMOS transistor 518 turns "OFF". Thus, PMOS transistor 516 promotes the transition of the output signal 524 once input signal A transitions low. Because the voltage of the output signal 524 is already about one threshold above ground, the transition of the output signal 524 is even further sped up.

As can be seen from the above discussion, the synchronization circuit of Figure 4 tends to slow the transition of the output signal 524 upon the transition of the leading input signal, and accelerates or speeds up the transition of the output signal upon the transition of the lagging input signal. The output signal 524 thus transitions at a time that is slowed relative to the leading input signal and is sped up relative to the lagging input signal.

Figure 5 is a schematic diagram of the same synchronization circuit if Figure 4, with the input signals reversed. That is, input signal $\overline{A}$ is now connected to the gate terminals of PMOS transistor 516 and NMOS transistor 518, and input signal A is connected to the gate terminals of PMOS transistor 522 and NMOS transistor 520. This circuit operates similar to that described above. It is contemplated that both circuits of Figure 4 and 5 may be provided to provide complementary synchronized outputs 524 and 544, as shown.

Figure 6 is a schematic diagram of two stages of synchronization circuits cascaded together to provide increased synchronization. The circuit is shown generally at 550. The synchronized complementary signals produced by circuit 550 may be used to control, for example, the flip-flop circuit as that depicted in Figure 1.

In the illustrative embodiment, an input signal 560 is provided to an inverter 562 to produce a clock signal C 563 as shown. Clock signal C 563 is then provided to inverter 564, which produces a complement clock signal CB 565. The complement clock signal CB 565 is provided to inverter 567 to produce a clock signal C 580. The clock signal C 580 is provided to inverter 568 to produce a complement clock signal CB 578.

The clock signal C 580 is provided to the source-follower input of synchronization circuit 554, and to the inverter input of synchronization circuit 552. The complement clock signal CB 578 is provided to the inverter input of synchronization circuit 552, and to the source-follower input of synchronization circuit 554. The synchronization circuits 552 and 554 are preferably constructed in accordance with the synchronization circuit shown in Figure 4. The synchronization circuit 552 preferably synchronizes the clock signal C 580 and the complement clock signal CB 578 to produce a C1 signal 579. Likewise, the synchronization circuit 554 preferably synchronizes the complement clock signal CB 578 and the clock signal C 580 to produce a C1B signal 576.

The C1B signal 576 is provided to the source-follower input of synchronization circuit 566, and to the inverter input of synchronization circuit 568. Signal C1 579 is provided to the inverter input of synchronization circuit 566, and to the source-follower input of synchronization circuit 568. Again, the synchronization circuits 566 and 568 are preferably constructed in accordance with the synchronization circuit shown in Figure 4. The synchronization circuit 566 preferably synchronizes the complement clock signal C1B 576 and the clock signal C1 579 to produce a C2B signal 570.

Likewise, the synchronization circuit 568 preferably synchronizes the clock signal C1 579 and the complement clock signal C1B 576 to produce a C2 signal 572.

The outputs of synchronization circuits 552 and 554 may be more synchronized than the input signals 578 and 580, which naturally differ by the gate delay imposed by inverter 568. The synchronization switches 566 and 568 provide additional synchronization. Additional synchronization switches, not depicted, may be cascaded together in the same manner to provide additional synchronization, if desired.

Figure 7 is a graph showing simulated voltages for the C and CB signals of Figure 6 versus time. As can be seen, clock signals C 563 and CB 565 of Figure 6 are offset in time by about one gate delay, or the delay of inverter 564. As described above, such unsynchronized signals can increase the setup time and clock-to-Q times of a conventional flip-flop.

Figure 8 is a graph showing simulated voltages for the C1 and C1B signals of Figure 6 versus time. Clock signals C1 576 and C1B 579 are provided by synchronization circuits 554 and 552, respectively. As can readily be seen, clock signals C1 576 and C1B 579 are much more synchronized than clock signals C 563 and CB 565 shown in Figure 7.

Figure 9 is a graph showing simulated voltages for the C2 and C2B signals of Figure 6 versus time. Clock signals C2 572 and C2B 570 are provided by the second stage of synchronization circuits 568 and 566, respectively. As can readily be seen, clock signals C2 572 and C2B 570 appear to be even more synchronized than clock signals C1 576 and C1B 579 shown in Figure 8.

Figure 10 is a schematic diagram of a synchronizing NAND logic gate according to the present invention. As indicated above, it is contemplated that the synchronization circuits of the present invention may be configured to provided a logic function, as well as a synchronization function. The may allow various unsynchronized complementary input signals to be logically combined, as well as synchronized if desired.

An illustrative NAND gate is shown generally at 580. The circuit receives two input signals, A and B, and their respective complements $\overline{A}$ and $\overline{B}$, on terminals 582, 584, 586, and 588, respectively. The output on output terminal 590 is a synchronized NAND of input signals A and B.

The NAND gate 580 includes a first logic gate and a second logic gate. The first logic gate has one or more PMOS transistors coupled between the output 590 and the power supply, and one or more NMOS transistors coupled between the output 590 and

ground to form a desired logic function. In the illustrative case, the logic function is a NAND function. The first logic gate includes transistors 592, 594, 596 and 598. The source of PMOS transistors 592 and 594 are connected to the power supply (VDD). The drains of PMOS transistors 592 and 594 are connected to the output 590. The gate of PMOS transistor 592 is connected to input signal A, and the gate of PMOS transistor 594 is connected to input signal B.

The drain of NMOS transistor 596 is connected to the output 590, and the source of NMOS transistor 598 is connected to ground. The drain of NMOS transistor 598 is connected to the source of NMOS transistor 596. The gate of NMOS transistor 598 is connected to input signal A, and the gate of NMOS transistor 596 is connected to input signal B, as shown.

The second logic gate preferably has the same structure as the first logic gate, but with the PMOS transistors replaced with NMOS transistors and the NMOS transistors replaced with PMOS transistors. Also, the second logic gate receives the complement input signals $\overline{A}$ and $\overline{B}$ rather than the true input signals A and B. The second logic gate of Figure 10 includes transistors 593, 594, 597 and 599. The source of NMOS transistors 593 and 595 are connected to the power supply (VDD). The drains of NMOS transistors 593 and 595 are connected to the output 590. The gate of NMOS transistor 593 is connected to input signal AB, and the gate of NMOS transistor 595 is connected to input signal $\overline{B}$.

The drain of PMOS transistor 597 is connected to the output 590, and the source of PMOS transistor 599 is connected to ground. The drain of PMOS transistor 599 is connected to the source of PMOS transistor 597. The gate of PMOS transistor 599 is connected to input signal AB, and the gate of PMOS transistor 597 is connected to input signal $\overline{B}$, as shown.

In this configuration, the synchronization circuit 580 provides a NAND function, as well as a synchronization function. That is, the output on output terminal 590 is a synchronized NAND of input signals A and B, regardless of the order of arrival or degree of synchronization.

Figure 11 is a schematic diagram of a synchronizing AND logic gate 600 according the present invention. The circuit 600 receives as input two data signals, A and B, and their respective complements $\overline{A}$ and $\overline{B}$, on terminals 602, 604, 606, and

608, respectively. The output on output terminal 610 is a synchronized AND of input signals A and B.

The AND gate 600 includes a first logic gate and a second logic gate. The first logic gate includes transistors 612, 614, 616 and 618. The source of NMOS transistors 612 and 614 are connected to the ground. The drains of NMOS transistors 612 and 614 are connected to the output 610. The gate of NMOS transistor 612 is connected to input signal AB, and the gate of NMOS transistor 614 is connected to input signal $\bar{B}$.

The drain of PMOS transistor 616 is connected to the output 610, and the source of PMOS transistor 618 is connected to the power supply (VDD). The drain of PMOS transistor 618 is connected to the source of PMOS transistor 616. The gate of PMOS transistor 618 is connected to input signal AB, and the gate of PMOS transistor 616 is connected to input signal $\bar{B}$, as shown.

The second logic gate preferably has the same structure as the first logic gate, but with the PMOS transistors replaced with NMOS transistors and the NMOS transistors replaced with PMOS transistors. Also, the second logic gate preferably receives the true input signals A and B rather than the complement input signals $\bar{A}$ and $\bar{B}$.

In Figure 11, the second logic gate includes transistors 613, 615, 617 and 619. The source of PMOS transistors 613 and 615 are connected to ground. The drains of PMOS transistors 613 and 614 are connected to the output 610. The gate of PMOS transistor 613 is connected to input signal A, and the gate of PMOS transistor 615 is connected to input signal B. The drain of NMOS transistor 617 is connected to the output 610, and the source of NMOS transistor 619 is connected to the power supply (VDD). The drain of NMOS transistor 619 is connected to the source of NMOS transistor 617. The gate of NMOS transistor 619 is connected to input signal A, and the gate of NMOS transistor 617 is connected to input signal B, as shown.

In this configuration, the synchronization circuit 600 provides an AND function, as well as a synchronization function. That is, the output on output terminal 610 is a synchronized AND of input signals A and B, regardless of the order of arrival or degree of synchronization.

When the synchronization circuit shown in Figure 10 is used in conjunction with the synchronization circuit shown in Figure 11, output signals 590 and 610 provide synchronized complementary NAND/AND outputs.

Having thus described the preferred embodiments of the present invention, those of skill in the art will readily appreciate that the teachings found herein may be applied to yet other embodiments within the scope of the claims hereto attached. For example, the invention may be implemented in other semiconductor technologies or media. The
5 invention may also be used to create logic gates other than those specifically identified herein.

WHAT IS CLAIMED IS:

The embodiments of the invention in which an exclusive property or right is claimed are defined as follows:

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1. A synchronizing circuit for providing a synchronized output signal from non-synchronized complementary first and second input signals, the first input signal of the non-synchronized complementary input signals leading the second input signal, the synchronizing circuit comprising:

10 means for slowing down a transition of the output signal caused by the leading first input signal; and

means for speeding up the transition of the output signal caused by the lagging second input signal.

15 2. A synchronizing circuit according to claim 1, wherein the means for slowing down the transition of the output signal caused by the leading first input signal impedes the transition of the output signal until the lagging input signal arrives.

20 3. A synchronizing circuit according to claim 2, wherein the means for slowing down the transition of the output signal caused by the leading first input signal comprises a first switching element that is controlled by the lagging input signal, the first switching element attempting to maintain the state of the output signal until the lagging input signal arrives.

25 4. A synchronizing circuit according to claim 3, wherein the means for speeding up the transition of the output signal caused by the lagging second input signal comprises a second switching element that is controlled by the lagging input signal, the second switching element promoting the transition of the output signal when the lagging input signal arrives.

30

5. A synchronizing circuit according to claim 1, wherein the means for speeding up the transition of the output signal caused by the lagging second input signal promotes the transition of the output signal before the lagging input signal arrives.

6. A synchronizing circuit according to claim 5, wherein the means for speeding up the transition of the output signal caused by the lagging second input signal comprises a first switching element that is controlled by the leading input signal, the switching element attempting to promote the transition of the output signal when the leading input signal arrives.

7. A synchronizing circuit according to claim 6, wherein the means for speeding up the transition of the output signal caused by the lagging second input signal comprises a second switching element that is controlled by the lagging input signal, the second switching element further promotes the transition of the output signal when the lagging input signal arrives.

8. A synchronizing circuit coupled between power and ground for providing an output signal responsive to two unsynchronized input signals, the synchronizing circuit comprising:

- a first data input terminal for receiving a first data input signal;
- a second data input terminal for receiving a second data input signal, wherein the second data input signal is the complement of the first data input signal;
- an output terminal for carrying a data output signal;
- a first switching element coupled between the output terminal and ground and enabled by the first data input signal; and
- a second switch element coupled between the output terminal and power and enabled by the second data input signal.

9. The synchronizing circuit of claim 8, further comprising:

- a third switching element coupled between output terminal and ground and enabled by the second data input signal; and
- a fourth switching element coupled between output terminal and power and enabled by the first data input signal.

10. The synchronizing circuit of claim 9, wherein the first, second, third and fourth switching elements are transistors.

11. The synchronizing circuit of claim 10, wherein the first and second switching elements are transistors of a first polarity, and the third and fourth switching elements are transistors of an opposite polarity.

5 12. The synchronizing circuit of claim 8, wherein the synchronizing circuit inverts the first data input signal.

13. The synchronizing circuit of claim 8, wherein the second data signal is the complement of the first data signal.

10

14. A synchronizing circuit coupled between power and ground for providing a data output signal responsive to two unsynchronized data input signals, the synchronizing circuit comprising:

a first data input terminal for receiving a first data input signal;

15 a second data input terminal for receiving a second data input signal, wherein the second data input signal is the complement of the first data input signal;

an output terminal for carrying the data output signal;

a first PMOS transistor having a gate, a source, and a drain, the source of the first PMOS transistor is coupled to power, the drain of the first PMOS transistor is coupled to the output terminal, and the gate of the first PMOS transistor is coupled to the first data input terminal;

20 a first NMOS transistor having a gate, a source, and a drain, the source of the first NMOS transistor is coupled to ground, the drain of the first NMOS transistor is coupled to the output terminal, and the gate of the first NMOS transistor is coupled to the first data input terminal;

25 a second PMOS transistor having a gate, a source, and a drain, the source of the second PMOS transistor is coupled to ground, the drain of the second PMOS transistor is coupled to the output terminal, and the gate of the second PMOS transistor is coupled to the second data input terminal; and

30 a second NMOS transistor having a gate, a source, and a drain, the source of the second NMOS transistor is coupled to power, the drain of the second NMOS transistor is coupled to the output terminal, and the gate of the second NMOS transistor is coupled to the second data input terminal.

15. A synchronizing circuit for providing synchronized complementary first and second output signals responsive to unsynchronized complementary first and second input signals, the synchronizing circuit comprising:

5 a first and a second synchronization circuit, each synchronization circuit having a first and second input terminal and an output terminal and further having means for slowing down the input signal on the first input terminal if leading, and means for speeding up the input signal on the first input terminal if lagging;

10 the first input signal coupled to the first input terminal of the first synchronization circuit and the second input terminal of the second synchronization circuit; and

the second input signal coupled to the second input terminal of the first synchronization circuit and the first input terminal of the second synchronization circuit.

16. The synchronizing circuit of claim 15, further comprising:

15 a third and a fourth synchronization circuit, each synchronization circuit having a first and second input terminal and an output terminal and further having means for slowing down the input signal on the first input terminal if leading, and means for speeding up the input signal on the first input terminal if lagging;

20 the output terminal of the first synchronization circuit being coupled to the first input terminal of a third synchronization circuit and to the second input terminal of the fourth synchronization circuit;

the output terminal of the second synchronization circuit being coupled to the second input terminal of the third synchronization circuit and to the first input terminal of the fourth synchronization circuit;

25 the output terminal of the third synchronization circuit providing the first output signal, and the output terminal of the fourth synchronization circuit providing the second output signal.

17. A synchronizing circuit comprising:

30 a first logic gate having a number of inputs and an output, the first logic gate having one or more PMOS transistors coupled between the output and a power supply terminal, and one or more NMOS transistors coupled between the output and a ground terminal to form a logic function;

a second logic gate having a number of inputs and an output, the second logic gate having the same structure as the first logic gate, but with the PMOS transistors replaced with NMOS transistors and the NMOS transistors replaced with PMOS transistors.

5

18. The synchronizing circuit of claim 17, wherein the first logic gate is a NAND gate.

19. The synchronizing circuit of claim 18, wherein the first logic gate
10 comprises:

a first PMOS transistor and a second PMOS transistor, each of the first and second PMOS transistors having a gate, a source, and a drain;

a first NMOS transistor and a second NMOS transistor, each of the first and second NMOS transistors having a gate, a source, and a drain;

15 the source of the first PMOS transistor and the source of the second PMOS transistor are coupled to the power supply terminal;

the drain of the first PMOS transistor and the drain of the second PMOS transistor are coupled to the output;

20 the source of the first NMOS transistor is coupled to the ground terminal, the drain of the second NMOS transistor is coupled to the output, and the drain of the first NMOS transistor is coupled to the source of the second NMOS transistor;

the gate of one of the first and second PMOS transistors is coupled to a first input signal, and the gate of the other first and second PMOS transistors is coupled to a second input signal; and

25 the gate of one of the first and second NMOS transistors is coupled to the first input signal, and the gate of the other first and second NMOS transistors is coupled to the second input signal.

20. The synchronizing circuit of claim 19, wherein the second logic gate
30 comprises:

a third NMOS transistor and a fourth NMOS transistor, each of the third and fourth NMOS transistors having a gate, a source, and a drain;

a third PMOS transistor and a fourth PMOS transistor, each of the third and fourth PMOS transistors having a gate, a source, and a drain;

the source of the third NMOS transistor and the source of the fourth NMOS transistor are coupled to the power supply terminal;

the drain of the third NMOS transistor and the drain of the fourth NMOS transistor are coupled to the output;

5 the source of the third PMOS transistor is coupled to the ground terminal, the drain of the fourth PMOS transistor is coupled to the output, and the drain of the third PMOS transistor is coupled to the source of the fourth PMOS transistor;

the gate of one of the third and fourth NMOS transistors is coupled to the first input signal, and the gate of the other third and fourth NMOS transistors is coupled to
10 the second input signal; and

the gate of one of the third and fourth PMOS transistors is coupled to the first input signal, and the gate of the other third and fourth PMOS transistors is coupled to the second input signal.

15 21. The synchronizing circuit of claim 17, wherein the first logic gate is a AND gate.

22. The synchronizing circuit of claim 20, wherein the first logic gate comprises:

20 a first PMOS transistor and a second PMOS transistor, each of the first and second PMOS transistors having a gate, a source, and a drain;

a first NMOS transistor and a second NMOS transistor, each of the first and second NMOS transistors having a gate, a source, and a drain;

the source of the first NMOS transistor and the source of the second NMOS
25 transistor are coupled to the ground terminal;

the drain of the first NMOS transistor and the drain of the second NMOS transistor are coupled to the output;

the source of the first PMOS transistor is coupled to the power supply terminal, the drain of the second PMOS transistor is coupled to the output, and the drain of the
30 first PMOS transistor is coupled to the source of the second PMOS transistor;

the gate of one of the first and second NMOS transistors is coupled to a first input signal, and the gate of the other first and second NMOS transistor is coupled to a second input signal; and

the gate of one of the first and second PMOS transistors is coupled to the first input signal, and the gate of the other first and second PMOS transistor is coupled to the second input signal.

5 23. The synchronizing circuit of claim 21, wherein the second logic gate comprises:

 a third PMOS transistor and a fourth PMOS transistor, each of the third and fourth PMOS transistors having a gate, a source, and a drain;

 a third NMOS transistor and a fourth NMOS transistor, each of the third and
10 fourth NMOS transistors having a gate, a source, and a drain;

 the source of the third PMOS transistor and the source of the fourth PMOS transistor are coupled to the ground terminal;

 the drain of the third PMOS transistor and the drain of the fourth PMOS transistor are coupled to the output;

15 the source of the third NMOS transistor is coupled to the power supply terminal, the drain of the fourth NMOS transistor is coupled to the output, and the drain of the third NMOS transistor is coupled to the source of the fourth NMOS transistor;

 the gate of one of the third and fourth PMOS transistors is coupled to the first input signal, and the gate of the other third and fourth PMOS transistor is coupled to the
20 second input signal; and

 the gate of one of the third and fourth NMOS transistors is coupled to the first input signal, and the gate of the other third and fourth NMOS transistor is coupled to the second input signal.

25 24. A method for synchronizing complementary first and second output signals from non-synchronized complementary first and second input signals, the first input signal of the non-synchronized complementary input signals leading the second input signal, the method comprising:

 slowing down a transition of the output signal caused by the leading first input
30 signal; and

 speeding up the transition of the output signal caused by the lagging second input signal.

25. The method of claim 23, wherein the slowing down step includes impeding the transition of the output signal until the lagging input signal arrives.

26. The method of claim 24, wherein the slowing down step includes
5 attempting to maintain the state of the output signal until the lagging input signal arrives.

27. The method of claim 23 wherein the speeding up step further includes promoting the transition of the output signal when the lagging input signal arrives.
10

28. The method of claim 23, wherein the speeding up step includes promoting the transition of the output signal before the lagging input signal arrives.

29. The method of claim 27, wherein the transition of the output signal is
15 promoted when the leading input signal arrives.

30. The method of claim 28, wherein the speeding up step further includes promoting the transition of the output signal when the lagging input signal arrives.

PRIOR ART

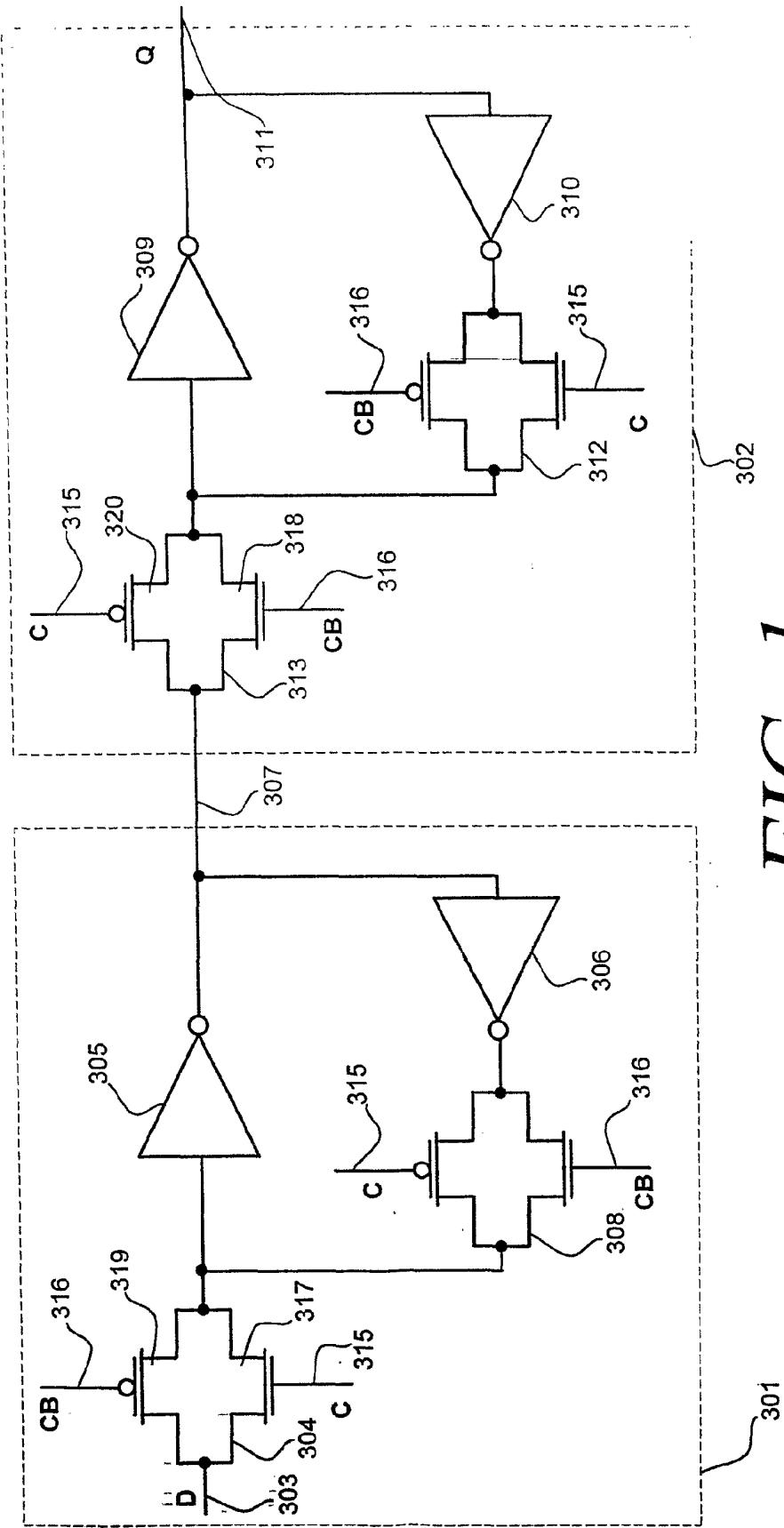


FIG. 1

PRIOR ART

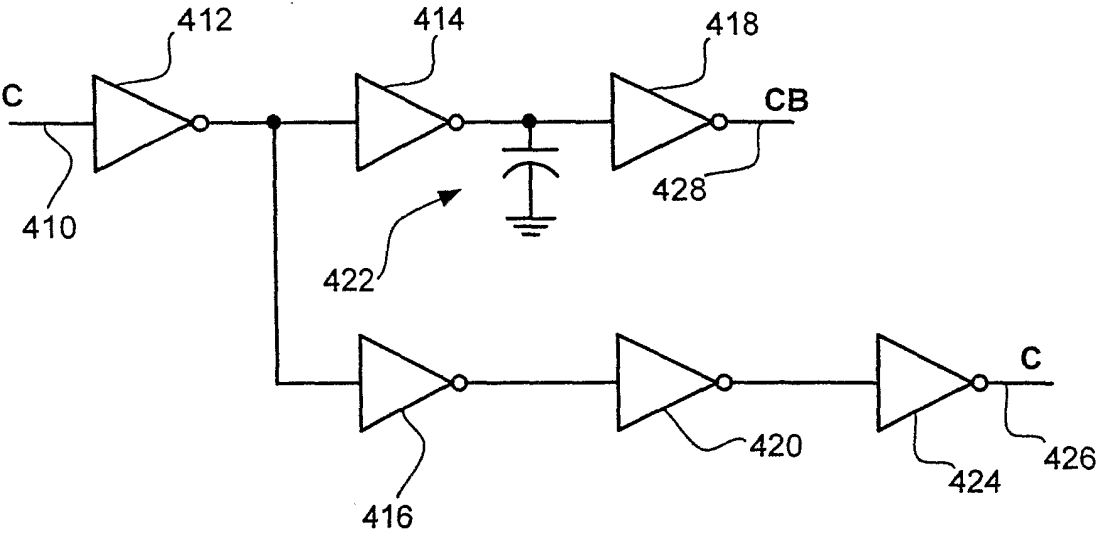
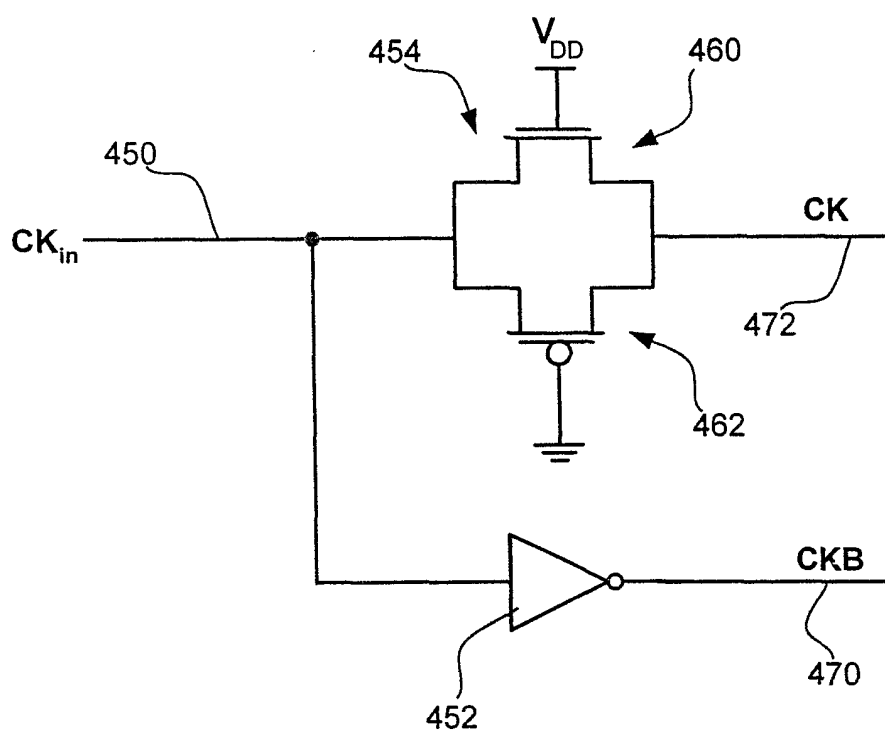
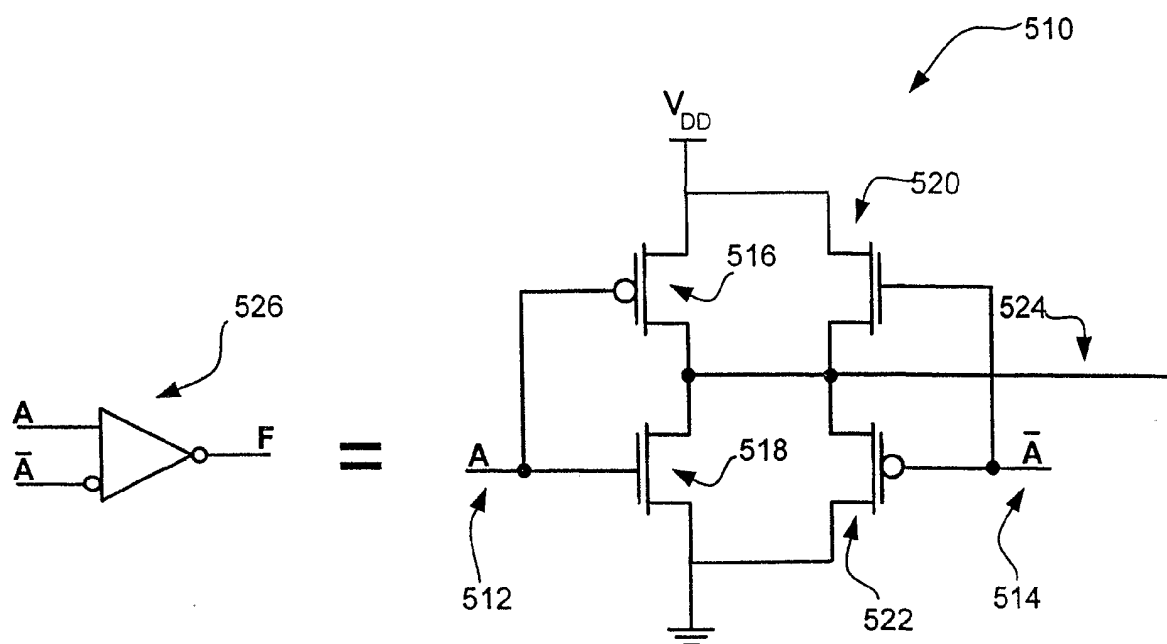
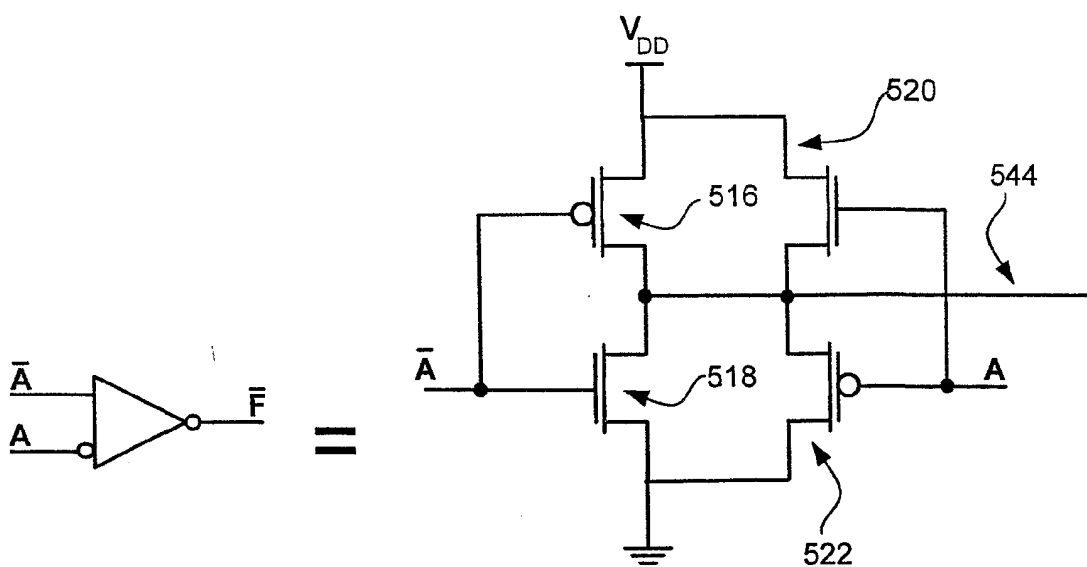


FIG. 2

PRIOR ART

*FIG. 3*

*FIG. 4**FIG. 5*

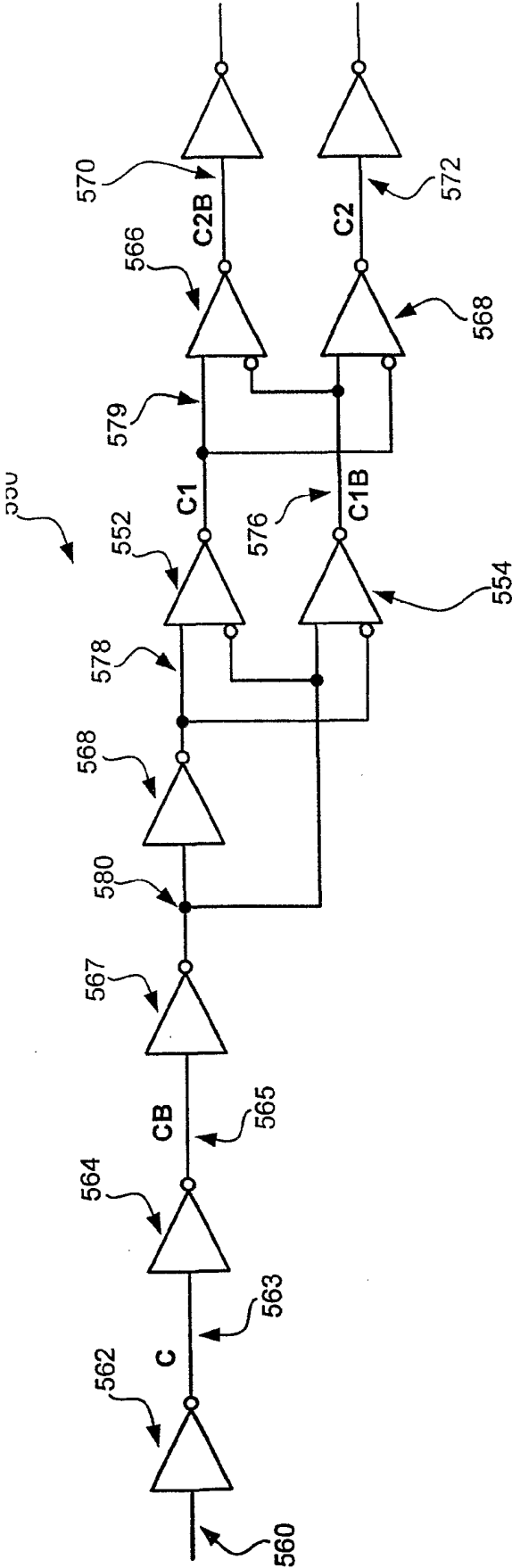
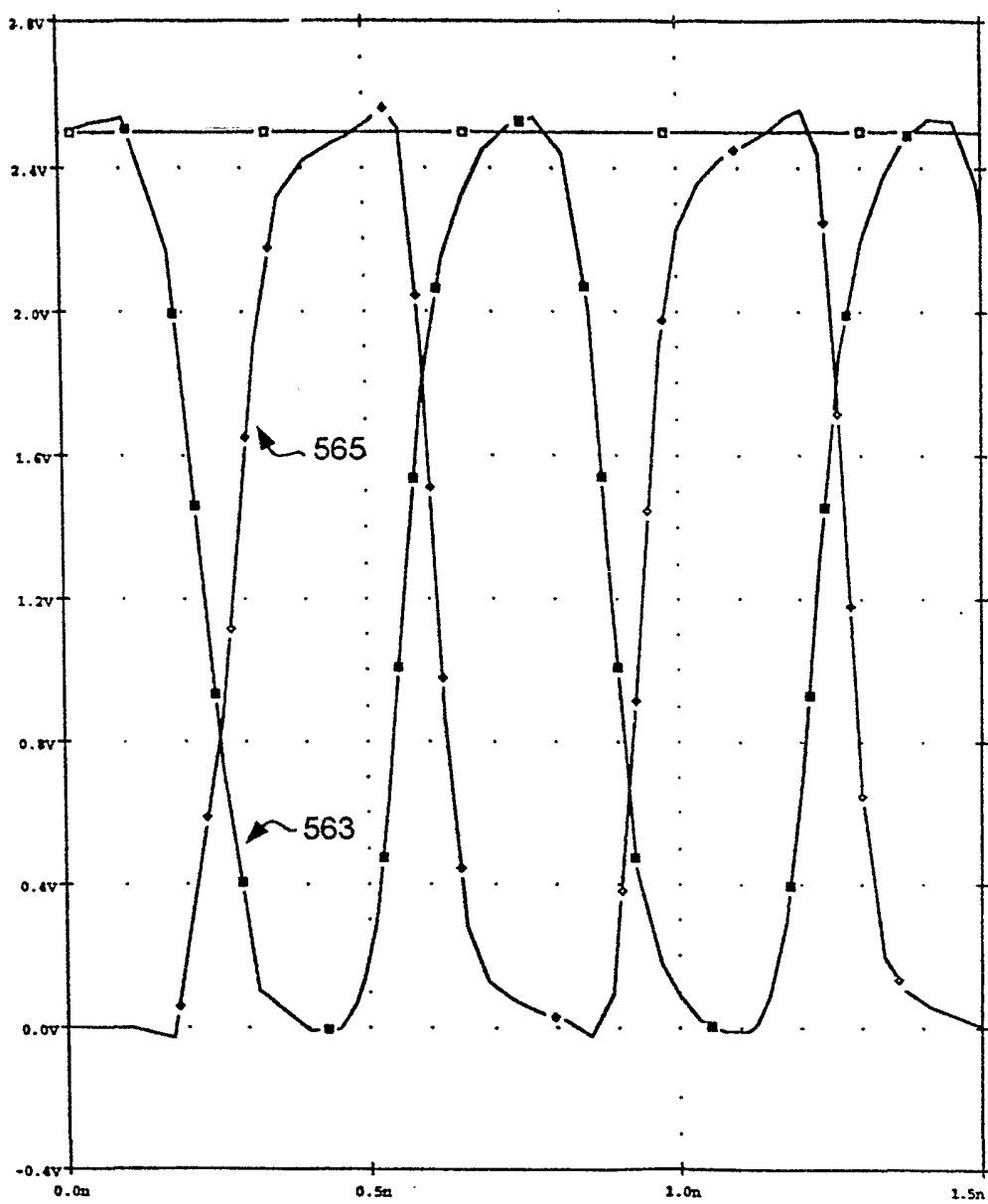
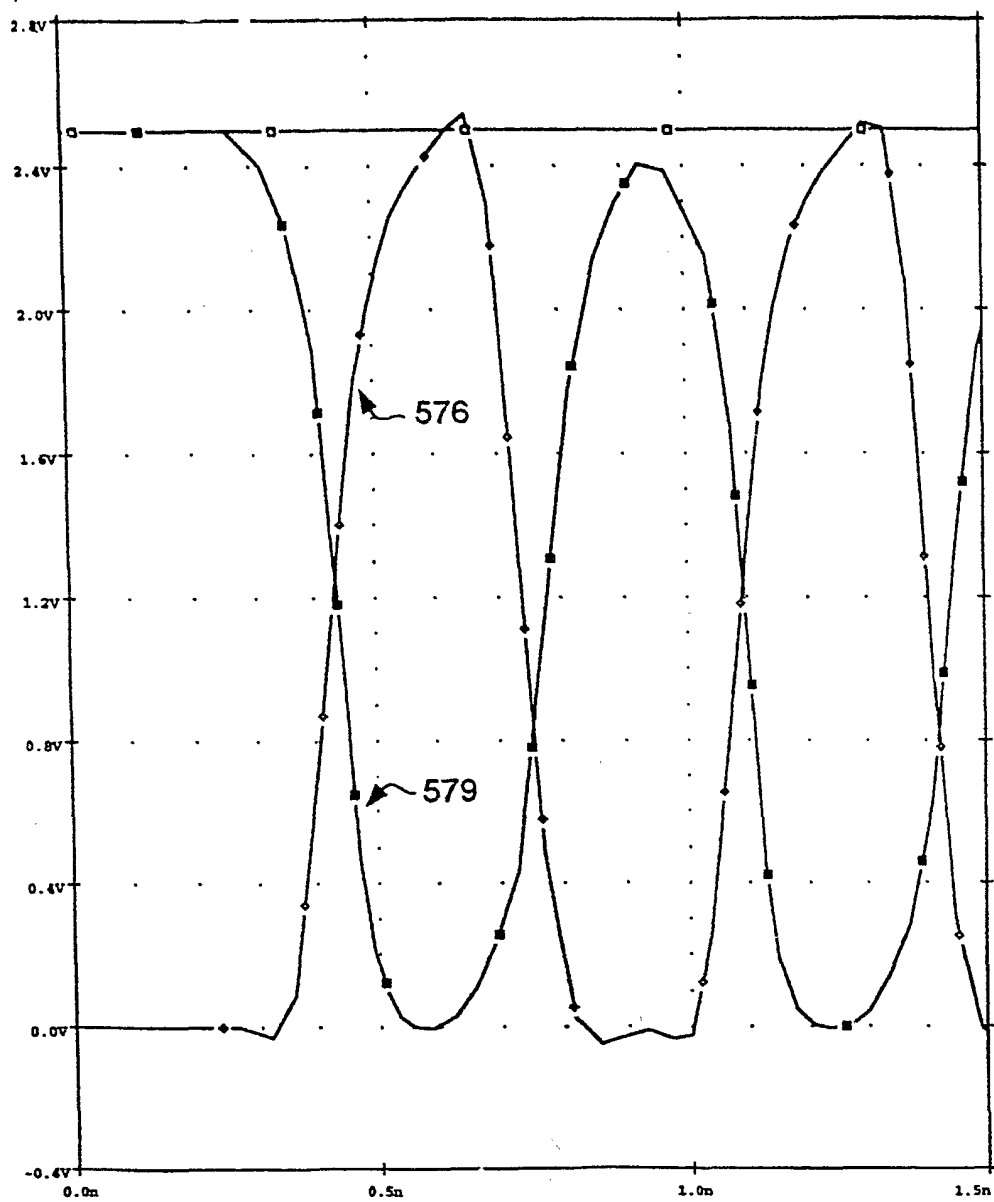
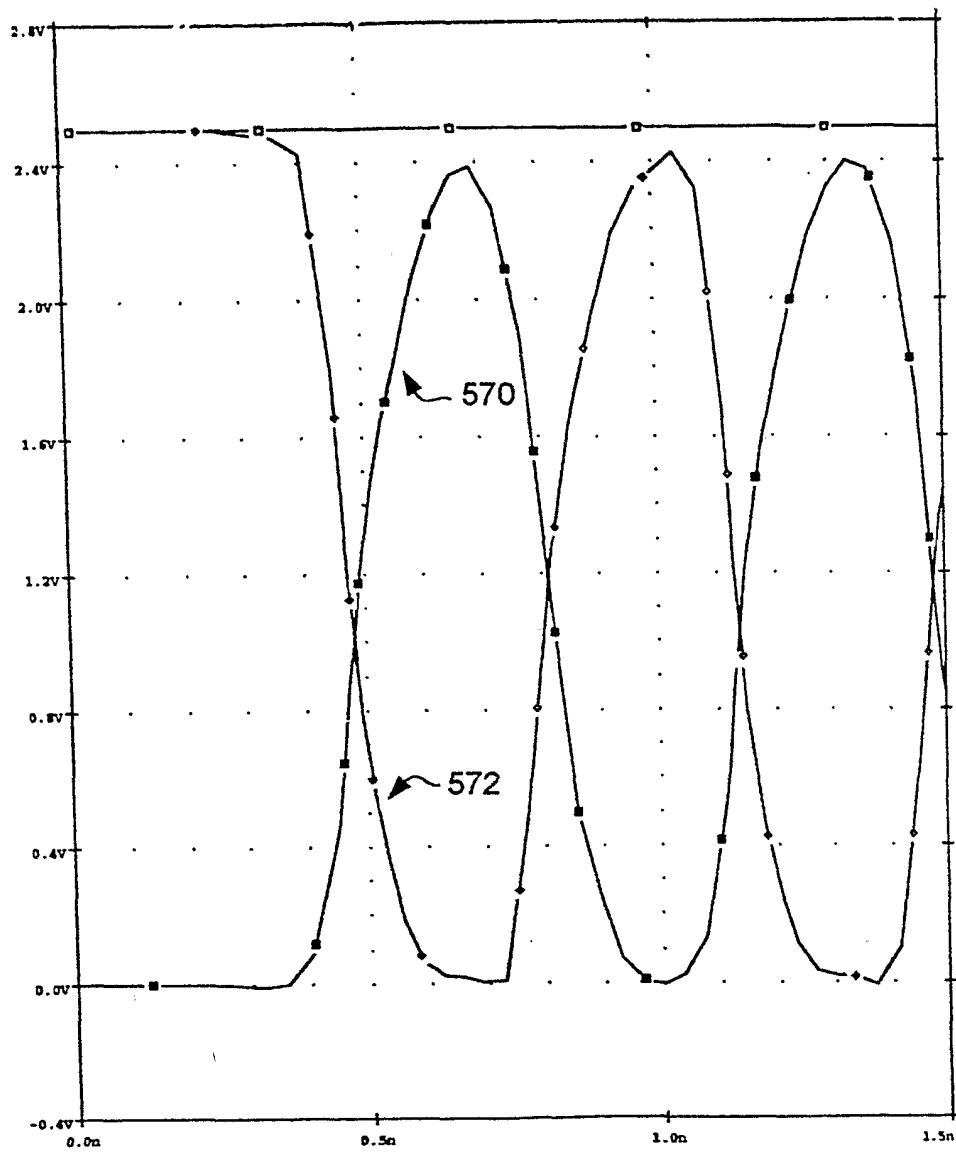
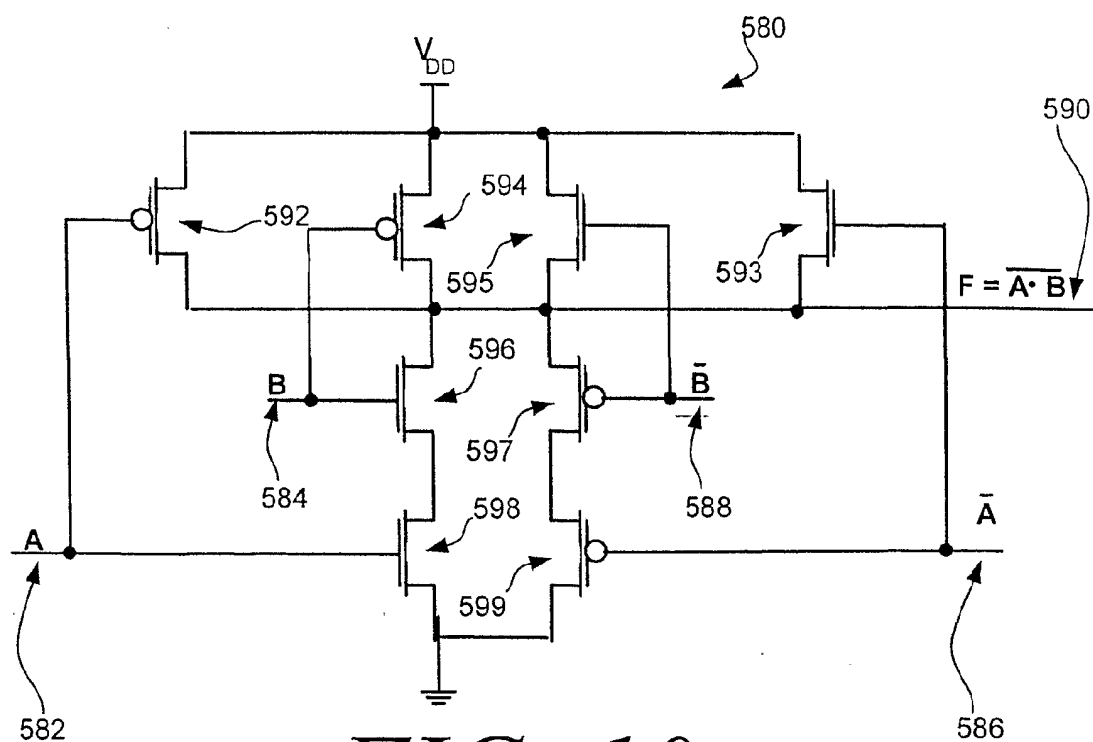
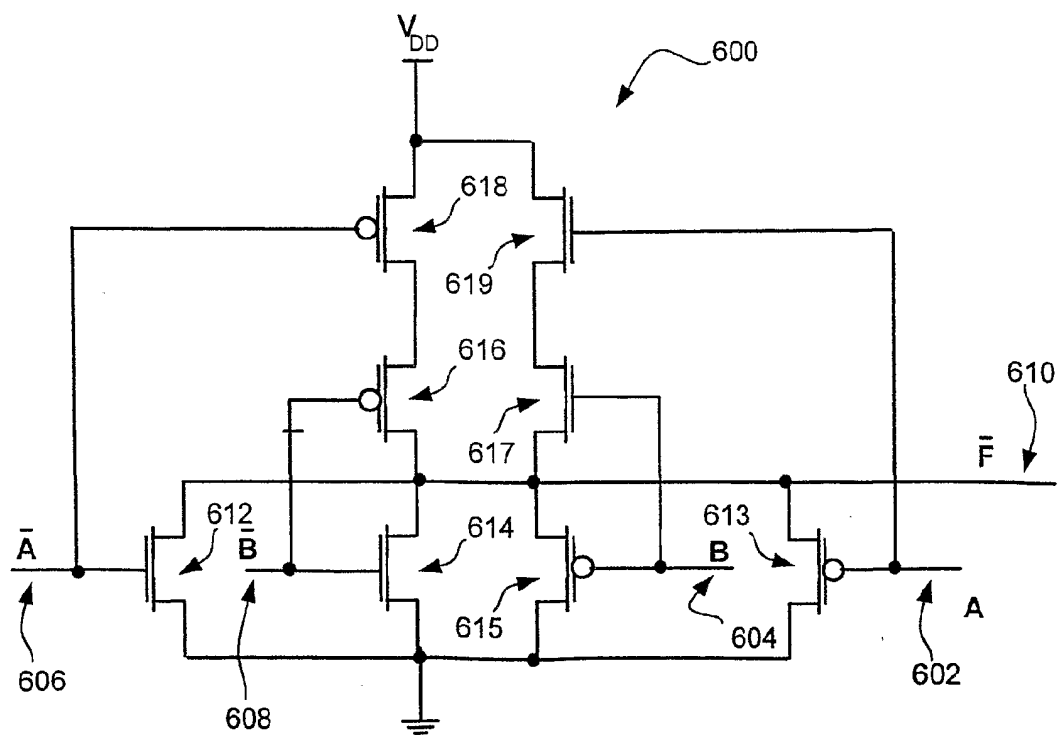


FIG. 6



*FIG. 8*

*FIG. 9*

*FIG. 10**FIG. 11*