United States Patent

Hogan et al.

[15] **3,641,559**

[45] **Feb. 8, 1972**

[54] STAGGERED VIDEO-DIGITAL TV SYSTEM

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[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[22] Filed: **Nov. 21, 1969**

[21] Appl. No.: **878,712**

[52] **U.S. Cl.** .....**340/324 A**, 340/172.5

[51] **Int. Cl.**.....**G06f 3/14**

[58] **Field of Search** .....340/324 A, 172.5

[56] **References Cited**

UNITED STATES PATENTS

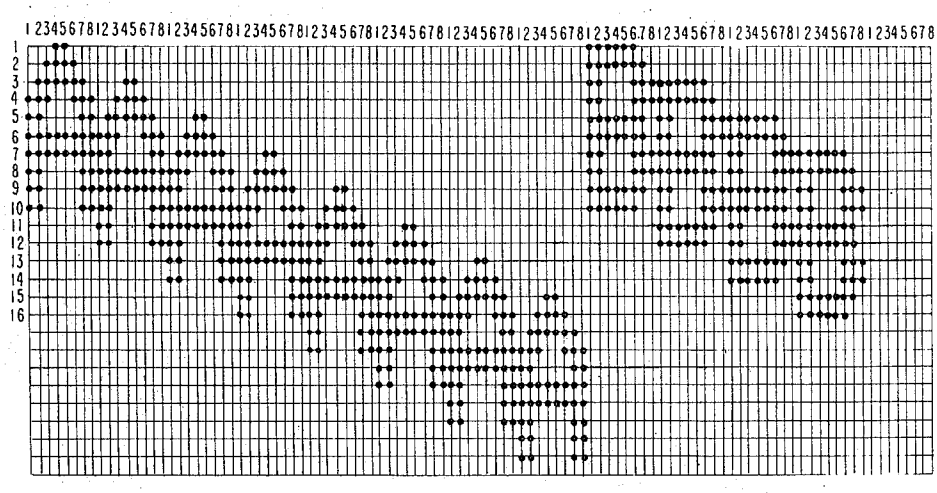
3,453,384	7/1969	Donner et al.	340/324
3,497,613	2/1970	Botjer et al.	340/324
3,555,520	1/1971	Helbig et al.	340/324

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Assistant Examiner—Marshall M. Curtis
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[57] **ABSTRACT**

A display system including a symbol generator which consists of a group of segment generators. Each segment generator generates a portion of the symbol to be displayed in time sequence so that the segment generator which generates the first portion of the symbol would be free to generate first portion of a following symbol or the first portion of a symbol on an other display device while the other segment generators are generating the remainder of the first symbol. The outputs from this group of segment generators are transmitted through a group of multiplex gates which assemble the symbol segments into video data signals for a group of display devices. The transmission of the information signals to the segment generators is staggered so that during a specified period of time mutually exclusive symbol segments are presented on different displays. Since the staggering of the display presentation would result in the rows of symbols being displaced vertically on the different display devices, the vertical synchronization signals are also staggered to allow the vertical positioning of rows of symbols on all displays to be the same.

3 Claims, 12 Drawing Figures



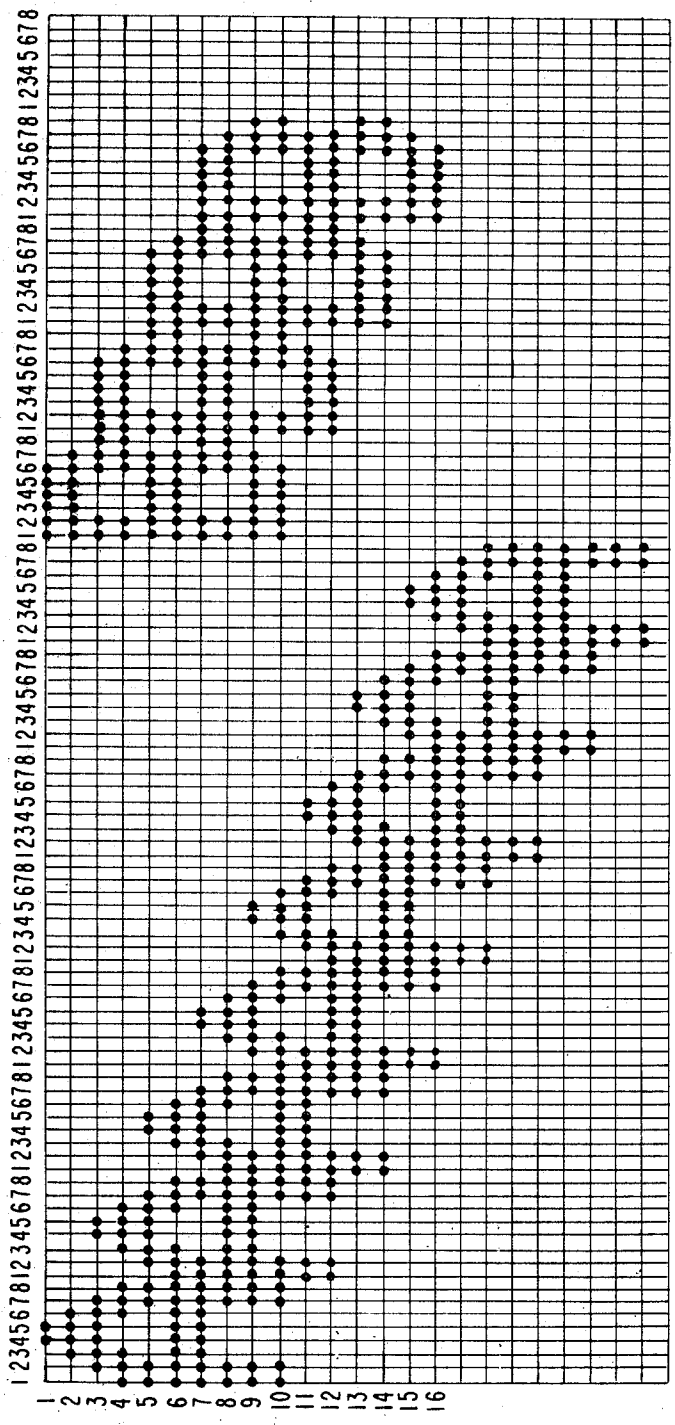


FIG. 1

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FIG. 2

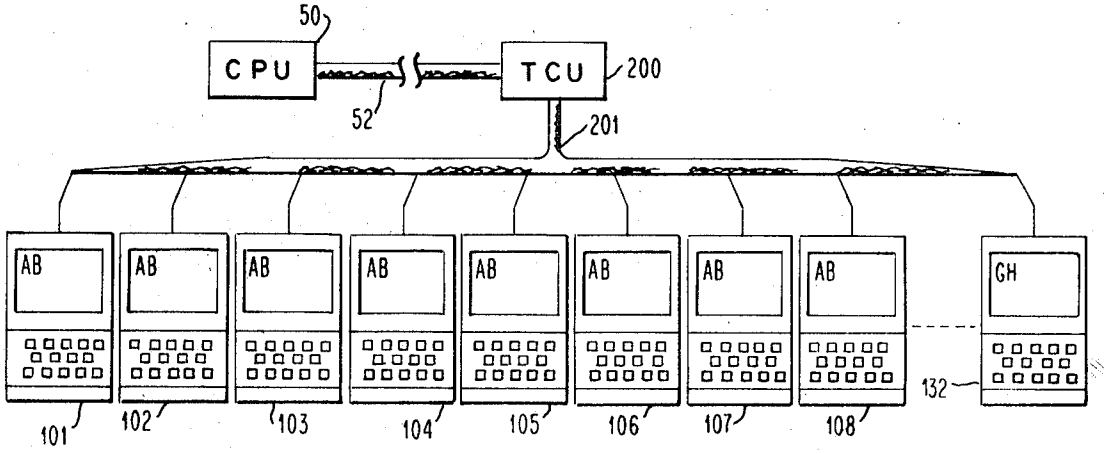

50
CPU
52
TCU
200
201
AB
AB
AB
AB
AB
AB
AB
AB
GH
101
102
103
104
105
106
107
108
132

FIG. 3

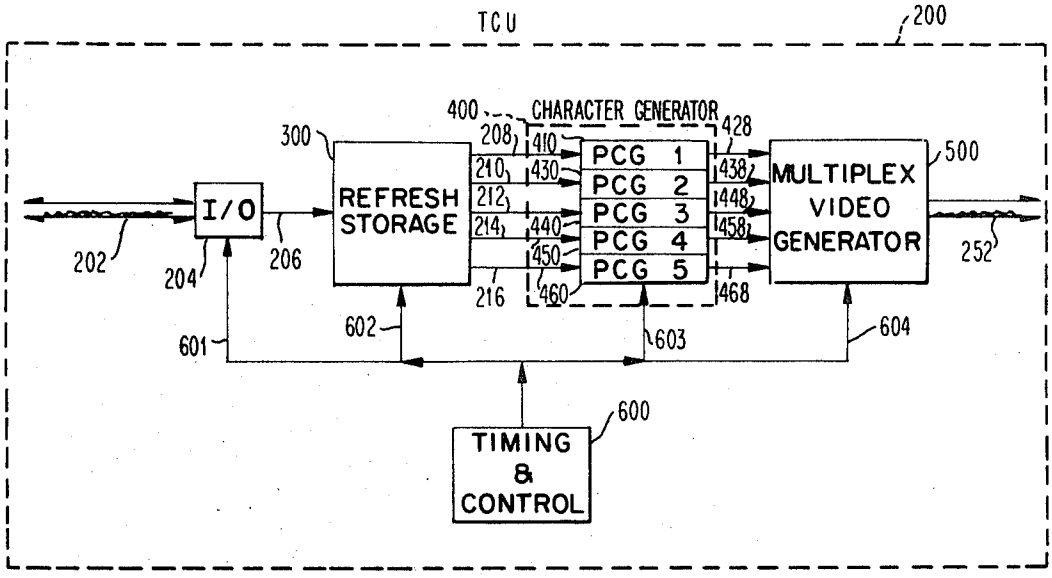

TCU
200
400
CHARACTER GENERATOR
428
300
208
410
PCG 1
438
210
430
PCG 2
448
212
PCG 3
458
214
440
PCG 4
450
PCG 5
216
460
468
I/O
REFRESH STORAGE
MULTIPLEX VIDEO GENERATOR
500
202
204
206
252
601
602
603
604
TIMING & CONTROL
600

FIG. 5

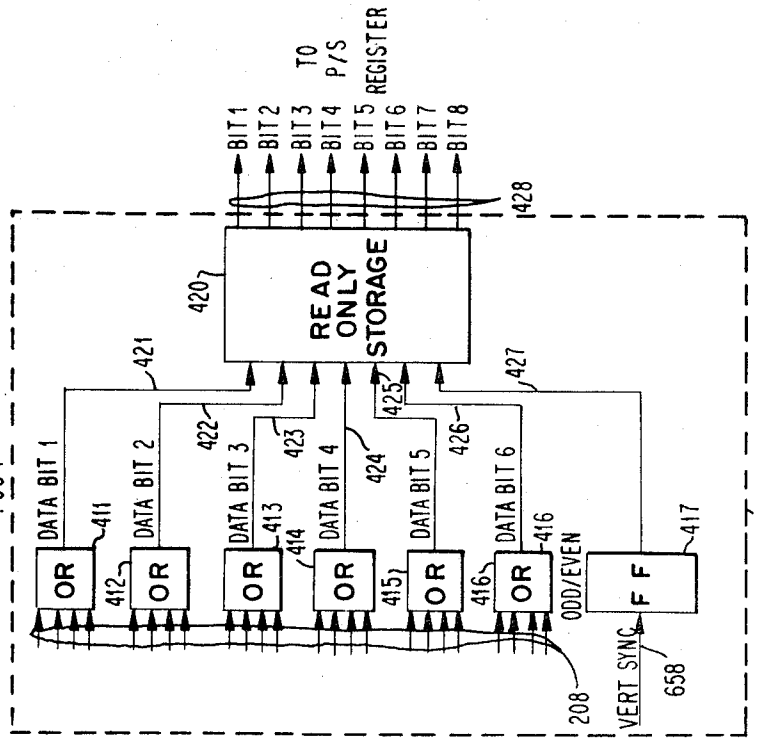
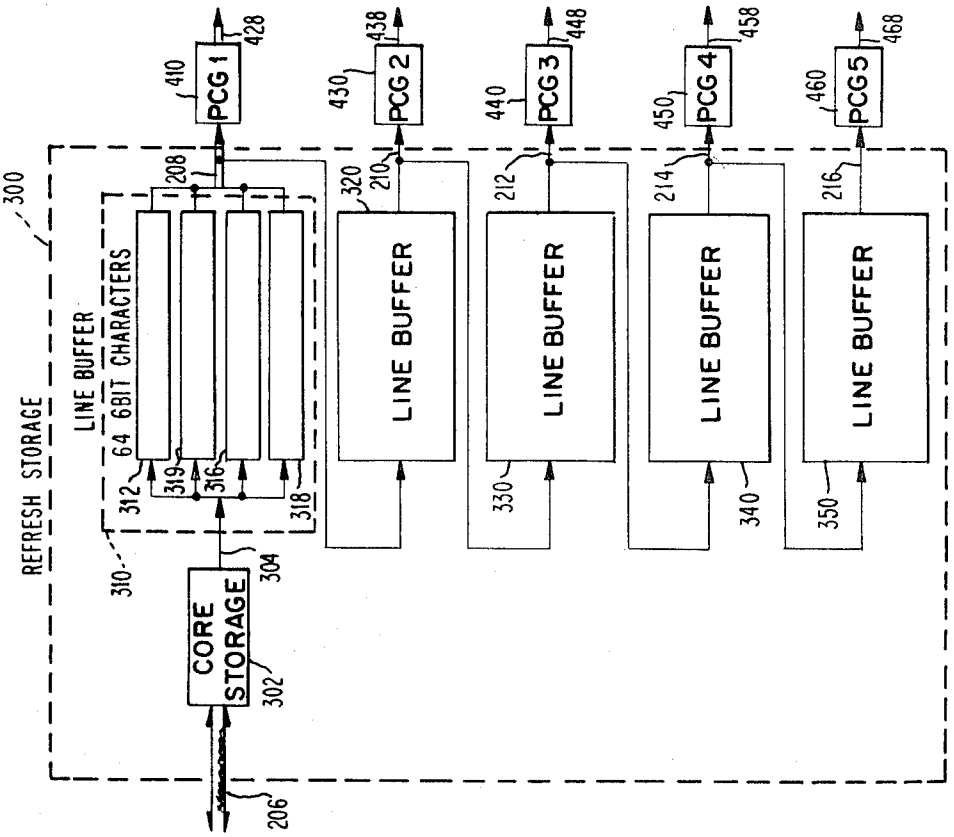

PCG 1
DATA BIT 1
DATA BIT 2
DATA BIT 3
DATA BIT 4
DATA BIT 5
DATA BIT 6
OR
ODD/EVEN
F F
VERT SYNC
READ ONLY STORAGE
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
TO P/S REGISTER
410
411
412
413
414
415
416
417
420
421
422
423
424
425
426
427
428
208
658

FIG. 4


REFRESH STORAGE
LINE BUFFER
64 6BIT CHARACTERS
CORE STORAGE
LINE BUFFER
PCG 1
PCG 2
PCG 3
PCG 4
PCG 5
300
302
304
310
312
316
318
319
320
330
340
350
410
428
430
438
440
448
450
458
460
468
206
208
210
212
214
216

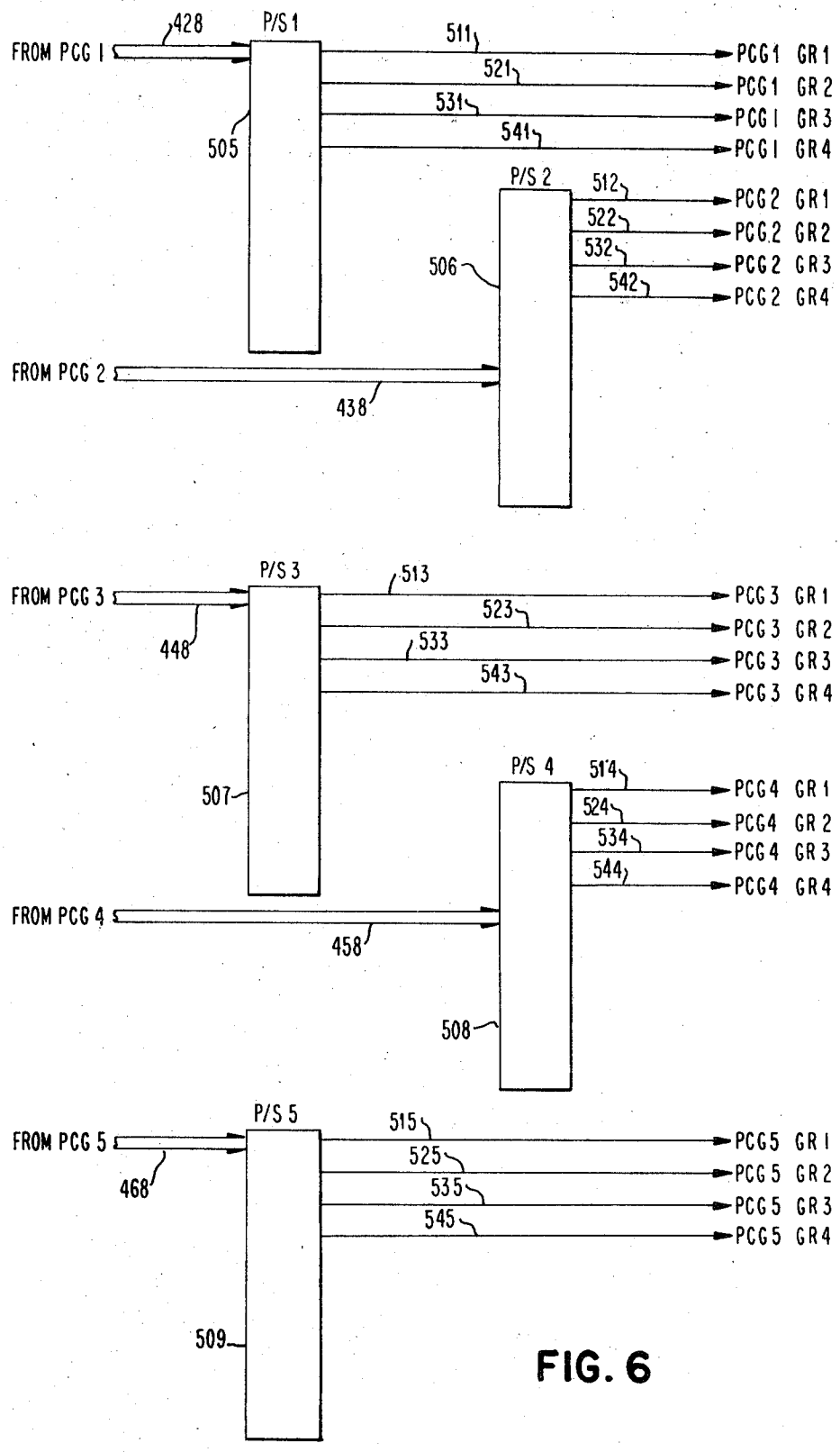

FROM PCG 1
428
P/S 1
505
511
521
531
541
PCG1 GR1
PCG1 GR2
PCG1 GR3
PCG1 GR4
P/S 2
506
512
522
532
542
PCG2 GR1
PCG2 GR2
PCG2 GR3
PCG2 GR4
FROM PCG 2
438
FROM PCG 3
448
P/S 3
507
513
523
533
543
PCG3 GR1
PCG3 GR2
PCG3 GR3
PCG3 GR4
P/S 4
514
524
534
544
PCG4 GR1
PCG4 GR2
PCG4 GR3
PCG4 GR4
FROM PCG 4
458
508
FROM PCG 5
468
P/S 5
509
515
525
535
545
PCG5 GR1
PCG5 GR2
PCG5 GR3
PCG5 GR4

FIG. 6

FIG. 6A

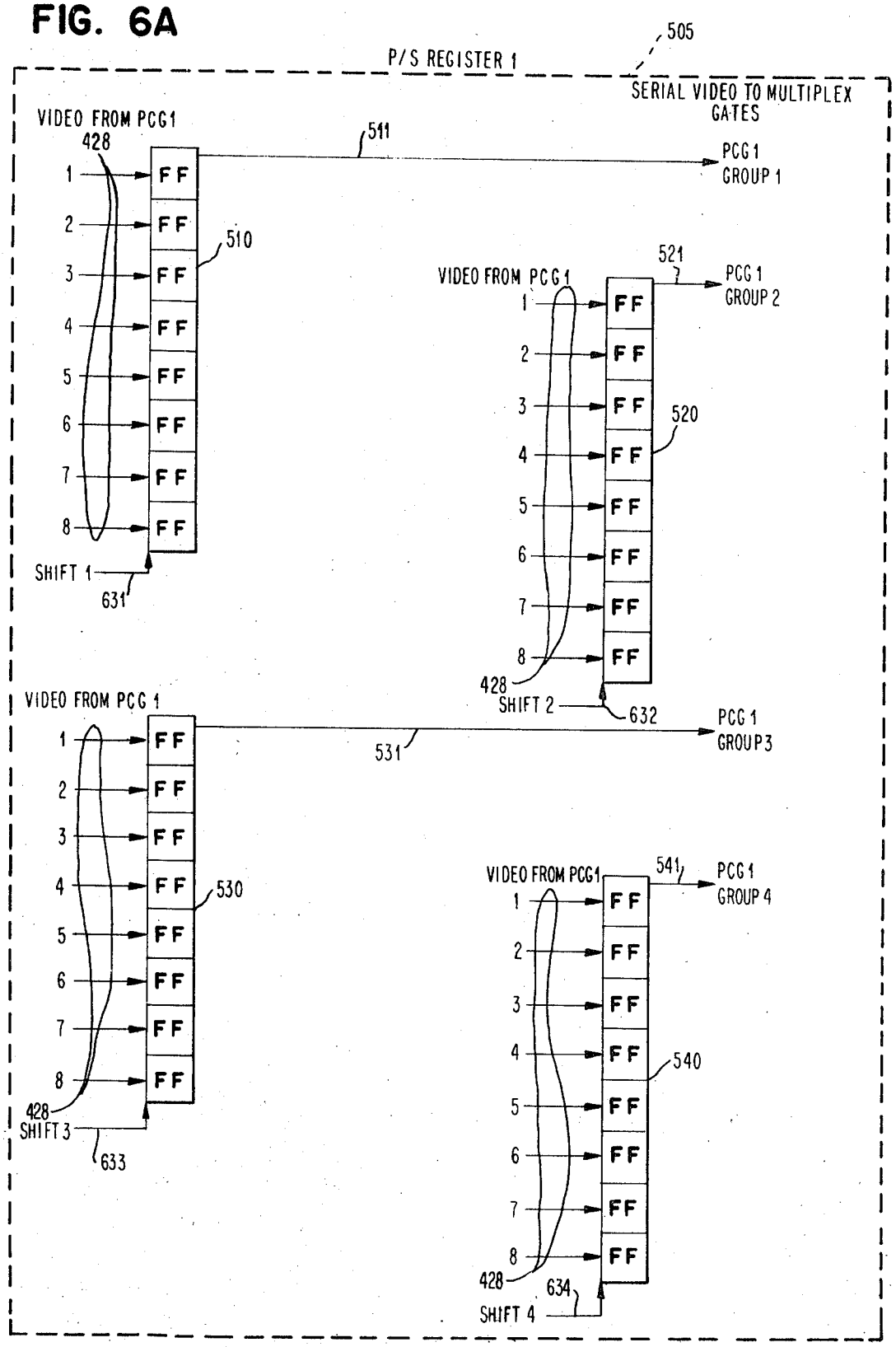

505
P/S REGISTER 1
SERIAL VIDEO TO MULTIPLEX GATES
VIDEO FROM PCG1
428
1
2
3
4
5
6
7
8
FF
510
511
PCG 1 GROUP 1
SHIFT 1
631
VIDEO FROM PCG 1
521
PCG 1 GROUP 2
520
SHIFT 2
632
VIDEO FROM PCG 1
531
PCG 1 GROUP 3
530
SHIFT 3
633
VIDEO FROM PCG1
541
PCG 1 GROUP 4
540
SHIFT 4
634

FIG. 7

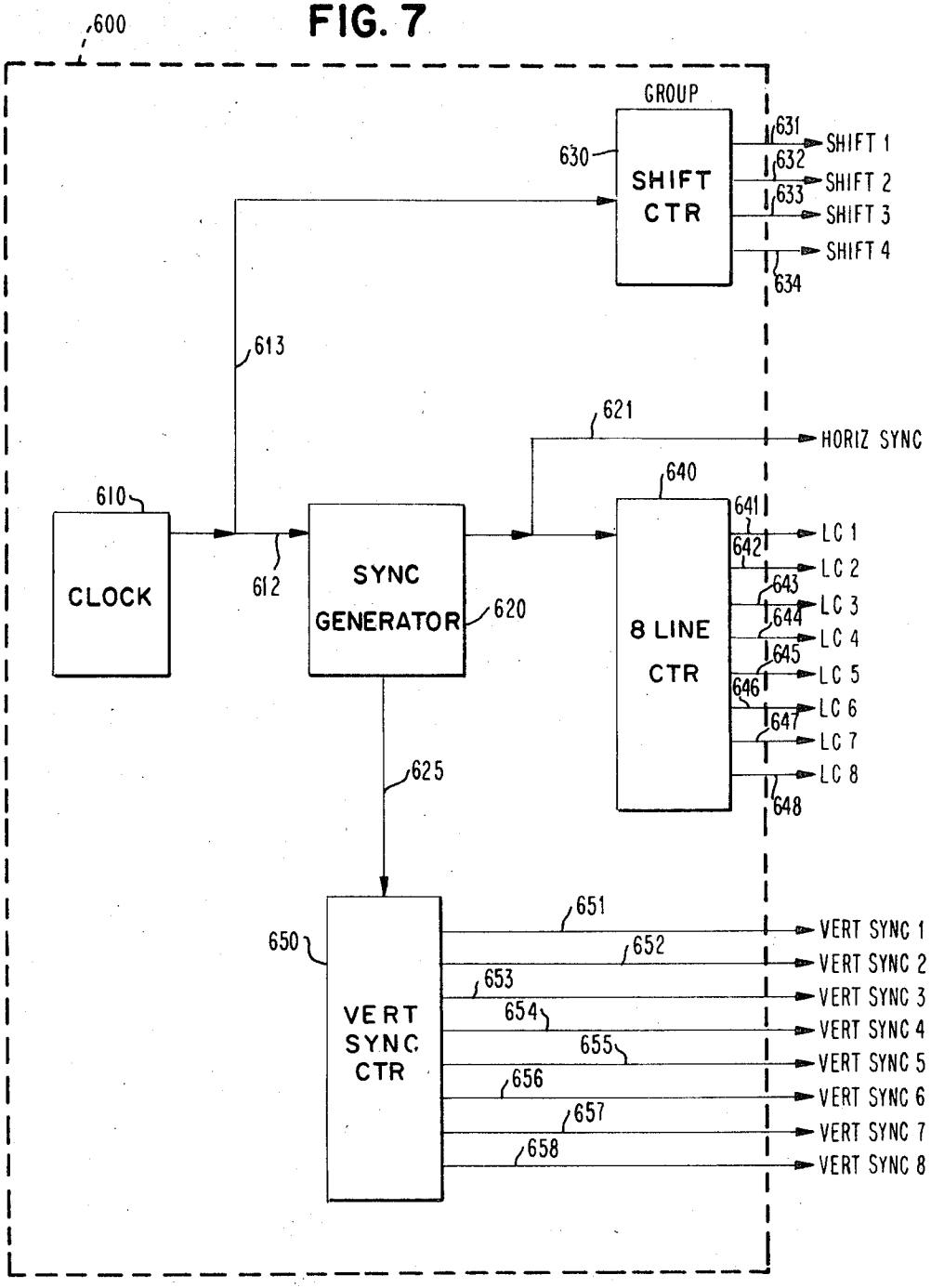

600
GROUP
630
SHIFT CTR
631
632
633
634
SHIFT 1
SHIFT 2
SHIFT 3
SHIFT 4
613
621
HORIZ SYNC
610
CLOCK
612
SYNC GENERATOR
620
640
8 LINE CTR
641
642
643
644
645
646
647
648
LC 1
LC 2
LC 3
LC 4
LC 5
LC 6
LC 7
LC 8
625
650
VERT SYNC CTR
651
652
653
654
655
656
657
658
VERT SYNC 1
VERT SYNC 2
VERT SYNC 3
VERT SYNC 4
VERT SYNC 5
VERT SYNC 6
VERT SYNC 7
VERT SYNC 8

FIG. 8

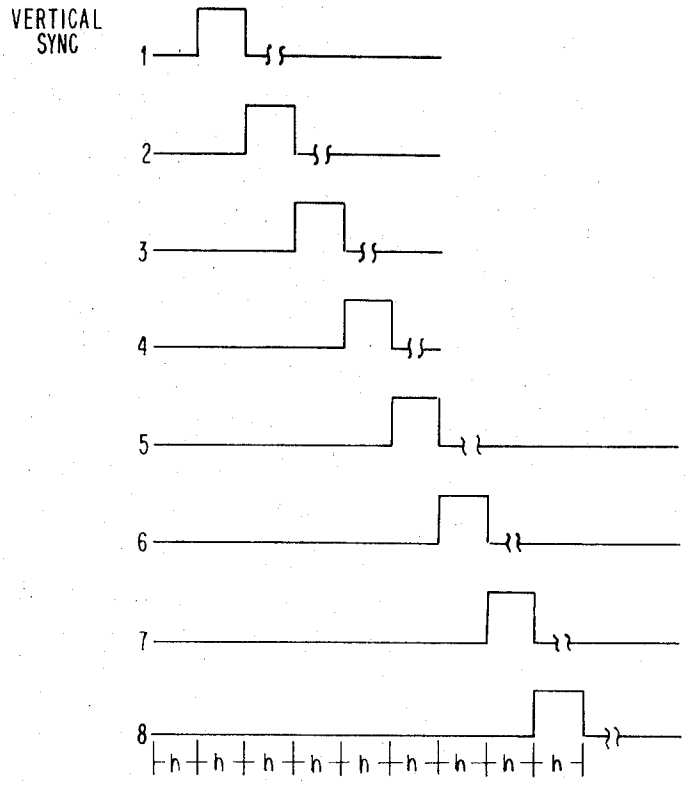
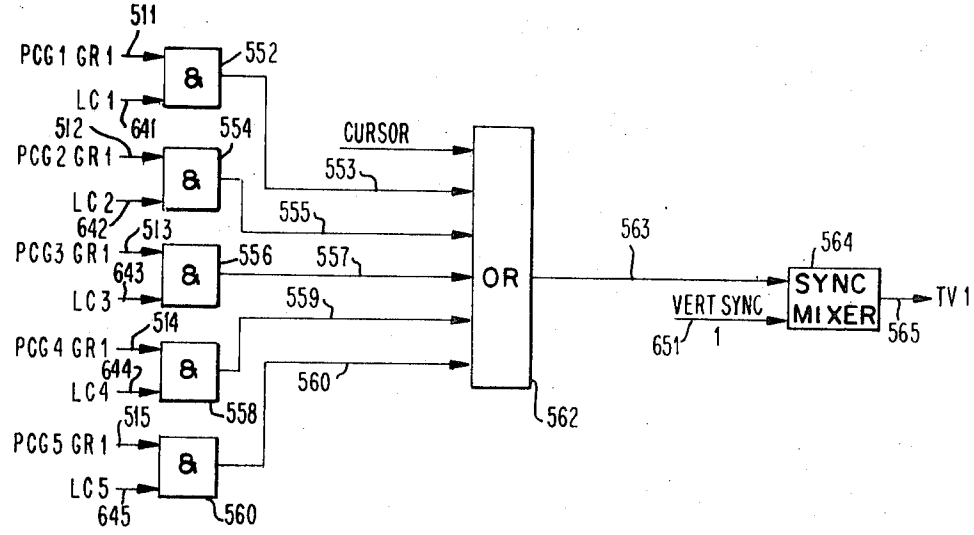


FIG. 9

	LINE COUNT							
	1	2	3	4	5	6	7	8
PCG 1 GR 1	(1)	2	3	4	5	6	7	8
2	9	10	11	12	13	14	15	16
3	17	18	19	[20]	21	22	23	24
4	25	26	27	28	29	30	31	32
PCG 2 GR 1	8	(1)	2	3	4	5	6	7
2	16	9	10	11	12	13	14	15
3	24	17	18	19	[20]	21	22	23
4	32	25	26	27	28	29	30	31
PCG 3 GR 1	7	8	(1)	2	3	4	5	6
2	15	16	9	10	11	12	13	14
3	23	24	17	18	19	[20]	21	22
4	31	32	25	26	27	28	29	30
PCG 4 GR 1	6	7	8	(1)	2	3	4	5
2	14	15	16	9	10	11	12	13
3	22	23	24	17	18	19	[20]	21
4	30	31	32	25	26	27	28	29
PCG 5 GR 1	5	6	7	8	(1)	2	3	4
2	13	14	15	16	9	10	11	12
3	21	22	23	24	17	18	19	[20]
4	29	30	31	32	25	26	27	28

FIG.10

MULTIPLEX VIDEO GENERATOR



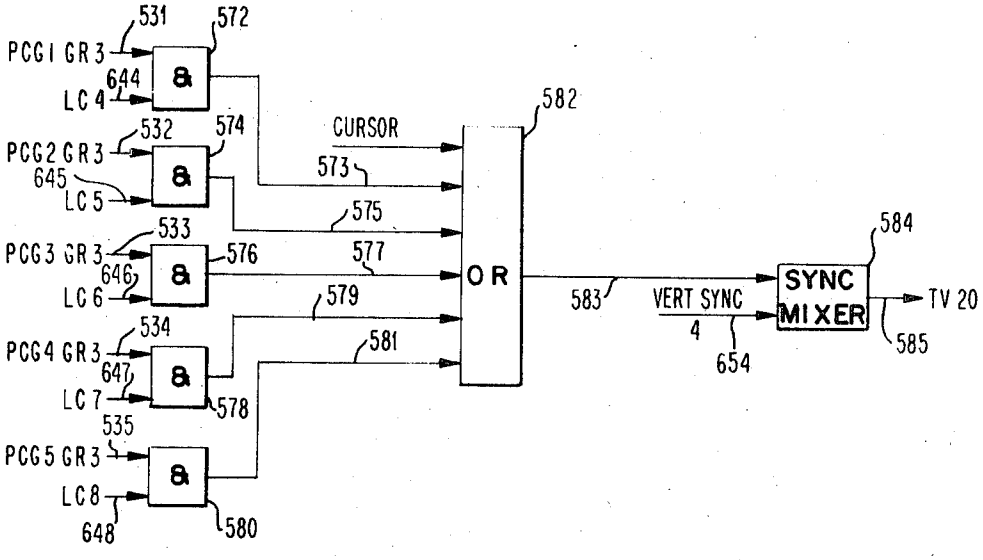


FIG. 11

HEXADECIMAL REPRESENTATION OF VIDEO DATA-ROW 1 ODD

	1	2	3	4	5	6	7	8	1	2	3	4	5
PCG 1	18	18	18	18	18	18	18	18	FC				
2		7E	7E	7E	7E	7E	7E	7E	7E	C7			
3			C3	C3	C3	C3	C3	C3	C3	C3	FE		
4				FF	FF	FF	FF	FF	FF	FF	FF	C7	
5					C3	C3	C3	C3	C3	C3	C3	C3	FE

HEXADECIMAL REPRESENTATION OF VIDEO DATA-ROW 1 EVEN

PCG 1	3C	3C	3C	3C	3C	3C	3C	3C	FE				
2		E7	E7	E7	E7	E7	E7	E7	E7	C7			
3			FF	FF	FF	FF	FF	FF	FF	FF	FE		
4				C3	C3	C3	C3	C3	C3	C3	C3	C7	
5					C3	C3	C3	C3	C3	C3	C3	C3	FC

STAGGERED VIDEO-DIGITAL TV SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

1. Multiplex Character Generator, A. E. Malden, Ser. No. 878,713, filed Nov. 21, 1969.

2. Multiplexed Video Generation, W. C. Cook, et al., Ser. No. 878,711, filed Nov. 21, 1969.

BACKGROUND OF THE INVENTION

This invention relates to computer-connected input/output systems and more particularly to systems for generating symbols for display on display devices in response to information signals from a central processor unit.

In the prior art, symbol generators have been described in which a group of display devices received inputs from a corresponding group of synchronous refresh storage devices such as delays lines or rotating magnetic disks. These synchronous storage devices received as inputs a stream of video information generated by a corresponding group of character generators wherein each character generator generated the complete character for one or possibly two display devices. The inputs to this group of character generators was in the form of parallel digital information usually from some form of temporary storage.

Systems of this nature require many character generators and many synchronous storage elements to generate information for presentation on a large cluster of display devices. Due to limitations of cost and size, systems of this nature were usually limited to a maximum of eight display devices per control unit.

Accordingly, it is an object of this invention to more efficiently generate symbols for presentation on a large cluster of input/output devices.

It is another object of this invention to generate symbols for a large cluster of input/output devices by staggering the input data signals to allow multiplexed use of a segmented character generator.

It is a further object of this invention to generate symbols for a large cluster of input/output devices wherein the vertical synchronization signals are staggered to allow uniform presentation of staggered video signals.

SUMMARY OF THE INVENTION

Accordingly, the invention comprises apparatus for generating symbols for display on a group of input/output devices including a set of sequential line buffers, which stagger the presentation of input data to a set of symbol segment generators and a set of staggered vertical synchronization signals which act in conjunction with the staggered input data signals to achieve uniform video presentation position on each of the input/output devices.

The various features of the invention and details of operation are defined with particularity in the following specification.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a graphical illustration of the formation of individual symbol patterns for a group of eight display terminals;

FIG. 2 is a block diagram showing a systems environment embodying the invention;

FIG. 3 is a block diagram of a terminal control unit embodying the invention;

FIG. 4 is a block diagram illustrating a segmented character generator with a refresh storage connected to the inputs of the various segment generators;

FIG. 5 shows a block diagram which illustrates an embodiment of a single segment generator;

FIG. 6 is a block diagram showing the connections between the segmented character generator and a group of parallel to serial registers;

FIG. 6A shows in more detail the construction of a representative parallel to serial register;

FIG. 7 is a block diagram showing the generation of the various synchronization and control signals necessary for the operation of the multiplexed character generator;

FIG. 8 is a timing diagram showing the relationship between the vertical synchronization signals used to drive the group of display terminals;

FIG. 9 is a chart illustrating how the video signals for display terminal No. 1 and display terminal No. 20 are multiplexed;

FIG. 10 shows the gating circuits which perform the multiplexing of the signals shown in the chart of FIG. 9 to generate the video signals for representative video terminals No. 1 and No. 20;

FIG. 11 shows a hexidecimal representation of the video data for a row of characters on the odd and even scan, showing the data that is being generated by each of the segment generators at any instant of time; the first eight symbols generated are the letter A the ninth symbol generated is the letter B. This corresponds to the illustration shown in FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

System Environment

Referring now to FIG. 2, a group of display terminals **101** through **132** are connected to a terminal control unit (TCU) **200** by lines **201**. TCU **200** communicates with central processing unit (CPU) **50** by lines **52**. For illustrative purposes the symbols A and B are shown to be the first two symbols of the first row of characters on each of the first eight display terminals **101** through **108**.

TERMINAL CONTROL UNIT

Referring now to FIG. 3, TCU 200 is shown in block diagram form. Incoming information is presented to I/O unit **204** on lines **202**. I/O unit **204** then transfers in parallel the appropriate signals to refresh storage **300** on lines **206**. Refresh storage **300** has a plurality of output lines **208**, **210**, **212**, **214** and **216** which are connected respectively to segment generators PCG1 **410** PCG2 **430**, PCG3 **440**, PCG4 **450** and PCG5 **460**. The data transferred between refresh storage **300** and character generator **400** along each of the lines mentioned is in parallel byte form. The segmented character generator has a plurality of output lines, one group of lines in parallel from each of the five segment generators. PCG1 is connected to multiplex generator **500** by line **428**, PCG2 by line **438**, PCG3 by line **448**, PCG4 by lines **458** and PCG5 by line **468**. Multiplex video generator **500** accepts the video signals from said segmented character generator **400** and synchronization signals from timing & control unit **600** and generates appropriate video-scanning signals which are distributed to the plurality of display terminals by lines **252**. Timing and control unit **600** is connected to I/O unit **204** by lines **601**, to refresh storage **300** by lines **602**, to segmented character generator **400** by lines **603** and to multiplex video generator **500** by lines **604**.

REFRESH STORAGE

Referring now to FIG. 4, refresh storage **300** has two major sections. Information bytes in binary form are presented to core storage **302** by line **206** which connects the I/O unit **204** (see also FIG. 3) to the refresh storage **300**. Core storage **302** stores command and data information in parallel in byte form for transmission to a group of line buffers. Core storage **302** is connected to the first line buffer **310** by lines **304**. In an exemplary embodiment line buffer **310** contains four parallel, six bit, 64 character buffers **312**, **319**, **316** and **318**. Four parallel buffers allow simultaneous generation of video symbols for four times as many display terminals as if a single six bit, 64 character buffer were used. Line buffers **320**, **330**, **340** and **350** are identical to line buffer **310**. The outputs of line buffer **310** are connected to the inputs of segment generator PCG1 **410** and also to the inputs of line buffer **320**. In like manner, the outputs of line buffer **320** are connected by lines **210** to

the inputs of segment generator **430** and to the inputs of line buffer **330**. The outputs of line buffer **330** are connected by lines **212** to the inputs of segment generator **440** and to the inputs of line buffer **340**. The outputs of line buffer **340** are connected by lines **214** to the inputs of segment generator **450** and to the inputs of line buffer **350**. The outputs of line buffer **350** are connected by lines **216** to segment generator **460**. It can be seen that in like manner, if the number of segment generators PCGn are increased, the number of line buffers can also be increased to adapt the system to any font of symbols desired.

SEGMENTED SYMBOL GENERATOR

Referring now to FIG. **5**, an exemplary segment generator **410** is shown. Lines **208** which are the outputs of the four buffers which make up line buffer **310** (see also FIG. **4**) are connected to a plurality of OR circuits **411**, **412**, **413**, **414**, **415**, and **416**. The output **421** of OR-circuit **411** represents symbol data bit 1. The output **422** of OR-circuit **412** represents symbol data bit 2. The output **423** of OR-circuit **413** represents symbol data bit 3. The output **424** or OR-circuit **414** represents symbol data 4. The output **425** or OR-circuit **415** represents symbol data bit 5 and the output **426** of OR-circuit **416** represents symbol data bit 6. It can be seen also that a number of data bits used to encode the symbol information could be either contracted or expanded depending upon the specific group of symbols involved. For example, an eight-bit code could be used wherein additional OR circuits and inputs to read-only storage **420** would be necessary.

The odd/even signal is presented to read-only storage **420** on line **427**. This signal is generated by flip-flop **417** which has as its input the vertical synchronization signal which appears on line **658**.

Read-only storage **420** accepts as its input a data byte representative of a particular symbol to be generated. The output lines **428** of read-only storage **420** represent a single horizontal line segment of the symbol to be generated, which in the exemplary case is an eight-bit parallel byte.

Read-only storage output lines **428** from PCG1 are connected to parallel-to-serial register P/S **1** 505 (see FIG. **6**). In like manner, the outputs **438**, (see also FIG. **4**) **448**, **458**, and **468** from segment generators **430**, **440**, **450**, and **460**, respectively, are connected to P/S **2** 506, P/S **3** 507, P/S **4** 508, and P/S **5** 509, respectively.

Referring now to FIG. **6A**, an exemplary P/S register is shown. Register P/S **1** 505 contains four *n*-bit shift registers where n is equal to the number of bits in the data byte from the read-only storage elements. Since in the preferred embodiment being described, **32** display terminals are being controlled by one terminal control unit, four distinct shift lines are necessary which correspond to the four distinct buffers in each of the line buffers **310**, **320**, **330**, **340** and **350** (see also FIG. **4**). Line **428** is connected in parallel to *n*-bit shift registers **510**, **520**, **530**, and **540**. Referring also to FIG. **7**, group shift lines are generated in group shift counter **630** which is connected to basic clock **610** by lines **613**. Line shift **1** 631 is connected to shift input of shift register **510** (see FIG. **6A**). Line shift **2** is connected to shift register **520** on line **632**. Line shift **3** is connected to shift register **530** on line **633**. Line shift **4** is connected to shift register **540** on line **634**. The serial outputs from the shifts registers are presented to the multiplexed video gates, an example of which is shown in FIG. **10** as AND-circuits **552**, **554**, **556**, **558**, **560**, **572**, **574**, **576**, **578** and **580**.

MULTIPLEXED VIDEO GENERATOR

Referring to FIGS. **6**, **6A**, **9** and **10**, the multiplexed data connections necessary to generate the video signals for representative terminals **1** and **20** of a group of 32 terminals are shown.

In order to generate the correct video signals for display terminal **1**, it can be seen from FIG. **9** that at line count **1** time the segment generator output PCG1GR1 (see also FIG. **6**) must be gated to the video line, and at line count **2** PCG2GR1 must be gated to the video line. In like manner PCG3GR1 at line count **3**, PCG4GR1 at line count **4**, and PCG5GR1 at line count **5** must be gated to the video line for each field of data to achieve a complete horizontal line row of symbols for display terminal **1**.

In like manner, to generate the video signals for display terminal **20**, at line count **4**, segment generator PCG1GR3 is gated; and at line count, **5** PCG2GR3 is gated; at line count **6** PCG3GR3 is gated; at line count **7**, PCG4GR3 is gated; and at line count **8** PCG5GR3 is gated to the video line for display terminal **20**.

The outputs from P/S registers **505**, **506**, **507**, **508**, **509**, are presented to the multiplex video gates according to the chart shown in FIG. **9**.

For display terminal **1**, P/S register output **511** (see FIG. **6**) is connected to AND-circuit **552** (see also FIG. **10**) as one input. Line **641** (see also FIG. **7**) is connected from **8**-line counter **640** to a second input of AND-circuit **552** (FIG. **10**) such that the information presented on line **511** will be gated to OR-circuit **562** along output line **553** at count LC1. In like manner, output line **512** representing PCG2GR1 is connected to a first input to AND-circuit **554** while line **642** is connected from **8**-line counter **640** to a second input of AND-**554**. The output **555** of AND-circuit **554** is connected to a second input of OR-circuit **562** and represents the second horizontal line in each field to be displayed on display terminal **1**. Line **643** is connected to an input of AND-circuit **556** along with PCG3GR1 **513**. The output **557** of AND-circuit **556** is connected to a third input of OR-circuit **562** and represents the third horizontal line in each field for each row of symbols to be generated on display terminal **1**. Line **644** is connected to an input of AND-circuit **558** as is PCG4GR1 **514**. The output **559** of AND-circuit **558** is connected to a fourth input to OR-circuit **562** and represents the fourth line to be generated in each field of each row of symbols to be generated on display terminal **1**. Line **645** is connected to an input of AND-circuit **560** while PCG5GR1 **515** is connected to a second input of AND-circuit **560**. The output **561** of AND-circuit **560** is connected to a fifth input of OR-circuit **562** to provide the fifth line of each field of each row of symbols to be generated on display terminal **1**.

It is clear that if a different symbol set were used, the number of segment generators or the line count outputs could be increased or decreased to meet the requirements of a particular symbol set. In such a case the number of AND-circuits **552** through **560** would accordingly be increased or decreased as well as the number of inputs to OR-circuit **562**.

The output **563** of OR-circuit **562** is connected to one input of sync mixer **564**. The second input to sync mixer **564** is vertical sync **1** 651 (see FIG. **7**) which is generated by vertical sync counter **650**.

Sync mixer **564** can be any one of a number of circuits known in the television art to add a synchronization signal to an information signal for proper display on a display terminal.

The output **565** of sync mixer **564** is then connected to the No. **1** display terminal **101** (FIG. **2**). Referring to FIG. **9**, it can be seen that the video signals for display terminals **1** through **8** are generated from the GR1 signals of segment generators PCG1, 2, 3, 4 and 5. GR2 provides a gating signal for the generation of the video signals for display terminals **9** through **16**. GR3 provides the gating signals for the generation of video signals for display terminals **17** through **24** and GR4 generates the gating signal for the generation of video signals for display terminals **25** through **32**.

Referring again to FIG. **10** and to FIG. **9**, the video signals for display terminal **20** (not shown) is generated in AND-circuit **572** by line count **4** 644 and PCG1GR3, 531, in AND-circuit **574** by line count **5** 645 and PCG2GR3 532, in AND-circuit **576** by line count **6** 646 and PCG3, GR3 533, ANDing in AND-circuit **578** line count **7** 647 and PCG4 GR3 534 and in AND-circuit **580** by line count **8** 648 and PCG5 GR3 535. The outputs **573**, **575**, **577**, **579**, **581** of AND-circuits **572**, **574**,

576, 578, 580 respectively are connected to respective inputs of OR*ircuits* 562 along with a cursor input as in the circuitry for generating the video signals for No. 1 display terminal 101 (FIG. 2).

The cursor can be generated by any conventional means and is ORed into the video stream at AND-circuits 562 or 682. The output 583 of OR-circuit 582 is connected to sync mixer 584 which has as another input vertical sync 4 654 which is generated by vertical sync counter 650. Sync mixer 584 is an identical circuit to sync mixer 564 and circuits of this type are well known in the art. The output 585 of sync mixer 584 is connected to display terminal 20 120.

TIMING AND CONTROL

Referring now to FIGS. 7, 8 and 12, a clock signal generator 610 generates a basic timing signal which is used to generate all the necessary timing signals for the terminal control unit 200. The output of clock generator 610 is connected to sync generator 620 by line 612 and to group shift counter 630 by line 613. Sync generator 620 generates a base vertical synchronization signal which is presented on line 625.

Sync generator 620 is connected to vertical sync counter 650 by line 625 and to 8 line counter 640 by line 621.

Eight-line counter 640 generates signal line count 1 through line count 8 which are required for the multiplex video gating. Vertical sync counter 650 generates a series of n vertical synchronization signals each of which is staggered in time by one horizontal time period. Vertical sync 1 through vertical sync 8 are presented on lines 651 through 658. The time displacement of the vertical synchronization signals is shown clearly in FIG. 8. Where *h* is equal to 1 horizontal line time, including trace and retrace.

The time displacement of vertical synchronization signals 2 through 8 allows the video signals for each of the 32 display terminals 101 (see FIG. 2) through 132 to begin at the same relative position on the face of the display device. Referring to FIG. 11, it can be seen that if the vertical synchronization signals were not displaced in time, at a first instant in time, a video signal would appear only on display terminals 1, 9, 17, and 25. At the beginning of a second horizontal line scan in each field, a video signal would appear in addition only on display terminals 2, 10, 18 and 26, on the third horizontal line scan display terminals 3, 11, 19 and 27 and so on with an additional 4 displays beginning with each successive horizontal line until all 32 displays are presenting symbols.

The staggering of the vertical synchronization signal allows the video signal for each of the 32 display terminals to begin the first horizontal line of each field at the same relative position on each display device.

Group shift counter 630 provides four shift signals shift 1, 631, shift 2, 632, shift 3, 633 and shift 4 634. These shift signals are presented to P/S registers to gate the video information for the proper display terminal to the multiplex gate at the correct time.

OPERATION

Referring now to FIGS. 2, 3, 4 and 5, the operation of a preferred embodiment of the invention will be described.

Information to be displayed is transmitted from CPU 50 (FIG. 2) to terminal control unit 200 along lines 52. Terminal control unit 200 then generates appropriate video signals for the various display terminals in response to the information from the CPU 50. These video signals are transmitted to display terminals 101 through 132 along line 201.

Terminal control unit 200 receives the information from CPU 50 in I/O control 204 (FIG. 3) which performs all necessary interface communications with the CPU 50. The information is then transmitted to refresh storage 300 and stored in core storage 302. At the appropriate time under the control of timing and control element 600 (FIG. 3), information bytes representing symbols to be displayed are transmitted to a first line buffer 310. Line buffer 310 acts as a buffer between core storage 302 and the first segment generator PCG1 410. Line buffer 310 is not necessary in applications where the operating speed of the core storage and the segment generator are comparable. Segment generator 410 generates the first scan line of a symbol in each row of symbols on the odd horizontal scans and the second line of a symbol in each row of symbols on the even horizontal scans in response to the information byte from line buffer 310.

Each of the line buffers 310, 320, 330, 340 and 350 provides a delay of one horizontal line scan time so that the output signals from line buffer 310 to line buffer 320, from line buffer 320 to line buffer 330, from line buffer 330 to line buffer 340 and from line buffer 340 to line buffer 350 begin at the start of a row of symbols. Thus, in response to the inputs from the respective line buffers, PCG2 430 generates the third line of each symbol in a row on the odd horizontal scans and the fourth line of each symbol in a row on the even horizontal scans, PCG3 440 generates the fifth line of each symbol in a row on the odd horizontal scans and the sixth line of each symbol in a row on the even horizontal scans, PCG4 450 generates the seventh line of each symbol in a row on the odd horizontal scans and the eighth line of each symbol in a row on the even horizontal scans and the PCG5 460 generates the ninth line of each symbol in a row on the odd horizontal scans and the 10th line of each symbol in a row on the even horizontal scans.

It is clear that this apparatus could be extended to accommodate larger character sizes or reduced to accommodate smaller character sizes by adding or deleting line buffers and segment generators.

Timing and control circuitry 600 controls the gating of each of the four groups of information signals from the line buffers to the segment generators along lines 208 and also controls the timing of the output signals from the read-only storage elements 240 to multiplex video generator 500.

The outputs from character generator 400 present a parallel signal which contains the video information. Timing and control unit 600 also provides control signals and timing signals along lines 604 to multiplex video generator 500. Multiplex video generator 500 transmits the video signals to the appropriate display terminal for visual display.

Referring now to FIGS. 1, 2, 3, and 11, the generation of representative symbols will be explained.

If for example, as shown in FIG. 2, it is desired to generate the symbol uppercase A in the first symbol position in the first row of symbols on each of the first eight display devices, and the symbol upper case B in the second symbol position on the first row of symbols in each of the first display devices, the apparatus embodying the invention would operate in the following manner.

A group of information signals in parallel byte form representing the symbol A is transmitted from CPU 50 to terminal control 200 and stored in core storage 302. Assuming each of these information bytes takes the binary form 000001, which is the binary representation for the symbol A. At the appropriate instant of time, in synchronism with the raster scan for the display devices, the information byte representing the symbol A for the first row of symbols of the first display device is gated to the sequential line buffers (FIG. 4).

The binary representation 000001 acts as an address for a particular group of storage elements in segment generator 410 which have stored therein the video representation for the first line of the symbol A.

In eight-bit binary form, the video representation for the first line of the symbol A is 00011000. This binary information is also represented in hexadecimal notation as "18".

The eight-bit binary representation is transmitted on lines 428 to P/S converter 505 (FIGS. 6, 6A).

P/S converter 505 serializes the eight-bit video representation and presents this serial representation along line 511 to multiplex video generator gates 552 (FIG. 10).

Since this example deals only with the data generated for the first eight display devices 101 through 108, the other outputs 521, 531, and 541 of P/S converter 505 will not be ex-

plained in detail. These outputs represent the video signals for display devices **109** through **116**, **117** through **124** and **125** through **132** respectively.

Due to the speed of operation of the core storage **302** and the segment generators **410** through **460**, it is possible to operate four groups of signals in parallel through a single set of line buffers and a single segmented character generator.

Referring now to FIGS. **6** & **10**, the output line **511** which transmits the video signals for the first segment of each symbol to be displayed on display devices **101** through **108**, multiplex gate **552** is turned on by signal LC1 on line **641** during line **1** of each row of symbols on odd horizontal scans and line **2** the first line of each row of symbols on even horizontal scans. The video being presented on line **511** at the time of the first line of an odd horizontal scan is hexadecimal "18," which is transmitted to sync mixer **564** (FIG. **10**) through OR-circuit **562**.

In sync mixer **564** synchronization signals are added to the video signals to form a composite video signal for transmission to display terminal **101**. The sync signal vertical sync **1** represents a set of scanning synchronization signals which cause the raster on display devices **101**, **109**, **117**, **125** to begin one horizontal scanning line time in advance of the beginning of the raster scan, for display devices **102**, **110**, **118**, and **126**, which is in synchronism with sync signal vertical sync **2**.

This "staggering" of the synchronization signals, and therefore of the raster scan of the groups of display devices, allows the visual image presented by each display device to begin at the same relative location on the face of each display device.

If the synchronization signals were not "staggered" the visual impression obtained on viewing eight display devices side-by-side would be that each row of characters in the second and subsequent displays would be displaced vertically down two horizontal lines from the preceding display device. This would result in an effect similar to that shown in FIG. **1** if the first symbol from each display device were placed side-by-side on a single composite display device.

In a similar manner as described above, one horizontal line time after the information byte has passed through line buffer **320**, the binary representation 000001 is presented to segment generator **430** which then in response to this input address signal and ODD/EVEN flip-flop **417** in ODD state, generates the binary representation 011111110 which represents line **3** of the symbol A. At the same time, the information signal representative of the first symbol on display device **102** is presented to segment generator **410**.

For simplicity of explanation, the symbol A will be generated also as the first symbol in the first line of symbols on display device **102**.

In a similar manner to that described above, the video signal from segment generator **430** (FIG. **4**) is serialized and presented to gate **554** (FIG. **10**) which is turned on by LC2 during the second line of each row of symbols in each horizontal scan. Thus, the video representation 01111110 is transmitted to display device **101** in proper time sequence.

As can be seen from FIG. **1**, the data representing the first line of the first row of symbols for the display device **102** is similarly presented to the display device at the same time. However, the gating for display terminal **102** is not shown since the chart of FIG. **9** sets out the appropriate gating conditions for each of the display terminals for each line count and segment generator.

In like manner, one horizontal line time later the information signal, representing upper case A, is presented to segment generator **440** (FIG. **4**) which responds by generating video representation 11000011 which corresponds to the fifth line of the symbol A. At the same time, line **3** of the first symbol on display device **102** is being generated and line **1** of the first symbol for display device **103** is being generated.

In like manner, line **7** and **9** of the first symbol in the first row of symbols for display device **101** is generated on the first odd horizontal scan. The video representation for line **7** being 11111111 and for line **9** being 11000011.

At the time line **7** is being generated on display device **101**, line **5** is being generated for display device **102**, line **3** is being generated for display device **103** and line **1** is being generated for display device **104**. It may be noted at this point, that when the first symbol to be generated on each display is being displayed, the segment generators **410**, **430**, **440**, **450** and **460** (FIG. **4**) are operated in a staggered manner as shown in FIG. **11**, with segment generator **460** not active to generate line **9** for the first display device **101** until PCGI segment generator **410** is generating the first line of the first symbol for display device **105**.

In the manner described above, the first line of the first symbol to be displayed on each of the display devices **101** through **108** is generated in the first eight multiplexed symbol positions. In the ninth symbol position, the first scan line of the first symbol in the second row of symbols on display device **101** can be generated since segment generator **410** is free. In like manner, one horizontal line time later the third line of the first symbol in the second row to be generated on the first display device **101** is generated while the first scan line of the first symbol in the second row to be generated on display device **102** is generated. Similarly, the second and further symbols on each row of symbols for each display device are generated in the staggered manner described above.

Referring to FIGS. **9** and **10**, the multiplexing of the video representations to form the visual images on display device **120** is shown.

Display device **120** is contained in the third group of eight multiplexed video display devices. It can be seen that the video signals representing the video to be displayed on display device **120** are represented in each case by PCGIGR3 on line **531**, PCG2GR3 on line **532**, PCG3GR3 on line **533**, PCG4GR3 on line **534** and PCG5GR3 on line **535**.

Since display device **120** is the fourth unit in the third group, the staggered synchronization signals are the same as for display device **104**.

Thus, the first line of video for each symbol to be generated on display device **120** is gated by signal LC4 along line **644**. This means that while the fourth segment (lines **7** on odd or **8** on even scans) of each symbol on display device **101** is being generated, the first segment (lines **1** on odd or **2** on even scans) of each symbol on display device **120** is being generated. In like manner, the second segment is generated at LC5 time, the third segment is generated at LC6 time, the fourth segment is generated at LC7 time and the fifth segment is generated at LC8 time.

The video signals are mixed in sync mixer **584** with vertical sync **4** to allow the visual image presented to begin at the same relative location on the display device as each of the other display devices.

The particular font of characters employed requires eight spots in the horizontal direction and ten lines in the vertical direction with an additional six vertical lines providing the space between row of symbols and two spots providing the horizontal space between characters in each row. This format, of course, is completely flexible and the invention as described could be used with any symbol format.

While the operation of the invention has been primarily described for an odd horizontal field, operation on the even horizontal field would be identical with line counts **1** through **8** representing horizontal lines **2**, **4**, **6**, **8**, **10**, **12**, **14** and **16** respectively, rather than lines **1**, **3**, **5**, **7**, **9**, **11**, **13** and **15** for each row of symbols.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. Apparatus for staggering information signals for simultaneous generation of a plurality of symbol segments for display on a plurality of display devices, comprising:

storage means for storing information signals representative of all symbols to be displayed on all of said plurality of display devices;

a plurality of sequential buffer storage registers, wherein said information signals are transmitted to the input of a first buffer register and the output of each said buffer register is connected to the input of a succeeding buffer register in series, each of said buffer registers storing sequentially a plurality of said information signals representative of a plurality of rows of information to be displayed on a plurality of said display devices.

2. Apparatus according to claim 1 wherein each of said buffer registers comprises a plurality of parallel shift registers to store symbol representations for a complete row of symbols for four display devices; and

wherein said symbol representations are presented to a plurality of segment generators in a time-staggered manner to allow multiplexing of display information for a further plurality of display devices.

3. Apparatus according to claim 2, further comprising:

a plurality of vertical synchronization signal generators for staggering the scanned raster of the display presentation of said plurality of display devices to achieve uniformity of vertical position for rows of symbols generated on each display device.

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