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(19)

(54) BUS-CONNECTED DATA PROCESSING SYSTEM INCLUDING A DIAGNOSTIC DEVICE

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to data processing systems incorporating diagnostic units.

In the past few years data processing systems, particularly of the micro-and minicomputer type, have a plurality of either synchronous or asynchronously operating units which are all tied together via a multiconductor bus. When such units include programmable units having multi-programming capabilities, diagnosis of error conditions within such a system becomes extremely complex. Such error conditions can result from software errors or microde errors, as well as hardware errors. Accordingly, such diagnostic unit must be capable of being selectively inserted at one of any diverse locations in the bus for maximizing testing flexibility.

Some prior art testing techniques have included a separate diagnostic bus independent of the data transfer busses. Such diagnostic busses include addressing unit techniques for isolating a failing unit, whether it be caused by software or hardware. However, such units do not have the facility for testing the system of such interconnected units in a system sense, particularly for injection of anomalous signals for test purposes. United States Patent No. 3,603,936 shows simulating conditions by injection of microde within a control memory. While this system is highly advantageous for debugging microcode sequences, it is not particularly adaptable for testing multiunit systems of the bus connected type. An example of additional testing for diagnostic circuits incorporated with the data processing system is shown United States Patent No. 3,553,654. There, a rack fault circuit is connected to a plurality of computing elements, however, not of the bus connected type. Additional examples of diagnostic connections are included in the IBM Technical Disclosure Bulletin in articles by W. A. Boothroyd and P. M. Chan, "Half Duplex Teleprocess Organization", May 1970, pages 2319-2320, as well as by R. W. Macak and J. R. Mathis in "Program Controlled Test of External Interface", March 1970, page 1614. The latter shows testing interfaces of cascade connected units using simulation hardware integral with the units connected to a computer or CPU.

According to the present invention there is provided a bus-connected data processing system including a diagnostic signal source, said system including an interrupted bus line having its ends formed by the interruption connected to first and second terminals respectively, in which the first terminal is connected to a first input of a first AND circuit, the output of which is coupled, through a first OR circuit, to the second terminal, and the second terminal is connected to a first input of a second AND circuit, the output of which is coupled, through a second OR circuit, to the first terminal, a signal direction control circuit coupled to second inputs of the AND circuits, and operable selectively to disable either of the AND circuits, said diagnostic signal source being coupled to inputs of the OR circuits selectively to deliver diagnostic signals to the bus line through either or both of the OR circuits.

In order that the invention can be fully understood, a preferred embodiment thereof

will now be described with reference to the accompanying drawings, in which:—

FIGURE 1 is a block diagram of a bus-connected data-processing system having interleaved test vehicles for diagnostic purposes; and

FIGURE 2 is a schematic diagram of a test vehicle employed in the Figure 1 system.

A bus-connected data-processing system 10 includes a bidirectional data bus 11 connected at various points to a plurality of data processing units collectively denoted by numeral 12. A diagnostic unit 13 such as a System 7 computer constructed by International Business Machines Corporation, Armonk, NY, contains programs (not shown) designed to exercise the data processing units 12 as they are connected via bus 11. One or more test vehicles are selectively interleaved in bus 11. For example, unit 15 is electrically interposed between bus connecting points 11A and 11B, respectively, between units 12A and 12B. A control connection 16 extends from diagnostic unit 13 to test vehicle 15. A pair of terminals 20 and 21 connect test vehicle 15 to bus 11 and interrupts the bus connections between points 11A and 11B.

While a single test vehicle 15 may be used in diagnosing bus-connected data-processing system 10, a plurality of such units may be simultaneously used as well as being individually placed in diverse locations of the bus. For example, test vehicle 23 is located to the right of bus point 11B, while test vehicle 24 is interconnected between bus point 11B and data processing unit 12B. The other test vehicles 23, 24 are respectively connected to diagnostic unit 13 as shown for receiving control signals in the same manner that test vehicle 15 receives control signals. In this regard it should be noted that when bus 11 has a plurality of conductors, test vehicles 15, 23, 24 include a like plurality of the later described transmission units, one for each conductor in each direction of transmission with a single controller for controlling the entire test vehicle.

FIGURE 2 is a detailed showing of a single conductor connection for test vehicle 15 together with a preferred form of a direction controller 26. Right transmission unit 27 and a left transmission unit 28 are actuated by controller 26 under direction of diagnostic unit 13 as well as by the operation of the data processing system 10.

Diagnostic unit 13 has output cable 16 for controlling test vehicle 15 in one of a plurality of modes. Assuming that no transmissions have occurred on bus 11 and that diagnostic unit 13 has supplied a test vehicle reset signal over line 30, resetting direction controller 26 to a reset state by resetting the right latch 31 and left latch 32. Right latch 31 disables the left transmission unit while permitting signal transmissions from terminal 20 to terminal 21. Similarly, left latch 31 disables right transmission unit 27 while permitting transmission of signals from terminal 21 to terminal 20. Signal transmissions may include interjected diagnostic signals from unit 13 via line 33 for the right transmission unit 27 and over line 34 for the left transmission unit 28. Additionally, diagnostic unit 16 supplies transmission controlling signals respectively over lines 35 and 36 to transmission units 27, 28.

Assume that unit 12A transmits signals to unit 12B. Such data processing signals are received by test vehicle 15 at terminal 20 and supplied to AND circuit 40 within transmission unit 27. Direction controller 26 being reset provides a gate enabling signal over line 41. The line 41 signal together with the diagnostic unit 13 supplied signal over line 35 enables AND circuit 40 to pass the terminal 20 received signals to line 42. A signal on line 42 travels to direction controller 26 setting right latch 31 to the active state. This action causes latch 31 to supply a transmission unit disabling signal over line 43 to left transmission unit 48. The line 42 signal also travels through delay circuit 43, thence through OR or combining circuit 44 for retransmission to bus 11 via terminal 21. In the event the diagnostic unit 13 desires to supply interjected signals, the diagnostic signals to be interjected are supplied over line 33 to combining circuit 44.

In a first mode, AND circuit 40 is disabled by the signal on line 35 preventing the passage of signals from terminal 20 to line 42. As a result, terminal 21 only passes signals from line 33. On the other hand, AND circuit 40 may be enabled by the line 35 signal for passing the data processing signals from unit 12A while diagnostic unit 13 interleaves further diagnostic signals from line 33 with the data processing signals over terminal 21. It should be noted that if unit 12A does not supply signals through AND circuit 40, direction controller 26 operation is not affected by the injection of signals from diagnostic unit 13 via combiner circuit 44. Additionally, the diagnostic signals on line 33 can travel not only through terminal 21, but also through left transmission unit 28 then over terminal 20 to unit 12A.

The left transmission unit 28 is constructed identically with unit 27. That is, AND circuit 50 receives control signals via lines 36 from diagnostic unit 13 and via line 43 from direction controller 26. Data signals from terminal 21 or from combiner circuit

44 are selectively passed through AND circuit 50 in accordance with the above-described control signals. A signal on line 52 sets latch 32 for supplying it disabling signal over line 41 to AND circuit 40 of transmission unit 27. The AND circuit 50 signal also travels through delay circuit 53, then through OR or combiner circuit 54 to terminal 20. Similarly, combiner circuit 54 can receive diagnostic injection signals over line 34 for transmission to terminal 20 in the same manner that combiner circuit 44 received signals over line 33.

In accordance with all of the above, it is seen that diagnostic unit 13 has complete control over the bus connected data processing system 10 for injecting signals either in one direction on bus 11, in both directions to or from any of the units in the data processing system, as well as interleaving data processing and diagnostic signals on the bus. It is to be understood that with regard to Figure 2 there is one transmission unit 27, 28 for each of the conductors in the bus.

WHAT WE CLAIM IS:—

1. A bus-connected data processing system including a diagnostic signal source, said system including an interrupted bus line having its ends formed by the interruption connected to first and second terminals respectively, in which the first terminal is connected to a first input of a first AND circuit, the output of which is coupled, through a first OR circuit, to the second terminal, and the second terminal is connected to a first input of a second AND circuit, the output of which is coupled, through a second OR circuit, to the first terminal, a signal direction control circuit coupled to second inputs of the AND circuits, and operable selectively to disable either of the AND circuits, said diagnostic signal source being coupled to inputs of the OR circuits selectively to deliver diagnostic signals to the bus line through either or both of the OR circuits.

2. A system as claimed in claim 1, in which the signal direction control circuit is connected to receive outputs from the AND circuits and is operable, upon receipt of a signal from one of the AND circuits, to disable the other of the AND circuits.

3. A system as claimed in claim 1 or claim 2, in which the signal direction control circuit is connected to receive a signal from the diagnostic signal source operable to reset the control circuit thereby to remove any disabling signal from the AND circuits.

4. A system as claimed in any of the previous claims, in which the diagnostic signal source is connected to third inputs of the AND circuits, and is operable, by energisation of one or both of the third inputs, to enable one or both of the AND circuits.

5. A system as claimed in any of the previous claims, in which each AND circuit is coupled to the corresponding OR circuit through a delay circuit.

6. A bus-connected data processing system substantially as described herein with reference to the accompanying drawings.

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1 SHEET *This drawing is a reproduction of the Original on a reduced scale*

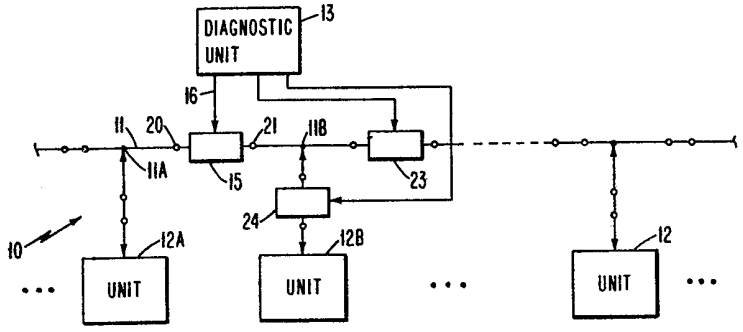

FIG. 1

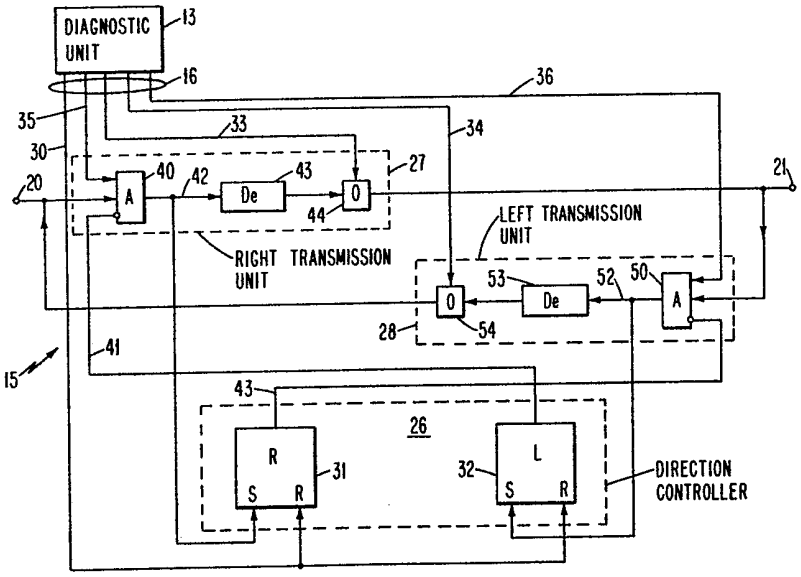

FIG. 2