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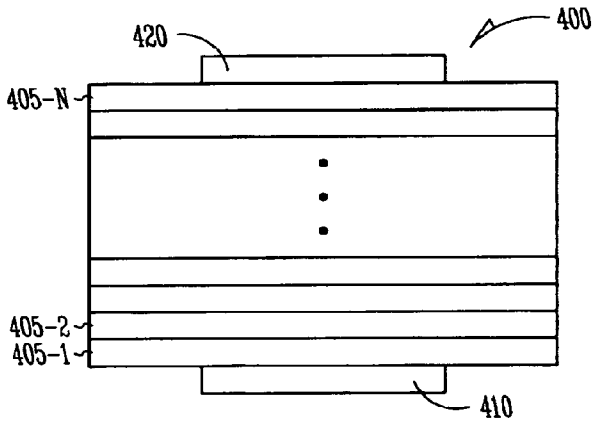
(54) **Title:** BARIUM STRONTIUM TITANIUM OXIDE FILMS



(57) **Abstract:** Apparatus and methods of forming the apparatus include a dielectric layer containing barium strontium titanium oxide layer, an erbium-doped barium strontium titanium oxide layer, or a combination thereof. Embodiments of methods of fabricating such dielectric layers provide dielectric layers for use in a variety of devices. Embodiments include forming barium strontium titanium oxide film using atomic layer deposition. Embodiments include forming erbium-doped barium strontium titanium oxide film using atomic layer deposition.

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BARIUM STRONTIUM TITANIUM OXIDE FILMS

Claim Of Priority

Benefit of priority is hereby claimed to U.S. Patent Application Serial Number 11/510,803, filed on August 25, 2006, which application is herein incorporated by reference.

Technical Field

This application relates generally to semiconductor devices and device fabrication.

Background

The semiconductor device industry has a market driven need to reduce the size of devices used in products such as processor chips, mobile telephones, and memory devices such as dynamic random access memories (DRAMs). Currently, the semiconductor industry relies on the ability to reduce or scale the dimensions of its basic devices. This device scaling includes scaling dielectric layers in devices such as, for example, capacitors and silicon based metal oxide semiconductor field effect transistors (MOSFETs) and variations thereof, which have primarily been fabricated using silicon dioxide. A thermally grown amorphous SiO_2 layer provides an electrically and thermodynamically stable material, where the interface of the SiO_2 layer with underlying silicon provides a high quality interface as well as superior electrical isolation properties. However, increased scaling and other requirements in microelectronic devices have created the need to use other materials as dielectric regions in a variety of electronic structures.

Brief Description of the Drawings

Figure 1 shows a representation of an embodiment of a transistor having a dielectric layer containing a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof.

Figure 2 shows a representation of an embodiment of a floating gate transistor having a dielectric layer containing a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof.

Figure 3 shows a representation of an embodiment of a capacitor having a dielectric layer containing a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof.

Figure 4 depicts a representation of an embodiment of a dielectric layer having multiple layers including a barium strontium titanium oxide layer, an erbium-doped barium strontium titanium oxide layer, or a combination thereof.

Figure 5 illustrates a representation of an embodiment of a flat panel display having an erbium-doped barium strontium titanium oxide film.

Figure 6 depicts a representation of an embodiment of an optoelectronic apparatus having an electrooptic region that includes a barium strontium titanium oxide layer, an erbium-doped barium strontium titanium oxide layer, or a combination thereof.

Figure 7 depicts a representation of a simplified diagram for an embodiment of a controller coupled to an electronic device having a dielectric layer containing a barium strontium titanium oxide layer, an erbium-doped barium strontium titanium oxide layer, or a combination thereof.

Figure 8 illustrates a representation of a block diagram for an embodiment of an electronic system having devices with a dielectric film containing a barium strontium titanium oxide layer, an erbium-doped barium strontium titanium oxide layer, or a combination thereof.

Detailed Description

The following detailed description refers to the accompanying drawings that show, by way of illustration, embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice embodiments of the present invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made. The various embodiments are not necessarily mutually

exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

The term substrate used in the following description includes any structure having an exposed surface with which to form a structure such as an integrated circuit (IC) structure. The term substrate is understood to include a semiconductor wafer. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. A substrate includes doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures known to those skilled in the art. The term conductor is understood to generally include n-type and p-type semiconductors, and the term insulator or dielectric is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense.

In an embodiment, a barium strontium titanium oxide film is formed using atomic layer deposition (ALD). In an embodiment, an erbium-doped barium strontium titanium oxide film is formed using atomic layer deposition. Various forms of ALD may be used including radical-enhanced atomic layer deposition. Embodiments include structures for capacitors, transistors, memory devices, optoelectronic devices, and systems with a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof structured as one or more monolayers, and methods for forming such structures. Forming such a dielectric film using atomic layer deposition allows for the control of transitions between material layers. As a result of such control, both atomic layer deposited barium strontium titanium oxide dielectric films and atomic layer deposited erbium-doped barium strontium titanium oxide dielectric films can have an engineered transition with the surface of a material on which is configured.

ALD, also known as atomic layer epitaxy (ALE), is a modification of chemical vapor deposition (CVD) and is also called "alternatively pulsed-CVD." In ALD, gaseous precursors are introduced one at a time to the substrate surface

mounted within a reaction chamber (or reactor). This introduction of the gaseous precursors takes the form of pulses of each gaseous precursor. In a pulse of a precursor gas, the precursor gas is made to flow into a specific area or region for a short period of time. Between the pulses, the reaction chamber may be purged with a gas, where the purging gas may be an inert gas. Between the pulses, the reaction chamber may be evacuated. Between the pulses, the reaction chamber may be purged with a gas and evacuated.

In a chemisorption-saturated ALD (CS-ALD) process, during the first pulsing phase, reaction with the substrate occurs with the precursor saturatively chemisorbed at the substrate surface. Subsequent pulsing with a purging gas removes precursor excess from the reaction chamber.

The second pulsing phase introduces another precursor on the substrate where the growth reaction of the desired film takes place. Subsequent to the film growth reaction, reaction byproducts and precursor excess are purged from the reaction chamber. With favourable precursor chemistry where the precursors adsorb and react with each other aggressively on the substrate, one ALD cycle can be performed in less than one second in properly designed flow type reaction chambers. Typically, precursor pulse times range from about 0.5 sec to about 2 to 3 seconds. Pulse times for purging gases may be significantly longer, for example, pulse times of about 5 to about 30 seconds.

In ALD, the saturation of all the reaction and purging phases makes the growth self-limiting. This self-limiting growth results in large area uniformity and conformality, which has important applications for such cases as planar substrates, deep trenches, and in the processing of porous silicon and high surface area silica and alumina powders. Atomic layer deposition provides control of film thickness in a straightforward manner by controlling the number of growth cycles.

The precursors used in an ALD process may be gaseous, liquid or solid. However, liquid or solid precursors should be volatile. The vapor pressure should be high enough for effective mass transportation. Also, solid and some liquid precursors may need to be heated inside the reaction chamber and introduced through heated tubes to the substrates. The necessary vapor pressure

should be reached at a temperature below the substrate temperature to avoid the condensation of the precursors on the substrate. Due to the self-limiting growth mechanisms of ALD, relatively low vapor pressure solid precursors can be used, though evaporation rates may vary somewhat during the process because of changes in their surface area.

There are several other characteristics for precursors used in ALD. The precursors should be thermally stable at the substrate temperature, because their decomposition may destroy the surface control and accordingly the advantages of the ALD method that relies on the reaction of the precursor at the substrate surface. A slight decomposition, if slow compared to the ALD growth, may be tolerated.

The precursors should chemisorb on or react with the surface, though the interaction between the precursor and the surface as well as the mechanism for the adsorption is different for different precursors. The molecules at the substrate surface should react aggressively with the second precursor to form the desired solid film. Additionally, precursors should not react with the film to cause etching, and precursors should not dissolve in the film. Using highly reactive precursors in ALD contrasts with the selection of precursors for conventional CVD.

The by-products in the reaction should be gaseous in order to allow their easy removal from the reaction chamber. Further, the by-products should not react or adsorb on the surface.

In a reaction sequence ALD (RS-ALD) process, the self-limiting process sequence involves sequential surface chemical reactions. RS-ALD relies on chemistry between a reactive surface and a reactive molecular precursor. In an RS-ALD process, molecular precursors are pulsed into the ALD reaction chamber separately. A metal precursor reaction at the substrate is typically followed by an inert gas pulse to remove excess precursor and by-products from the reaction chamber prior to pulsing the next precursor of the fabrication sequence.

By RS-ALD, films can be layered in equal metered sequences that may all be identical in chemical kinetics, deposition per cycle, composition, and

thickness. RS-ALD sequences generally deposit less than a full layer per cycle. Typically, a deposition or growth rate of about 0.25 to about 2.00 Å per RS-ALD cycle may be realized.

Processing by RS-ALD provides continuity at an interface avoiding poorly defined nucleating regions that are typical for chemical vapor deposition (< 20 Å) and physical vapor deposition (< 50 Å), conformality over a variety of substrate topologies due to its layer-by-layer deposition technique, use of low temperature and mildly oxidizing processes, lack of dependence on the reaction chamber, growth thickness dependent solely on the number of cycles performed, and ability to engineer multilayer laminate films with a resolution of one to two monolayers. RS-ALD processes allow for deposition control on the order of monolayers and the ability to deposit monolayers of amorphous films.

Herein, a sequence refers to the ALD material formation based on an ALD reaction of a precursor with its reactant precursor. An ALD sequence for a metal oxide may be referenced with respect to the metal and oxygen. For example, erbium oxide may be formed using a sequence including $Er(thd)_3$ (thd = 2,2,6,6 tetramethyl-3,5-heptanedone) and ozone, as its reactant precursor, where such a sequence may be referred to as an erbium/oxygen sequence or an erbium sequence. In various ALD processes that form an oxide or a compound that contains oxygen, a reactant precursor that contains oxygen is used to supply the oxygen. Herein, a precursor that contains oxygen and that supplies oxygen to be incorporated in the ALD composition formed, which may be used in an ALD process with precursors supplying the other elements in the ALD compound, is referred to as an oxygen reactant precursor. With an ALD process using $Er(thd)_3$ and ozone, ozone is an oxygen reactant precursor. An ALD cycle may include pulsing a precursor, pulsing a purging gas for the precursor, pulsing a reactant precursor, and pulsing the reactant precursor's purging gas. An ALD cycle may include pulsing a precursor, evacuating the reactant chamber, pulsing a reactant precursor, and evacuating the reactant chamber. An ALD cycle may include pulsing a precursor, pulsing a purging gas for the precursor and evacuating the reactant chamber, pulsing a reactant precursor, and pulsing the reactant precursor's purging gas and evacuating the reactant chamber.

In forming a layer of a metal species, an ALD sequence may deal with pulsing a reactant precursor to the substrate surface on which a metal-containing species has been adsorbed such that the reactant precursor reacts with the metal-containing species resulting in the metal and a gaseous by-product that can be removed during the subsequent purging/evacuating process. Alternatively, in forming a layer of a metal species, an ALD sequence may deal with reacting a precursor containing the metal species with a substrate surface. A cycle for such a metal forming sequence may include pulsing a purging gas after pulsing the precursor containing the metal species to deposit the metal. Additionally, deposition of a semiconductor material may be realized in a manner similar to forming a layer of a metal, given the appropriate precursors for the semiconductor material.

In an ALD formation of a material composition having more than two elements, a cycle may include a number of sequences to provide the elements of the composition. For example, a cycle for an ALD formation of an ABO_x composition may include sequentially pulsing a first precursor / a purging gas for the first precursor / a first reactant precursor / the first reactant precursor's purging gas / a second precursor / a purging gas for the second precursor / a second reactant precursor / the second reactant precursor's purging gas, which may be viewed as a cycle having two sequences. In an embodiment, a cycle may include a number of sequences for element A and a different number of sequences for element B. There may be cases in which ALD formation of an ABO_x composition uses one precursor that contains the elements A and B, such that pulsing the AB containing precursor followed by its reactant precursor onto a substrate may include a reaction that forms ABO_x on the substrate to provide an AB/oxygen sequence. A cycle of an AB/oxygen sequence may include pulsing a precursor containing A and B, pulsing a purging gas for the precursor, pulsing an oxygen reactant precursor to the A/B precursor, and pulsing a purging gas for the reactant precursor. A cycle may be repeated a number of times to provide a desired thickness of the composition. In an embodiment, a cycle for an ALD formation of a composition of barium strontium titanium oxide may include a number of barium, strontium, and titanium sequences, which may be

viewed as a cycle having multiple sequences. In an embodiment, a cycle for an ALD formation of a composition of erbium-doped barium strontium titanium oxide may include interspersing erbium sequences among a number of barium, strontium, and titanium sequences. In an embodiment, a layer substantially of a barium strontium titanium oxide is formed on a substrate mounted in a reaction chamber using ALD in repetitive barium/strontium/titanium sequences using precursor gases individually pulsed into the reaction chamber. In an embodiment, a layer substantially of a barium strontium titanium oxide doped with erbium is formed on a substrate mounted in a reaction chamber using ALD in repetitive barium/strontium/titanium sequences with a limited number of erbium sequences using precursor gases individually pulsed into the reaction chamber. Solid or liquid precursors can be used in an appropriately designed reaction chamber.

In an embodiment, a barium strontium titanium oxide layer may be structured as one or more monolayers. A film of barium strontium titanium oxide, structured as one or more monolayers, may have a thickness that ranges from a monolayer to thousands of angstroms or more. In an embodiment, an erbium-doped barium strontium titanium oxide layer may be structured as one or more monolayers. A film of erbium-doped barium strontium titanium oxide, structured as one or more monolayers, may have a thickness that ranges from a monolayer to thousands of angstroms or more. Both the film of barium strontium titanium oxide and the film of erbium-doped barium strontium titanium oxide may be processed using atomic layer deposition. Embodiments of an atomic layer deposited barium strontium titanium oxide layer, an atomic layer deposited erbium-doped barium strontium titanium oxide, or combinations thereof have a larger dielectric constant than silicon dioxide. Such dielectric layers provide a significantly thinner equivalent oxide thickness compared with a silicon oxide layer having the same physical thickness. The equivalent oxide thickness, t_{eq}, quantifies the electrical properties, such as capacitance, of the gate dielectric in terms of a representative physical thickness. t_{eq} is defined as the thickness of a theoretical SiO_2 layer that would be required to have the same capacitance density as a given dielectric, ignoring leakage current and reliability

considerations. Alternatively, such dielectric layers provide a significantly thicker physical thickness than a silicon oxide layer having the same equivalent oxide thickness. This increased physical thickness aids in reducing leakage current.

The term barium strontium titanium oxide is used herein with respect to a composition that essentially consists of barium, strontium, titanium, and oxygen. The term erbium-doped barium strontium titanium oxide is used herein with respect to a composition that essentially consists of erbium, barium, strontium, titanium, and oxygen in which the form of the composition has a limited amount of erbium relative to barium, strontium, and titanium. Barium strontium titanium oxide may be constructed as a film or other form that may be stoichiometric, non-stoichiometric, or a combination thereof. Erbium-doped barium strontium titanium oxide may be constructed as a film or other form that may be near stoichiometric, non-stoichiometric, or a combination thereof. Herein, a barium strontium titanium oxide composition may be expressed as BaSrTiO, $BaSrTiO_x$, BST, or other equivalent form. Herein, an erbium-doped barium strontium titanium oxide composition may be expressed as Er-doped BaSrTiO, Er-doped $BaSrTiO_x$, Er-doped BST, BST:Er, or other equivalent form. The term barium oxide is used herein with respect to a composition that essentially consists of barium and oxygen. The term strontium oxide is used herein with respect to a composition that essentially consists of strontium and oxygen. The term titanium oxide is used herein with respect to a composition that essentially consists of titanium and oxygen. The term erbium oxide is used herein with respect to a composition that essentially consists of erbium and oxygen. The expression BaO_u layer may be used to include a barium oxide layer that is substantially stoichiometric, non-stoichiometric, or a combination thereof. Expressions SrO_v, TiO_r, and ErO_w may be used in the same manner as BaO_u. In various embodiments, a barium strontium titanium oxide film may be doped with elements or compounds other than barium, strontium, titanium, and oxygen. In various embodiments, an erbium-doped barium strontium titanium oxide film may be doped with elements or compounds other than erbium, barium, strontium, titanium, and oxygen.

Prior to forming a $BaSrTiO_x$ film or an Er-doped $BaSrTiO_x$ film using ALD, the surface on which the $BaSrTiO_x$ film or Er-doped $BaSrTiO_x$ film is to be deposited may undergo a preparation stage. The surface may be the surface of a substrate for an electronic device, such as an integrated circuit, or an optoelectronic device. In an embodiment, the substrate used for forming a transistor may include a silicon or silicon containing material. In other embodiments, germanium, gallium arsenide, indium phosphide, silicon-on-sapphire substrates, or other suitable substrates may be used. A preparation process may include cleaning the substrate and forming layers and regions of the substrate, such as drains and sources, prior to forming a gate dielectric in the formation of a metal oxide semiconductor (MOS) transistor. Alternatively, active regions may be formed after forming the dielectric layer, depending on the over-all fabrication process implemented. In an embodiment, the substrate is cleaned to provide an initial substrate depleted of its native oxide. In an embodiment, the initial substrate is cleaned also to provide a hydrogen-terminated surface. In an embodiment, a silicon substrate undergoes a final hydrofluoric (HF) rinse prior to ALD processing to provide the silicon substrate with a hydrogen-terminated surface without a native silicon oxide layer.

Cleaning immediately preceding atomic layer deposition aids in reducing an occurrence of a native oxide as an interface between a substrate and a BaSrTiO dielectric or an Er-doped BaSrTiO dielectric formed using the atomic layer deposition process. The material composition of an interface layer and its properties are typically dependent on process conditions and the condition of the substrate before forming the dielectric layer. Though the existence of an interface layer may effectively reduce the dielectric constant associated with the dielectric layer and its substrate, an interface layer, such as a native oxide interface layer, a SiO_2 interface layer, or other composition interface layer, may improve the interface density, fixed charge density, and channel mobility of a device having this interface layer.

The sequencing of the formation of the regions of an electronic device, such as a transistor, being processed may follow typical sequencing that is generally performed in the fabrication of such devices as is well known to those

skilled in the art. Included in the processing prior to forming a dielectric may be the masking of substrate regions to be protected during the dielectric formation, as is typically performed in semiconductor fabrication. In an embodiment, the unmasked region includes a body region of a transistor; however, one skilled in the art will recognize that other semiconductor device structures may utilize this process.

In various embodiments, between each pulsing of precursors used in an atomic layer deposition process, a purging gas may be pulsed into the ALD reaction chamber. Between each pulsing of precursors, the ALD reactor chamber may be evacuated using vacuum techniques as is known by those skilled in the art. Between each pulsing of precursors, a purging gas may be pulsed into the ALD reaction chamber and the ALD reactor chamber may be evacuated.

In an embodiment, layers of barium titanium oxide, $BaTiO_y$, are formed by atomic layer deposition among layers of strontium titanium oxide, $SrTiO_z$, that are formed by atomic layer deposition. The $BaTiO_y$ layers and the $SrTiO_z$ layers may be annealed to form a layer of $BaSrTiO_x$. The order of forming the $BaTiO_y$ layers and the $SrTiO_z$ layers may be selected dependent upon a desired application. In an embodiment, layers of ErO_w formed by atomic layer deposition may be interspersed among layers of $BaTiO_y$ that are formed by atomic layer deposition and layers of $SrTiO_z$ that are formed by atomic layer deposition. The ErO_w layers, the $BaTiO_y$ layers, and the $SrTiO_z$ oxide layers may be annealed to form a layer of Er-doped $BaSrTiO_x$. The order of forming ErO_w layers, the $BaTiO_y$ layers, and the $SrTiO_z$ layers may be selected dependent upon a desired application.

In an embodiment, to form barium titanium oxide by atomic layer deposition, a barium-containing precursor is pulsed onto a substrate in an ALD reaction chamber. A number of precursors containing barium may be used to provide the barium to a substrate. In an embodiment, a precursor containing barium may include barium bis(pentamethlcyclopentadienyl, $[Ba(C_5Me_5)_2$ where $Me = CH_3]$. Water vapor may be used as an oxygen reactant precursor in an ALD sequence with $Ba(C_5Me_5)_2$. In an embodiment, the substrate temperature

may be maintained at a temperature of about 275 °C. A titanium-containing precursor is used in a titanium sequence and may be pulsed to the substrate after the barium sequence. A number of precursors containing titanium may be used to provide the titanium to the substrate. In an embodiment, a titanium precursor pulsed may be titanium tetraisopropoxide, also written as $Ti(O^{i}\text{-}Pr)_4$, where Pr = $CH_2CH_2CH_3$. In an embodiment, the substrate temperature may be maintained at a temperature ranging from less than 250 °C to about 325 °C. Other titanium precursors that may be used in an ALD process include titanium halides, such as $TiCl_4$ or TiI_4, and $Ti(NO_3)_4$. In an embodiment, during formation of a $BaTiO_y$ film, the substrate may be maintained at a temperature of about 275 °C. In an embodiment, during formation of a $BaTiO_y$ film, the substrate may be maintained at a temperature ranging from about 250 °C to about 500 °C. Use of the individual precursors is not limited to the temperature ranges of the above embodiments. Further, forming barium titanium oxide by atomic layer deposition is not limited to the abovementioned precursors. In various embodiments for ALD formation of $BaTiO_y$, the reactant precursor used in the different sequences may be an oxygen reactant precursor including, but not limited to, one or more of water vapor, atomic oxygen, molecular oxygen, ozone, hydrogen peroxide, a water – hydrogen peroxide mixture, alcohol, or nitrous oxide. In addition, the pulsing of the individual precursors in a sequence may use a pulsing period that provides uniform coverage of a monolayer on the surface or may use a pulsing period that provides partial coverage of a monolayer on the surface during a given sequence.

Embodiments for forming a $BaTiO_y$ film by atomic layer deposition may include numerous permutations of barium sequences and titanium sequences for forming the $BaTiO_y$ film. In an embodiment, a titanium sequence is conducted before a barium sequence. In an embodiment, a barium sequence is conducted before a titanium sequence. In an embodiment, a barium/titanium cycle may include a number, n, of barium sequences, and a number, p, of titanium sequences. The number of sequences n and p may be selected to engineer the relative amounts of titanium to barium. The permittivity of the formed $BaTiO_y$ film may be engineered based on the ratio of barium sequences to titanium

sequences. In an embodiment, associated pulsing periods and times for the ALD sequences may be selected along with the number of sequences n and p to form an engineered barium titanium oxide film.

The thickness of a barium titanium oxide layer formed by atomic layer deposition may be determined by a fixed growth rate for the pulsing periods and precursors used, set at a value such as N nm/cycle, dependent upon the number of cycles of the barium/titanium sequences. Once an ALD cycle is determined, a growth rate per cycle may be determined. As can be understood by those skilled in the art, particular growth rates can be determined during normal initial testing of the ALD system for processing a barium titanium oxide dielectric film for a given application without undue experimentation. For a desired barium titanium oxide layer thickness, t, in an application, the ALD process is repeated for t/N total cycles. Once the t/N cycles have completed, no further ALD processing for the barium titanium oxide layer may be required. After repeating a number of ALD cycles, a determination may be made as to whether the number of barium/titanium cycles equals a predetermined number to form the desired barium titanium oxide layer. If the total number of cycles to form the desired thickness has not been completed, a number of cycles of the barium and titanium sequences may be repeated.

In an embodiment, to form strontium titanium oxide by atomic layer deposition, a strontium-containing precursor is pulsed onto a substrate in an ALD reaction chamber. A number of precursors containing strontium may be used to provide the strontium to a substrate. In an embodiment, a precursor containing strontium may include strontium bis(triisopropyicyclopentadienyl [$Sr(C_5$-i-$Pr_3H_2)$ where Pr = $CH_2CH_2CH_3$]. Water vapor may be used as an oxygen reactant precursor in an ALD sequence with $Sr(C_5$-i-$Pr_3H_2)$. In an embodiment, the substrate temperature may be maintained at a temperature of about 275 °C. A titanium-containing precursor is used in a titanium sequence and may be pulsed to the substrate after the barium sequence. A number of precursors containing titanium may be used to provide the titanium to the substrate. In an embodiment, a titanium precursor pulsed may be titanium tetraisopropoxide, also written as $Ti(O^i$-$Pr)_4$. In an embodiment, during

formation of a $SrTiO_z$ film, the substrate may be maintained at a temperature of about 325 °C. In an embodiment, the substrate temperature may be maintained at a temperature ranging from less than 250 °C to about 325 °C. Other titanium precursors that may be used in an ALD process include titanium halides, such as $TiCl_4$ or TiI_4, and $Ti(NO_3)_4$. In an embodiment, during formation of a $SrTiO_z$ film, the substrate may be maintained at a temperature of about 325 °C. In an embodiment, during formation of a $SrTiO_z$ film, the substrate may be maintained at a temperature ranging from about 250 °C to about 500 °C. Use of the individual precursors is not limited to the temperature ranges of the above embodiments. Further, forming strontium titanium oxide by atomic layer deposition is not limited to the abovementioned precursors. In various embodiments for ALD formation of $SrTiO_z$, the reactant precursor used in the different sequences may be an oxygen reactant precursor including, but not limited to, one or more of water vapor, atomic oxygen, molecular oxygen, ozone, hydrogen peroxide, a water – hydrogen peroxide mixture, alcohol, or nitrous oxide. In addition, the pulsing of the individual precursors in a sequence may use a pulsing period that provides uniform coverage of a monolayer on the surface or may use a pulsing period that provides partial coverage of a monolayer on the surface during a given sequence.

Embodiments for forming a $SrTiO_z$ film by atomic layer deposition may include numerous permutations of strontium sequences and titanium sequences for forming the $SrTiO_z$ film. In an embodiment, a titanium sequence is conducted before a strontium sequence. In an embodiment, a strontium sequence is conducted before a titanium sequence. In an embodiment, a strontium /titanium cycle may include a number, m, of strontium sequences, and a number, q, of titanium sequences. The number of sequences m and q may be selected to engineer the relative amounts of titanium to strontium. The permittivity of the formed $SrTiO_y$ film may be engineered based on the ratio of strontium sequences to titanium sequences. In an embodiment, associated pulsing periods and times for the ALD sequences may be selected along with the number of sequences m and q to form an engineered strontium titanium oxide film.

The thickness of a strontium titanium oxide layer formed by atomic layer deposition may be determined by a fixed growth rate for the pulsing periods and precursors used, set at a value such as M nm/cycle, dependent upon the number of cycles of the strontium/titanium sequences. Once an ALD cycle is determined, a growth rate per cycle may be determined. As can be understood by those skilled in the art, particular growth rates can be determined during normal initial testing of the ALD system for processing a strontium titanium oxide dielectric film for a given application without undue experimentation. For a desired strontium titanium oxide layer thickness, d, in an application, the ALD process is repeated for d/M total cycles. Once the d/M cycles have completed, no further ALD processing for the strontium titanium oxide layer may be required. After repeating a number of ALD cycles, a determination may be made as to whether the number of strontium/titanium cycles equals a predetermined number to form the desired strontium titanium oxide layer. If the total number of cycles to form the desired thickness has not been completed, a number of cycles of the strontium and titanium sequences may be repeated.

Layers of atomic layer deposited $SrTiO_z$ and layers of atomic layer deposited $BaTiO_y$ may be annealed to form a layer of $BaSrTiO_x$. In an embodiment, alternating layers of ALD $BaTiO_y$ and ALD $SrTiO_z$ may be annealed to form a layer of $BaSrTiO_x$. A layer of $BaSrTiO_x$ may be engineered to have a selected amount of barium, strontium, and titanium using a number of different criteria. Such criteria may include selecting the number $SrTiO_z$ layers relative to the number of $BaTiO_y$ layers and selecting the thickness of the $SrTiO_z$ layers relative to the thickness of $BaTiO_y$ layers. Various permutations of the thickness of the $SrTiO_z$ layers and various permutations of the thickness of the $BaTiO_y$ layers may be used to form the layer of $BaSrTiO_x$. Within each layer of $SrTiO_z$ the ratio of Sr to Ti may be regulated. Within each layer of $BaTiO_y$ the ratio of Ba to Ti may be regulated. Using these various criteria a layer of $BaSrTiO_x$ may be engineered with a desired dielectric constant. In an embodiment, a layer of $BaSrTiO_x$ may have a permittivity in range from 165 to 180. In various embodiments, a layer of $BaSrTiO_x$ formed using atomic layer deposition may be doped with appropriate elements. Doping may be realized by

a number of different processes including ion implantation. In an embodiment, a layer of $BaSrTiO_x$ is doped with erbium.

Alternatively, in an embodiment, a BaSrTiO film may be grown to a desired thickness by repetition of a process including atomic layer deposition of layers of BaO_u, SrO_v, TiO_r followed by annealing. In an embodiment, a base thickness may be formed according to various embodiments such that forming a predetermined thickness of a BaSrTiO film may be conducted by forming a number of layers having the base thickness. As can be understood by one skilled in the art, determining the base thickness depends on the application and can be determined during initial processing without undue experimentation. Relative amounts of barium, strontium, and titanium in a BaSrTiO film may be controlled by regulating the relative thicknesses of the individual layers of BaO_x, SrO_y, TiO_z formed. In addition, relative amounts of barium, strontium, and titanium in a BaSrTiO film may be controlled by forming a layer of BaSrTiO as multiple layers of different base thickness and by regulating the relative thicknesses of the individual layers of BaO_u, SrO_v, TiO_r formed in each base layer. In various embodiments, a layer of BaSrTiO formed using atomic layer deposition may be doped with appropriate elements. Doping may be realized by a number of different processes including ion implantation. In an embodiment, a BaSrTiO layer is doped with erbium.

In an alternative embodiment, an ALD cycle for forming BaSrTiO may include sequencing metal-containing precursors in the order of barium, strontium, and titanium in which partial coverage of a monolayer on a substrate surface is attained for pulsing of a metal-containing precursor. Embodiments for forming barium strontium titanium oxide film by atomic layer deposition may include numerous permutations of barium sequences, strontium sequences, and titanium sequences for forming a barium strontium titanium oxide film. In an embodiment, a barium / strontium / titanium cycle may include a number, nx, of barium sequences, a number, ny, of strontium sequences, and a number, nz, of titanium sequences, in which reactant precursors associated with each metal are applied with the associated sequence. The number of sequences nx, ny, and nz may be selected to engineer the relative amounts of barium, strontium, and

titanium. In an embodiment, the number of sequences nx, ny, and nz are selected to form a barium-rich barium strontium titanium oxide. Alternatively, the number of sequences nx, ny, and nz are selected to form a strontium-rich barium strontium titanium oxide. Additionally, the number of sequences nx, ny, and nz are selected to form a titanium-rich barium strontium titanium oxide.

After repeating a selected number of ALD cycles, a determination may be made as to whether the number of barium / strontium / titanium cycles equals a predetermined number to form the desired barium strontium titanium oxide layer. If the total number of cycles to form the desired thickness has not been completed, a number of cycles for the barium, strontium, and titanium sequences is repeated. The thickness of a barium strontium titanium oxide layer formed by atomic layer deposition may be determined by a fixed growth rate for the pulsing periods and precursors used, dependent upon the number of cycles of the barium/strontium/titanium sequences. Depending on the precursors used for ALD formation of a BaSrTiO film, the process may be conducted in an ALD window, which is a range of temperatures in which the growth rate is substantially constant. If such an ALD window is not available, the ALD process may be conducted at the same set of temperatures for each ALD sequence in the process. A barium strontium titanium oxide layer processed at relatively low temperatures associated with atomic layer deposition may provide an amorphous layer.

In an embodiment, a layer of $BaSrTiO_x$ doped with erbium may be constructed by forming layers of erbium oxide by atomic layer deposition interspersed among layers of barium titanium oxide that are formed by atomic layer deposition and layers of strontium titanium oxide that are formed by atomic layer deposition. In an embodiment, to form erbium oxide by atomic layer deposition, an erbium-containing precursor is pulsed onto a substrate in an ALD reaction chamber. A number of precursors containing erbium may be used to provide the erbium to a substrate. In an embodiment, a precursor containing erbium may include $Er(thd)_3$. Ozone may be used as an oxygen reactant precursor in an ALD sequence with $Er(thd)_3$. In an embodiment, during formation of an ErO_w film, the substrate may be maintained at a temperature

ranging from about 250 °C to about 450 °C. Below 325 °C an erbium oxide film may be amorphous. Polycrystalline erbium oxide films may be grown at higher temperatures with orientation changing from (4 0 0) to (2 2 2) at deposition temperatures above 325 °C. Use of the individual precursors is not limited to the temperature ranges of the above embodiments. In various embodiments for ALD formation of ErO_w using different erbium-containing precursors, the reactant precursor used in the different sequences may be an oxygen reactant precursor including, but not limited to, one or more of water vapor, atomic oxygen, molecular oxygen, ozone, hydrogen peroxide, a water – hydrogen peroxide mixture, alcohol, or nitrous oxide. In various embodiments, forming erbium oxide by atomic layer deposition is not limited to the abovementioned precursor and use of individual erbium-containing precursors is not limited to the temperature ranges of the above example embodiment. In addition, the pulsing of the individual precursors in a sequence may use a pulsing period that provides uniform coverage of a monolayer on the surface or may use a pulsing period that provides partial coverage of a monolayer on the surface during an erbium sequence.

In an embodiment, a number of ErO_w layers, a number of $BaTiO_y$ layers, and a number of $SrTiO_z$ layers may be formed by atomic layer deposition, where the number of ErO_w layers is selected to be significantly less than the number of $BaTiO_y$ layers and the number of $SrTiO_z$ layers. The ErO_w layers, $BaTiO_y$ layers, and $SrTiO_z$ layers may be annealed to form Er-doped $BaSrTiO_x$. In an embodiment, a laminate structure of alternating layers of ALD $SrTiO_3$ and ALD $BaTiO_3$, interspersed with ALD Er_2O_3 layers are annealed to produce an Er-doped $Ba_{0.7}Sr_{0.3}TiO_3$ film. In an embodiment, the number of ErO_w layers is selected such that the percentage of ErO_w in the total number of ErO_w layers, $BaTiO_y$ layers, and $SrTiO_z$ layers is less than or equal to 10%. In an embodiment, the number of ErO_w layers is selected such that the atomic concentration of erbium in the formed Er-doped $BaSrTiO_x$ is less than or equal to 10%. In an embodiment, the number of ErO_w layers may be interspersed among the number of ErO_w layers in a predetermined arrangement prior to annealing. In an embodiment, the number of ErO_w layers may be interspersed

among the number of $BaTiO_y$ layers and $SrTiO_z$ layers in a random order prior to annealing. In various embodiments, the order of forming $BaTiO_y$, $SrTiO_z$, and ErO_w layers may be permutated. The annealing may be conducted in a nitrogen ambient. In an embodiment, annealing may be conducted in a nitrogen ambient having a small amount of oxygen. However, annealing is not limited to these ambient conditions. The annealing may be performed at about 600 °C or higher. The annealing may be conducted for about 60 minutes or less. In an embodiment, annealing is conducted for less than one minute. The annealing may be performed at other temperatures and with other annealing times. The annealing temperatures and annealing time periods may be selected based on the desired structure for the Er-doped $BaSrTiO_x$ layer.

In an embodiment, layers of $BaTiO_y$, layers of $SrTiO_z$, and layers of ErO_w are each grown by atomic layer deposition to a thickness such that annealing these layers at appropriate temperatures essentially converts these layers to a layer of Er-doped $BaSrTiO_x$. In an embodiment, an Er-doped $BaSrTiO_x$ film may be grown to a desired thickness by repetition of a process including atomic layer deposition of $BaTiO_y$, layers of $SrTiO_z$, and layers of ErO_w followed by annealing. In an embodiment, a base thickness may be formed according to various embodiments such that forming a predetermined thickness of an Er-doped $BaSrTiO_x$ film may be conducted by forming a number of layers having the base thickness. As can be understood by one skilled in the art, determining the base thickness depends on the application and can be determined during initial processing without undue experimentation. Relative amounts of erbium, barium, strontium, titanium, and oxygen in an Er-doped $BaSrTiO_x$ film may be controlled by regulating the relative thicknesses of the individual layers of oxides formed. In addition, relative amounts of erbium, barium, strontium, titanium, and oxygen in a Er-doped $BaSrTiO_x$ film may be controlled by forming a layer of Er-doped $BaSrTiO_x$ as multiple layers of different base thickness and by regulating the relative thicknesses of the individual layers of oxides formed in each base layer prior to annealing. As can be understood by those skilled in the art, particular effective growth rates for the engineered Er-doped $BaSrTiO_x$ film can be determined during normal initial

testing of the ALD system used for a given application without undue experimentation.

In an alternative embodiment, an ALD cycle for forming Er-doped BaSrTiO may include repetitive sequencing of metal-containing precursors of barium, strontium, and titanium, in which an erbium sequence is substituted for one or more of the main sequences or one or more erbium sequences is added to the main sequences of a ALD cycle in which partial coverage of a monolayer on a substrate surface is attained for pulsing of a metal-containing precursor. Embodiments for forming erbium-doped barium strontium titanium oxide film by atomic layer deposition may include numerous permutations of erbium sequences interspersed among the main barium sequences, strontium sequences, and titanium sequences in an ALD cycle. In an embodiment, a barium / strontium / titanium /erbium cycle may include a number, mx, of barium sequences, a number, my, of strontium sequences, a number, mz, of titanium sequences, and a number, mr, of erbium sequences, in which reactant precursors associated with each metal are applied with the associated sequence. The number of sequences mx, my, mz, and mr may be selected to engineer the relative amounts of barium, strontium, titanium, and erbium. In an embodiment, the number of sequences mx, my, mz and mr are selected to form a barium-rich erbium-doped barium strontium titanium oxide. Alternatively, the number of sequences mx, my, mz and mr are selected to form a strontium-rich erbium-doped barium strontium titanium oxide. Additionally, the number of sequences mx, my, mz and mr are selected to form a titanium-rich erbium-doped barium strontium titanium oxide. The number of sequences mx, my, mz and mr may be chosen to limit the amount of erbium doped in a $BaSrTiO_x$ film.

After repeating a selected number of ALD cycles, a determination may be made as to whether the number of barium / strontium / titanium / erbium cycles equals a predetermined number to form the desired erbium-doped barium strontium titanium oxide layer. If the total number of cycles to form the desired thickness has not been completed, a number of cycles for the barium, strontium, titanium, and erbium sequences is repeated. The thickness of an erbium-doped barium strontium titanium oxide layer formed by atomic layer deposition may be

determined by a fixed growth rate for the pulsing periods and precursors used, set at a value such as P nm/cycle, dependent upon the number of cycles of the barium / strontium / titanium / erbium sequences. Depending on the precursors used for ALD formation of a BaSrTiO film, the process may be conducted in an ALD window. If such an ALD window is not available, the ALD process may be conducted at the same set of temperatures for each ALD sequence in the process. For a desired erbium-doped barium strontium titanium oxide layer thickness, l, in an application, the ALD process is repeated for l/P total cycles. Once the l/P cycles have completed, no further ALD processing for the erbium-doped barium strontium titanium oxide layer is required. An erbium-doped barium strontium titanium oxide layer processed at relatively low temperatures associated with atomic layer deposition may provide an amorphous layer.

In various embodiments, nitrogen may be used as a purging gas and a carrier gas for one or more of the sequences for forming BaO_u, SrO_v, TiO_r, $BaTiO_y$, $SrTiO_z$, ErO_w, and $BaSrTiO_x$. Alternatively, hydrogen, argon gas, or other inert gases may be used as the purging gas. Excess precursor gas and reaction by-products may be removed by the purge gas. Excess precursor gas and reaction by-products may be removed by evacuation of the reaction chamber using various vacuum techniques. Excess precursor gas and reaction by-products may be removed by the purge gas and by evacuation of the reaction chamber.

Atomic layer deposition of the individual components or layers allows for individual control of each precursor pulsed into the reaction chamber. Thus, each precursor is pulsed into the reaction chamber for a predetermined period, where the predetermined period can be set separately for each precursor. Additionally, for various ALD formations, each precursor may be pulsed into the reaction chamber under separate environmental conditions. The substrate may be maintained at a selected temperature and the reaction chamber maintained at a selected pressure independently for pulsing each precursor. Appropriate temperatures and pressures may be maintained, whether the precursor is a single precursor or a mixture of precursors.

Either before or after forming a BaSrTiO film in accordance with any embodiment, other dielectric layers such as nitride layers, dielectric metal silicates, insulating metal oxides, or combinations thereof may be formed as part of a dielectric layer or dielectric stack. These one or more other layers of dielectric material may be provided in stoichiometric form, in non-stoichiometric form, or a combination thereof. Depending on the application, a dielectric stack containing a $BaSrTiO_x$ film may include a silicon oxide layer. In an embodiment, the dielectric layer may be formed as a nanolaminate. Alternatively, a dielectric layer may be formed substantially as a barium strontium titanium oxide film or as an erbium-doped barium strontium titanium oxide film.

In various embodiments, the structure of an interface between a dielectric layer and a substrate on which it is disposed is controlled to limit the inclusion of a native oxide. A native oxide, such as a silicon oxide layer on silicon, would reduce the effective dielectric constant of the dielectric layer. The material composition and properties for an interface layer may be dependent on process conditions and the condition of the substrate before forming the dielectric layer. Though the existence of an interface layer may effectively reduce the dielectric constant associated with the dielectric layer and its substrate, the interface layer, such as a silicon oxide interface layer or other material interface layer, may improve the interface density, fixed charge density, and channel mobility of a device having this interface layer.

Figure 1 shows an embodiment of a transistor 100 having a dielectric layer 140 containing a $BaSrTiO_x$ film. The $BaSrTiO_x$ film may be doped with erbium. Transistor 100 may include a source region 120 and a drain region 130 in a silicon-based substrate 110, where source and drain regions 120, 130 are separated by a body region 132. Body region 132 defines a channel having a channel length 134. A gate dielectric 140 may be disposed on substrate 110 with gate dielectric 140 formed as a dielectric layer containing $BaSrTiO_x$. Gate dielectric 140 may be realized as a dielectric layer formed substantially of $BaSrTiO_x$. Gate dielectric 140 may be constructed as multiple dielectric layers, that is, as a dielectric stack, containing at least one $BaSrTiO_x$ film and one or

more layers of insulating material other than a barium strontium titanium oxide film. The $BaSrTiO_x$ film may be structured as one or more monolayers. An embodiment of a $BaSrTiO_x$ film or an Er-doped $BaSrTiO_x$ film may be formed using atomic layer deposition. A gate 150 may be formed over and contact gate dielectric 140.

An interfacial layer 133 may form between body region 132 and gate dielectric 140. In an embodiment, interfacial layer 133 may be limited to a relatively small thickness compared to gate dielectric 140, or to a thickness significantly less than gate dielectric 140 as to be effectively eliminated. Forming the substrate and the source and drain regions may be performed using standard processes known to those skilled in the art. Additionally, the sequencing of the various elements of the process for forming a transistor may be conducted with fabrication processes known to those skilled in the art. In an embodiment, gate dielectric 140 may be realized as a gate insulator in a silicon complimentary metal oxide semiconductor (CMOS) transistor. Use of a gate dielectric containing a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof is not limited to silicon based substrates, but may be used with a variety of semiconductor substrates.

Figure 2 shows an embodiment of a floating gate transistor 200 having a dielectric layer containing $BaSrTiO_x$ film. The $BaSrTiO_x$ film may be doped with erbium. The $BaSrTiO_x$ film may be structured as one or more monolayers. The $BaSrTiO_x$ film or Er-doped $BaSrTiO_x$ film may be formed using atomic layer deposition techniques. Transistor 200 may include a silicon-based substrate 210 with a source 220 and a drain 230 separated by a body region 232. Body region 232 between source 220 and drain 230 defines a channel region having a channel length 234. Located above body region 232 is a stack 255 including a gate dielectric 240, a floating gate 252, a floating gate dielectric 242, and a control gate 250. An interfacial layer 233 may form between body region 232 and gate dielectric 240. In an embodiment, interfacial layer 233 may be limited to a relatively small thickness compared to gate dielectric 240, or to a

thickness significantly less than gate dielectric 240 as to be effectively eliminated.

In an embodiment, gate dielectric 240 includes a dielectric containing an atomic layer deposited $BaSrTiO_x$ film. Gate dielectric 240 may be realized as a dielectric layer formed substantially of $BaSrTiO_x$. Gate dielectric 240 may be a dielectric stack containing at least one $BaSrTiO_x$ film or Er-doped $BaSrTiO_x$ film and one or more layers of other insulating materials. In an embodiment, floating gate 252 may be formed over and contact gate dielectric 240.

In an embodiment, floating gate dielectric 242 includes a dielectric containing a $BaSrTiO_x$ film. The $BaSrTiO_x$ film may be doped with erbium. The $BaSrTiO_x$ film may be structured as one or more monolayers. In an embodiment, the $BaSrTiO_x$ film or the Er-doped $BaSrTiO_x$ film may be formed using atomic layer deposition techniques. Floating gate dielectric 242 may be realized as a dielectric layer formed substantially of $BaSrTiO_x$. Floating gate dielectric 242 may be a dielectric stack containing at least one $BaSrTiO_x$ film and one or more layers of other insulating materials. In an embodiment, control gate 250 may be formed over and contact floating gate dielectric 242.

Alternatively, both gate dielectric 240 and floating gate dielectric 242 may be formed as dielectric layers containing a $BaSrTiO_x$ film structured as one or more monolayers. The $BaSrTiO_x$ film may be doped with erbium. Gate dielectric 240 and floating gate dielectric 242 may be realized by embodiments similar to those described herein, with the remaining elements of the transistor 200 formed using processes known to those skilled in the art. In an embodiment, gate dielectric 240 forms a tunnel gate insulator and floating gate dielectric 242 forms an inter-gate insulator in flash memory devices, where gate dielectric 240 and floating gate dielectric 242 may include a erbium-doped barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or combination thereof structured as one or more monolayers. Such structures are not limited to silicon based substrates, but may be used with a variety of semiconductor substrates.

Embodiments of a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or combinations thereof structured

as one or more monolayers may also be applied to capacitors in various integrated circuits, memory devices, and electronic systems. In an embodiment for a capacitor 300 illustrated in Figure 3, a method includes forming a first conductive layer 310, forming a dielectric layer 320 containing a barium strontium titanium oxide film structured as one or more monolayers on first conductive layer 310, and forming a second conductive layer 330 on dielectric layer 320. The $BaSrTiO_x$ film may be doped with erbium. Dielectric layer 320 may be a dielectric stack containing at least one $BaSrTiO_x$ film or Er-doped $BaSrTiO_x$ film and one or more layers of other insulating materials. An interfacial layer 315 may form between first conductive layer 310 and dielectric layer 320. In an embodiment, interfacial layer 315 may be limited to a relatively small thickness compared to dielectric layer 320, or to a thickness significantly less than dielectric layer 320 as to be effectively eliminated.

Embodiments for a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof structured as one or more monolayers may include, but are not limited to, a capacitor in a DRAM and capacitors in analog, radio frequency (RF), and mixed signal integrated circuits. Mixed signal integrated circuits are integrated circuits that may operate with digital and analog signals.

Figure 4 depicts an embodiment of a dielectric structure 400 having multiple dielectric layers 405-1, 405-2, ... 405-N, in which at least one layer is a barium strontium titanium oxide layer. The $BaSrTiO_x$ film may be doped with erbium. Layers 410 and 420 may provide means to contact dielectric layers 405-1, 405-2, ... 405-N. Layers 410 and 420 may be electrodes forming a capacitor. Layer 410 may be a body region of a transistor with layer 420 being a gate. Layer 410 may be a floating gate electrode with layer 420 being a control gate.

In an embodiment, dielectric structure 400 includes one or more layers 405-1, 405-2 ... 405-N as dielectric layers other than a BaSrTiO layer, where at least one layer is a BaSrTiO layer. The $BaSrTiO_x$ film may be doped with erbium. Dielectric layers 405-1, 405-2 ... 405-N may include an insulating metal oxide layer. Dielectric layers 405-1, 405-2, ... 405-N may include an insulating nitride layer. Dielectric layers 405-1, 405-2, ... 405-N may include

an insulating oxynitride layer. Dielectric layers 405-1, 405-2, ... 405-N may include a silicon nitride layer. Dielectric layers 405-1, 405-2, ... 405-N may include an insulating silicate layer. Dielectric layers 405-1, 405-2, ... 405-N may include a silicon oxide layer.

Various embodiments for a dielectric layer containing a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof structured as one or more monolayers may provide for enhanced device performance by providing devices with reduced leakage current. Such improvements in leakage current characteristics may be attained by forming one or more layers of a barium strontium titanium oxide in a nanolaminate structure with other metal oxides, non-metal-containing dielectrics, or combinations thereof. One or more layers of $BaSrTiO_x$ may be doped with erbium. The transition from one layer of the nanolaminate to another layer of the nanolaminate provides disruption to a tendency for an ordered structure in the nanolaminate stack. The term "nanolaminate" means a composite film of ultra thin layers of two or more materials in a layered stack. Typically, each layer in a nanolaminate has a thickness of an order of magnitude in the nanometer range. Further, each individual material layer of the nanolaminate may have a thickness as low as a monolayer of the material or as high as 20 nanometers.

In an embodiment, dielectric structure 400 may be structured as a nanolaminate structure 400 including a $BaSrTiO_x$ film structured as one or more monolayers. The $BaSrTiO_x$ film may be doped with erbium. Nanolaminate structure 400 includes a plurality of layers 405-1, 405-2 to 405-N, where at least one layer contains a $BaSrTiO_x$ film structured as one or more monolayers. The other layers may be insulating nitrides, insulating oxynitrides, and other dielectric materials such as insulating metal oxides. The sequencing of the layers depends on the application. The effective dielectric constant associated with nanolaminate structure 400 is that attributable to N capacitors in series, where each capacitor has a thickness defined by the thickness and composition of the corresponding layer. By selecting each thickness and the composition of each layer, a nanolaminate structure can be engineered to have a predetermined

dielectric constant. Embodiments for structures such as nanolaminate structure 400 may be used as nanolaminate dielectrics in non-volatile read only memory (NROM) flash memory devices as well as other integrated circuits. In an embodiment, a layer of the nanolaminate structure 400 is used to store charge in a NROM device. The charge storage layer of a nanolaminate structure 400 in a NROM device may be a silicon oxide layer.

Rare-earth doped materials have various applications in optoelectronic devices and displays based on the luminescent properties of these materials. Application of erbium-doped oxides may be directed to use of its characteristic emission at 1.54 μm. The 1.54 μm wavelength also corresponds to a minimum loss in silica based fiber. Additionally, devices may take advantage of Er^{+3} transitions in the blue, green, and red spectral regions. The energy of transitions for erbium doped materials is relatively independent of its host matrix and ambient temperature, though the host matrix affects the relative intensity of photoluminescence, chemical stability, and sensitivity to the operational environment. With respect to typical sulfide luminescent phosphors, oxide film phosphors provide atmospheric stability, anticorrosive properties, and reduced degradation under applied voltages. In various embodiments, ALD Er-doped $BaSrTiO_x$ may be used in place of luminescent phosphors in optoelectronic devices. Er^{+3} ions may be incorporated into barium strontium titanate to form an extended solution using atomic layer deposition. ALD Er-doped $Ba_{0.7}Sr_{0.3}TiO_3$ films may be used in electroluminescent devices, such as displays and flat panel displays, and in place of luminescent phosphors in optoelectronic devices.

Figure 5 illustrates a representation of an embodiment of a flat panel display 500 having an erbium-doped barium strontium titanium oxide film 520. Flat panel display 500 may include BST:Er film 520 separated by a dielectric layer 530 from a transparent conductive oxide (TCO) layer 510 and separated by a dielectric layer 540 from a conductive layer 550. Conductive layer 550 may be a metal layer. TCO layer 510 and conductive layer 550 are configured to contact an appropriate voltage source, which enables a voltage, $V_{APPLIED}$, to be applied between TCO layer 510 and conductive layer 550. Various types or configurations of voltage sources may be used to provide $V_{APPLIED}$. Other

configurations for a flat panel display or other displays having an erbium-doped barium strontium titanium oxide film may be used.

Figure 6 depicts a representation of an embodiment of an optoelectronic apparatus 600 having an electrooptic region 620 that includes an ALD BST film, an ALD BST:Er film, or a combination thereof. In an embodiment, optoelectronic apparatus 600 includes a substrate 605, a bottom cladding layer 610, a top cladding layer 630, and layer 620 of electrooptic material between bottom cladding layer 610 and a top cladding layer 630. Layer 620 of electrooptic material is an optical layer, which is used for propagation of light and/or modification of the propagation of light. Substrate 605 may be a silicon substrate, a silicon-germanium substrate, a glass substrate, a GaAs substrate, an InP substrate, or a substrate of other III-V compositions. Substrate 605 is not limited to these materials. Substrate 605 may be configured to be combined with cladding 610. Cladding material may include silicon oxide or other appropriate dielectric material. Electrodes may be provided to modulate optoelectronic apparatus 600 to utilize the optical-related properties of electrooptic material 620. The electrodes may be connected to TCO layers disposed on the top and bottom of electrooptic material 620. The electrodes may be connected in other configurations that do not interfere with the optical operation of optoelectronic apparatus 600. The materials selected for substrate 605, cladding layer 610, cladding layer 630, and electrooptic material layer 620 may be chosen based on the characteristics of the application, such as the wavelengths of interest. Optoelectronic apparatus 600 may be structured as an integrated optic device. Optoelectronic apparatus 600 may be configured in a variety of devices and systems.

Transistors, capacitors, displays, waveguide structures, and other electronic and optoelectronic devices may include dielectric films containing a layer of a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof structured as one or more monolayers. The erbium-doped barium strontium titanium oxide layer may be formed by atomic layer deposition. Dielectric films containing a barium strontium titanium oxide layer, an erbium-doped barium strontium titanium

oxide layer, or a combination thereof may be implemented into memory devices and electronic systems including information handling devices. Barium strontium titanium oxide layers may be structured to provide high permittivity and low leakage currents in electronic devices. Further, embodiments of electronic devices and optoelectronic apparatus may be realized as integrated circuits. Embodiments of information handling devices may include wireless systems, telecommunication systems, and computers.

Figure 7 illustrates a block diagram for an electronic system 700 having one or more devices having a dielectric structure including a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof structured as one or more monolayers. The thickness of such a $BaSrTiO_x$ layer may range from a monolayer to thousands of angstroms or more, and may be processed using atomic layer deposition. Electronic system 700 includes a controller 705, a bus 715, and an electronic device 725, where bus 715 provides electrical conductivity between controller 705 and electronic device 725. Electronic device 725 may be an optoelectronic device. In various embodiments, controller 705 may include an embodiment of a $BaSrTiO_x$ film. The $BaSrTiO_x$ film may be doped with erbium. In various embodiments, electronic device 725 may include an embodiment of a $BaSrTiO_x$ film. The $BaSrTiO_x$ film may be doped with erbium. In various embodiments, controller 705 and electronic device 725 may include embodiments of a $BaSrTiO_x$ film. The $BaSrTiO_x$ film may be doped with erbium. Electronic system 700 may include, but is not limited to, fiber optic systems, electro-optic systems, and information handling systems such as wireless systems, telecommunication systems, and computers.

Figure 8 depicts a diagram of an embodiment of a system 800 having one or more devices containing a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof structured as one or more monolayers. System 800 also includes a controller 805, a memory 825, an electronic apparatus 835, and a bus 815, where bus 815 provides electrical conductivity between controller 805 and electronic apparatus 835 and between controller 805 and memory 825. Bus 815 may include an

address bus, a data bus, and a control bus, each independently configured. Alternatively, bus 815 may use common conductive lines for providing one or more of address, data, or control, the use of which is regulated by controller 805. In an embodiment, apparatus 835 may be additional memory configured in a manner similar to memory 825. In an embodiment, system 800 may include an additional peripheral device or devices 845 coupled to bus 815. Peripheral devices 845 may include displays, additional storage memory, or other control devices that may operate in conjunction with controller 805. Alternatively, peripheral devices 845 may include displays, additional storage memory, or other control devices that may operate in conjunction with memory 825, or controller 805 and memory 825. In an embodiment, controller 805 is a processor. One or more of controller 805, memory 825, bus 815, apparatus 835, or peripheral devices 845 may include an embodiment of a dielectric layer having a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof structured as one or more monolayers. The thickness of such a $BaSrTiO_x$ structure may range from a monolayer to thousands of angstroms or more, and may be processed using atomic layer deposition.

Memory 825 may be realized as a memory device containing a barium strontium titanium oxide film, an erbium-doped barium strontium titanium oxide film, or a combination thereof structured as one or more monolayers. The $BaSrTiO_x$ structure may be formed in a memory cell of a memory array. The $BaSrTiO_x$ structure may be formed in a capacitor in a memory cell of a memory array. The $BaSrTiO_x$ structure may be formed in a transistor in a memory cell of a memory array. It will be understood that embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to a particular type of memory device. Memory types include a DRAM, SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as other emerging DRAM technologies. System 800 may include, but is

not limited to, fiber optic systems, electro-optic systems, and information handling systems including wireless devices, wireless systems, and computers.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. It is to be understood that the above description is intended to be illustrative, and not restrictive, and that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Combinations of the above embodiments and other embodiments will be apparent to those of skill in the art upon studying the above description.

What is claimed is:

1. A method comprising:
forming a layer of strontium titanium oxide by atomic layer deposition;
forming a layer of barium titanium oxide by atomic layer deposition; and
annealing the layers of strontium titanium oxide and barium titanium oxide to form a layer of barium strontium titanium oxide.

2. The method of claim 1, wherein the method includes doping the barium strontium titanium oxide with erbium.

3. The method of claim 1, wherein the method includes forming alternating layers of $SrTiO_z$ and $BaTiO_y$ before annealing.

4. The method of claim 1, wherein the method includes forming an amorphous barium strontium titanium oxide layer.

5. The method of claim 1, wherein the method includes forming a $Ba_{0.7}Sr_{0.3}TiO_3$ layer.

6. The method of claim 1, wherein forming the layer of barium strontium titanium oxide includes forming the layer of barium strontium titanium oxide as a capacitor dielectric in a capacitor in an integrated circuit.

7. The method of claim 1, wherein forming the layer of barium strontium titanium oxide includes forming the layer of barium strontium titanium oxide as a dielectric layer in a memory.

8. The method of claim 1, wherein forming the layer of barium strontium titanium oxide includes forming the layer of barium strontium titanium oxide as a gate insulator in a transistor.

9. The method of claim 1, wherein forming the layer of barium strontium titanium oxide includes forming the layer of barium strontium titanium oxide as a gate insulator in a silicon-based complementary metal oxide semiconductor transistor.

10. The method of claim 1, wherein forming the layer of barium strontium titanium oxide includes forming the layer of barium strontium titanium oxide as a tunnel gate insulator in a flash memory device.

11. The method of claim 1, wherein forming the layer of barium strontium titanium oxide includes forming the layer of barium strontium titanium oxide as an inter-gate insulator in a flash memory device.

12. The method of claim 1, wherein forming the layer of barium strontium titanium oxide includes forming the layer of barium strontium titanium oxide as a dielectric region in a nanolaminate of a NROM flash memory.

13. The method of claim 1, wherein the method includes doping the layer of barium strontium titanium oxide with erbium during formation of the layer of barium strontium titanium oxide to form an emissive element in electroluminescent device.

14. The method of claim 1, wherein the method includes doping the layer of barium strontium titanium oxide with erbium during formation of the layer of barium strontium titanium oxide as a film in an optoelectronic device.

15. A method comprising:

forming a layer of strontium titanium oxide by atomic layer deposition;

forming a layer of barium titanium oxide by atomic layer deposition;

forming a layer of erbium oxide by atomic layer deposition, the layer of erbium oxide between the layers of strontium titanium oxide and barium titanium oxide; and

annealing the layers of strontium titanium oxide, barium titanium oxide, and erbium oxide to form a layer of erbium-doped barium strontium titanium oxide.

16. The method of claim 15, wherein the method includes forming an amorphous Er-doped barium strontium titanium oxide layer.

17. The method of claim 15, wherein the method includes forming the erbium-doped barium strontium titanium oxide with a composition that deviates from $Ba_{0.7}Sr_{0.3}TiO_3$ due to the erbium doping.

18. The method of claim 15, wherein forming the layer of erbium-doped barium strontium titanium oxide includes the layer of erbium-doped barium strontium titanium oxide as a gate insulator in a transistor.

19. The method of claim 15, wherein forming the layer of erbium-doped barium strontium titanium oxide includes forming the layer of erbium-doped barium strontium titanium oxide in a memory.

20. The method of claim 15, wherein the method includes forming the layer of erbium-doped barium strontium titanium oxide as a film in an electroluminescent display.

21. The method of claim 15, wherein the method includes forming the layer of erbium-doped barium strontium titanium oxide as a film in a flat panel display.

22. The method of claim 15, wherein the method includes forming the layer of erbium-doped barium strontium titanium oxide as a film in an optoelectronic device.

23. A method comprising:

forming a array of memory cells; and

forming a dielectric layer in a memory cell of the array, wherein forming the dielectric layer includes forming a barium strontium titanium oxide film by:

forming a layer of strontium titanium oxide by atomic layer deposition;

forming a layer of barium titanium oxide by atomic layer deposition; and

annealing the layers of strontium titanium oxide and barium titanium oxide to form barium strontium titanium oxide.

24. The method of claim 23, wherein forming a dielectric layer includes forming the dielectric layer substantially of the barium strontium titanium oxide film.

25. The method of claim 23, wherein forming the dielectric layer includes forming the dielectric layer as a capacitor dielectric in a capacitor of a dynamic random access memory.

26. The method of claim 23, wherein forming the dielectric layer includes forming the dielectric layer as a tunnel gate insulator in a flash memory device.

27. The method of claim 23, wherein forming the dielectric layer includes forming the dielectric layer as an inter-gate insulator in a flash memory device.

28. The method of claim 23, wherein forming the dielectric layer includes forming the dielectric layer as a dielectric region to store charge in a NROM flash memory.

29. A method comprising:

forming an array of cells;

forming a dielectric layer in a cell of the array, wherein forming the dielectric layer includes forming an erbium-doped barium strontium titanium

oxide film by:

forming a layer of strontium titanium oxide by atomic layer deposition;

forming a layer of barium titanium oxide by atomic layer deposition;

forming a layer of erbium oxide by atomic layer deposition, the layer of erbium oxide between the layers of strontium titanium oxide and barium titanium oxide; and

annealing the layers of strontium titanium oxide, barium titanium oxide, and erbium oxide to form erbium-doped barium strontium titanium oxide.

30. The method of claim 29, wherein the method includes forming alternating layers of $BaTiO_x$ and $SrTiO_y$ with one or more layers of ErO_z interspersed among the layers of $BaTiO_x$ and $SrTiO_y$ in a dielectric stack before annealing to form erbium-doped barium strontium titanium oxide.

31. The method of claim 29, wherein forming the dielectric layer includes forming the dielectric layer as an emissive layer in a memory.

32. The method of claim 29, wherein forming the dielectric layer includes forming the dielectric layer in a flat panel display.

33. The method of claim 29, wherein forming the dielectric layer includes forming the dielectric layer as a dielectric layer in an electrooptic device.

34. A method comprising:

providing a controller;

coupling an integrated circuit to the controller, the integrated circuit having a dielectric layer containing a barium strontium titanium oxide film, the barium strontium titanium oxide film formed by:

forming a layer of strontium titanium oxide by atomic layer

deposition;

forming a layer of barium titanium oxide by atomic layer deposition; and

annealing the layers of strontium titanium oxide and barium titanium oxide to form barium strontium titanium oxide.

35. The method of claim 34, wherein coupling an integrated circuit to the controller includes coupling a memory device having the dielectric layer containing the barium strontium titanium oxide film.

36. The method of claim 34, wherein providing a controller includes providing a processor.

37. The method of claim 34, wherein coupling an integrated circuit to the controller includes coupling a mixed signal integrated circuit formed as the integrated circuit having the dielectric layer containing the barium strontium titanium oxide film.

38. The method of claim 34, wherein the method includes forming an information handling system.

39. The method of claim 34, wherein the method includes forming a wireless system.

40. A method comprising:

providing a controller;

coupling a device to the controller, the device having a dielectric layer containing an erbium-doped barium strontium titanium oxide film, the erbium-doped barium strontium titanium oxide film formed by:

forming a layer of barium oxide by atomic layer deposition;

forming a layer of strontium oxide by atomic layer deposition;

forming a layer of titanium oxide by atomic layer deposition; and

annealing the layers of barium oxide, strontium oxide, and titanium oxide to form the erbium-doped barium strontium titanium oxide film.

41. The method of claim 40, wherein coupling a device to the controller includes coupling a display having the dielectric layer containing the erbium-doped barium strontium titanium oxide film.

42. The method of claim 40, wherein coupling a device to the controller includes coupling a light-emitting device having the dielectric layer containing the erbium-doped barium strontium titanium oxide film.

43. The method of claim 40, wherein providing a controller includes providing a processor.

44. The method of claim 40, wherein the method includes forming a multimedia system.

45. The method of claim 40, wherein forming an information handling system includes forming a wireless device.

46. A device comprising:

a substrate; and

a dielectric layer disposed on the substrate, the dielectric layer including a barium strontium titanium oxide layer structured as one or more monolayers.

47. The electronic device of claim 46, wherein the electronic device includes a capacitor having the dielectric layer as a capacitor dielectric.

48. The electronic device of claim 46, wherein the electronic device includes a transistor in which the dielectric layer is disposed.

49. The electronic device of claim 46, wherein the electronic device includes a memory in which the dielectric layer is disposed.

50. The electronic device of claim 46, wherein the barium strontium titanium oxide layer includes an erbium-doped barium strontium titanium oxide film.

51. The electronic device of claim 50, wherein the electronic device includes an optoelectronic device in which the dielectric layer is disposed.

52. The electronic device of claim 50, wherein the electronic device includes an electroluminescent device in which the dielectric layer is disposed.

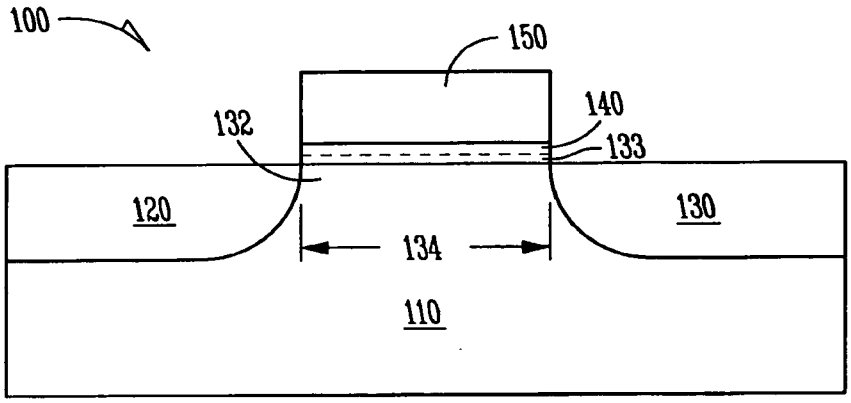
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FIG. 1

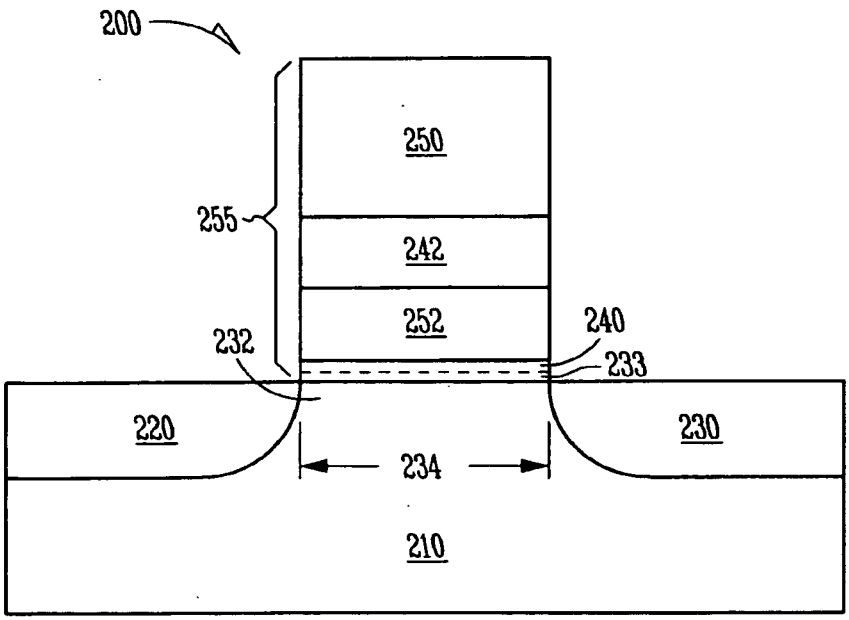
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FIG. 2

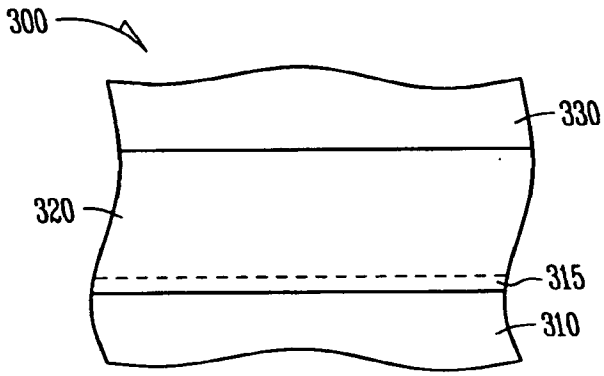


FIG. 3

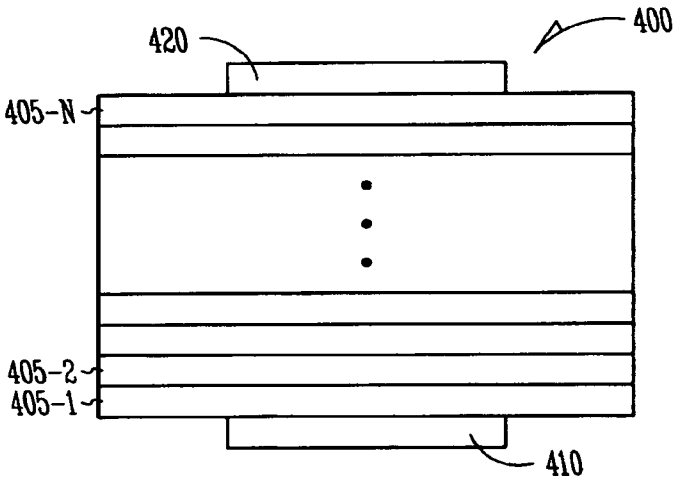
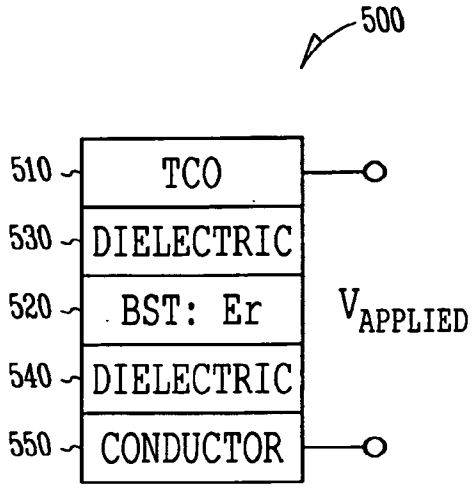


FIG. 4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BST: Er
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CONDUCTOR

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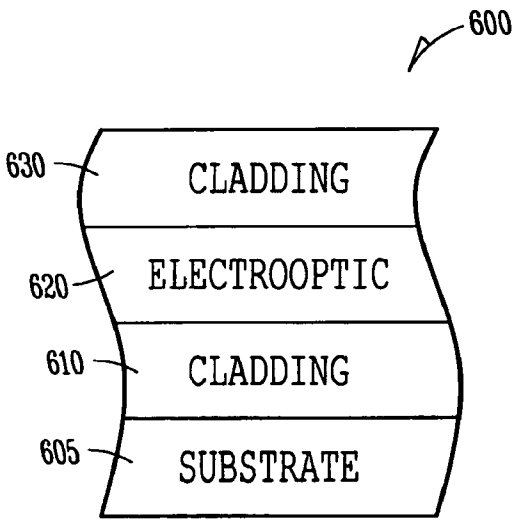
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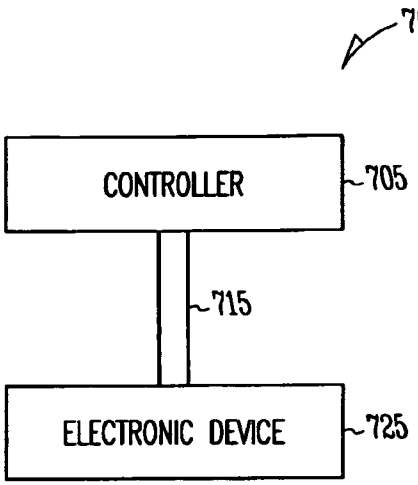
SUBSTRATE

FIG. 6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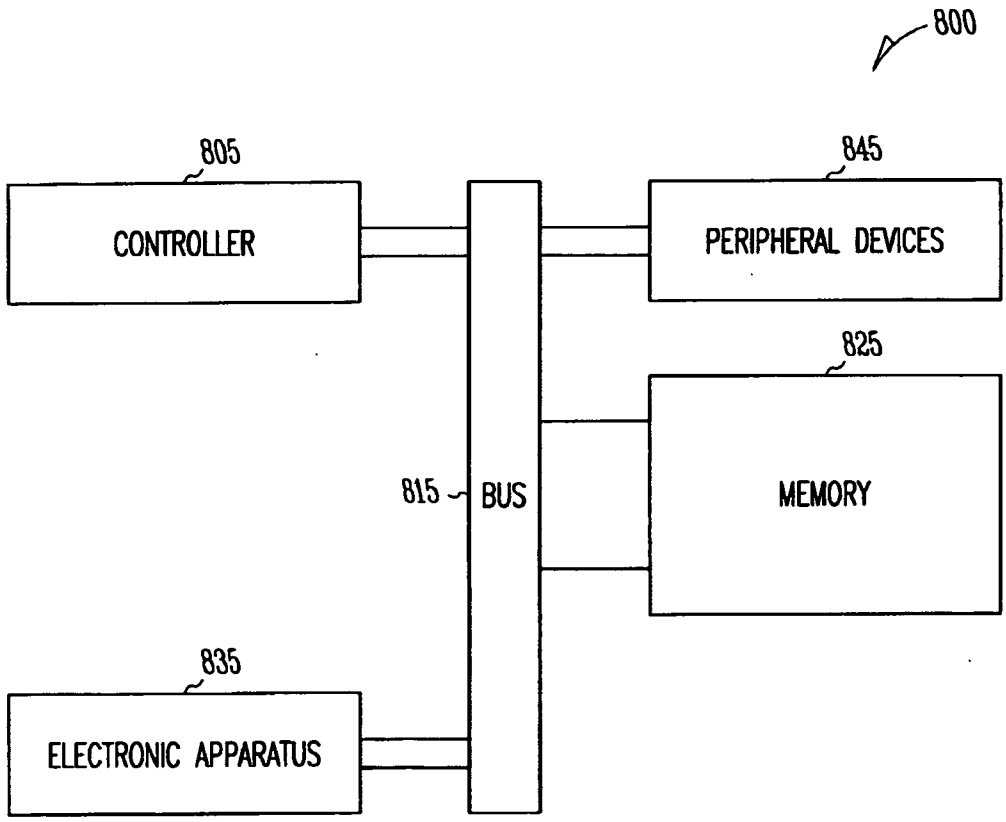
CONTROLLER
705
715
ELECTRONIC DEVICE
725

FIG. 7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CONTROLLER
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MEMORY
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BUS
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ELECTRONIC APPARATUS

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/018137

A. CLASSIFICATION OF SUBJECT MATTER
INV. C23C16/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WANG Z ET AL: "Electrical properties of SrTiO3/BaTiO3 strained superlattice films prepared by atomic layer metallorganic chemical vapor deposition" JOURNAL OF THE ELECTROCHEMICAL SOCIETY ELECTROCHEM. SOC USA, vol. 147, no. 12, December 2000 (2000-12), pages 4615-4617, XP002464071 ISSN: 0013-4651	1,3,6,7, 23-25, 34-39, 46,47,49
Y	page 4616, left-hand column, line 41 - page 4617, left-hand column, line 13	2,4,5, 8-22, 26-33, 40-45, 48,50-52

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 January 2008	25/01/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ekhult, Hans

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/018137

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6 501 121 B1 (YU ZHIYI [US] ET AL) 31 December 2002 (2002-12-31) column 4, line 30 - line 50; claims 1,2 column 5, line 52 - column 6, line 28	2,4,5, 8-22, 26-33, 40-45, 48,50-52
A	SHEN C ET AL: "Photoluminescence properties of Er<3+>-doped Ba0.5Sr0.5Ti03 prepared by sol-gel synthesis" MATERIALS SCIENCE AND ENGINEERING B, ELSEVIER SEQUOIA, LAUSANNE, CH, vol. 111, no. 1, 15 August 2004 (2004-08-15), pages 31-35, XP004517038 ISSN: 0921-5107 paragraph [0001]	1-52
A	EP 0 812 021 A (SHARP KK [JP] SHARP KK) 10 December 1997 (1997-12-10) claim 1	1-52
A	US 2004/040494 A1 (VAARTSTRA BRIAN A [US] ET AL) 4 March 2004 (2004-03-04) examples 1,2	1-52

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/018137

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6501121 B1	31-12-2002	AU 1458002 A	27-05-2002
		TW 511232 B	21-11-2002
		WO 0241378 A2	23-05-2002
EP 0812021 A	10-12-1997	DE 69707356 D1	22-11-2001
		DE 69707356 T2	04-07-2002
		JP 9331020 A	22-12-1997
		US 5907470 A	25-05-1999
US 2004040494 A1	04-03-2004	US 2004197946 A1	07-10-2004