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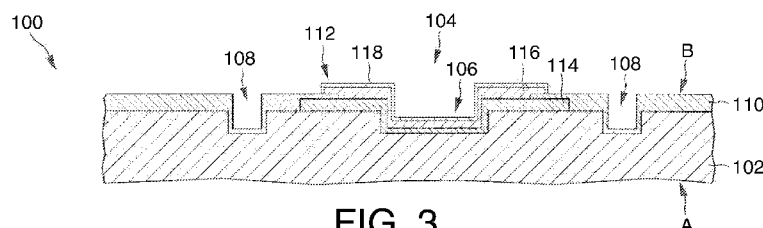
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(54) Title: ELECTRIC COMPONENT WITH UNDER-BUMP METALLIZATION AND INTEGRATED CONFINEMENT STRUCTURE



(57) Abstract: The present invention relates to an electric component with a substrate (102), an under-bump metallization (104) suitable for accommodating a solder bump, the under-bump metallization extending laterally between its lateral limits; and a confinement structure (108) arranged beyond the lateral limits (112) of the under-bump metallization, for confining a flow of liquid away from the under-bump metallization. The electric component according to the first aspect of the invention avoids problems associated with flow out of liquid, like flux, from a solder bump before and during a soldering process.

Electric component with under-bump metallization and integrated confinement structure

FIELD OF THE INVENTION

The present invention relates to an electric component, and electronic device comprising the electric component, and to a method of fabricating an electric component.

5 BACKGROUND OF THE INVENTION

Solder bumps or solder balls on the wafer or substrate level are used in semiconductor-component packages to achieve a reduced package height and a simplification of the layout of the package by eliminating bond wires. Various types of electric components in the form of semiconductor-component packages are known, for example chip-scale
10 package, ball-grid-array package, multi-chip-module package (MCM) and flip-chip package.

EP 0 540 312 A1 describes a bump electrode structure and a semiconductor chip having such a bump electrode structure. A V-shaped trench is arranged in a semiconductor substrate, which is covered with an insulation film. A metallization is arranged on the insulating film, extending also through the V-shaped trench. On top of this, a
15 thin metal subbing film connected to the metallization is provided, followed by a solder bump, which fills the V-shaped trench and protrudes from it.

Reflow soldering is a widely used soldering process in the semiconductor industry for package assembly in backend processing of electric components. Examples are the bonding of dies, comprising a semiconductor substrate with an under-bump-metallization
20 (UBM), to one or more other dies, printed-circuit boards (PCBs) or other substrates. A solder paste, which typically forms a mixture of a solder powder and flux, is applied to metal pads of one of the respective electric components to form solder balls, which as mentioned are also referred to herein as solder bumps without difference in meaning. Then, a second electric device is placed onto the solder bumps. Without going into details of the subsequent thermal
25 processing stages, which are typically performed at the board level in an oven, the assembly will for some time be heated to a temperature, at which the solder becomes a liquid. This process step is referred to as the reflow step or, in short, reflow. The reflow step is decisive for forming a metallurgical bond between the electric components via the solder balls.

When there is solder paste printed on a UBM, the flux in the solder paste can flow away from the UBM, even before the reflow step, which is referred to as flow out. Where two neighboring UBMs are close to each other, i.e., at a fine pitch, this is an unwanted effect. For when the flux flows from both solder bumps touch each other, solder bridging
5 between the UBMs will occur.

It is desirable to provide a semiconductor component with a solder-bump structure on it, which avoids solder bridging.

SUMMARY OF THE INVENTION

10 An electric component according to a first aspect of the invention has
- a substrate;
- at least one under-bump metallization suitable for accommodating a solder bump, the under-bump metallization extending laterally between its lateral limits; and
- a confinement structure arranged beyond the lateral limits of the under-bump
15 metallization, for confining a flow of liquid away from the under-bump metallization.

The electric component according to the first aspect of the invention avoids problems associated with flow out.

The electric component of the invention allows confining solder material, in particular flux, that, while liquid in the process of solder-ball fabrication, may flow away
20 from a solder ball to a region where no functional damage can be caused to the electric component. This way, undesired effects such as solder bridging can be avoided. Therefore, even if the presence or creation of paths for undesired flow out cannot be avoided as such, the invention avoids the negative effects by confining the flow out to the limits defined by the confinement structure. As such, the invention turns away from trying to avoid the possible
25 causes of an undesired flow out.

In the following, embodiments of the semiconductor component of the first aspect of the invention will be described. The additional features of different embodiments can be combined with each other to form further embodiments, unless respective different embodiments are described as forming alternatives to each other.

30 The under-bump metallization is sometimes herein also referred to as UBM, bump pad or simply as a pad. The under-bump metallization serves for bonding a solder bump to the substrate in a solder process. The UBM typically comprises a layer structure. For instance, an adhesion layer, diffusion-barrier layer, a solder-wettable layer, and a protective layer may be provided in a UBM layer structure on a substrate. In the case of an intermediate

product, which is also claimed, the under-bump metallization may not yet be present, but is to be added at a later processing stage.

Furthermore, even though the electric component is designed and fabricated to be provided with a solder bump, the solder bump may be added to the electric component in a different fab by a different manufacturer. As a traded product, the electric component of the first aspect of the invention is therefore not necessarily provided with a solder bump. Protection for the invention of the present electric component is therefore claimed independently of whether it comprises a solder bump or not.

Electric components according to the first aspect of the invention may for instance take the form of printed circuit boards, processed wafers, dies and chips, and may comprise an integrated circuit, a section of an integrated circuit or a single circuit element (transistor, diode, resistor, etc.). An electric component of the first aspect of the invention may also be a passive-integration substrate, i.e., additionally comprise integrated passive components such as capacitors or inductors.

The concept of the confinement structure can be implemented in many different ways, depending, for instance on the requirements of a particular device structure, fabrication process and choice of materials, to name only a few factors.

Generally speaking, the electric component of the first aspect of the invention provides a confinement structure associated with a respective under-bump metallization. One suitable way of the association of a confinement structure with a respective under-bump metallization is an arrangement of the confinement structure in a lateral periphery of the under-bump metallization. The lateral periphery is in the present context to be understood as the lateral neighborhood of the under-bump metallization, or, in other words, an area lying beyond, i.e., outside the lateral limits of the under-bump metallization.

By means of the confinement structure, any flow out from a solder bump before or during a soldering process is restricted to only the lateral periphery or neighborhood of the under-bump metallization, which lateral periphery is separated from areas with larger distances from the solder bump by the confinement structure. The extension of the lateral periphery of the under-bump metallization is thus given by the position of the confinement structure with respect to its associated under-bump metallization.

The confinement structure may for instance be arranged with a distance of at most half the distance between neighboring under-bump metallizations from its associated under-bump metallization. This allows arranging confinement structures around every under-bump metallization without mutual overlap.

The distance of the confinement structure from the associated under-bump metallization may be different in different lateral directions. Suitably, the different distance parameters between the confinement structure and the under-bump metallization are chosen with a view to the distance between the under-bump metallizations in respective lateral directions. Specifically, the distance between neighboring pads in one lateral direction, say, x-direction may be different from the distance between neighboring pads in a lateral direction perpendicular thereto, say, y-direction. In this case, the distance of a confinement structure from its associated under-bump metallization suitably reflects this anisotropy of the bump-pad arrangement.

In some embodiments, an overlap of neighboring confinement structures is useful. This will be explained further below by way of example in the context of an embodiment that uses a catchpot recess as the confinement structure.

The confinement structure as such can take different forms. In one embodiment just mentioned, the confinement structure comprises at least one catchpot recess extending around the under-bump metallization. The catchpot recess may for instance be provided in the form of a ring-shaped trench surrounding the under-bump metallization. The term “catchpot recess” is used herein as a pictorial expression, alluding to the function of this recess in the context of the present embodiment. Namely, the catchpot recess serves to collect and accommodate in its volume the liquid solder material, in particular flux, flowing away from the associated solder ball during fabrication.

The use of a catchpot recess has the additional advantage of providing improved anchoring of a molding between two coupled electric components in an electronic device. The changing height profile associated with the provision of catchpot recesses allows the molding to extend into the recesses and be “hooked” better than to a substrate surface without the catchpot recess. This reduces the risk of delamination of the molding.

After fabrication, the catchpot recess of an electric component of this embodiment may comprise at least partial filling with the solder-bump material, mostly flux. This is an indication of a successful prevention of an excessive flow out from the associated solder bump during fabrication by the catchpot recess, in fulfillment of the intended function of the catchpot recess according to the present invention. The substrate may be subjected to a cleaning step after the reflow for removal of any material collected in the catchpot recess.

Returning to the mentioned use of an overlap of confinement structures: by allowing catchpot recess structures of an embodiment explained below to cross each other or,

more generally speaking, share certain recess sections, communicating recess volumes can be provided. This way, the overall volume provided for accommodation of liquid such as flux is increased. This embodiment is also useful where a particularly small bump-to-bump pitch value shall be achieved. In an overlap configuration, the mentioned distance of the confinement structure from its associated under-bump metallization is typically larger than half the distance between neighboring under-bump metallizations. For the purpose of definition, the bump-to-bump pitch in a given direction is the distance value that is present between centers of two neighboring solder bumps in that direction. If the distance varies over a sample comprising a plurality of solder bumps, the pitch is suitably defined as the smallest distance value within that sample.

Note that, due to the effect of gravity, the catchpot recess is in particular useful in preventing undesired effects of an undesired flow out in a situation, where gravity supports the flow of the flux into the catchpot. As such, a catchpot recess is preferably provided on an upper surface of that electric component, which during the solder process is a lower component of a pair of electric components to be bonded by the solder process. Preferably, thus, the structure of the electric component allows such support by forces of gravity, before and while the solder paste is subjected to reflow during backend processing. To that end, the trench bottom may be arranged at a lower level than at least sections of the solder bump. Preferably, the trench bottom is even below the level of the under-bump metallization. Again, the presence of an at least partial filling of the catchpot trench with flux is an indication of such a suitable arrangement.

The electric component of the first aspect of the invention may combine the catchpot embodiment with a metallization recess that provides an improved adhesion or “anchorage” of the solder bump to the substrate. Such a metallization recess design increases the amount of solder material, which is deposited, in comparison with designs that do not employ a metallization recess, such that a considerable amount of solder material is deposited in the metallization recess. As a consequence, tapering is produced, typically by the wetting behavior of the solder on the lateral sides of the metallization recess. This reduces the mechanical stress at the sides of the solder bump.

Such a stabilization is particularly advantageous for small solder-bump structures, which are used in electric components having a small bump-to-bump pitch. The solder-bump structure of the semiconductor component of the first aspect of the invention is therefore particularly suitable for application in large-scale integration with small package size. In preferred embodiments, the semiconductor substrate comprises a plurality of solder-

bump structures with a lateral pitch of 300 micrometer or less. Modern components tend to decrease the bump-to-bump pitch even further. In some embodiments, the pitch even amounts to only 200 micrometer or less. The electric component of the first aspect of the invention is particularly useful at an even lower bump-to-bump pitch of today's leading-edge technologies, using a bump-to-bump pitch of only 100 micrometer or even less.

In one embodiment, an underbump metallization extends in the metallization recess, and, preferably, also in the closest periphery of the metallization recess. The under-bump metallization (UBM) preferably comprises a metallization pad containing nickel and gold and covering trench walls and a trench bottom of the metallization recess. In embodiments, where the under-bump metallization extends also on sections of the periphery of the metallization recess, the underbump metallization, however, does not reach the catchpot recess. It is not intended to let the under-bump metallization extend into the catchpot recess.

The bottom and trench walls of the catchpot recess are preferably covered by a passivation layer. Suitably, the wafer passivation layer, for instance made of silicon nitride (such as Si_3N_4) also covers the trench bottom and sidewalls.

In one embodiment, the catchpot recess and/or the metallization recess extend only within layers deposited on the substrate in backend processing, such as a passivation or UBM layer structure, or both.

In an alternative embodiment, the catchpot recess even extends into the substrate. In this embodiment, the confinement structure is defined on the wafer level. Preferably, in this embodiment, the under-bump metallization is also provided in the metallization recess, which extends into the substrate in the depth direction. This way, the adhesion or "anchorage" of the solder bump to the substrate is further improved.

Defining the confinement structure and/or the metallization on wafer level may require additional front-end processing steps performed on the substrate. To reduce the processing cost, a simplification of the processing can be achieved for this embodiment by performing the additional front-end processing steps in combination with routine processing steps at the respective processing stage. For instance, catchpot and metallization recesses may be fabricated together in the context of other recess formation processes in the substrate, such as the formation of trenches for a shallow-trench isolation, if applicable.

Alternatively to the catchpot recess or in combination with it, the confinement structure may advantageously comprise a dyke extending around the under-bump metallization. A dyke structure, which may also be called a dam structure, allows a

confinement of the flow of liquid such as flux by providing a hurdle which cannot be passed. Preferably, the dyke is closed, for instance ring-like, to the extent possible to avoid undesired leakage.

A height of the dyke in comparison with its immediate neighborhood can be selected with a view to the volume of liquid that can be expected to flow away from the solder bump. The height should also be selected with a view to the volume to be provided for collecting liquid between within the limits defined by the dyke. As a safeguard, a worst-case scenario might be used for the height calculation, assuming that the full volume of the solder ball is distributed within the volume defined by the dyke during a solder reflow process.

The dyke structure is also effective in situations where gravity does not favor the use of a catchpot recess. Considering for example a delamination problem as described with respect to Figs. 1 and 2, the dyke will prevent solder flow in the cavity, provided that the dyke protrudes from the substrate high enough. If the device is turned upside down and the solder does not stick to the substrate surface the dyke will still effectively block the solder flow if it reaches into the delaminated molding. As such, the dyke can also help increase the adherence of such a molding to the substrate.

A combination of a catchpot recess with a dyke confinement structure is advantageous to combine the effect achieved with both concepts. In particular, it is a suitable choice if orientation in space of the electric component during the solder process is not predictable.

The electric component has in some embodiments at least one electronic circuit element on the first substrate side of the semiconductor substrate. The electronic circuit element may be a passive circuit element, such as a capacitor or an inductor. Alternatively or additionally, at least one active electronic circuit element, such as a transistor, or a diode or a plurality of circuit elements, active and passive, for instance in the form of an integrated circuit (IC) may be present on the first substrate side.

To provide a low-resistance electrical path between the electronic circuit element and the solder-bump structure on the second substrate side, a through-substrate via is advantageously provided. The through-substrate via extends from the first substrate side to the metallization recess through the substrate, suitably a semiconductor substrate, and electrically connects the electronic circuit element on the first substrate side with the under-bump metallization on the second substrate side.

Of course, if a solder bump is present in the metallization trench, the electrical connection extends from the electronic circuit element on the first substrate side to the solder bump.

5 In accordance with its technical function, the catchpot trench may comprise an at least partial filling with the solder-bump material.

The through-substrate via used in previously mentioned embodiments is in one embodiment formed integrally with the solder bump. In this embodiment, the solder bump may thus continue into the through-substrate via, which provides an improved anchorage of the solder bump in the substrate. The solder-bump material can be used as the filling material
10 of the through-substrate via. This simplifies the fabrication process. However, other materials may alternatively be used for the filling of the through-substrate via.

In a second aspect of the invention, the electric component of the first aspect of the invention is used as a (first) electric component of an electronic device comprising two or more electric components. The electric components of the electronic device are coupled to
15 each other electrically, mechanically, or both electrically and mechanically by at least one solder bump on the under-bump metallization.

Notably, the term “electric component” is to be differentiated from the term “electronic device”. In the present application, the term “electronic device” is used with the meaning of a structure of connected electric components, at least one of which is an electric
20 component of the first aspect of the invention.

Such electronic devices are fabricated for instance as a system in package, or as a system on chip, for instance as a flip-chip arrangement, including, in particular, semiconductor dies, printed circuit boards (PCB), or passive-integration substrates, for instance made of Silicon. Examples of electronic devices including a electric component of
25 the first aspect of the invention will be given later in the context of the description of the enclosed Figures.

In such an electronic device, the solder bump of the electric component of the first aspect may fill a metallization recess and protrude from it, being connected to an electrical connection structure the second electric component. The connection between the
30 first and second electric components may use a contact pad according to the prior art on the side of the second electric component. However, the second electric component is preferably also an electric component according to the first aspect of the invention or one of its embodiments. This way, the failure risk due to flow of liquid from the allotted under-bump metallizations can be further reduced.

Some electronic devices have an electrically isolating underfill arranged between the first and second electronic components. For instance, a mold compound such as an epoxy mold compound may form an underfill for isolation and protection of the electric components. In such embodiments, the solder-confinement structure of the electric component of the first aspect of the invention provides a high profile that can advantageously be filled with the electrically isolating material of this underfill as well. The molding is applied after the soldering process. This way, an additional anchoring of the isolation layer in the height profile of the catchpot recess or confinement dyke is achieved, improving the adhesion of the isolating layer and therefore the reliability and lifetime of the electronic device.

Note that there is no restriction as to the number of electric components comprised by the electronic device of the second aspect of the invention. Some embodiments may use three or more electronic components for the formation of an electronic device.

According to a third aspect of the invention, a method for fabricating a semiconductor component is provided. The method comprises:

- providing a substrate;
- fabricating at least one under-bump metallization suitable for bonding a solder bump to the substrate in a solder process;
- fabricating at least one confinement structure in the lateral periphery of the under-bump metallization, suitable for confining a flow of a liquid away from the under-bump metallization.

The advantages of the method of the third aspect of the invention correspond to those set forth in the context of the description of the semiconductor component of the first aspect of the invention.

In the following, embodiments of the method of the third aspect will be described. The additional features of these embodiments may be combined with each other to form further embodiments, unless they are explicitly described as alternatives to each other.

There is no required order for the fabrication of the under-bump metallization and of the confinement structure. Either one can be fabricated first in alternative embodiments. In a further embodiment, they are fabricated in parallel at least partly.

In one embodiment, the formation of the electric component further comprises fabricating a metallization recess and an under-bump metallization, which extends in the metallization recess, and fabricating a solder bump of a solder-bump material on the under-bump metallization. The solder-bump fills the metallization recess and protrudes from it.

In another embodiment, a confinement structure in the form of a dyke is fabricated.

Corresponding to the function of the confinement structure, the method of fabricating the semiconductor component comprises in one embodiment collecting solder-bump material, in particular flux, before and/or during a soldering process of a solder bump. Note, however, that the provision of the confinement structure trench is a precautionary measure. Not all confinement structures provided according to the method of the invention in an electric component according to the invention may actually have to collect flux during the soldering process. It is therefore not a necessary feature of the invention that liquid is actually flowing away from the under-bump metallization and collected within the confinement structure in the soldering process.

As mentioned before, preferred embodiments of the electric component of the first aspect have a metallization recess and a catchpot recess integrated into the semiconductor substrate. To achieve this wafer-level recess structure, the metallization recess and the catchpot recess are preferably etched into the semiconductor substrate in the depth direction.

A method of fabricating an electronic device according to the present invention comprises providing a first electric component according to the first aspect of the invention (provided with a solder bump on the under-bump metallization), for instance using the method of the third aspect of the invention, and at least one second electric component, and then coupling the first and second electric components by means of the solder bump of the first electronic component in a soldering process.

Preferred embodiments of the invention are also defined in the dependent claims.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is further elucidated by the following Figures and examples, which are not intended to limit the scope of the invention. The person skilled in the art will understand that various embodiments may be combined.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter. Note that none of the drawings

referenced below may be drawn to scale, nor may they reproduce relative extensions of different structural features with respect to each other. In the following drawings

Figs. 1 and 2 show, for illustrating the problem of solder-bump migration, schematic cross-sectional views of an electronic device according to the prior art before and after a soldering process;

Fig. 3 is a schematic cross-sectional view of a semiconductor component according to a first embodiment of the electric component of the invention;

Fig. 4 is a schematic plan view of the semiconductor component of Fig. 3 at a reduced scale;

Fig. 5 is a schematic cross-sectional view of the semiconductor component of Fig. 3 during the fabrication of solder bumps at a first processing stage;

Fig. 6 is a schematic cross-sectional view of the semiconductor component of Fig. 3 after the fabrication of solder bumps, at the same time forming a second embodiment of the electric component of the invention;

Fig. 7 is a schematic cross-sectional view of a semiconductor component according to a third embodiment of the electric component of the invention;

Fig. 8 is a schematic cross-sectional view of a semiconductor component according to a fourth embodiment of the electric component of the invention;

Fig. 9 is a schematic cross-sectional view of an electronic device comprising a semiconductor component according to the third embodiment as a first electric component and further comprising a second electric component;

Fig. 10 is a schematic cross-sectional view of a second embodiment of an electronic device;

Fig. 11 is a schematic cross-sectional view of a third embodiment of an electronic device, which is suitable for memory applications;

Fig. 12 is a schematic cross-sectional view of a fourth embodiment of an electronic device, which is particularly suitable for high-power applications;

Fig. 13 is a schematic cross-sectional view of a semiconductor component according to a fifth embodiment of the electric component of the invention;

Fig. 14 is a schematic plan view of the semiconductor component of Fig. 13; and

Fig. 15 is a schematic cross-sectional view of a semiconductor component according to a fifth embodiment of the electric component of the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

One problem that occurs in packaged semiconductor devices is solder ball migration. This will be explained in more detail with respect to Figs. 1 and 2 in the following.

Figs. 1 and 2 show schematic sectional views of an electric component 10 according to a prior art before and after a reflow step during a reflow-soldering process.

The electric component 10 comprises a substrate 12, which may for instance be a silicon substrate or a printed-circuit board (PCB), on which a chip 14 is to be attached by a reflow soldering process using solder bumps 16 through 20. The electric component has the chip 14 embedded in an epoxy mould and underfill 15.

An undesired delamination between the underfill 15 and the chip 14 may occur. Such delamination may for instance be caused by the presence of flux remainders on the substrate surface when the molding is applied. It creates a cavity 22, which opens up a path for the a migration of the liquid solder material, flux and powder, during the reflow step. This way, the solder bump 18 adjacent to the cavity 22 at the position of the delamination, is displaced at the end of the soldering process. Since the positioning of the solder bumps must be performed with high accuracy on metallizations, a displacement such as this is likely to result in a mechanical instability of the bond between the chip 14 and the substrate 12. Even more seriously, electrical failure may be caused by solder shorts.

It has been observed, in particular at small bump-to-bump distances, that the undesired cavity 22 may even bridge the distance between neighboring solder balls. As an undesired consequence, this solder bridging between the neighboring solder bumps along the path of the cavity may form a short or an electrical connection with an otherwise undesired effect.

Fig. 3 shows a schematic cross-sectional view of a semiconductor component 100 according to a first embodiment of the invention. Reference is made in parallel to Fig. 4, which is a schematic plan view of the semiconductor component of Fig. 3 at a reduced scale in comparison with Fig. 3.

The semiconductor component 100 has a substrate 102. In the present embodiment the substrate 102 is semiconductor substrate, for instance is a silicon substrate, such as a silicon wafer widely used in the semiconductor industry.

The substrate 102 is not shown with its full extension in its depth direction pointing from a second substrate side B to a first substrate side A. In particular, the first substrate side A and any structure on it are not shown in Figs. 1 to 4 for reasons of graphical simplification. In many embodiments, the semiconductor component 100 comprises

integrated circuitry on the first substrate side A. Also in the lateral direction shown, only a portion of the substrate sufficient to illustrate the invention is illustrated.

An under-bump-metallization 104 is provided on the second substrate side B. The under-bump-metallization 104, also called pad metallization in the following, is a layer structure that serves for accommodating and bonding a solder bump (shown in Figs. 3 and 4) with high mechanical strength, and for providing a good electrical connection between the solder bump and the integrated circuitry on the first substrate side, and for avoiding diffusion or other harmful interaction between the solder bump and the underlying substrate. In the present embodiment, the under-bump-metallization structure extends in a metallization trench 106 and in an adjacent substrate zone 112.

A confinement structure in the form of a catchpot recess 108 is arranged around the under-bump metallization 104 in its lateral periphery. The catchpot recess 108 can be said to define an outer edge of a lateral periphery of the under-bump metallization 104. The catchpot recess 108 is a trench in the present embodiment and will in the following also be referred to as a catchpot trench.

Both the metallization trench 106 and the catchpot trench 108 extend into the substrate 102. To achieve this, the metallization and catchpot trenches 106 and 108 can be produced by selectively etching into the Si wafer 102, at the portion where the pad metallization should be, and, at a certain distance in its lateral periphery, around it. In an alternative embodiment, the metallization trench and the catchpot trench do not extend into the substrate in the depth direction, but into a layer structure deposited on the substrate. Reference is made to Fig. 13 for this alternative embodiment.

Returning to Fig. 3 and the fabrication process of the structure shown, the under-bump metallization 104, is fabricated in and around the metallization trench 106. The under-bump metallization comprises a pad metallization 114, which is made of aluminum Al and deposited directly on the substrate material inside the metallization trench 106 and on its periphery 112 between the metallization trench 106 and the catchpot trench 108. The pad metallization 114 is selectively deposited on the desired location, in such a way that the bottom and side walls of the trench 106 and a small part of the periphery outside the trench is covered. The under-bump metallization 104 further comprises, on the pad metallization 114, a nickel layer 116, followed by a gold layer 118. From a process viewpoint, only the nickel layer and gold layer, and not the aluminum pad metallization 114, are sometimes referred to as the under-bump metallization, as they form the layers closest to the solder bump to be fabricated and are fabricated separately from the pad metallization 114, typically using

electrolytical or electroless fabrication processes. However, this distinction in terms is not relevant for the description of the structure of the semiconductor component of Fig. 3. The term underbump-metallization is used in this structural context to denote the layer structure 104 comprising the layers 114 to 118. It should be noted that alternative layer structures of the under-bump metallization 104 can be used as well, and are well known to a person of ordinary skill in the art.

Additional reference is now made to Fig. 4, which is a schematic plan view of the semiconductor component of Fig. 3 at a reduced scale. As can be seen in the top view of Fig. 4, the catchpot trench 108 has a ring shape and extends around the metallization trench 106. A ring shape is not mandatory, but a closed shape with respect to the solder bump is advantageous to collect any solder flowing out off the solder bump in all directions during a reflow process. The catchpot trench is covered with a passivation layer 110. The passivation layer also covers other portions of the second substrate side B, except for the metallization trench 106 and its closest periphery, where the UBM is present. The passivation layer 110 may for instance be made of silicon nitride (Si_3N_4). It is deposited in the present embodiment after the fabrication of the pad metallization 114, and before the deposition of the Ni/Au layer structure 116, 118. The Ni layer 116 partly extends over the passivation layer 110.

The plan view of Fig. 4 shows three neighboring under-bump-metallization structures 104.1 to 104.3 on the second substrate side B. The individual under-bump-metallization structures 104.1 to 104.3 have a circular shape. That is, the metallization trenches 106 are circular, as are the deposited layers of the under-bump metallization (UBM) 112. In the plan view, the gold layer 118 of the under-bump metallization is the only visible layer of this layer structure of the UBM 112. It is clearly visible in Fig. 2 that the catchpot trenches 108 extend around the individual metallization trenches and under-bump metallizations in their lateral periphery.

The lateral extension of the catchpot trenches is chosen suitably in the layout process to accommodate liquid that may flow away from the respective solder bump during later fabrication stages. The lateral extension and depth of the catchpot trenches 108 depends on their distance to their respective associated UBM 112 and on the amount of flux used. For example, the volume of flux to be accommodated by the trench in the worst case can be considered. In one embodiment, where the catchpot trench is very close to its associated UBM, it has the capacity to collect about 40-50% of the available flux. A larger capacity would in this case imply the risk of hindering a reflow solder process too much. In another embodiment, where the catchpot trench is further away from the UBM, the total volume of

the catchpot trench itself can be smaller, for instance 10-20% of the available flux, and serves just to avoid a flow out of flux to a neighboring UBM, which can cause bridging between the two bumps.

In determining the volume of the catch pot trench, the lateral extension can be chosen in consideration of a given depth of the catchpot trench, or vice versa. The depth extension of the catchpot trench into the semiconductor substrate 102 is in the present embodiment chosen identical to that of the metallization trench 106, in order to keep the fabrication of the trench structure of the under-bump-metallization structure 104 simple. Assuming that as a constraint, the lateral extension may thus be adapted in the layout process to the needs of a particular fabrication process.

Other embodiments have an increased the depth of the catchpot trenches (and, optionally, of the metallization trenches, if the mentioned constraint shall be maintained) to handle a larger solder volume. A lateral extension of up to 10 micrometer could be used, depending on the desired pitch P between neighboring solder bumps. However, the catchpot concept works already in an embodiment, where the depth is 1 to 2 micrometer and the width is 5 micrometer.

The pitch P, measured as the distance between the centers of neighboring under-bump-metallization structures of the semiconductor component 100, can be as small as 100 micrometer or less. Pitch values of down to 20 micrometer can be achieved. On the other hand, the pitch can also be chosen larger, such as between 100 and 300 micrometer. Note that the under-bump-metallization structure 104 just described may also be used for semiconductor components with a pitch of more than 300 micrometer between neighboring UBM structures.

It is possible to let adjacent catchpot trenches merge, for instance in order to achieve a particularly small pitch value. However, care should be taken to avoid the formation of any electrical contact between neighboring solder bumps through such a merged catchpot structure in a solder reflow process.

In a subsequent processing stage, which may be performed immediately after the fabrication of the under-bump-metallization structure 104, or at any later point in time, even after trading of the semiconductor component 100, solder bumps 120 are fabricated on the under-bump-metallization structure 104.

Fig. 5 is a schematic cross-sectional view of the semiconductor component of Fig. 3 during the fabrication of solder bumps at a first processing stage. Fig. 6 is a schematic cross-sectional view of the semiconductor component of Fig. 3 after the fabrication of solder

bumps, at the same time forming a second embodiment of the electric component of the invention.

To indicate that the fabrication stages of Fig. 5 and 6 can be performed starting with an intermediate product after trading, the semiconductor component with solder bumps is given the reference label 100' in Figs. 5 and 6. All other reference labels are unchanged in comparison with Figs. 3 and 4.

The solder-bump material is in the present embodiment provided in the form of a solder paste 126 and deposited by means of a squeegee through a stencil 128. Solder paste is made of microscopic solder particles forming a metallic alloy powder, represented by small circles in Fig. 5, and of flux (not shown). Solder paste that is especially designed for making solder bumps on a silicon wafer has a weight percentage of the metallic alloy powder with respect to the solder paste of typically 85-95%. The solder particles are frequently an alloy of tin Sn and lead Pb. Lead-free solder material comprises for instance tin Sn, silver Ag, copper Cu, and/or Bismuth Bi. Flux is a substance which is nearly inert at room temperature, but becomes strongly reducing at elevated temperatures, preventing the formation of metal oxides. Additionally, flux allows solder to flow easily on the underbump metallization (UBM).

The characteristics and flow properties of a particular solder paste depend primarily on its chemical and physical composition.

The solder paste 126 is deposited in an amount that fills the metallization trench and creates a hillock protruding from the metallization trench 106. An arrow 130 in Fig. 5 indicates the direction of travel of the squeegee 124 during the deposition of the solder bumps 120.

During the production of bumped wafers, it is not desirable that the solder paste, after it has been printed on the wafer, experiences flow out. Normally there is some time span between the printing and the reflow step. In this time span, a flow out may occur, mostly of flux. To further reduce flux flow out, a hydrophobic surfactant can be applied in the flux, since the wafer surface normally is hydrophilic. Also Carbosil can be applied to the flux to reduce flow out. For instance, an admixture of 1-3% to the flux has a great effect on the cohesion of the flux. However, any flow out that still occurs in this time span, is collected in the catchpot trenches 108.

In a subsequent processing step, the wafer 102 with the solder bumps 120 of solder paste is reflowed at appropriate reflow conditions, which achieves homogeneous solder bumps 120, as shown in Fig. 6. Note that the solder material extends inside the

metallization trench to a large amount. Taking into account the wetting behavior of the solder material, the provision and lateral dimensioning of the under-bump-metallization 104 in the present embodiment achieves that most of the solder material is inside the lateral bounds of the metallization trenches 106, and that some solder material extends on the “wings” 112.1 and 112.2 of the under-bump metallization 104 outside the metallization trench 106. A tapered solder-bump shape is thus obtained by the wetting behavior of the solder material on the wings 112.1 and 112.2 of the under-bump metallization 112. This tapered solder-bump shape has the advantage of reducing mechanical stress at the sides of the solder bump, thus avoiding a problem, which is otherwise encountered in some prior-art solder bumps due to their approximately spherical shape.

As explained before, the provision of catchpot trenches 108 solves the problems of solder bridging and flow out, especially in fine-pitch structures and especially before and during a board-level reflow process, by collecting and accommodating any liquid that flows out of the solder bumps 120. To illustrate this advantageous technical effect, a partial filling 132 is shown in the catchpot trenches 108 on the left hand side of the substrate 102.

Fig. 7 shows a schematic cross-sectional view of a semiconductor component 200 according to a third embodiment. The illustration in Fig. 7, as well as the illustration in Figs. 8 to 12, is even more schematic than that of Figs. 3 to 6, and omits certain structural features for the purpose of simplicity of illustration. For instance, a passivation layer and a detailed layer structure of the under-bump metallization are not shown. For such details, reference is made to the embodiment of Figs. 3 to 6. Throughout the following Figures, reference numerals copy the second and third digit of the reference numerals of Figs. 3 to 6, where corresponding functional and structural features are concerned. For instance, additional information on the substrate 202 of the electric component 200 can be obtained by referring back to information given before on the substrate 102 of the electric components 100 and 100' of Figs. 3 and 6.

The electric (in the present case, one may also say: semiconductor) component 200 has a semiconductor substrate 202 with a first substrate side, on which electronic circuitry is provided, which is graphically represented without structural detail by an active layer 240 on the first substrate side A. On the second substrate side B, a solder bump 220 is provided on an under-bump metallization 212 and fills a metallization trench 206. A catchpot trench 208 is provided in the lateral periphery of the solder bump 220. In the present embodiment, a through-substrate via 242 connects the bump 220 with the integrated circuit in

the active layer 240. The through-substrate via is filled with an electrically conductive material and may be isolated from the surrounding semiconductor substrate 202. Techniques for fabricating a through-substrate via are well known in the art. With the through-substrate via 242, a direct electrical connection is provided between the front side A of the semiconductor substrate 202 and the backside B.

In comparison with known through-substrate-via technologies, the present semiconductor component provides an improved mechanical stability. For the substrate 202 is thicker than in known technologies by an amount that corresponds to the depth of the metallization trench 206. This way, the semiconductor component 200 is less sensitive with respect to breakage.

In an alternative embodiment of a semiconductor component 300, shown in Fig. 8, a through-substrate via 343, the metallization trench 306 at the same time forms the through-substrate via, and thus extends from the second substrate side B to the active layer 340. Filling the via 342 with solder-bump material can be performed by dipping the substrate 302 into solder material and subsequent cleaning.

Fig. 9 is a schematic cross-sectional view of an electronic device 400 comprising a semiconductor component of the third embodiment as a first electronic component and further comprising a second electronic component. The electronic device 400 has a first electric component in the form of the semiconductor component 200 of Fig. 5. The semiconductor component 200 is coupled to a second electronic component in the form of a second semiconductor component 500, which comprises integrated circuitry (not shown) in an active layer 540 on a semiconductor substrate 502. The semiconductor component 200 is coupled to the second semiconductor component 500 by means of its solder bumps 220, which are connected to correspondingly arranged metallization pads 544 on the first substrate side A of the semiconductor component 500. In the graphical illustration of Fig. 9, the second semiconductor component 500 appears upside-down, as does the first semiconductor component 200. The integrated circuitry of the first semiconductor component 200 can be accessed directly by using this configuration. This provides an advantage during development and in circuit analysis. Solder bumps 546 on the first substrate side A of the semiconductor component 500 serve for coupling the electronic device 400 to other electronic components, such as a printed-circuit board.

Fig. 10 is a schematic cross-sectional view of a second embodiment of an electronic device 600. The electronic device 600 has the semiconductor component 200 according to the embodiment of Fig. 7 coupled to a printed circuit board 650. Between the

printed circuit board 650 and the semiconductor component 200, an electrically isolating underfill 652 is arranged. The use of an underfill is as such well known in the art. The present electronic device, however, provides an improved anchoring of the underfill to the second substrate side B of the semiconductor component 200. This is achieved by letting the underfill, typically a polyimide, epoxy compound or another electrically isolating underfill-resin used in flip-chip packaging. As explained before, the improved anchoring of the underfill 652 achieved by the catchpot trenches 208 of the semiconductor component 200 strengthens the adherence of the underfill to the semiconductor component and prevents a delamination of the underfill 652 from the semiconductor substrate 202.

Fig. 11 shows a further embodiment of an electronic device, in which several semiconductor components such as the semiconductor component 200 of the embodiment of Fig. 7 are stacked. More specifically, four chips 200.1 to 200.4 are stacked in a flip-chip arrangement. The solder bumps 220 of the respective chips 200.1 to 200.3 are coupled to the active layers 240 of the respective semiconductor components 200.2. to 200.4. This example is particularly suitable in memory applications requiring a large amount of memory cells with small area consumption. A three-dimensional chip package, such as the electronic device 700 allows to achieve considerable savings on the lateral chip size.

Fig. 12 is a schematic cross-sectional view of a fourth embodiment of an electronic device, which is particularly suitable for high-power applications. The electronic device 800 of Fig. 10 comprises a chip package of two semiconductor components 200.1 and 200.2 according to the embodiment of Fig. 5. In the present embodiment, the semiconductor component 200.1 contains an active layer 240.2 with integrated circuitry design for high-power applications.

The first semiconductor component 200.1 is coupled to a support substrate 850 by means of a layer of thermal glue 852. Electronic coupling between the substrate 850 and a metallization on the back side B of the first electronic component 200.1 can be achieved by wire bonding, as shown on the right side of the semiconductor component.

The second semiconductor component 200.2 is coupled to the first semiconductor component through solder bumps on the respective second substrate sides B, which face each other. Depending on the pitch of the solder bumps on the second semiconductor component 200.2 the catchpot trench may be omitted, if larger distances are used. However, catchpot trenches may be provided as in the first semiconductor component 200.1. The second semiconductor component 200.2 suitably comprises supporting electronics for the high-power integrated circuitry on the first semiconductor component.

Fig. 13 is a schematic cross-sectional view of a semiconductor component 900 according to a fifth embodiment of the electric component of the invention. The embodiment provides an alternative structure in that the underbump metallization 904 and the confinement structure 908 do not have recesses on wafer level, i.e. in the substrate 902. Instead, the under-bump metallization 904 and the confinement structure 908 are made of a patterned layer structure. A patterned metallization 914.1, 914.2, in the present embodiment made of Aluminum Al, comprises a pad metallization layer 914.1 and metallization tracks 914.2 surrounding it in its lateral neighborhood. On the pad metallization, a layer structure 916, 918 is deposited, for instance by sputtering or plating. The layer structure comprises a nickel layer 916, followed by a gold layer 918. A passivation layer 910 is deposited between the pad metallization layer 914.1 and the metallization tracks 914.2, and in the area beyond the metallization tracks 914.2. The height profile of the metallization 914.1, 914.2 on the substrate 902 is reflected in a corresponding height profile of the passivation layer 910. The passivation layer also covers an outer edge of the pad metallization layer 914.1. This gives rise to a recessed arrangement of the nickel and gold layers 916, 918, thus allowing the provision of a metallization recess 906 between elevated edge portions 904.1 without having to etch the substrate. Also a confinement structure is created by the deposition of the passivation layer 910 on the metallization tracks 914.2. A dam or dyke 908.1 is generated this way, which serves as a confinement structure for flow out from a solder bump to be deposited on the the under-bump metallization 904.

The semiconductor component 902 is fabricated as a part of the interconnect structure in backend processing. It can alternatively be arranged at a larger distance from the substrate 902, e.g., at a higher interconnect level, than shown in the present example.

Fig. 14 shows a simplified plan view of the under-bump metallization 904 and the confinement structure 908. In addition to the information given in the context of Fig. 13, a solution for contacting the under-bump metallization is provided by an interconnect line 914.3 connected with the metallization pad 914.1. The interconnect line 914.3 is electrically isolated from the ring-shaped metallization tracks by the passivation layer 910 (not visible in Fig. 14). The ring formed by the metallization tracks is interrupted to this end. The space between the interconnect line 914.3 and the metallization tracks 914.2 can be filled with an isolating material to avoid an interruption of the height profile. However, the opening between the two may be made small enough so that the dam 908.1 does not any opening or only a very small one.

Fig. 15 is a schematic cross-sectional view of a semiconductor component 1000 according to a further embodiment of the invention. The embodiment differs from the previous embodiment shown in Figs. 13 and 14 in the construction of the under-bump metallization. The layer structure of the under-bump metallization on a substrate 1002 and an interconnect structure 1040, 1042 and of the confinement structure 1008 is fabricated in a backend process of an IC process like in the embodiment of Fig. 13 and 14. As such, it does not involve the fabrication of wafer-level recesses. The electrical connection is provided by means of an interconnect 1040 and a via 1042 on a lower interconnect level (i.e., closer to the substrate than the pad metallization 1014.1). The interconnect 1040 and the via are embedded in a dielectric material 1044. However, the present embodiment uses a so-called bump-on-active-area (BUMA) structure. Instead of the metallization recess a protruding and electrically conductive first UBM layer 1017 is formed on top of the metallization pad 1014.1 and the passivation layer 1010, the latter again covering the outer edges of the metallization pad 1014.1 to form elevated portions 1004.1. The first UBM layer has a thickness of approximately 2.5 micrometer. On top of it, a second UBM layer 1018 (e.g., NiAu) is fabricated with a thickness of approximately 5 micrometer. The confinement structure 1008 resembles the confinement structure 908 of Fig. 13, and uses ring-shaped Al tracks 1014.2 to provide a dam 1008 on the passivation-layer level. The dam forms the confinement structure that prevents a flow out. In further processing, a bump is to be deposited on the second UBM layer 1018.

While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims.

In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

Any reference signs in the claims should not be construed as limiting the scope.

CLAIMS:

1. An electric component (100) with
 - a substrate (102),
 - an under-bump metallization (104) suitable for accommodating a solder bump, the under-bump metallization extending laterally between its lateral limits; and
 - 5 - a confinement structure (108) arranged beyond the lateral limits (112) of the under-bump metallization, for confining a flow of liquid away from the under-bump metallization.
2. The electric component of claim 1, wherein the confinement structure
10 comprises at least one catchpot recess (108) extending around the under-bump metallization (106).
3. The electric component of claim 2, wherein the catchpot recess (108) extends into the substrate (102).
- 15 4. The electric component of claim 1 or 2, wherein the confinement structure comprises a dyke extending around the under-bump metallization.
5. The electric component of claim 1, comprising a plurality of under-bump
20 metallizations (106) with a lateral pitch (P) of less than 300 micrometer.
6. The electric component (200) of claim 1, wherein the substrate is a semiconductor substrate (202) and further comprises at least one active or passive circuit element (240).
- 25 7. The electric component of claim 1, wherein a through-substrate via (242) extends from a first substrate side (A) through the substrate and electrically connects the electronic circuit element (242) on the first substrate side with the under-bump metallization on a second substrate side (B) opposite to the first substrate side.

8. The electric component of claim 1, wherein the under-bump metallization (106) is arranged in a recess (206).

5 9. The electric component of claim 1, further comprising a solder bump (220) of a solder-bump material on the under-bump metallization.

10. The electric component of claim 9, wherein the confinement structure comprises an at least partial filling (132) with the solder-bump material.

10

11. The electric component of claim 7 and 10, wherein the through-substrate via is formed integrally with the solder bump.

12. The electric component of claim 1, further comprising a passivation layer
15 (110) covering side walls and a bottom wall of the confinement structure (108).

13. An electronic device (400, 600) comprising a first electric component (200) according to claim 9, and further comprising at least one second electric component (500, 650), which is coupled to the first electric component by means of the solder bump (220) of
20 the first electronic component.

14. The electronic device of claim 13, wherein an electrically isolating underfill is arranged between the first and the second electronic component, and wherein the underfill extends into the confinement structure of the first electric component.

25

15. A method for fabricating a semiconductor component, comprising:
- providing a substrate (102) and
- fabricating at least one under-bump metallization (106) having lateral limits and being suitable for bonding a solder bump to the substrate in a solder process; and
30 - fabricating a confinement structure arranged beyond the lateral limits of the under-bump metallization, for confining a flow of liquid away from the under-bump metallization.

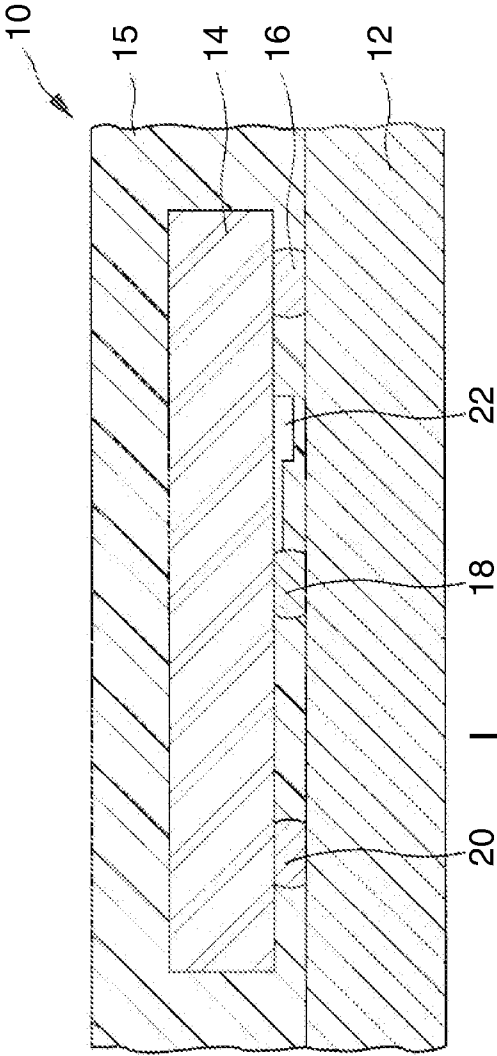


FIG. 1

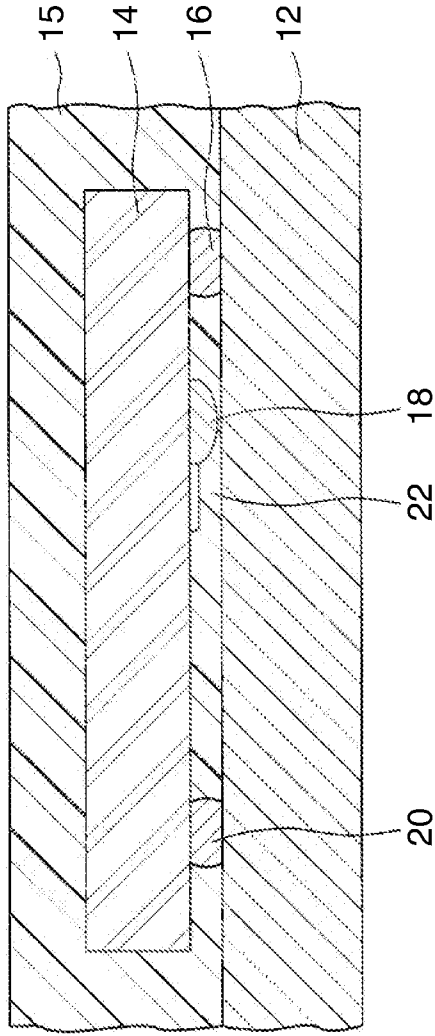


FIG. 2

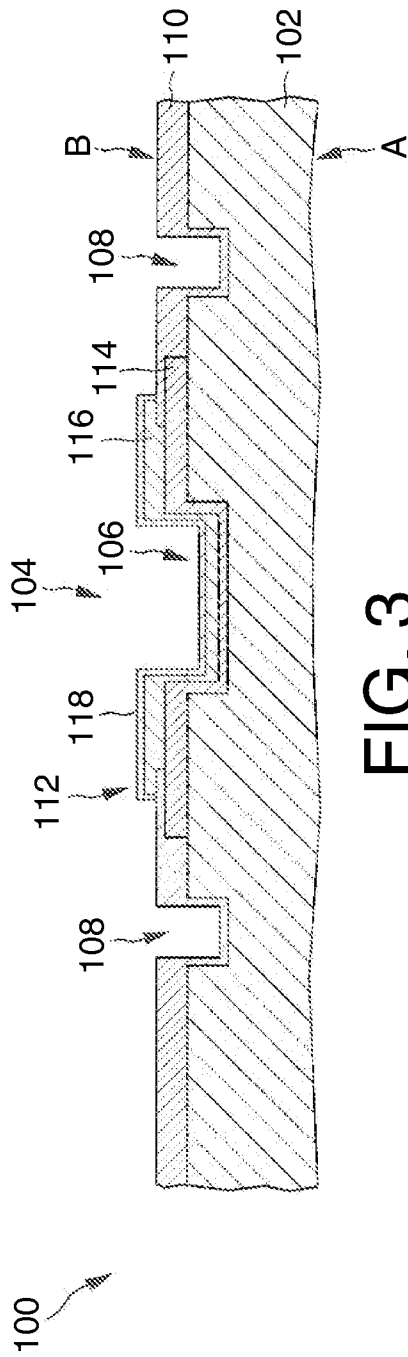


FIG. 3

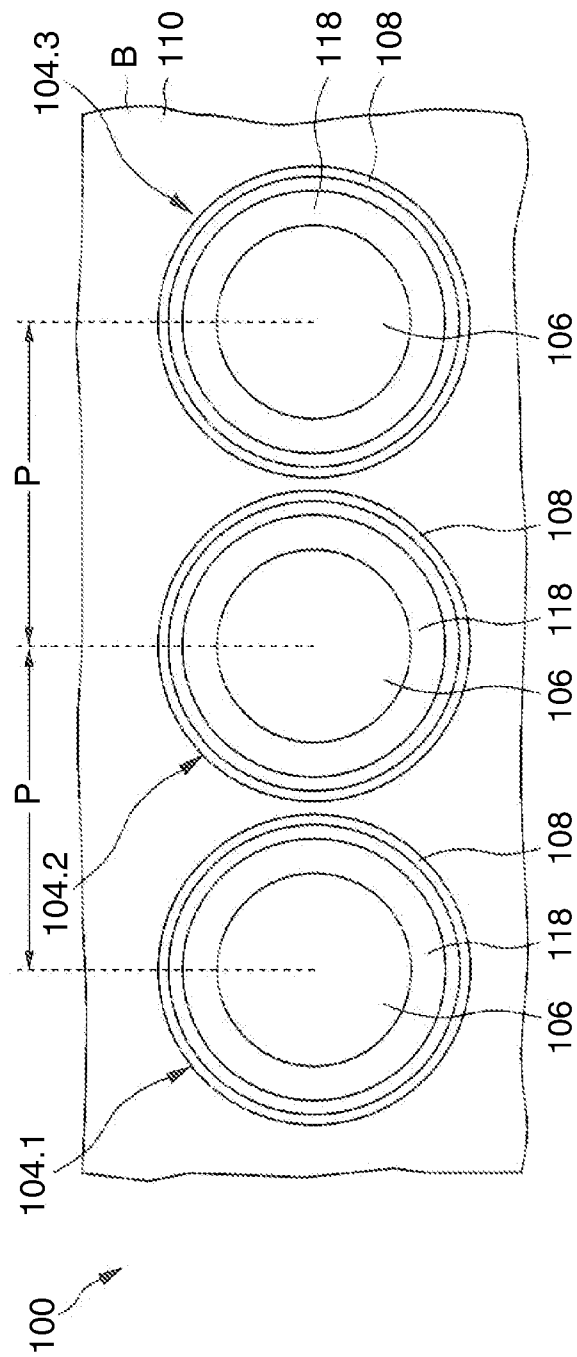


FIG. 4

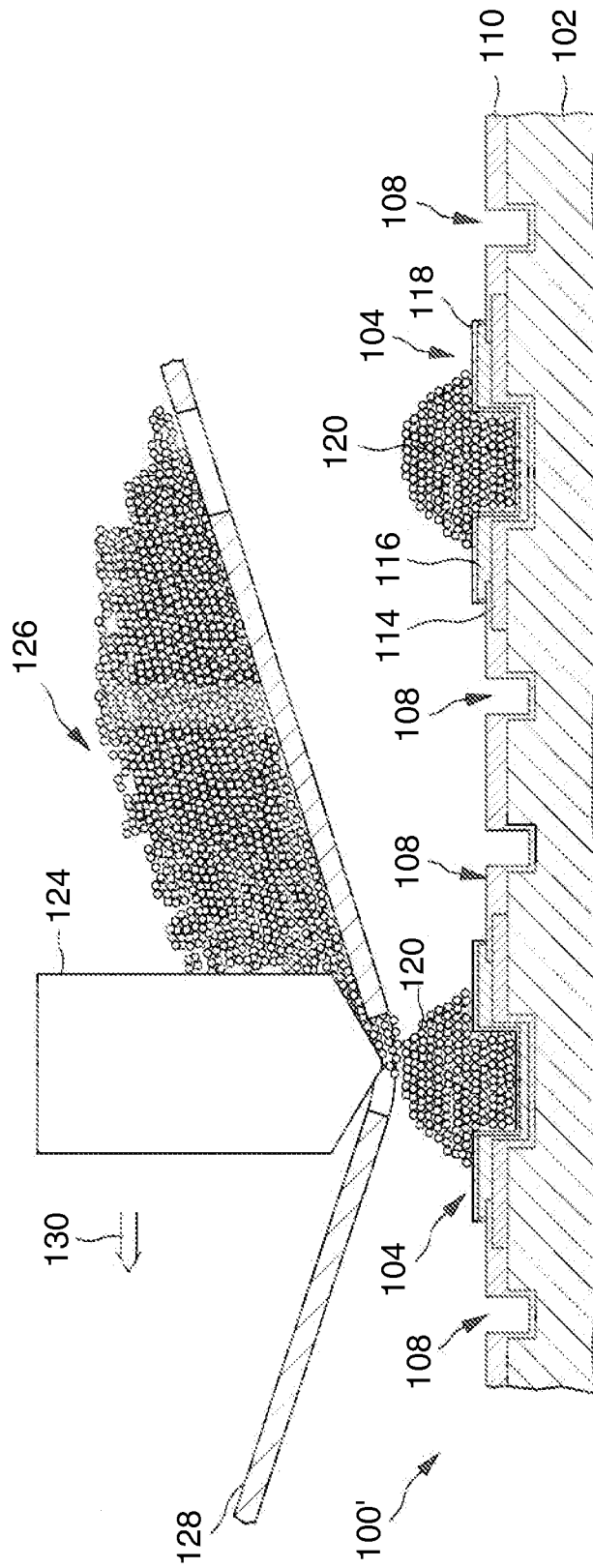


FIG. 5

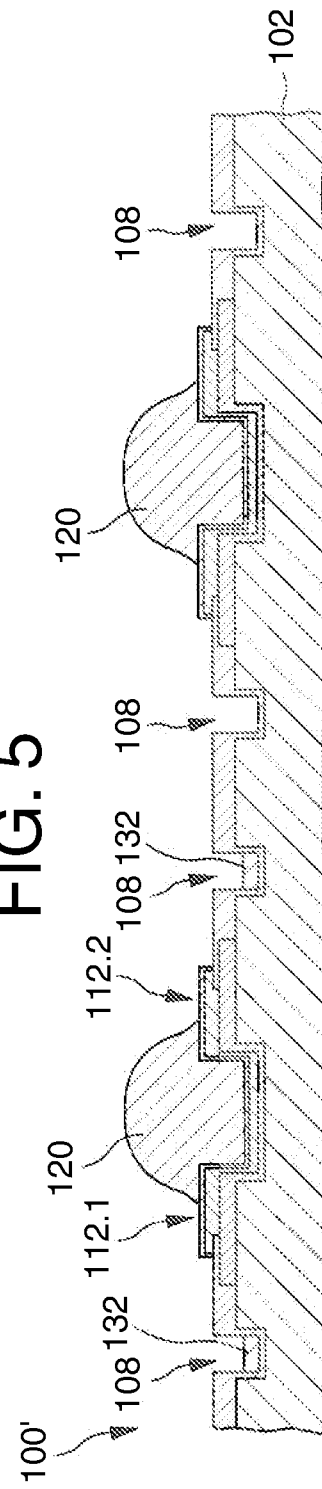


FIG. 6

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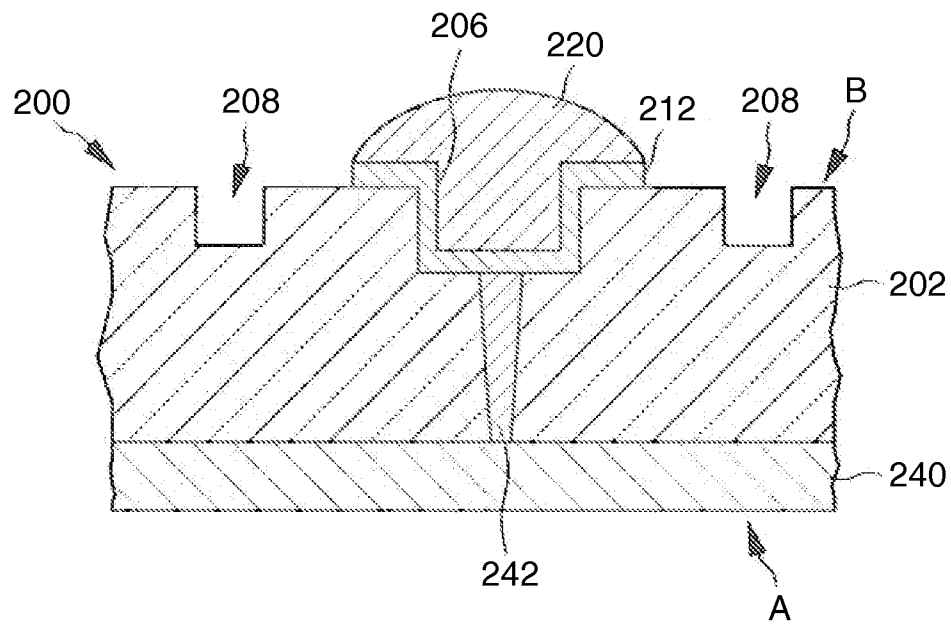


FIG. 7

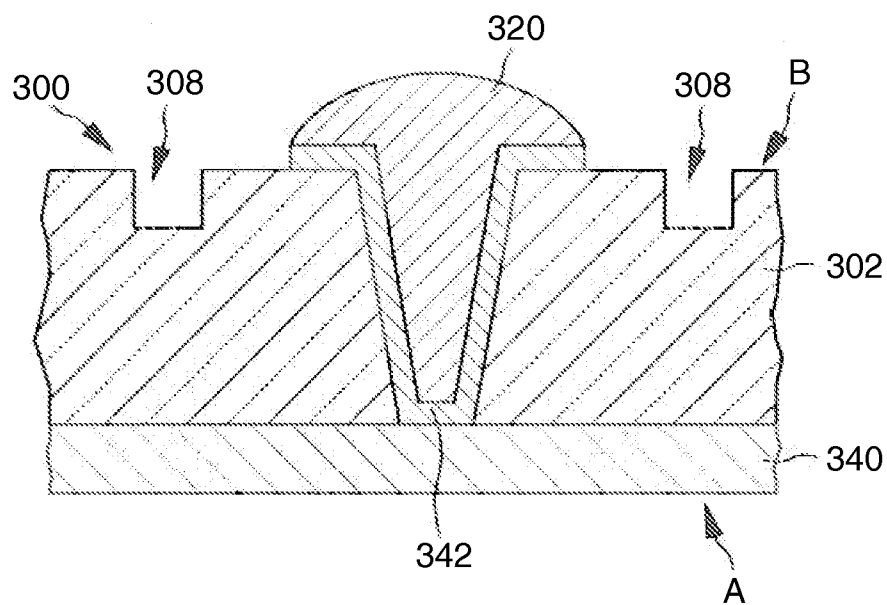


FIG. 8

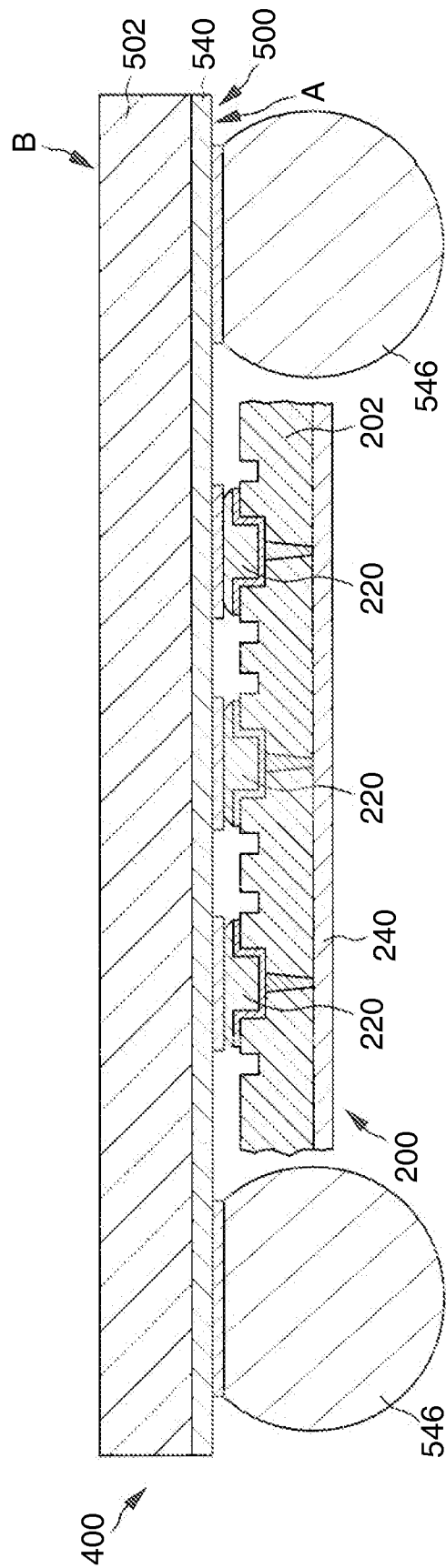


FIG. 9

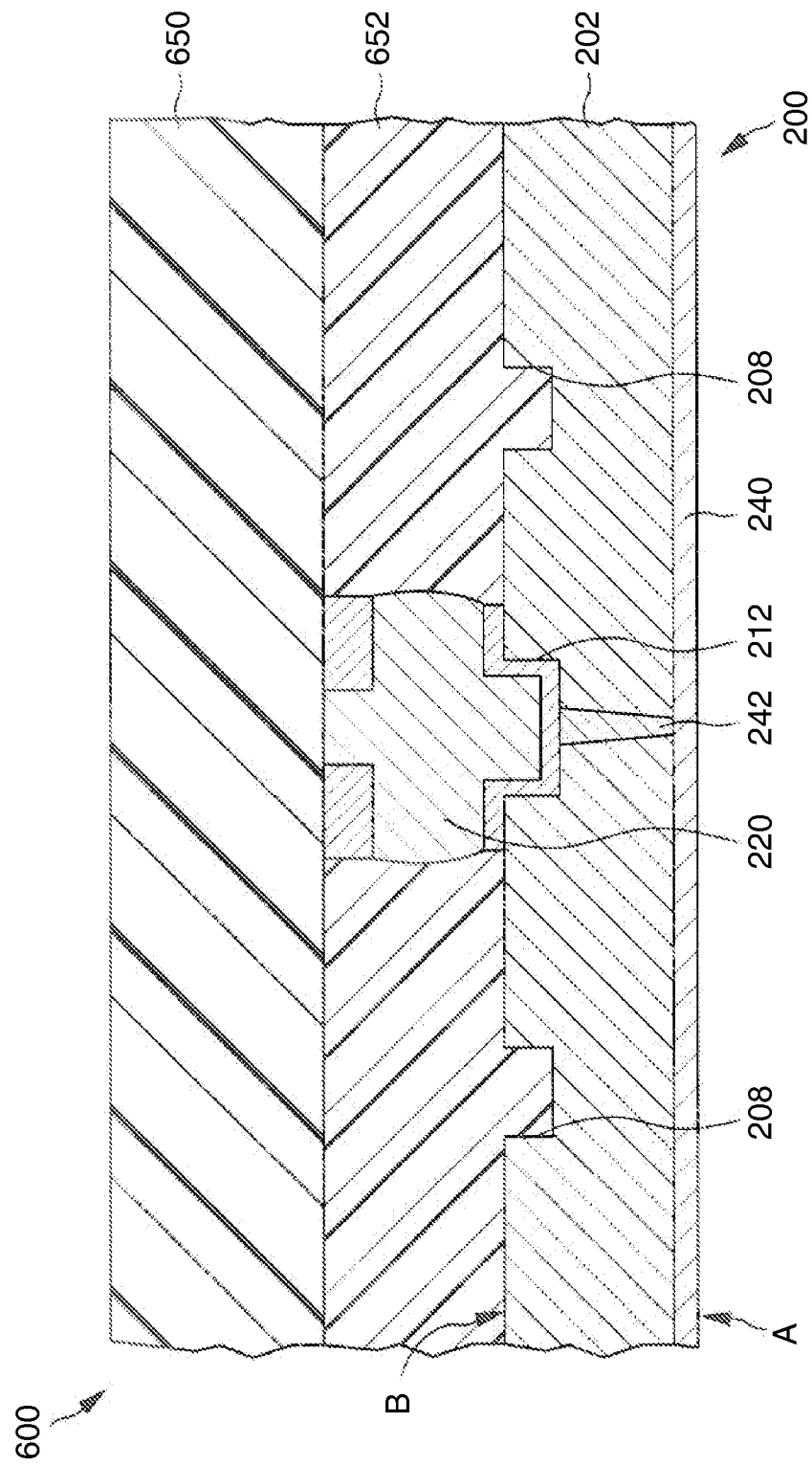


FIG. 10

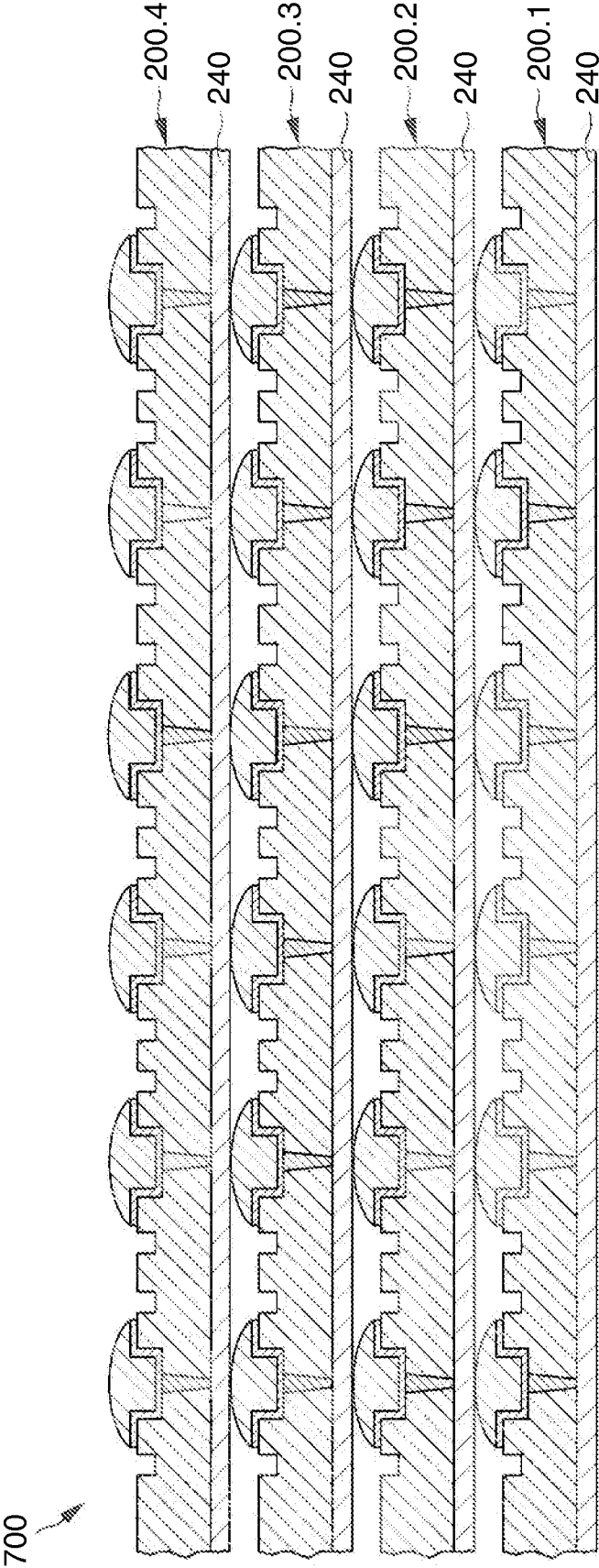


FIG. 11

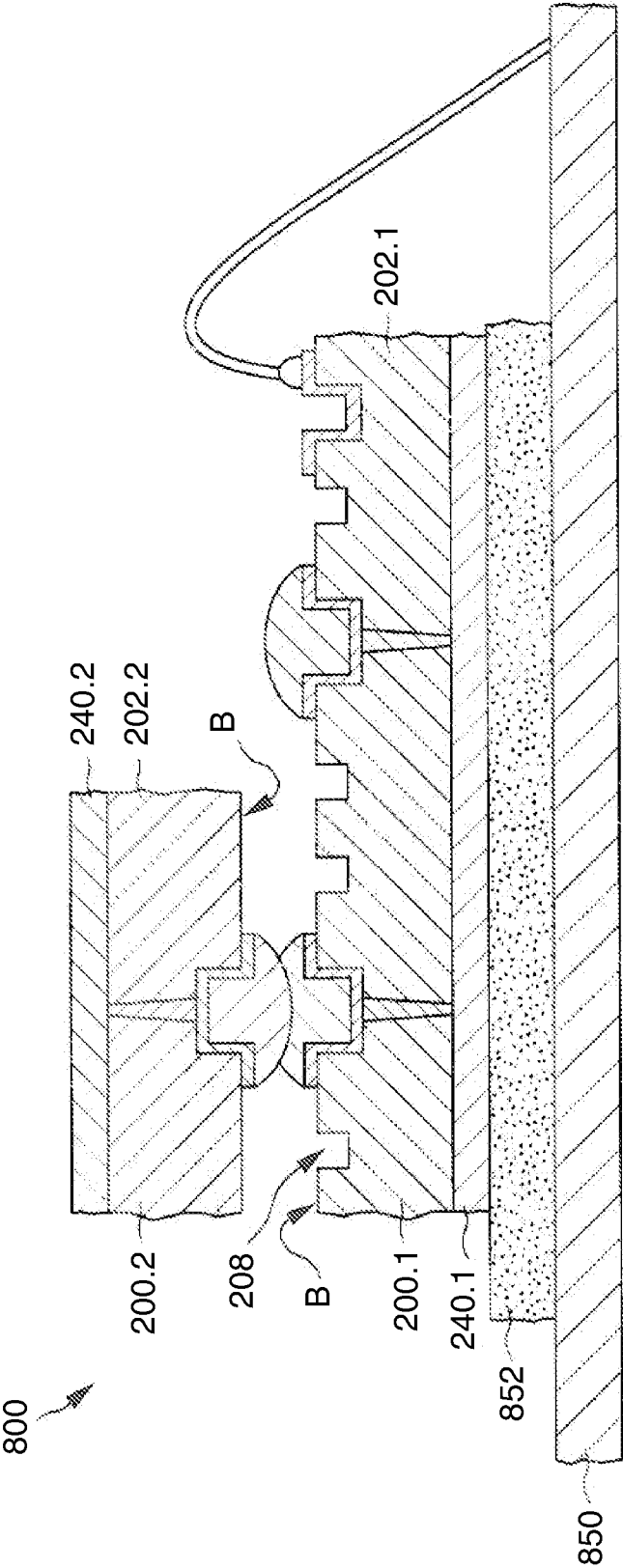


FIG. 12

9/11

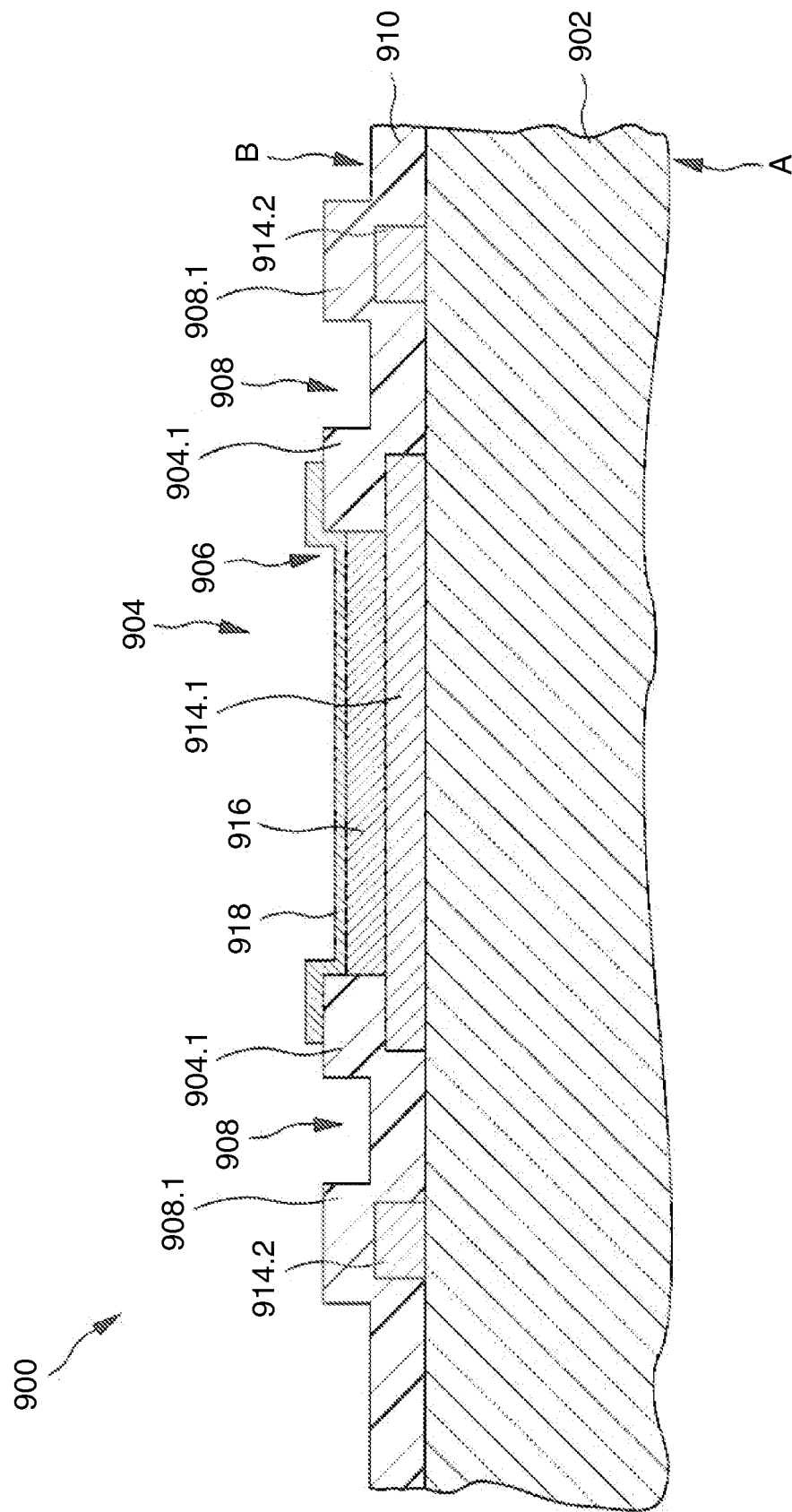


FIG. 13

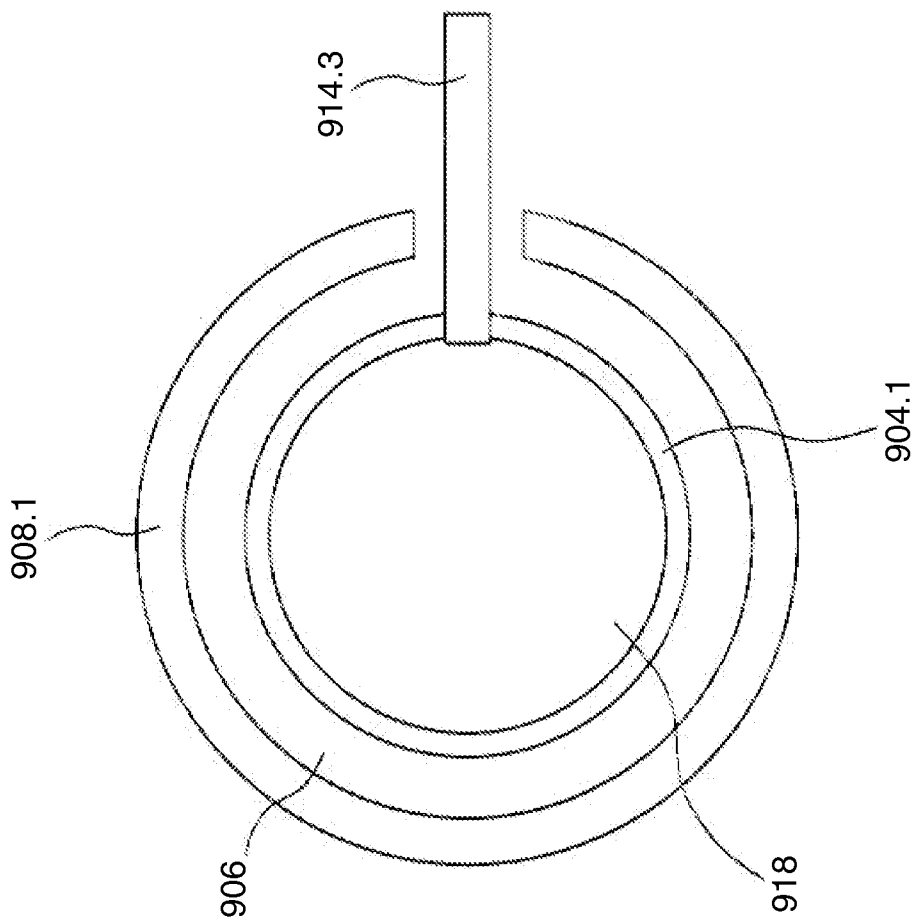


FIG. 14

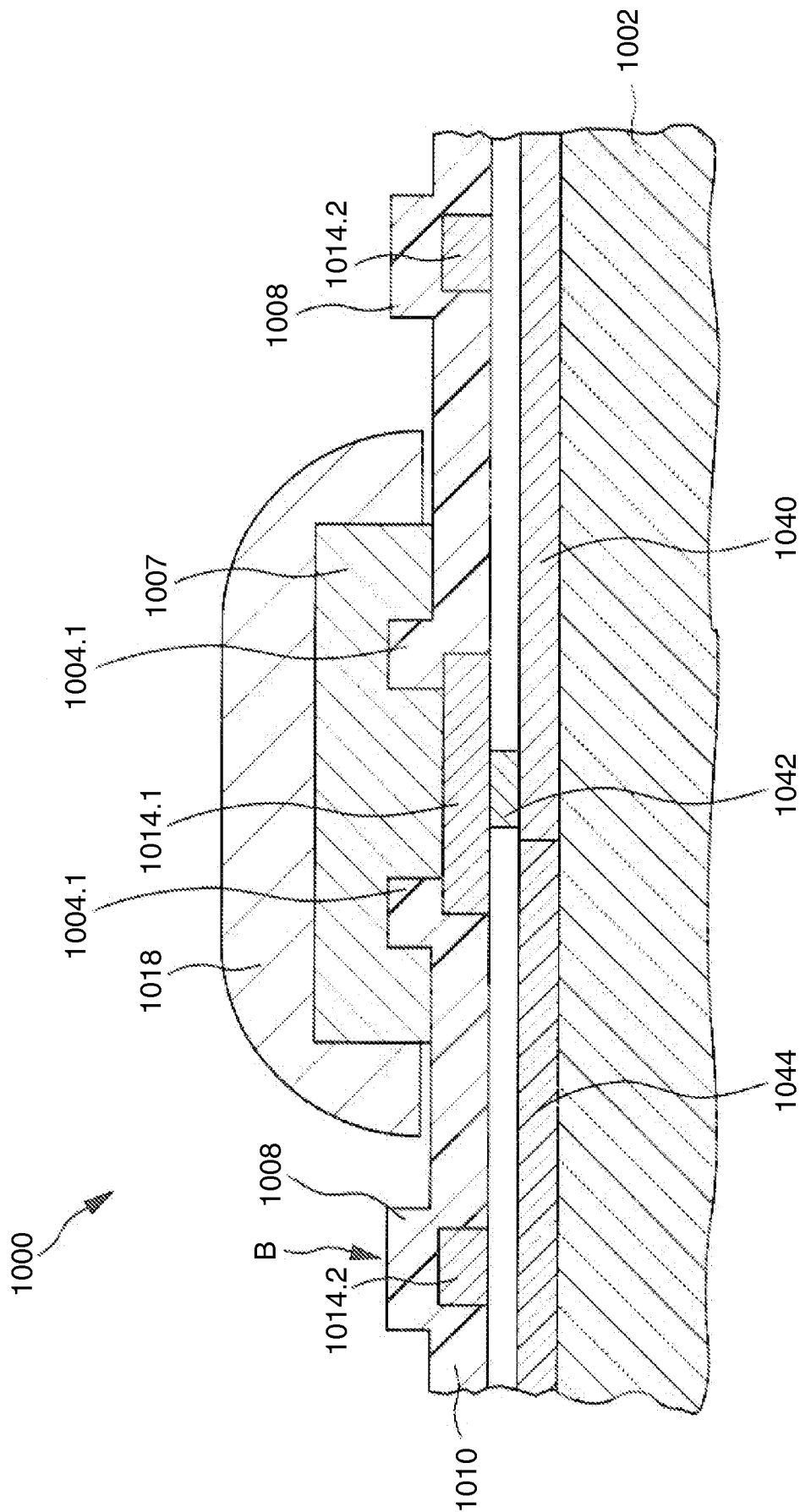


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/054009

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/60 H01L23/485 H01L25/065

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 408 543 A2 (FUJITSU LTD [JP]) 14 April 2004 (2004-04-14) paragraphs [0024] - [0031], [0 95], [0 96]; figures 2-6, 36-38	1,4,6,9, 13-15
X	EP 0 997 935 A1 (IBIDEN CO LTD [JP]) 3 May 2000 (2000-05-03) figures 1-4, 8	1,2,9, 13-15
X	EP 1 544 916 A1 (SAMSUNG ELECTRONICS CO LTD [KR]) 22 June 2005 (2005-06-22) paragraphs [0022] - [0036]; figures 2-4	1-3,9, 10,12-15
X	JP 10 294554 A (JAPAN AVIATION ELECTRON) 4 November 1998 (1998-11-04) abstract paragraph [0005] figures 1, 2	1-3,6,9, 10,12-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

* & * document member of the same patent family

Date of the actual completion of the international search

9 November 2009

Date of mailing of the international search report

03/02/2010

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Fax: (+31-70) 340-3016

Authorized officer

Crampin, Nicola

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2009/054009

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-4, 6, 9-10, 12-15

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-4, 6, 9-10, 12-15

Electric component with a substrate and an under-bump metallisation surrounded by a confinement structure for confining the flow of liquid from the under-bump metallisation, wherein the confinement structure is a recess extending around the under-bump metallisation

2. claim: 5

Electric component with a substrate and a plurality of under-bump metallisations surrounded by a confinement structure for confining the flow of liquid from the under-bump metallisation, wherein the under-bump metallisations have a lateral pitch of less than 300 micrometers

3. claims: 7, 11

Electric component with a substrate and an under-bump metallisation surrounded by a confinement structure for confining the flow of liquid from the under-bump metallisation, comprising a through-substrate via extending from a first substrate side including an electronic circuit element to connect with the under-bump metallisation on the second substrate side

4. claim: 8

Electric component with a substrate and an under-bump metallisation surrounded by a confinement structure for confining the flow of liquid from the under-bump metallisation, wherein the under-bump metallisation is arranged in a recess

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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