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(54) Title: METHODS OF ETCHING TRENCHES INTO SILICON OF A SEMICONDUCTOR SUBTRATE, METHODS OF FORMING TRENCH ISOLATION IN SILICON OF A SEMICONDUCTOR SUBSTRATE, AND METHODS OF FORMING A PLURALITY OF DIODES

(57) Abstract: A method of etching trenches into silicon of a semiconductor substrate includes forming a mask over silicon of a semiconductor substrate, with the mask comprising trenches formed there-through. Plasma etching is conducted to form trenches into the silicon of the semiconductor substrate using the mask. In one embodiment, the plasma etching includes forming an etching plasma using precursor gases which include SF_6, an oxygen-containing compound, and a nitrogen-containing compound. In one embodiment, the plasma etching includes an etching plasma which includes a sulfur-containing component, an oxygen- containing component, and NF_x.

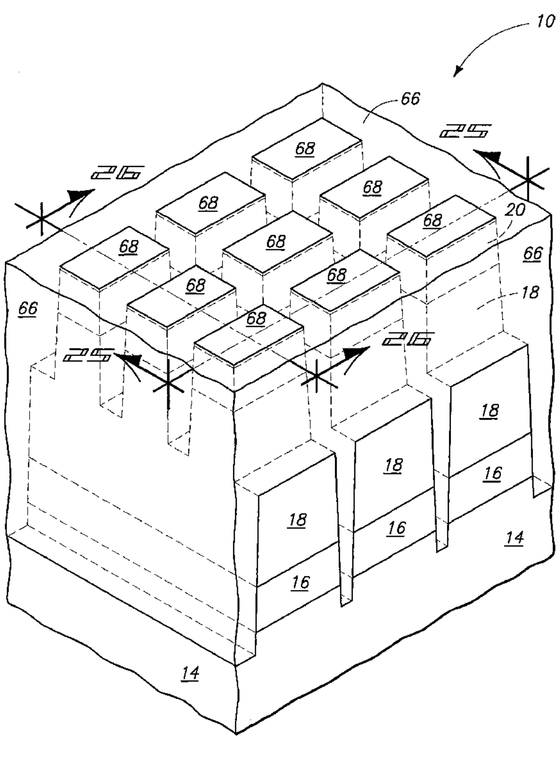

Fig 24

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DESCRIPTION

METHODS OF ETCHING TRENCHES INTO SILICON OF A SEMICONDUCTOR SUBSTRATE, METHODS OF FORMING TRENCH ISOLATION IN SILICON OF A SEMICONDUCTOR SUBSTRATE, AND METHODS OF FORMING A PLURALITY OF DIODES

TECHNICAL FIELD

Embodiments disclosed herein pertain to methods of etching trenches into silicon of a semiconductor substrate, to methods of forming trench isolation in silicon of a semiconductor substrate, and to methods of forming a plurality of diodes.

BACKGROUND

In the fabrication of integrated circuitry, numerous devices are packed into a small area of a semiconductor substrate to create an integrated circuit. Many of the individual devices are electrically isolated from one another. Accordingly, electrical isolation is an integral part of semiconductor device design for preventing unwanted electrical coupling between adjacent components and devices.

As the size of integrated circuits is reduced, the devices that make up the circuits are positioned closer together. Conventional methods of isolating circuit components include trench isolation. Such occurs by etching trenches into a semiconductor substrate and filling the trenches with insulative material. As the density of components on the semiconductor substrate has increased, the widths of the trenches have decreased. Further, the depths of the trenches have tended to increase. One type of semiconductor substrate material within which isolation trenches are formed is crystalline silicon, and which may include other materials such as germanium and/or conductivity modifying dopants. A need remains for developing improved etching chemistries which enable trenches to be etched into silicon, for example in the fabrication of trench isolation.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic isometric view of a portion of a semiconductor substrate in process in accordance with an embodiment of the invention.

Fig. 2 is a sectional view of the Fig. 1 substrate taken through line 2-2 in Fig. 1.

Fig. 3 is a view of the Fig. 2 substrate at a processing subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 3 substrate at a processing subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 substrate at a processing subsequent to that shown by Fig. 4.

Fig. 6 is a sectional view of the Fig. 5 substrate taken through line 5-5 in Fig. 5.

Fig. 7 is a sectional view of the Fig. 5 substrate taken through line 7-7 in Fig. 5.

Fig. 8 is a view of the Fig. 5 substrate at a processing subsequent to that shown by Fig. 5.

Fig. 9 is a sectional view of the Fig. 8 substrate taken through line 9-9 in Fig. 8.

Fig. 10 is a sectional view of the Fig. 5 substrate taken through line 10-10 in Fig. 8.

Fig. 11 is a view of the Fig. 8 substrate at a processing subsequent to that shown by Fig. 8.

Fig. 12 is a sectional view of the Fig. 11 substrate taken through line 12-12 in Fig. 11.

Fig. 13 is a sectional view of the Fig. 11 substrate taken through line 13-13 in Fig. 11.

Fig. 14 is a view of the Fig. 11 substrate at a processing subsequent to that shown by Fig. 11.

Fig. 15 is a sectional view of the Fig. 14 substrate taken through line 15-15 in Fig. 14.

Fig. 16 is a sectional view of the Fig. 14 substrate taken through line 16-16 in Fig. 14.

Fig. 17 is a view of the Fig. 14 substrate at a processing subsequent to that shown by Fig. 14.

Fig. 18 is a sectional view of the Fig. 17 substrate taken through line 18-18 in Fig. 17.

Fig. 19 is a sectional view of the Fig. 17 substrate taken through line 19-19 in Fig. 17.

Fig. 20 is a view of the Fig. 19 substrate at a processing subsequent to that shown by Fig. 19.

Fig. 21 is a view of the Fig. 17 substrate at a processing subsequent to that shown by Fig. 20.

Fig. 22 is a sectional view of the Fig. 21 substrate taken through line 22-22 in Fig. 21.

Fig. 23 is a sectional view of the Fig. 21 substrate taken through line 23-23 in Fig. 21.

Fig. 24 is a view of the Fig. 21 substrate at a processing subsequent to that shown by Fig. 21.

Fig. 25 is a sectional view of the Fig. 25 substrate taken through line 25-25 in Fig. 24.

Fig. 26 is a sectional view of the Fig. 25 substrate taken through line 26-26 in Fig. 24.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Embodiments of the invention include methods of etching trenches into silicon of the semiconductor substrate, and also methods of forming trench isolation in silicon of the semiconductor substrate. Further, embodiments of the invention also include methods of forming a plurality of diodes.

Referring initially to Figs. 1 and 2, a semiconductor substrate is indicated generally with reference numeral 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Substrate 10 is depicted as comprising a bulk semiconductor substrate, for example comprising monocrystalline silicon 12, although other silicon-comprising substrates such as semiconductor-on-insulator and other substrates might be used. Material 12 may include other materials, for example germanium and/or conductivity modifying dopants. In one embodiment, bulk silicon material 12 comprises a p-type bulk region 14 that is doped to any suitable p- level doping. Thereabove are sequentially depicted an n-type doped n+ region 16, an n-type n- doped region 18, and a p-type p+ doped region 20. Alternate silicon-containing substrates are also of course contemplated.

A series of masking layers is received above silicon material 20. Such includes a pad oxide layer 22, a silicon nitride or polysilicon layer 24, a hardmasking layer 26, an antireflective coating layer 28, and a patterned photoresist layer 30. Any of such layers are optional, and may comprise multiple different materials and/or layers with respect to each. Such materials may or may not be ultimately sacrificial. In certain embodiments, hardmask layer 26 may be any of insulative, semiconductive, or conductive. Example insulative materials for hardmask layer 26 include silicon dioxide, whether doped or undoped, as well as silicon nitride. Example conductive materials for hardmask layer 26 include any one or combination of refractory metal nitrides (i.e., TiN, WN, etc.), refractory metal silicides (WSi_x, TiS_x, etc.), or any metal in elemental form (Ti, W, etc.). Photoresist 30 is depicted as having been patterned to form trenches 32 to antireflective coating layer 28.

Referring to Fig. 3, photoresist 30 (not shown) and antireflective coating layer 28 (not shown) have been used as a mask to etch through hardmask layer 26, with photoresist layer 30 and antireflective coating 28 being removed at least in part by such etching and/or subsequently. An example anisotropic dry etching chemistry for conducting the same includes SO_2 + O_2 or O_2+HBr, or O_2 + N_2 for the photoresist, and for the antireflective coating generally one or more fluorocarbons, for example CF_4,+ HBr + He.

Referring to Fig. 4, patterned hardmask layer 26 has been used as a mask for etching through layers 24 and 22, thereby extending trenches 32 ultimately to silicon 12. An example etching chemistry for etching through a silicon nitride layer 24 includes one or more fluorocarbon + SF6 + NF3, while an example etching chemistry for clearing pad oxide 22 thereafter includes one or more fluorocarbons, for example CF_4, CHF_3, CH_2F_2, etc. Fig. 4 thereby depicts, in but one example embodiment, the formation of a mask 35 over silicon of the semiconductor substrate, with mask 35 comprising trenches 32 formed there-through. Such mask may or may not include a hardmask layer, and in but one example can be considered as a first mask comprising first trenches 32 formed there-through which run in a first major direction over substrate 10. The example first major direction in the depiction of Fig. 4 would be perpendicularly into and out of the plane of the page upon which Fig. 4 lies. Of course, first trenches 32 might not be entirely straight in such direction and might, by way of example only, serpentine relative to each other but nevertheless, in one embodiment, run in a first major direction over the substrate as just described.

Referring to Figs. 5, 6, and 7, trenches 32 have been extended relative to substrate 10 by plasma etching into silicon 12 thereof using mask 35. In one embodiment, the plasma etching comprises forming an etching plasma using precursor gases comprising SF_6, an oxygen-containing compound, and a nitrogen-containing compound. The oxygen-containing compound and the nitrogen-containing compound might comprise different compounds, and/or might comprise the same compound. For example in one embodiment, the oxygen-containing compound comprises O_2, and the nitrogen-containing compound comprises N_2. An example oxygen-containing compound and nitrogen-containing compound encompassed by the same compound includes NO_x, where "x" ranges from, for example, about 1 to 3.

Further of course, the precursor gases might comprise two oxygen-containing compounds, for example with one of the oxygen-containing compounds being void of nitrogen and another of the oxygen-containing compounds comprising nitrogen. For example in but one embodiment, the precursor gases might comprise SF_6, N_2, O_2, and NO_x. Alternately in such example, the precursor gases from which the plasma etching occurs might not include N_2. Further in one embodiment, the precursor gases might comprise, consist essentially of, or consist of SF_6, O_2, and N_2. Additional precursor gases might also of course be utilized, for example HBr. In one embodiment, the precursor gases from which the plasma etching is conducted might comprise more N_2 than each of SF_6 and O_2 where such three gases are used. In one embodiment, the mask used during the etch comprises an outermost hardmask layer during at least a latter portion of the plasma etching into the silicon, and in one embodiment such outer mask layer is void of carbon as the stated plasma etching chemistry may etch an outermost hardmask layer that comprises carbon.

The invention was reduced to practice using a LAM Kiyo plasma etching chamber. Regardless and by way of examples only, example pressure during etching may be from about 1 mTorr to about 50 mTorr, and an example temperature range for the susceptor upon which the substrate rests is from about 0°C to about 50°C. An example source power range is from about 100W to about 1,000W, and an example bias voltage is from about -20V to about -1,000V. Where, for example SF_6, O_2, N_2, and HBr are precursor gases, example flow rates include from about 1 sccm to about 100 sccm for SF_6; from about 10 sccm to about 500 sccm for O_2; from 0 sccm to about 500 sccm for HBr; and from about 1 sccm to about 500 sccm for N_2. A specific reduction-to-practice example in the LAM Kiyo plasma etching chamber included 5 mTorr, 7°C, -500V voltage bias, 400W source power, 350 sccm SF_6, 45 sccm O_2, 60 sccm N_2, and 20 sccm HBr. The particular plasma etcher used might be capable of operation such that either the bias voltage or the bias power can be the set point while the other is allowed to float. In one embodiment, bias voltage is set and bias power is allowed to float. In another embodiment, bias power is set and bias voltage is allowed to float.

It was determined that etching with SF_6 and O_2 without any nitrogen-containing compound may result in significant trench sidewall erosion, irregular trench sidewalls, and/or v-shaped trench bases. However, it was discovered that by adding a nitrogen-containing compound to the plasma etching chemistry, smoother and/or straighter trench sidewall resulted and with flatter trench bases, although the invention does not necessarily require achieving any of such results unless literally so claimed. Further, and without necessarily being limited by any theory of invention, presence of nitrogen in the plasma may be creating an NF_x species that may or may not be facilitating straighter sidewalls and flatter bases.

Regardless, one embodiment of the invention includes plasma etching trenches into silicon of a semiconductor substrate using a mask having trenches formed there-through, wherein the plasma etching comprises an etching plasma comprising a sulfur-containing component, an oxygen-containing component, and NF_x. In one embodiment, the sulfur-containing component is formed from a precursor gas comprising SF_6. In one embodiment, the oxygen of the oxygen-containing component may be formed from a precursor gas comprising O_2, and the nitrogen of the NF_x may be formed from a precursor gas compound which is void of oxygen. Further in one embodiment, the oxygen of the oxygen-containing component and the nitrogen of the NF_x may be formed from a precursor gas comprising NO_x. Further, example precursor gases include any of those described above, including any combinations thereof.

Example etch depths for trenches 32 within silicon 12 are from about 7,500 Angstroms to about 20,000 Angstroms, with 9,000 Angstroms being but one specific example.

Referring to Figs. 8, 9, and 10, masking layers 40 have been formed over substrate 10 and accordingly over first trenches 32 within silicon of the substrate. In one embodiment, masking layers 40 comprise multi-layer resist, with three such example layers being sequentially shown as comprising a first layer 42, a layer 44 thereover, and another layer 45. In one example, layer 42 is in the form of a liquid resin which deposits to completely fill first trenches 32 and be received over hardmask layer 26 of first mask 35, and thereafter is solidified. An example layer 44 is any silicon-containing hardmask, with an example layer 45 thereover comprising a photoimageable material such as photoresist.

Referring to Figs. 11, 12, and 13, photoimageable layer 45 has been patterned to form second trenches 50 which run in a second major direction over substrate 10 which is orthogonal to the first major direction. The example second major direction in Fig. 13 would be perpendicularly into and out of the plane of the page upon which Fig. 13 lies, and in the direction which arrows 13 point in Fig 11. Further, the first major direction as described above would be in the direction which arrows 12 point in Fig. 11. Of course, second trenches 50 might not be entirely straight in such second major direction and might, by way of example only, serpentine relative to each other but nevertheless, in one embodiment, run in a second major direction over the substrate as just described.

Referring to Figs. 14, 15, and 16, patterned photoimageable material 45 (not shown) has been used as a mask to etch silicon-containing hardmask layer 44, resin 42, and hardmask layer 26 of first mask 35 to extend second trenches 50 through hardmask layer 26 to silicon nitride layer 24, with photoimageable material 45 being removed during such etching and/or subsequently.

Referring to Figs. 17, 18, and 19, etching has been conducted to extend trenches 50 through silicon nitride layer 24 and pad oxide layer 22 to silicon material 12. Accordingly, and in but one embodiment, second trenches 50 extend through hardmask layer 26 of first mask 35 and a second mask 55 is formed over the first trenches and comprises hardmask layer 26 of the first mask.

Referring to Fig. 20, second trenches 50 have been extended into silicon 12 by plasma etching thereof using second mask 55. Some of material 42 (not shown or viewable in Fig. 20) may remain from the processing depicted by Figs. 14, 15, and 16 (not shown), or another material provided, at the bases of first trenches 32 (not shown or viewable in Fig. 20) to preclude portions of such first trenches to be etched deeper while etching second trenches 50. In one embodiment, the plasma etching of the second trenches into the silicon comprises forming an etching plasma using precursor gases comprising SF_6, an oxygen-containing compound, and a nitrogen-containing compound. Any of the above-described processing might be utilized. Further, the plasma etching to form the second trenches within the silicon might be the same as or different from the plasma etching to form the first trenches within the silicon material. Further and regardless, the plasma etching to form the second trenches might comprise an etching plasma comprising a sulfur-containing component, an oxygen-containing component, and NF_x, for example as also described above. Regardless and by way of example only, example depths of trenches 50 within silicon material 12 are from about 2,500 Angstroms to about 3,500 Angstroms, with about 3,000 Angstroms being a specific example.

Some or all of such materials 22, 24, 26, 42, and 44 may or may not be ultimately removed from the substrate. Figs. 21, 22, and 23, by way of example only, depict all of such materials having been removed and, regardless, the plasma etching of the second trenches resulting in the formation of spaced silicon-comprising mesas 65.

Embodiments of the invention include methods of forming trench isolation within silicon of a semiconductor substrate, and may or may not comprise formation of spaced silicon-comprising mesas. For example and by way of example only, the above-described processing after Figs. 5-7, or otherwise, might include depositing insulative trench isolation material to within such trenches without necessarily forming the above example second trenches. Further and regardless of forming mesas, insulative trench isolation material might be deposited to within first and second trenches formed within silicon.

Regardless, embodiments of the invention also encompass methods of forming a plurality of diodes in conjunction with forming spaced silicon-comprising mesas. For example and by way of example only, Figs. 24, 25, and 26 depict subsequent processing whereby insulative material 66 has been deposited to be received about spaced silicon-comprising mesas 65 and a conductive silicide layer 68 has been formed over mesas 65. Example insulative materials 66 include one or a combination of silicon nitride and silicon dioxide, and a specific example conductive silicide material 68 includes cobalt silicide. Alternate and/or additional materials might of course be used. The Figs. 24-26 construction might be fabricated, by way of example only, by deposition of material 66 to overfill the trenches, planarization thereof, and patterning to expose the silicon-comprising mesas, followed by the subsequent salicidation of the exposed silicon material of the mesas.

Regardless, Figs. 24-26 depict formation of individual example diodes 75 on individual of the spaced silicon-comprising mesas 65. In one embodiment, the individual diodes comprise a p-type silicon-comprising region (i.e., region 20), and an n-type silicon-comprising region (i.e., regions 16, 18). In one embodiment, individual diodes comprise a silicon-comprising region (i.e., region 20) and a metal region (i.e., region 68). By way of example only, the diodes might be used in Programmable Conductive Random Access Memory (PCRAM) applications.

CLAIMS

1. A method of etching trenches into silicon of a semiconductor substrate, comprising:

forming a mask over silicon of a semiconductor substrate, the mask comprising trenches formed there-through; and

plasma etching trenches into the silicon of the semiconductor substrate using the mask, the plasma etching comprising forming an etching plasma using precursor gases comprising SF_6, an oxygen-containing compound, and a nitrogen-containing compound.

2. The method of claim 1 wherein the oxygen-containing compound and the nitrogen-containing compound comprise different compounds.

3. The method of claim 1 wherein the oxygen-containing compound and the nitrogen-containing compound comprise the same compound.

4. The method of claim 3 wherein the same compound comprises NO_x.

5. The method of claim 1 wherein the precursor gases comprise HBr.

6. The method of claim 1 wherein the mask comprises an outermost hardmask layer during at least a latter portion of the plasma etching into the silicon, said outermost hardmask layer being void of carbon.

7. The method of claim 1 wherein the nitrogen-comprising compound comprises N_2.

8. The method of claim 7 wherein the precursor gases comprise HBr.

9. The method of claim 1 wherein the precursor gases comprise two oxygen-containing compounds, one of the oxygen compounds being void of nitrogen, another of the oxygen-containing compounds comprising the nitrogen-containing compound.

10. The method of claim 9 wherein the one comprises O_2 and the another comprise NO_x.

11. A method of etching trenches into silicon of a semiconductor substrate, comprising:

forming a mask over silicon of a semiconductor substrate, the mask comprising trenches formed there-through; and

plasma etching trenches into the silicon of the semiconductor substrate using the mask, the plasma etching comprising an etching plasma comprising a sulfur-containing component, an oxygen-containing component, and NF_x.

12. The method of claim 11 the sulfur of the sulfur-containing component is formed from a precursor gas comprising SF_6.

13. The method of claim 11 wherein the oxygen of the oxygen-containing component is formed from a precursor gas comprising O_2, and the nitrogen of the NF_x is formed from a precursor gas compound which is void of oxygen.

14. The method of claim 11 wherein the oxygen of the oxygen-containing component and the nitrogen of the NF_x are formed from a precursor gas comprising NO_x.

15. A method of forming trench isolation in silicon of a semiconductor substrate, comprising:

forming a mask over silicon of a semiconductor substrate, the mask comprising trenches formed there-through;

plasma etching trenches into the silicon of the semiconductor substrate using the mask, the plasma etching comprising forming an etching plasma using precursor gases comprising SF_6, O_2, and N_2; and

depositing insulative trench isolation material to within the trenches.

16. The method of claim 15 wherein the precursor gases comprise HBr.

17. The method of claim 15 wherein the precursor gases comprises more N_2 than each of SF_6 and O_2.

18. The method of claim 15 wherein the forming of the etching plasma is from using precursor gases consisting essentially of SF_6, O_2, and N_2.

19. A method of forming trench isolation in silicon of a semiconductor substrate, comprising:

forming a first mask over silicon of a semiconductor substrate, the first mask comprising first trenches formed there-through running in a first major direction over the substrate, the first mask comprising a hardmask layer;

plasma etching first trenches into the silicon of the semiconductor substrate using the first mask, the plasma etching of the first trenches into the silicon comprising forming an etching plasma using precursor gases comprising SF_6, an oxygen-containing compound, and a nitrogen-containing compound;

forming a second mask over the first trenches, the second mask comprising second trenches formed there-through running in a second major direction over the substrate which is orthogonal to the first major direction, the second mask comprising the hardmask layer of the first mask;

plasma etching second trenches into the silicon of the semiconductor substrate using the second mask, the plasma etching of the second trenches into the silicon comprising forming an etching plasma using precursor gases comprising SF_6, an oxygen-containing compound, and a nitrogen-containing compound; and after plasma etching the second trenches, depositing insulative trench isolation material to within the first and second trenches in the silicon.

20. The method of claim 19 wherein the second mask is formed from multilayer resist received over the hardmask layer of the first mask.

21. The method of claim 19 wherein the hardmask layer of the first mask is insulative.

22. The method of claim 19 wherein the hardmask layer of the first mask is conductive.

23. The method of claim 22 wherein the conductive hardmask layer of the first mask comprises at least one of a refractory metal nitride, a refractory metal silicide, or a metal in elemental-form.

24. A method of forming a plurality of diodes, comprising:

forming a first mask over silicon of a semiconductor substrate, the first mask comprising first trenches formed there-through running in a first major direction over the substrate, the first mask comprising a hardmask layer;

plasma etching first trenches into the silicon of the semiconductor substrate using the first mask, the plasma etching of the first trenches into the silicon comprising forming an etching plasma using precursor gases comprising SF_6, an oxygen-containing compound, and a nitrogen-containing compound;

forming a second mask over the first trenches, the second mask comprising second trenches formed there-through running in a second major direction over the substrate which is orthogonal to the first major direction, the second mask comprising the hardmask layer of the first mask, the second trenches extending through the hardmask layer of the first mask;

plasma etching second trenches into the silicon of the semiconductor substrate using the second mask, the plasma etching of the second trenches into the silicon comprising forming an etching plasma using precursor gases comprising SF_6, an oxygen-containing compound, and a nitrogen-containing compound, the plasma etching of the second trenches into the silicon forming spaced silicon-comprising mesas; and

providing individual diodes on individual of the mesas and depositing insulative material to be received about the spaced silicon-comprising mesas.

25. The method of claim 24 wherein the individual diodes comprise a p-type silicon-comprising region and an n-type silicon-comprising region.

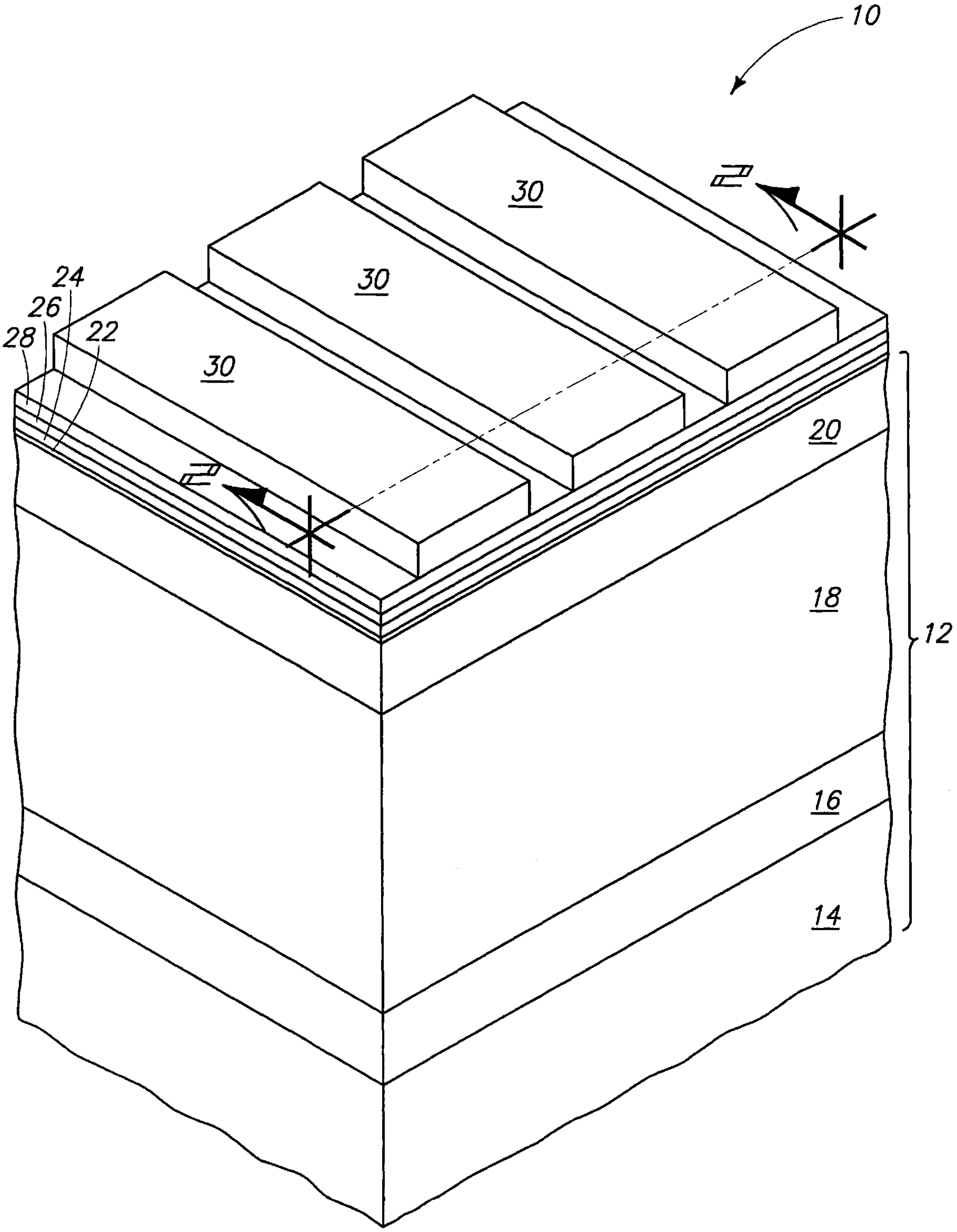

Fig 1

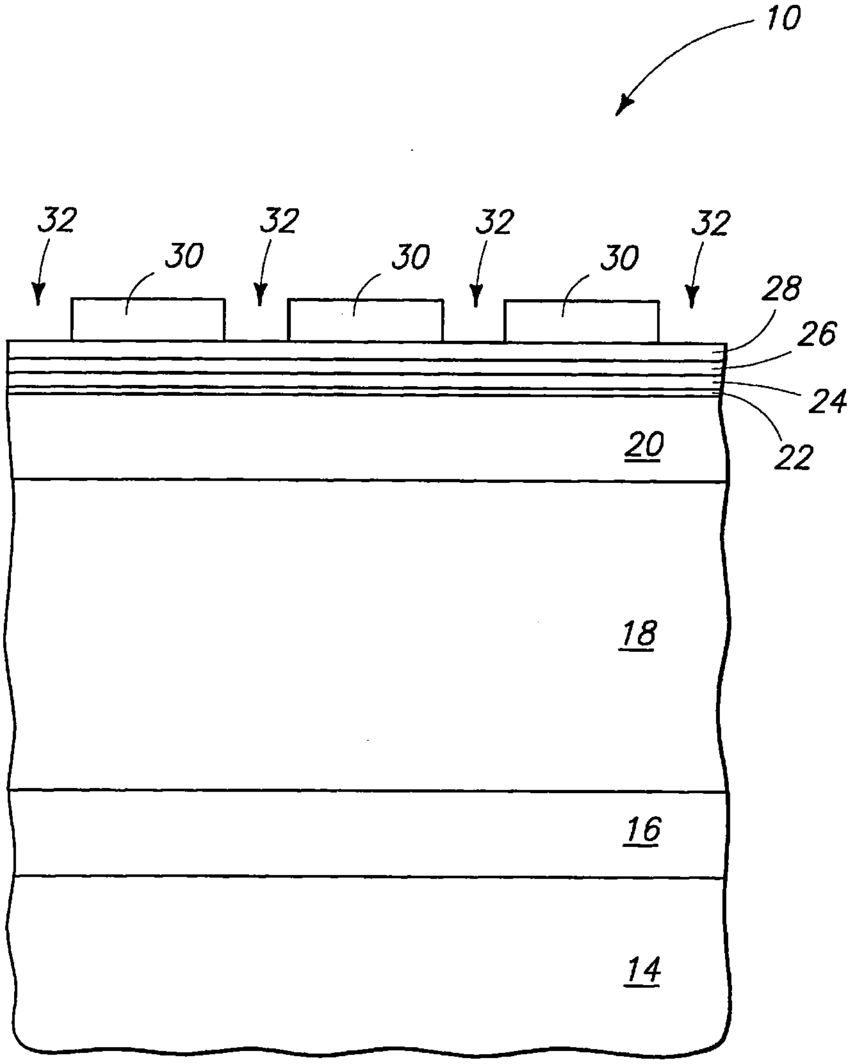

Fig 2

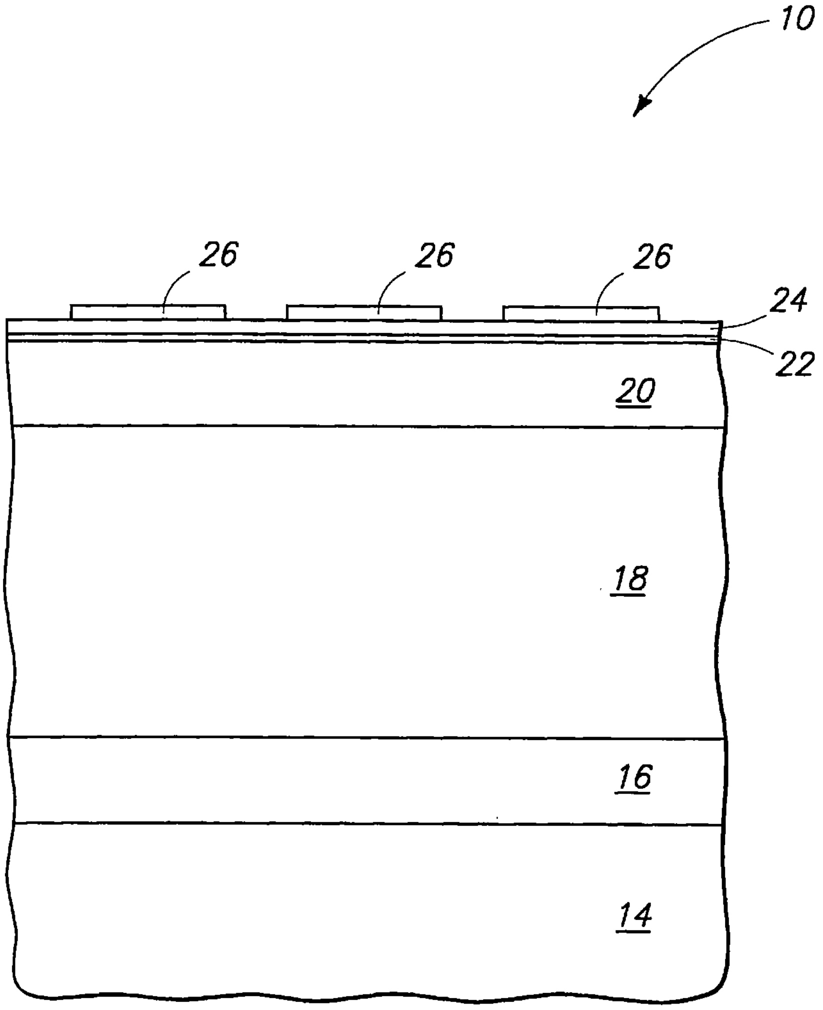

FIG 3

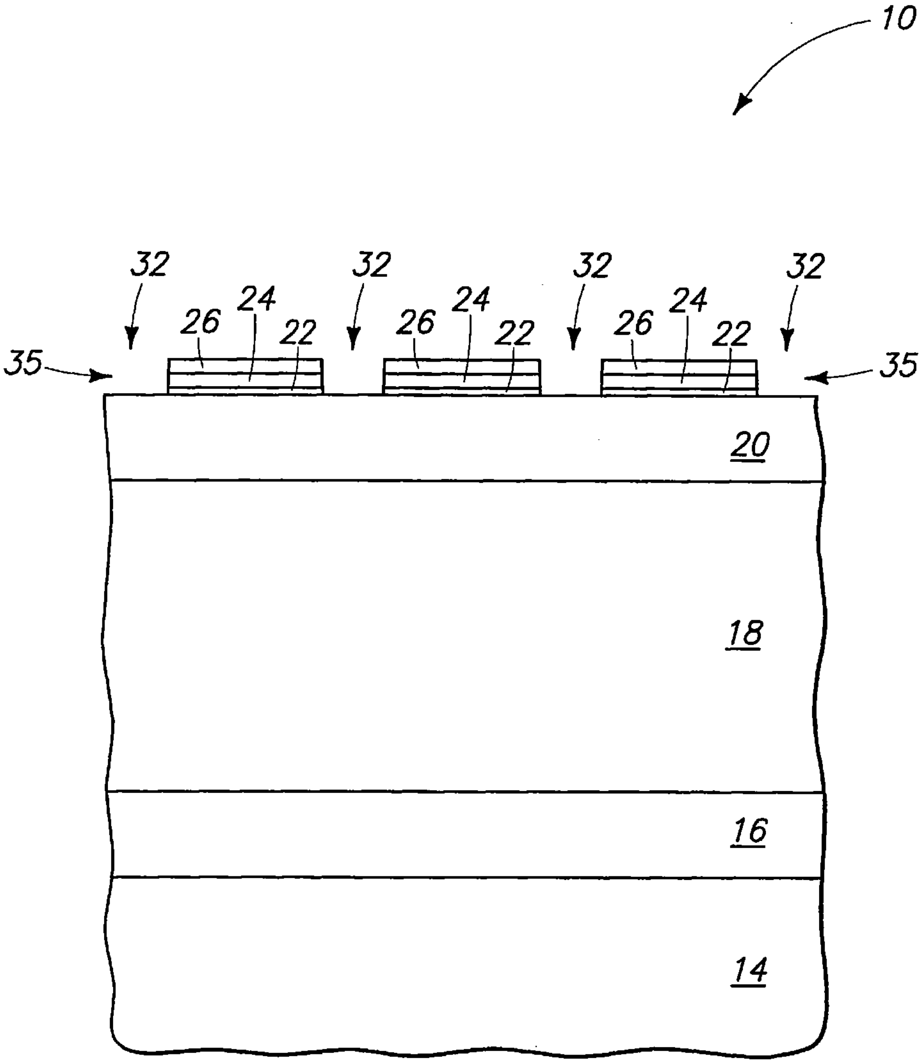

Fig 4

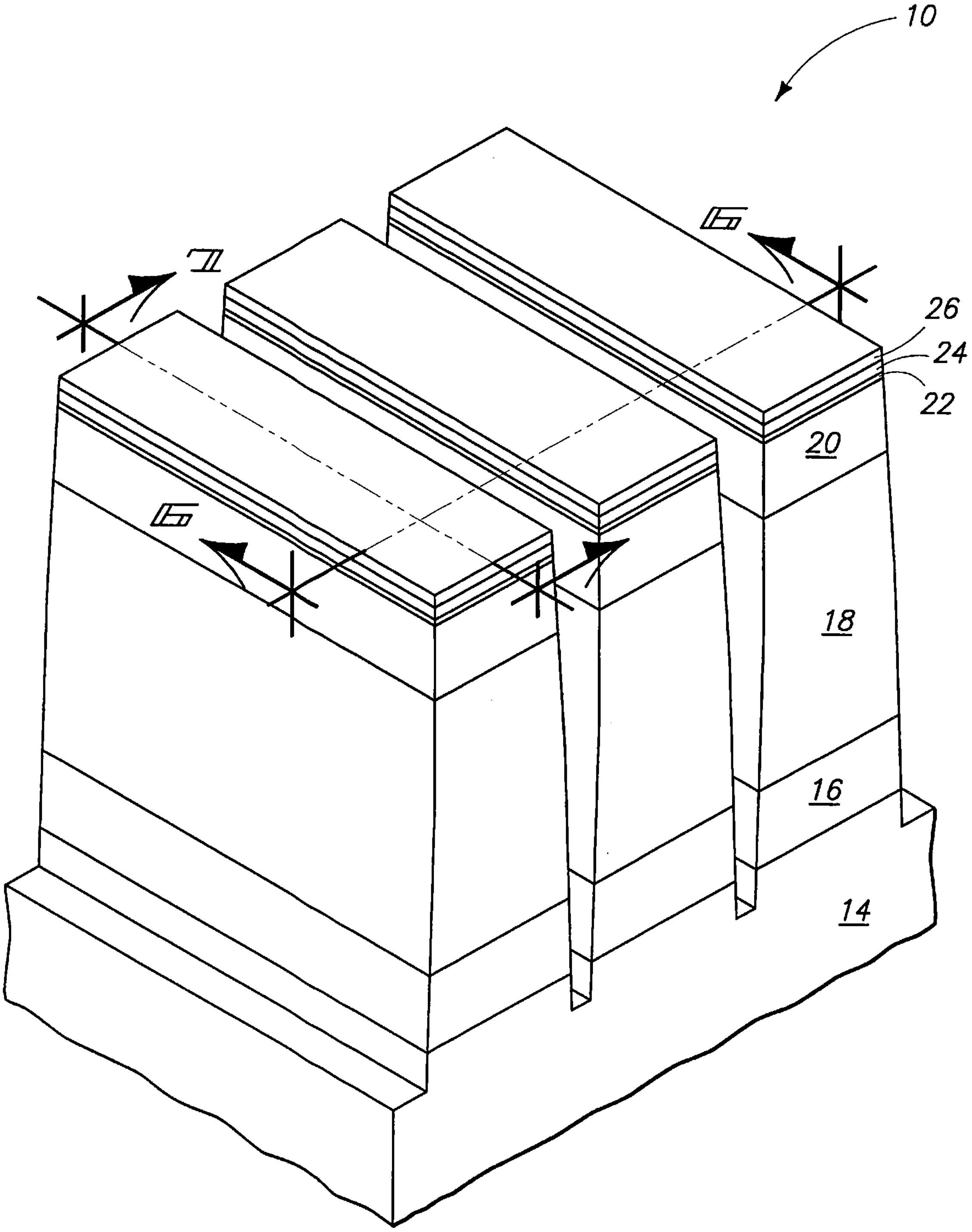

Fig 5

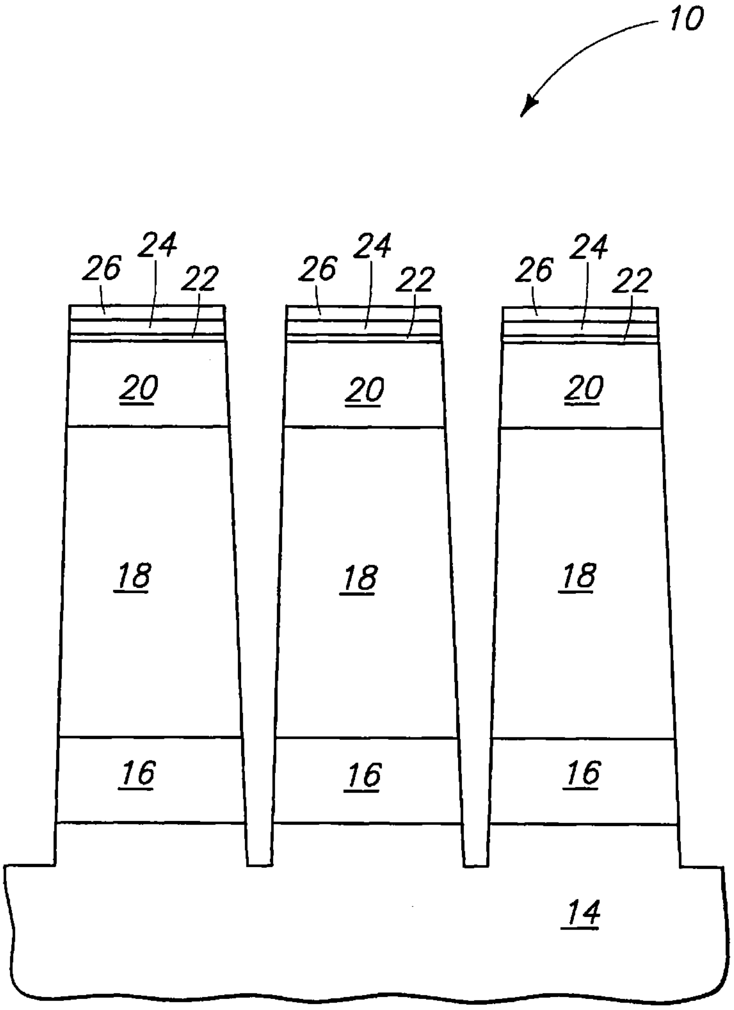

Fig 6

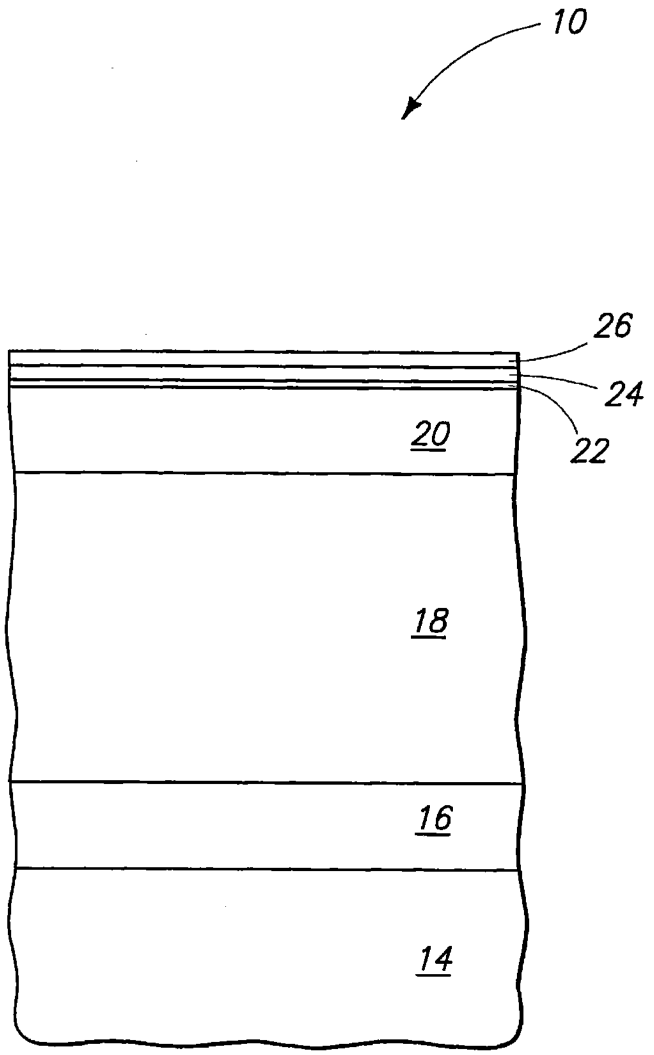

Fig 7

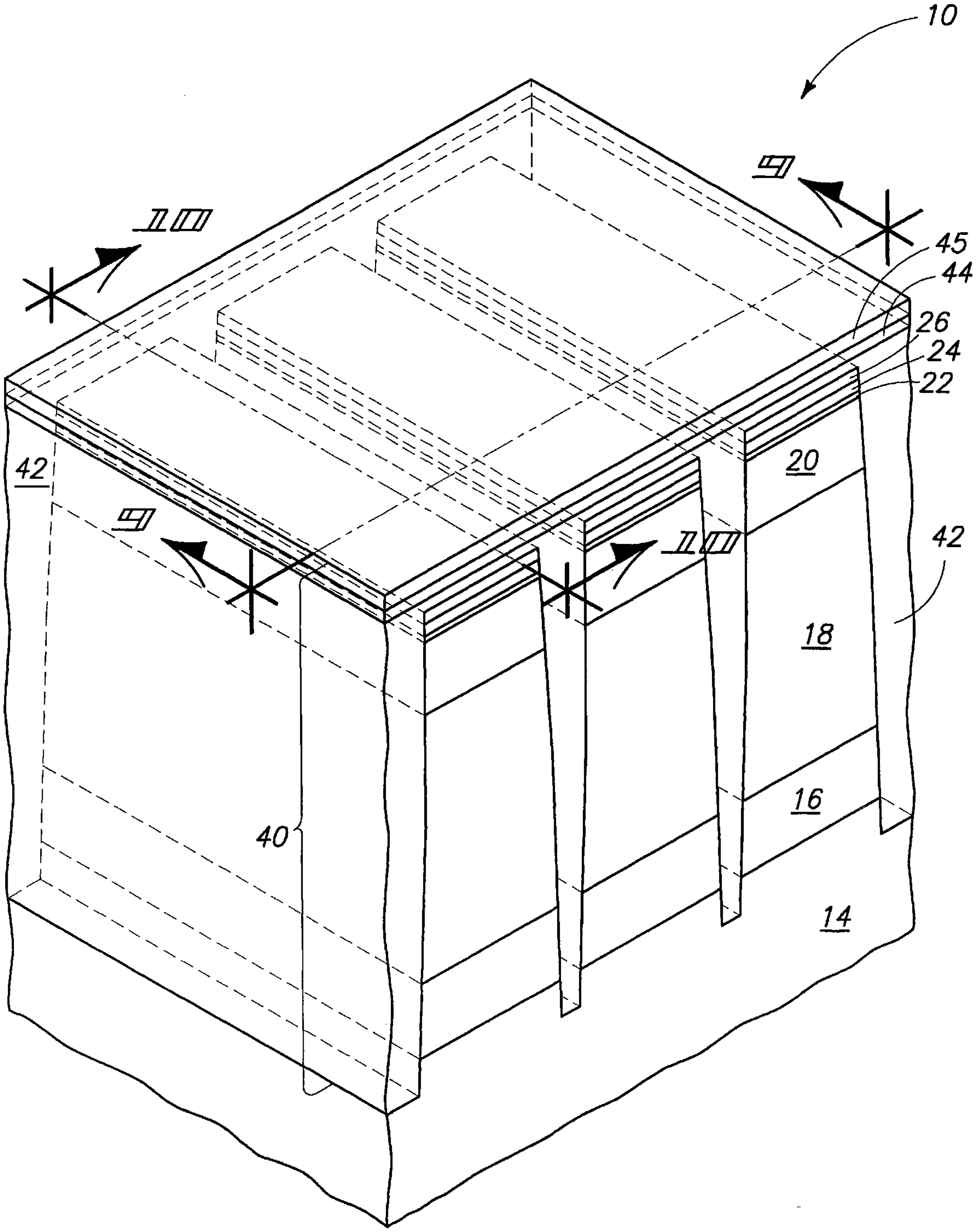

FIG 8

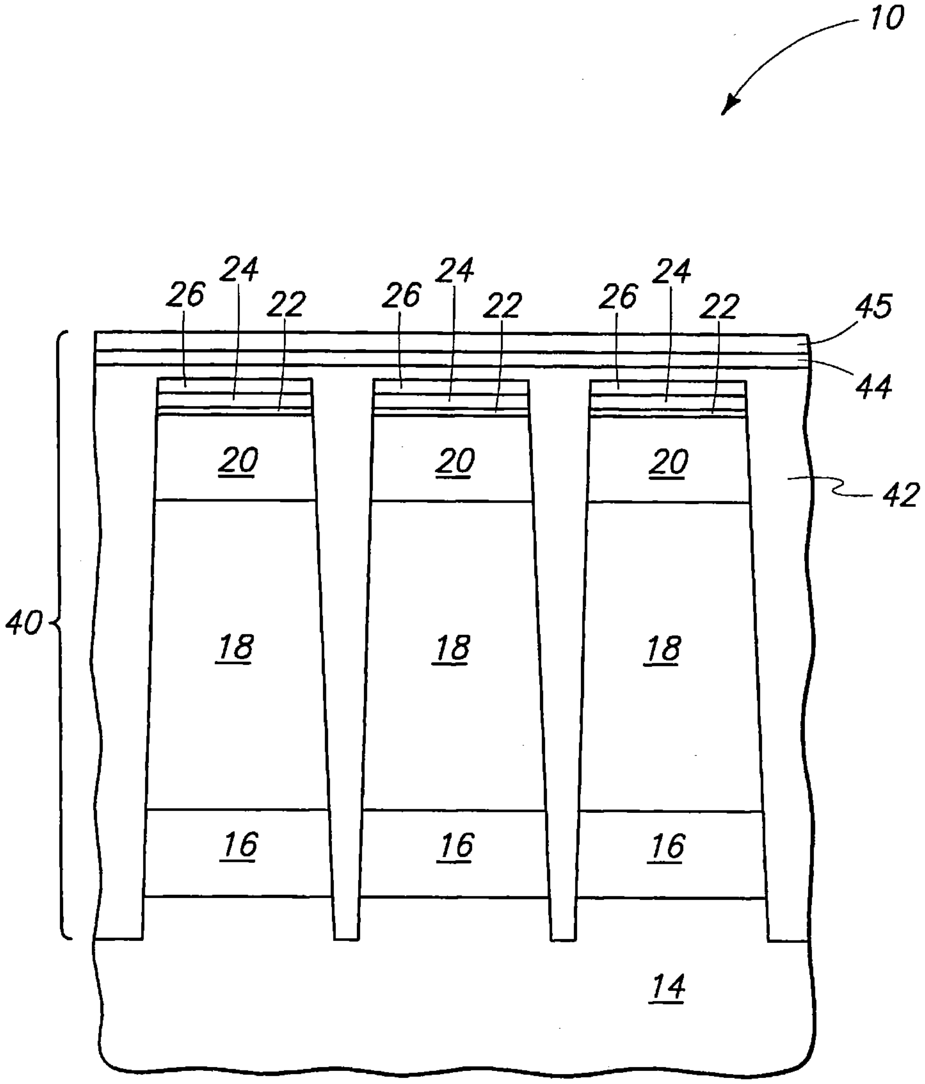

Fig 9

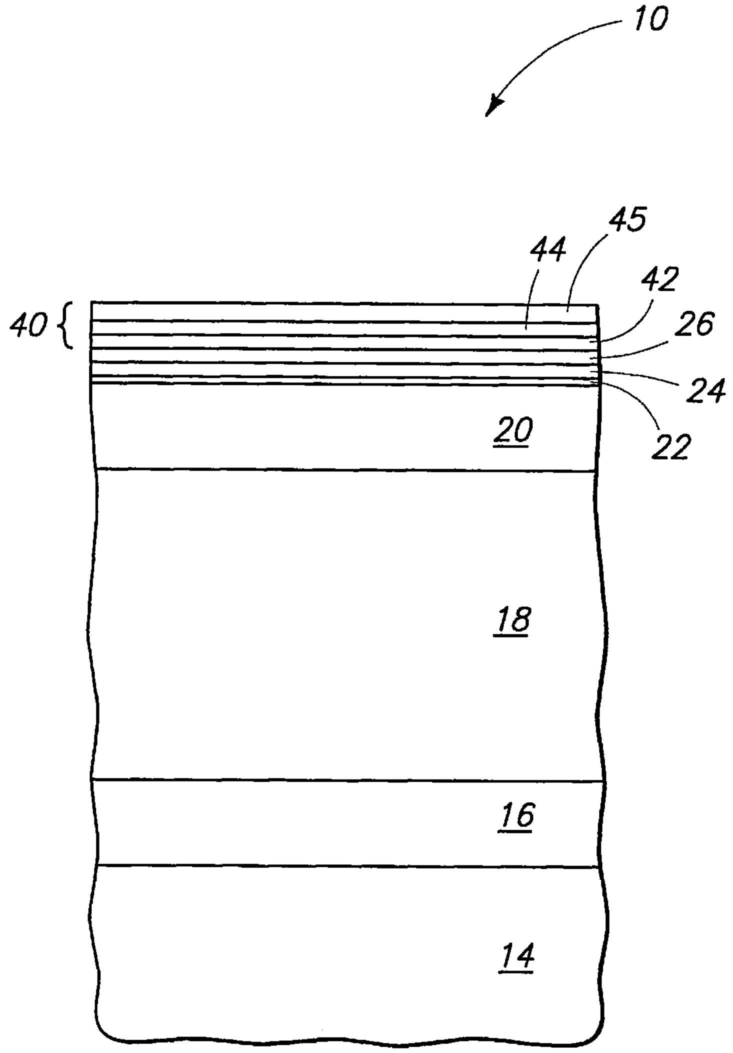

Fig 10

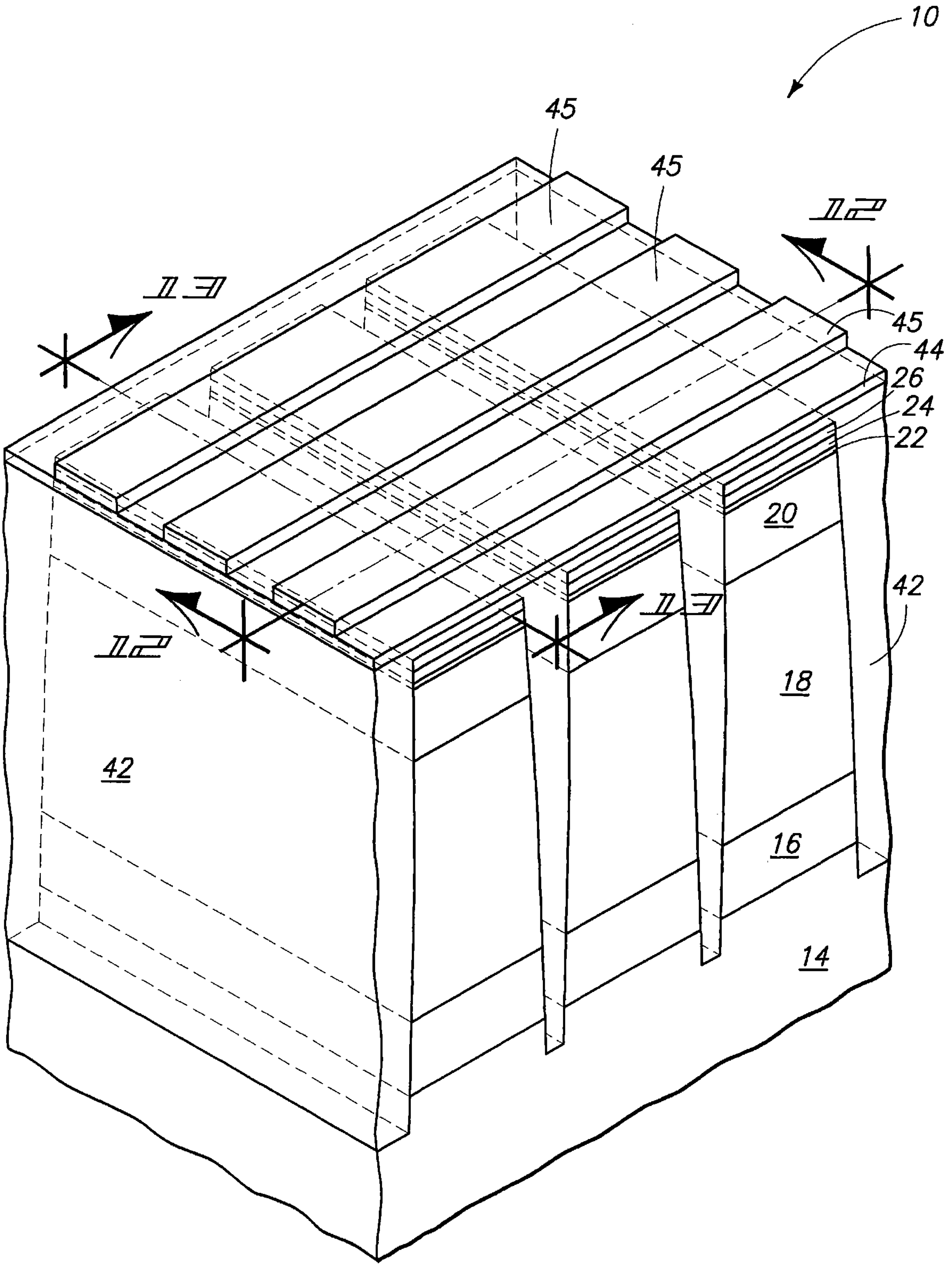

Fig 11

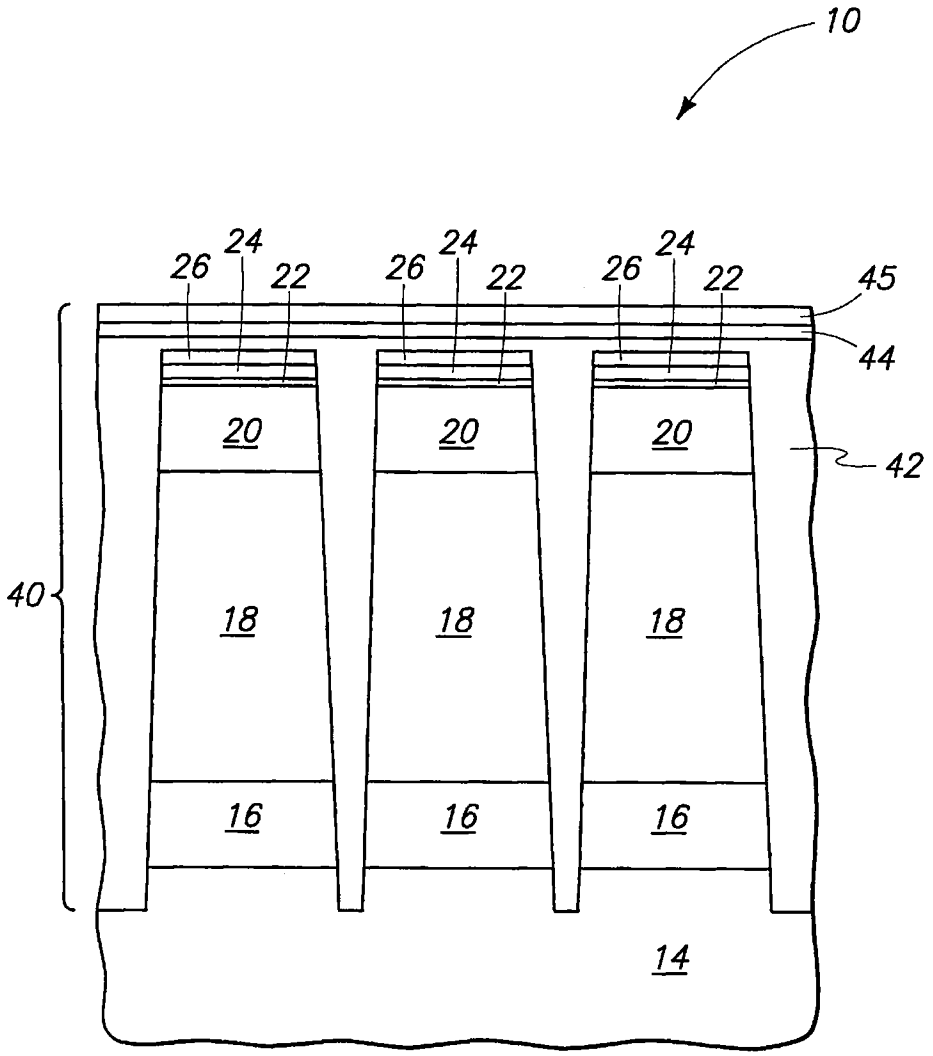

Fig 12

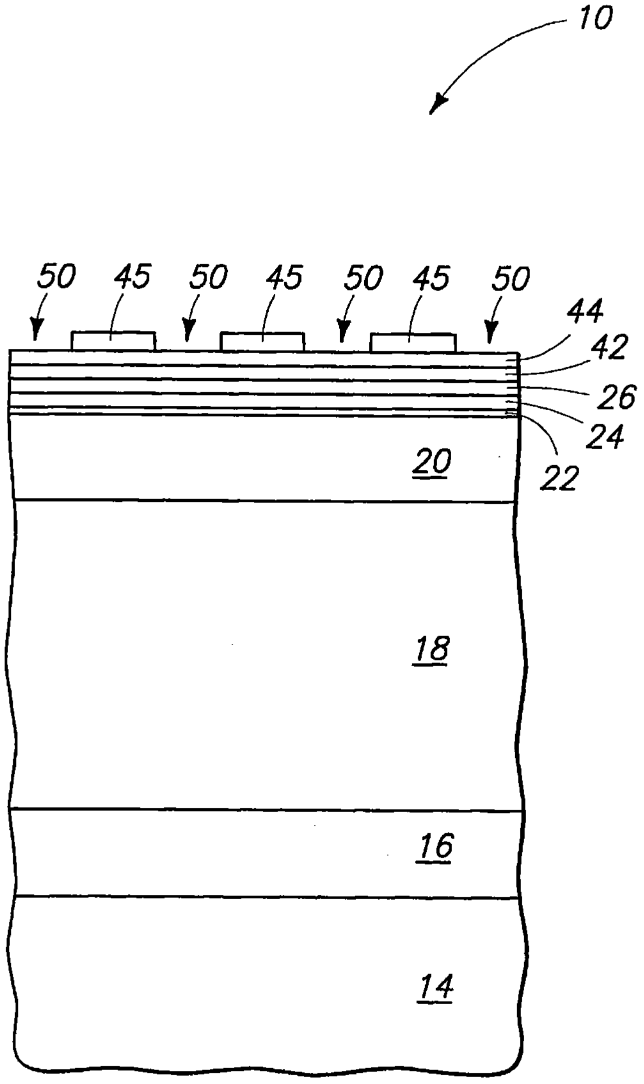

Fig 13

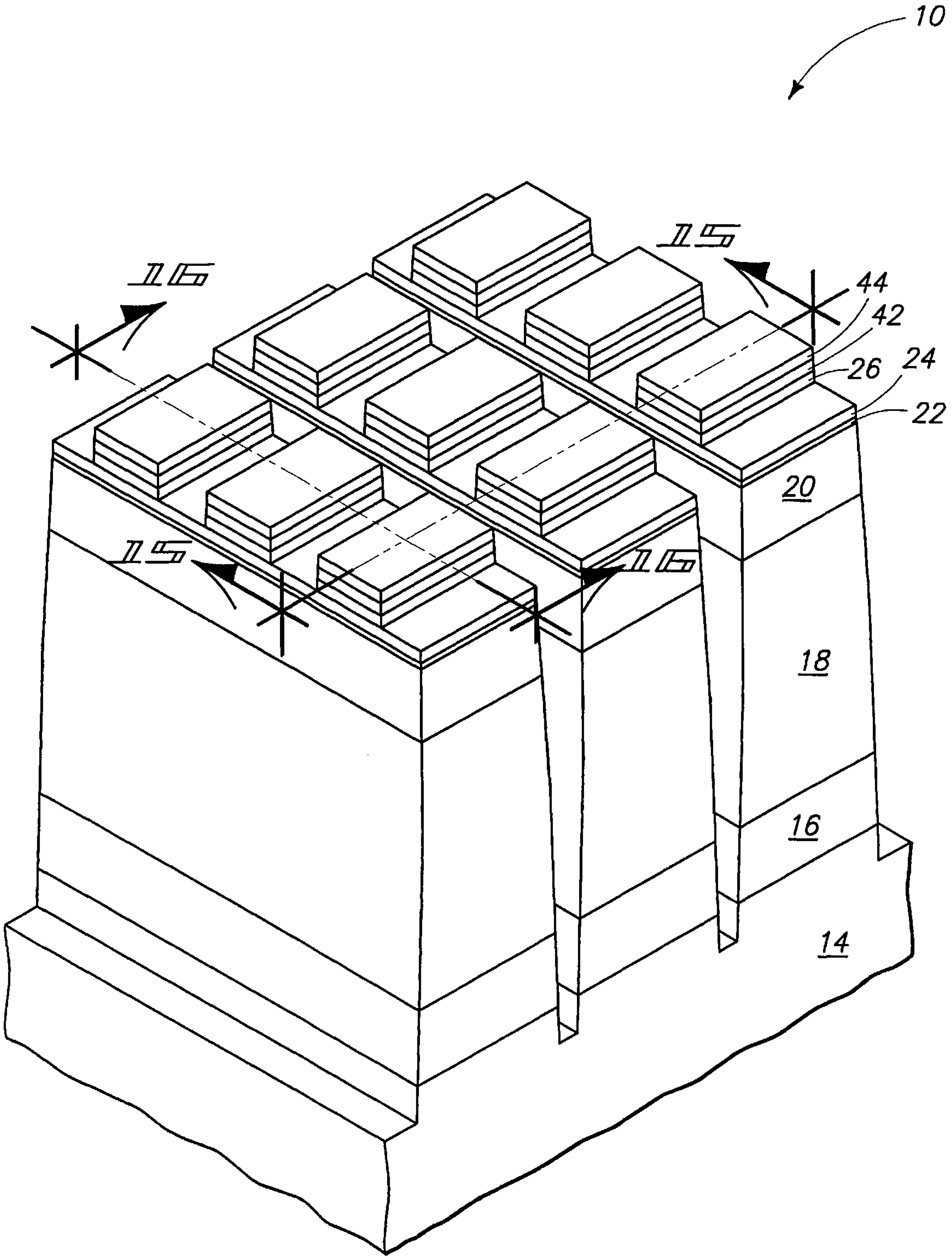

Fig 14

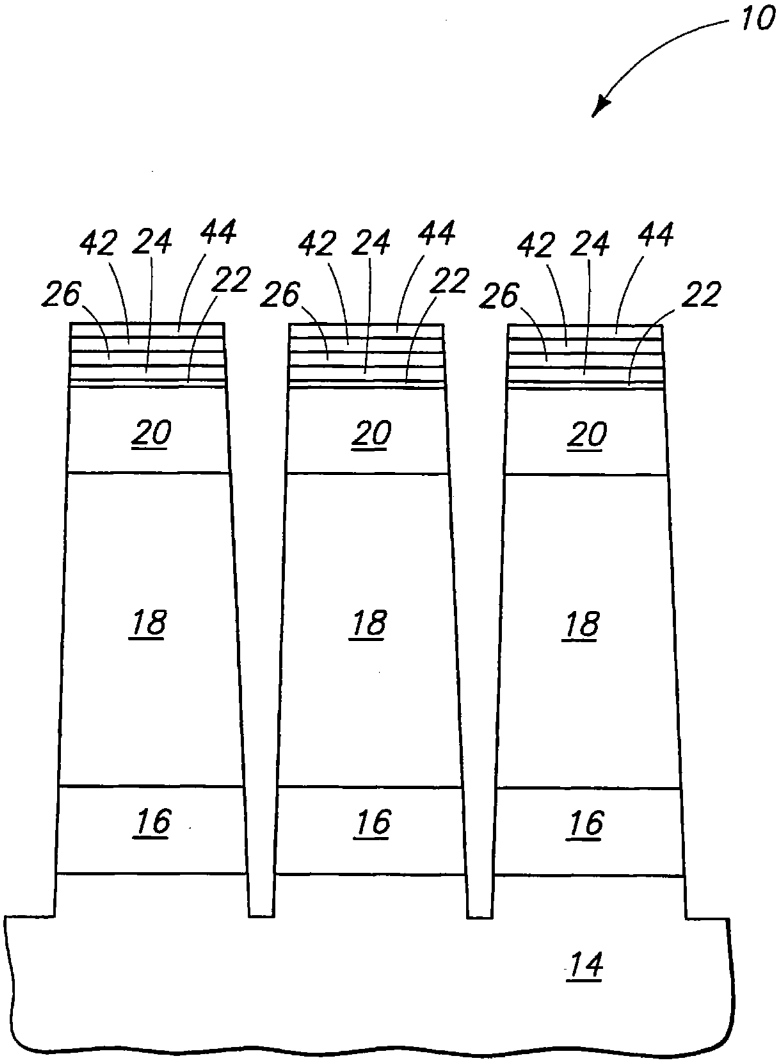
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Fig 15

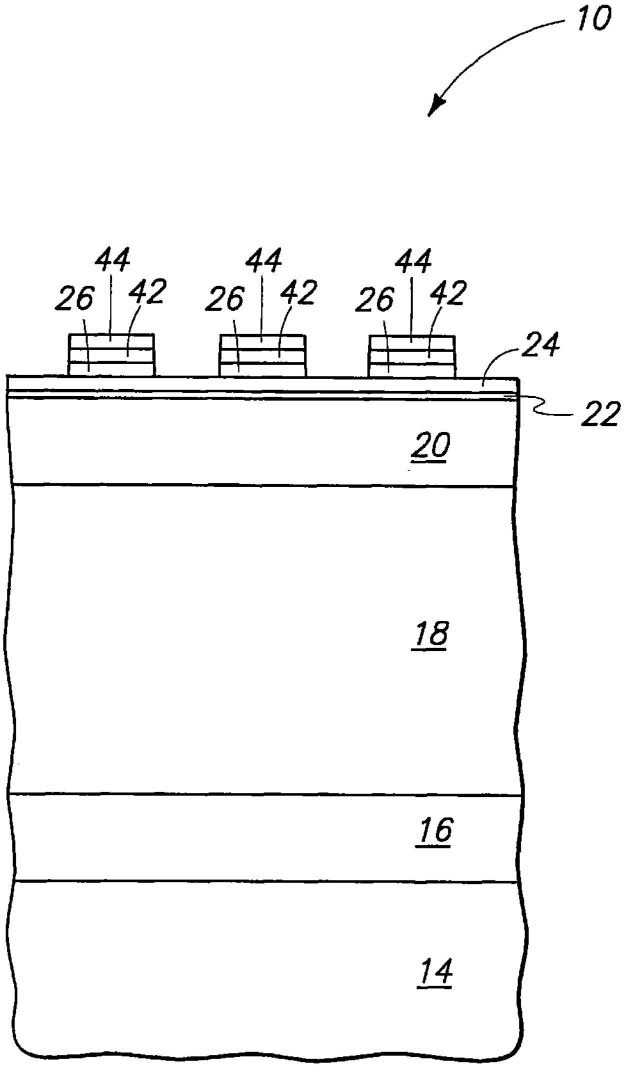

Fig 16

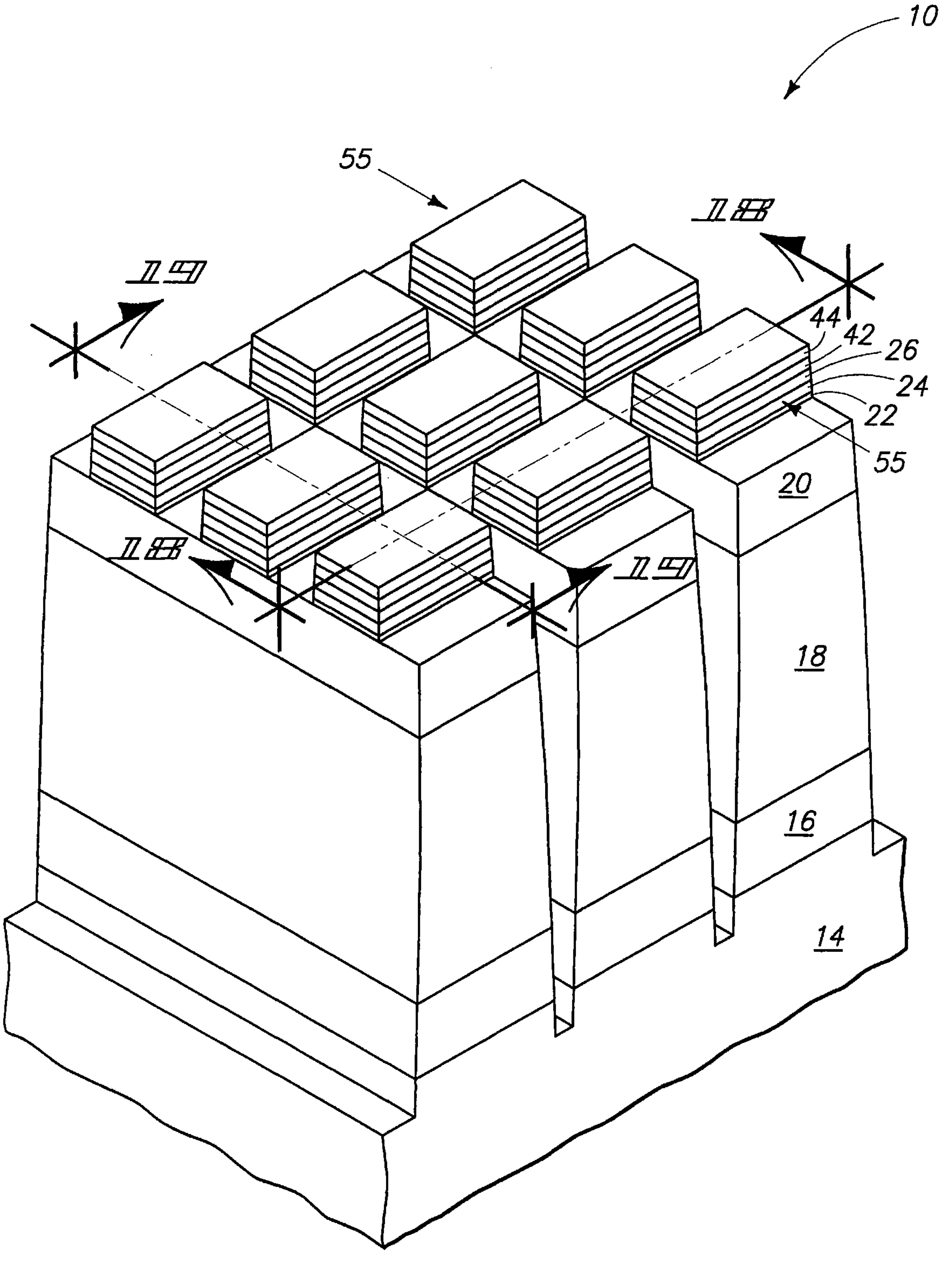

Fig 17

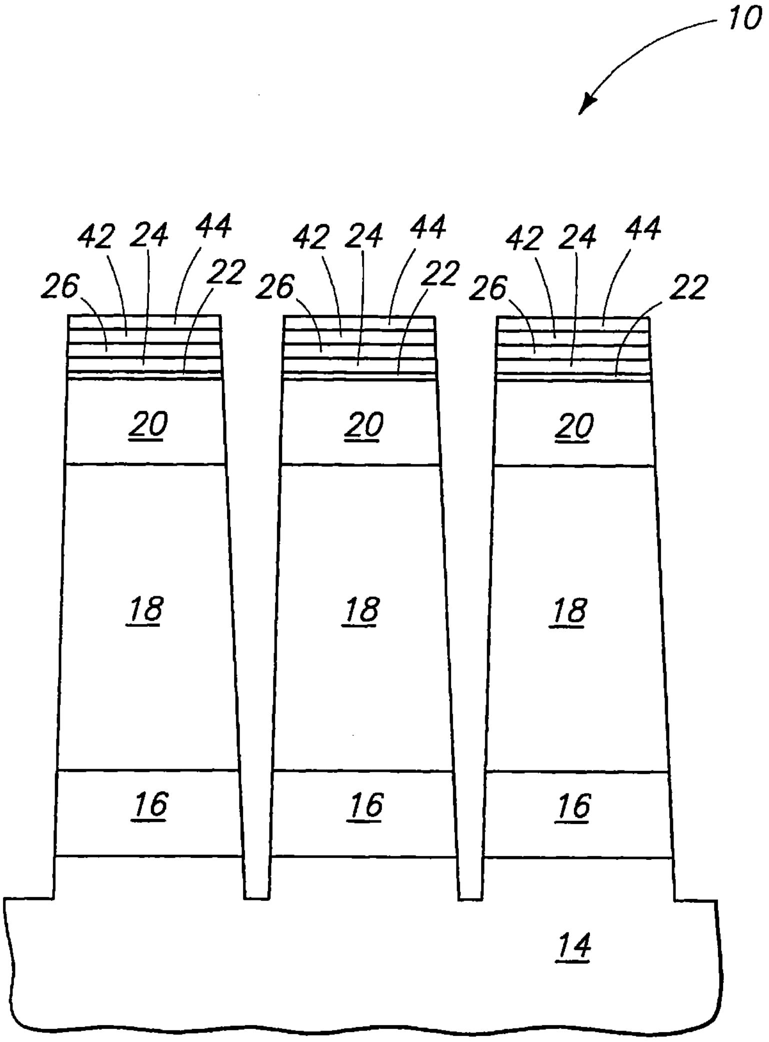
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Fig 18

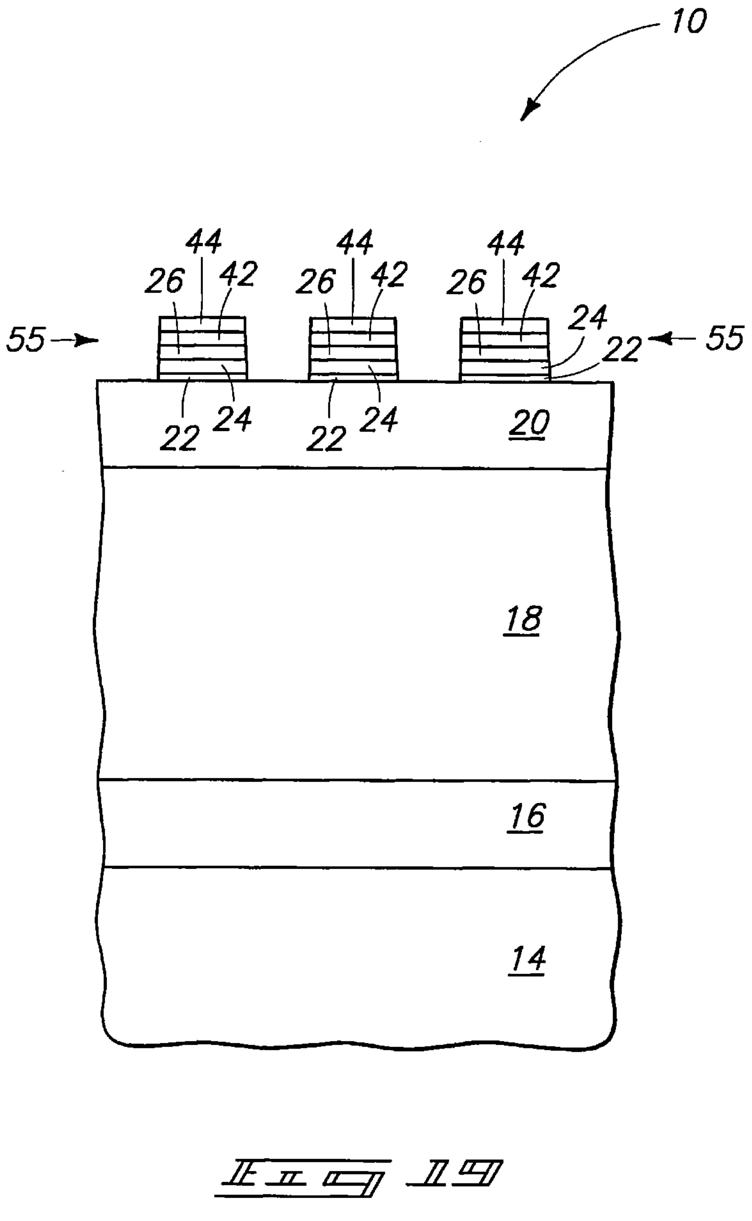

Fig 19

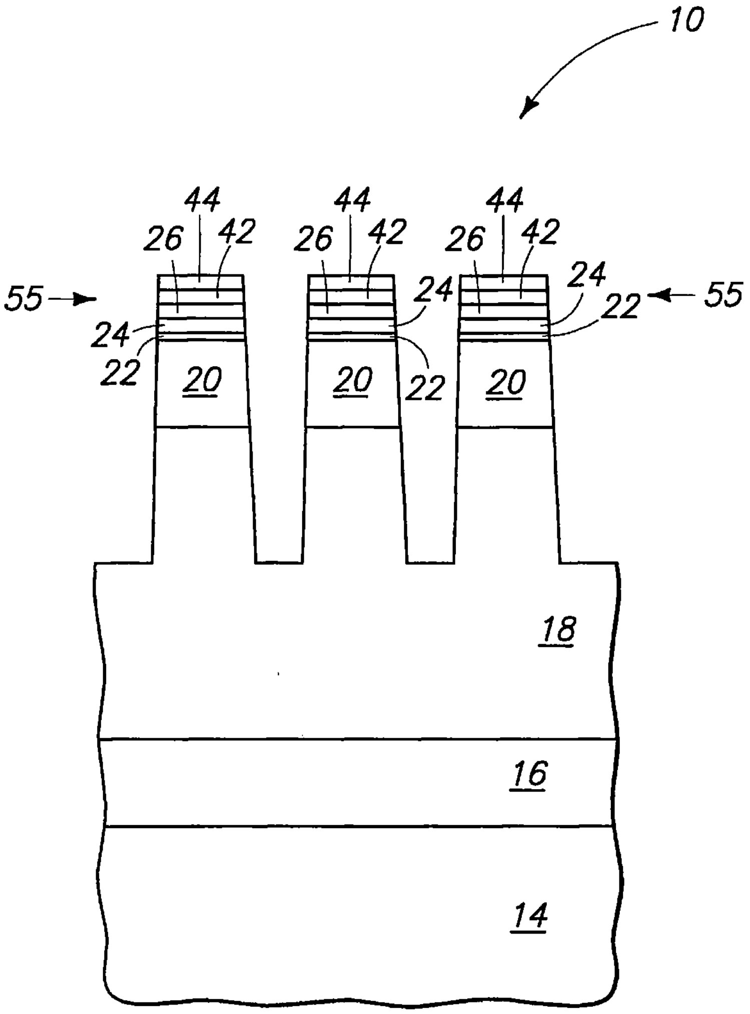
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Fig 20

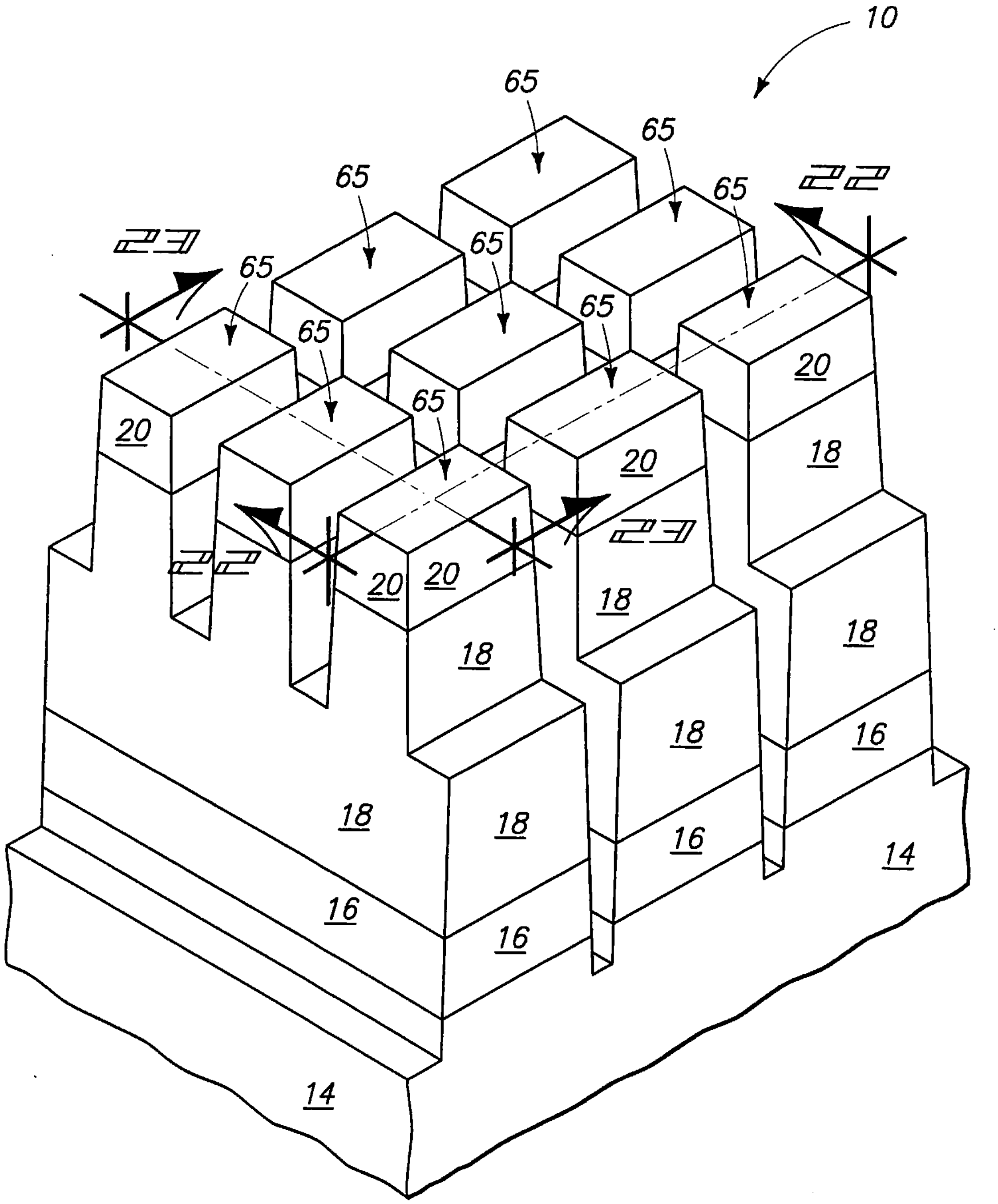
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Fig 21

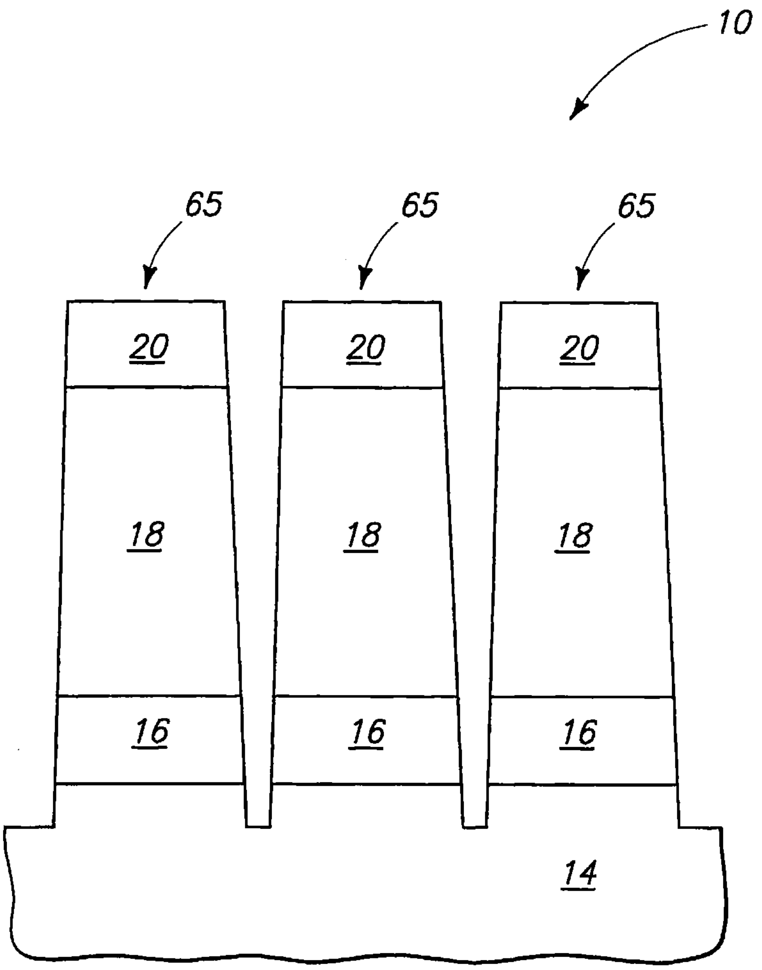

Fig 22

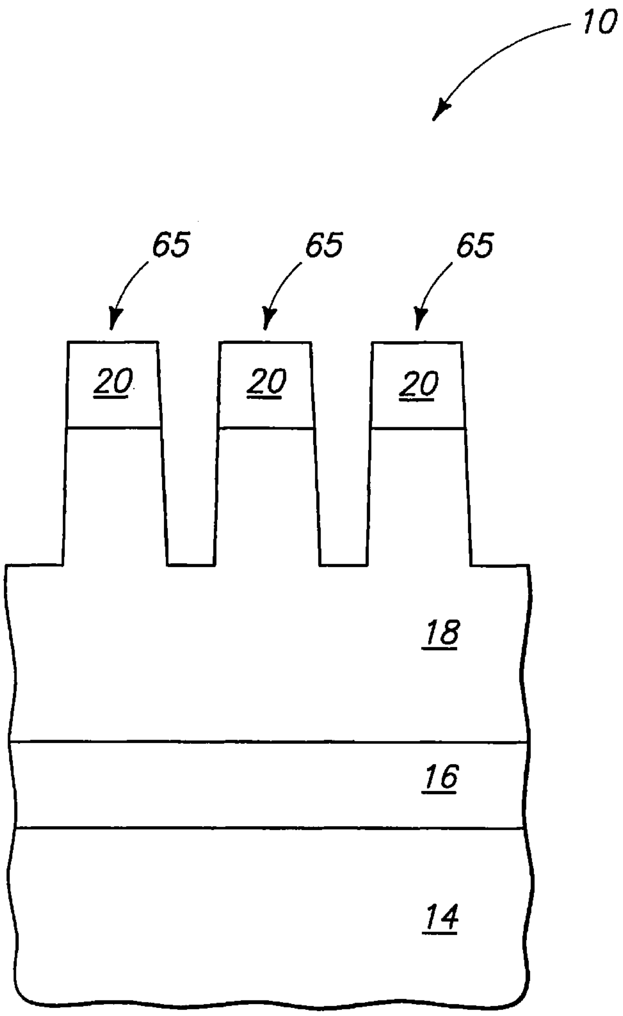

Fig 23

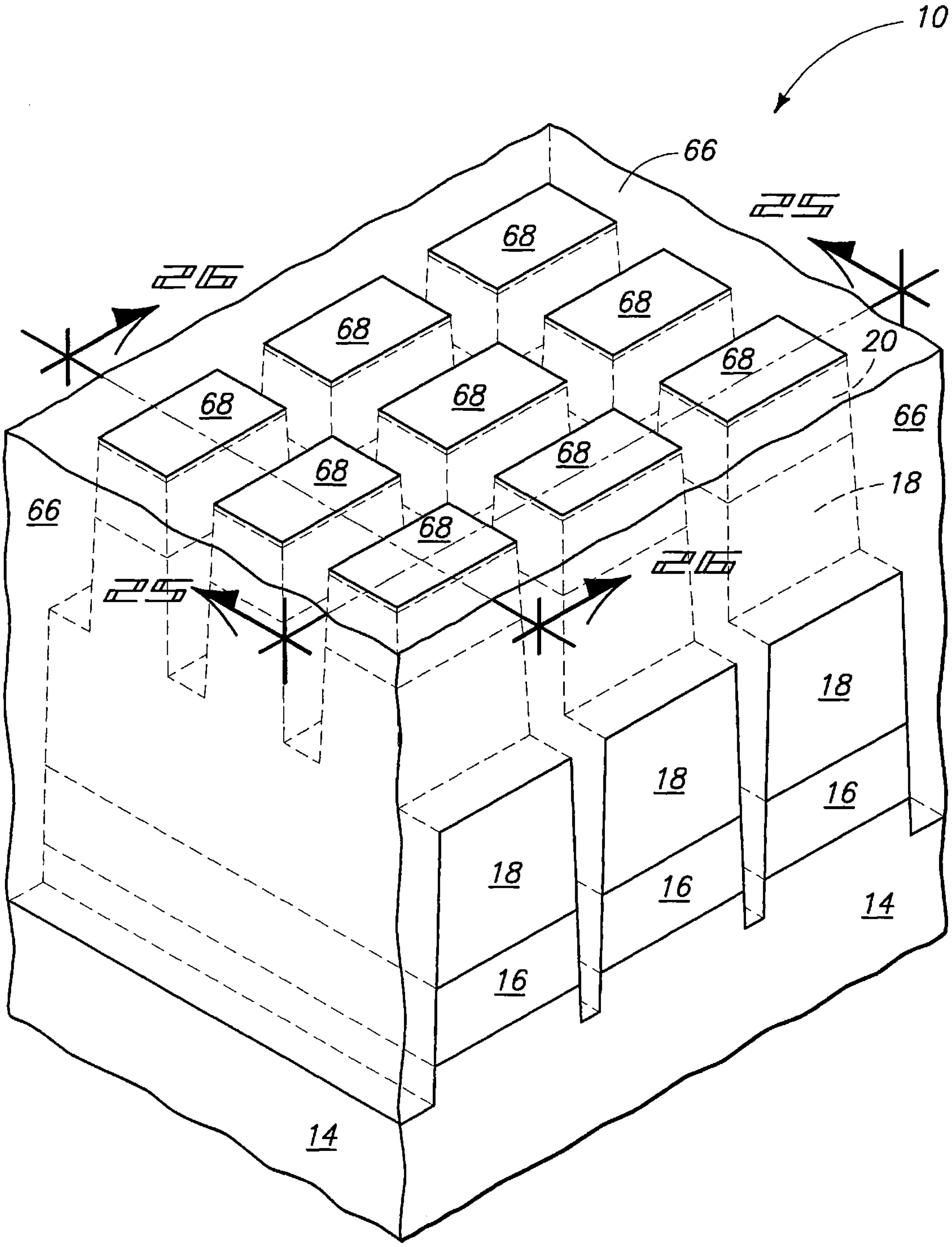
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Fig 24

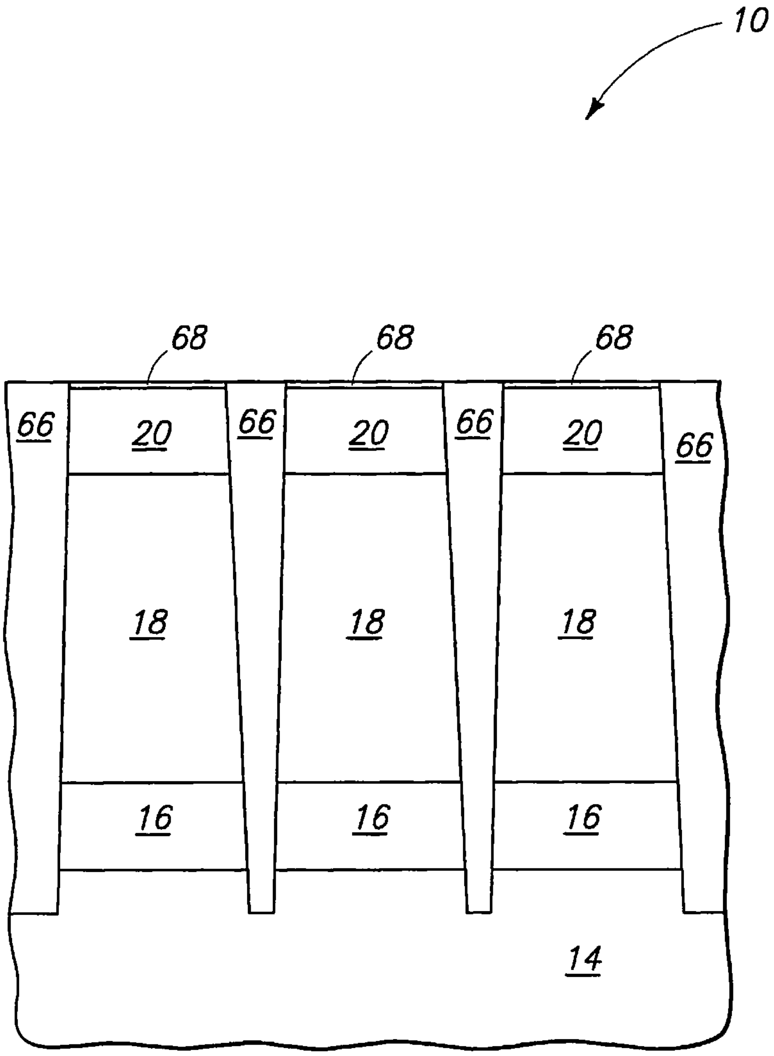

Fig 25

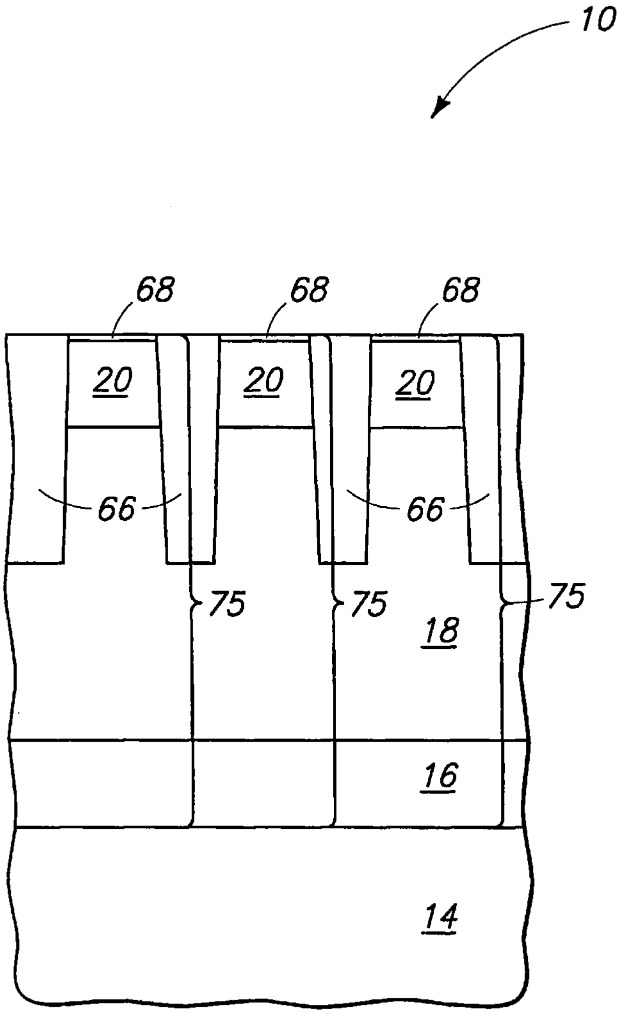

Fig 26

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/082719

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/3065(2006.01)i, H01L 21/76(2006.01)i, H01L 29/861(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC : B44C 1/22, C23F 1/00, 4/00, H01L 21/306, 21/302, 21/3065,21/336, 29/786, H05H 1/46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Utility models and applications for Utility models since 1975
Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKIPASS(KIPO Internal) & Keyword: plasma, mask, etch, SF6 and NF

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 6372151 B1 (TAEHO SHIN et al.) 16 April 2002 See Abstract; Claim1; Claim3 and Claim4	1-3,5,7,8 11-13 4,6,9,10,14-25
Y A	JP 05-055178 A (FUJITSU LTD) 05 March 1993 See Abstract and Figure1	11-13 1-10,14-25
A	JP 09-186139 A (CANON INC) 15 July 1997 See Abstract	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search 22 APRIL 2009 (22.04.2009)	Date of mailing of the international search report **22 APRIL 2009 (22.04.2009)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer Hong, Sung Ui Telephone No. 82-42-481-8496

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2008/082719

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6372151 B1	16.04.2002	JP 2001-093879 A TW 573326 A	06.04.2001 21.01.2004
JP 05-055178 A	05.03.1993	None	
JP 09-186139 A	15.07.1997	None	