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(54) INTERCONNECT FOR TESTING SEMICONDUCTOR DICE HAVING RAISED BOND PADS

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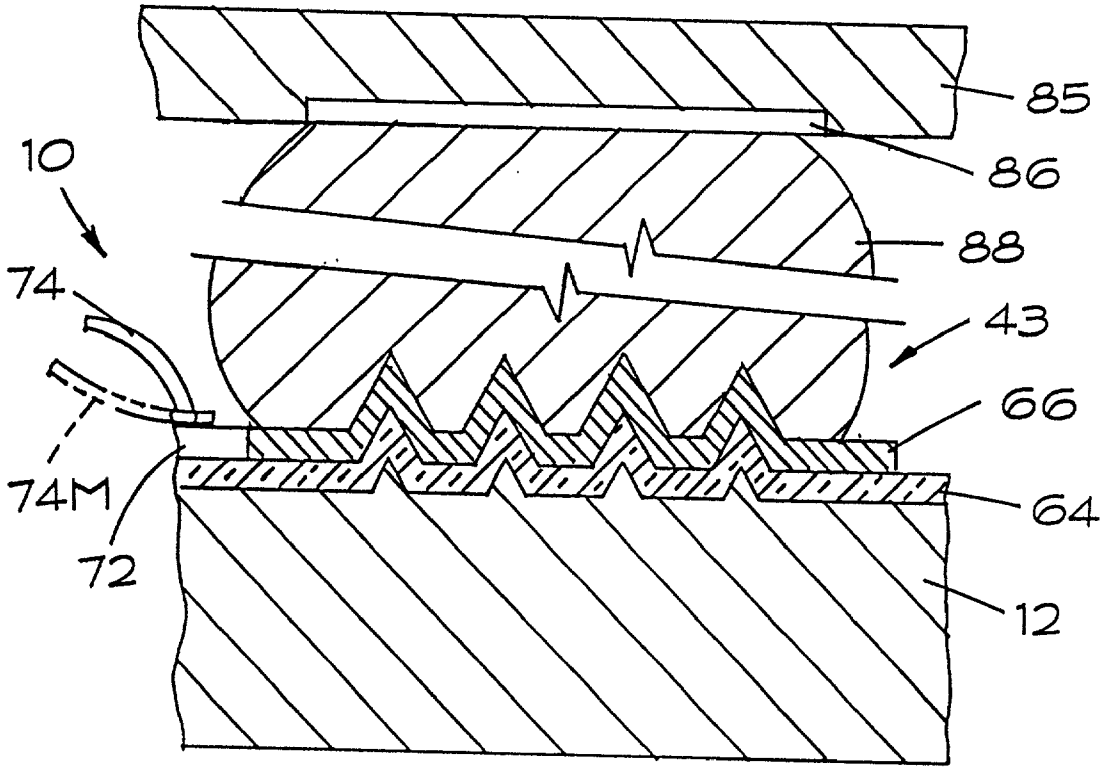
(57) ABSTRACT

A method for testing unpackaged semiconductor dice having raised contact locations (e.g., bumped bond pads) and a method for forming an interconnect suitable for testing this type of dice are provided. The interconnect includes a substrate having contact members comprising an array of sharpened elongated projections. The sharpened projections are formed by etching (or by growing and removing an oxide) through exposed areas of a mask. A conductive layer is formed on the sharpened projections and is in electrical communication with conductive traces formed on the substrate. The conductive layer can be formed as a layer of metal, as a stack of metals including a barrier metal, as a silicide, or as a layer of polysilicon. For testing an unpackaged die, the interconnect and die are placed in a temporary carrier and biased together. The sharpened projections are adapted to penetrate the contact location on the die to a limited penetration depth to establish an ohmic connection while minimizing damage to the contact location.



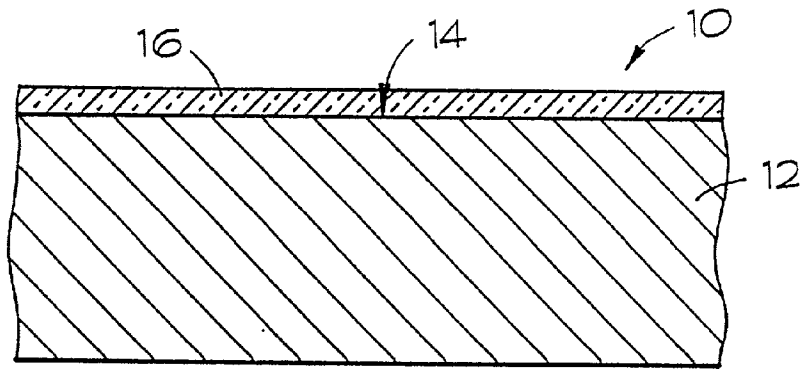


Figure 1

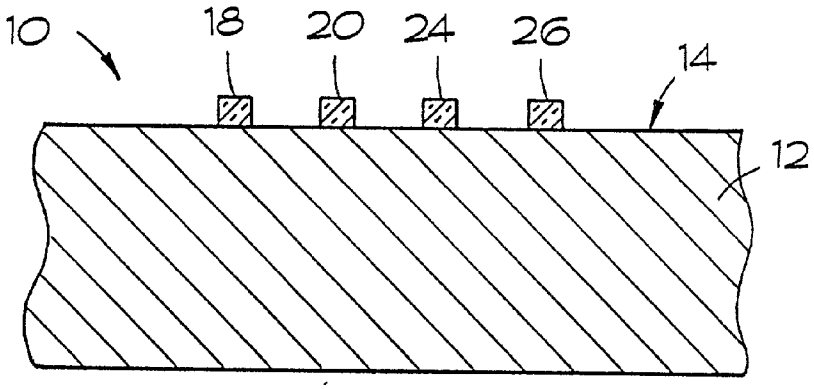


Figure 2

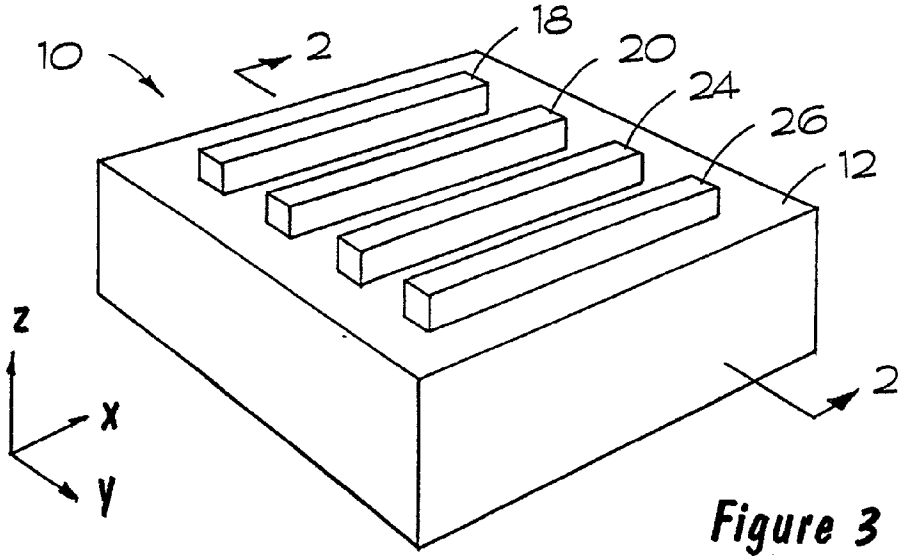
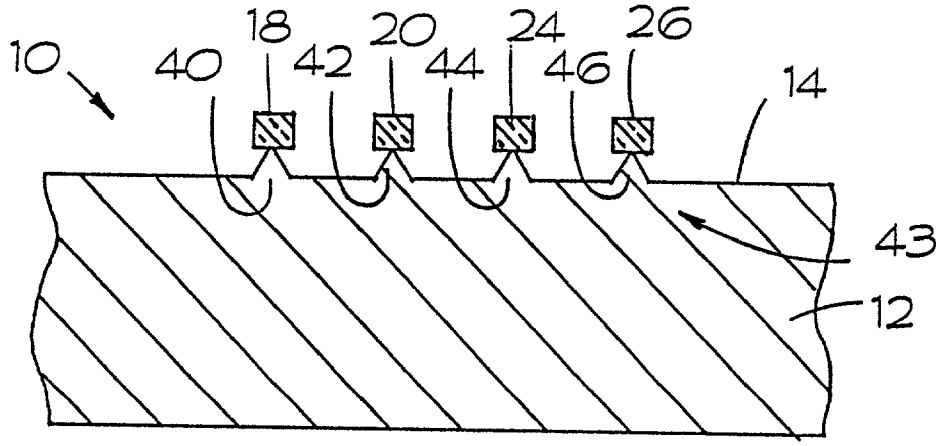


Figure 3



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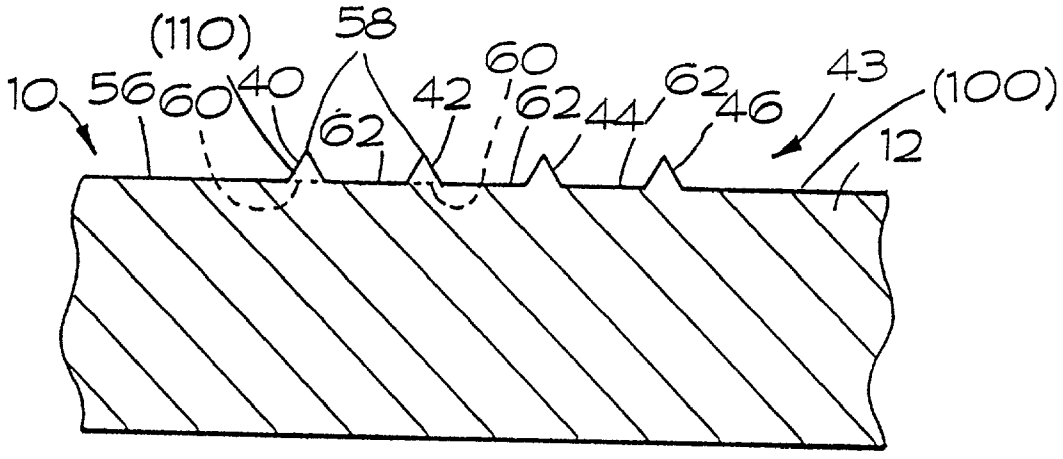

Figure 5A

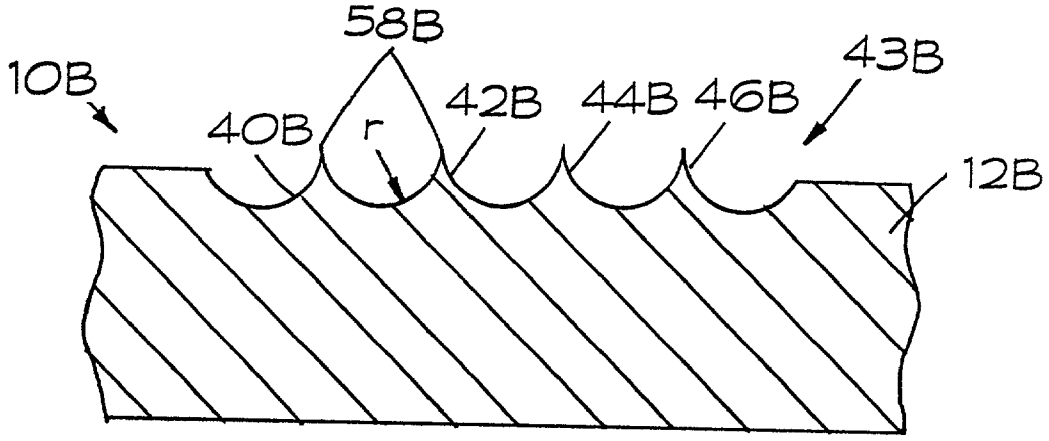

Figure 5B

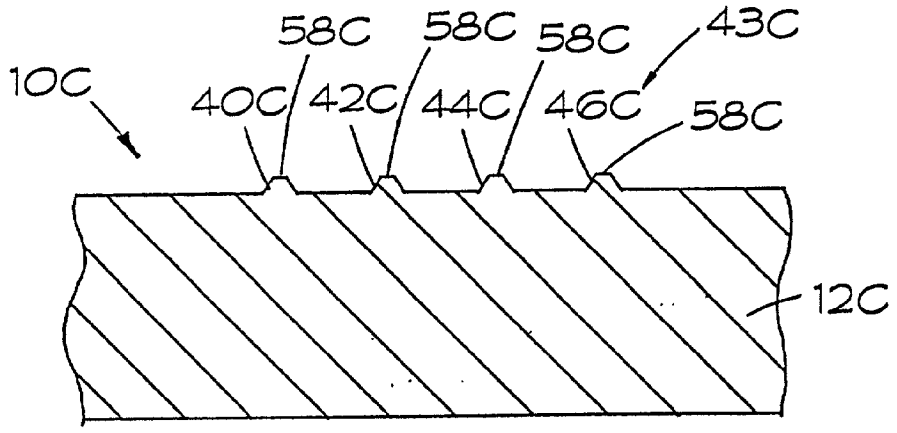

Figure 5C

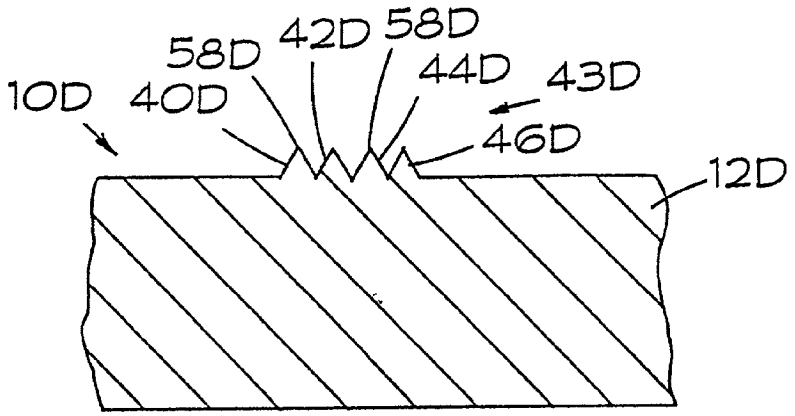

Figure 5D

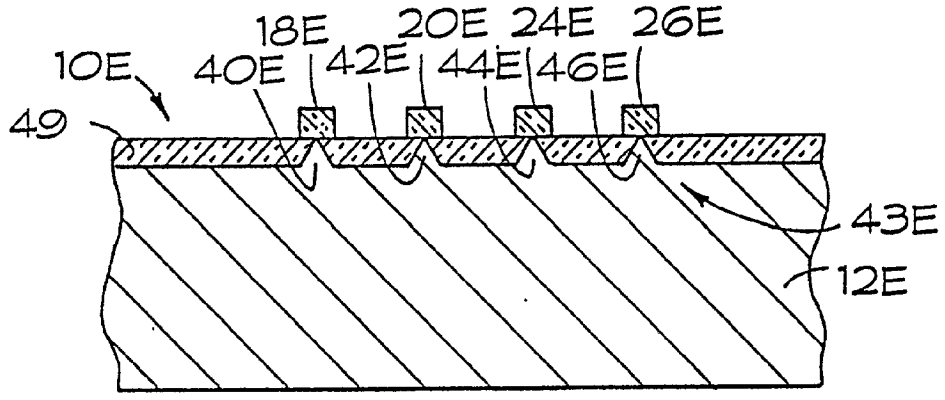

Figure 5E

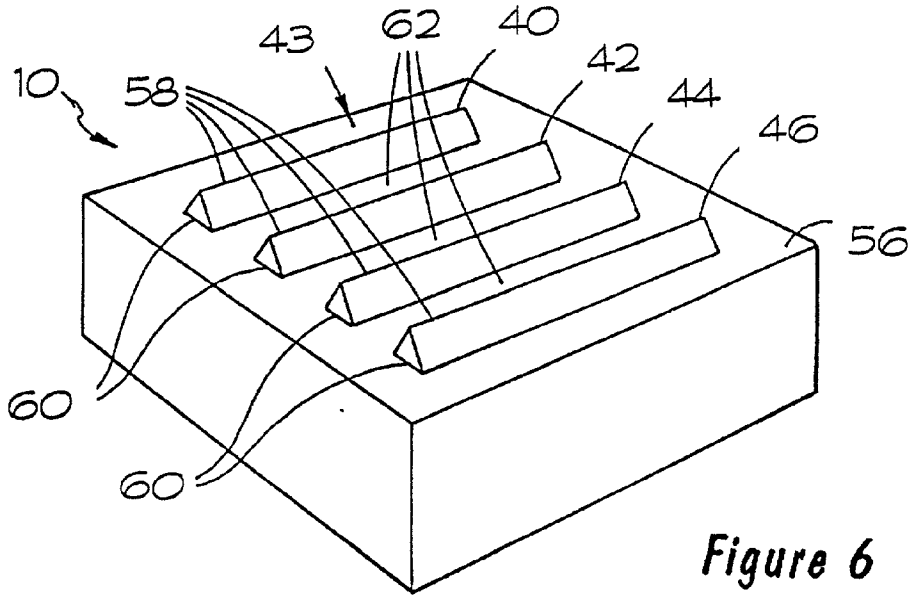

Figure 6

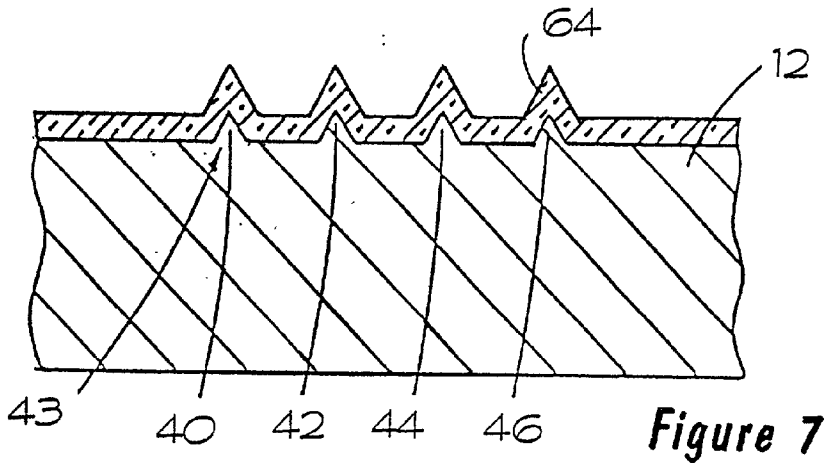

Figure 7

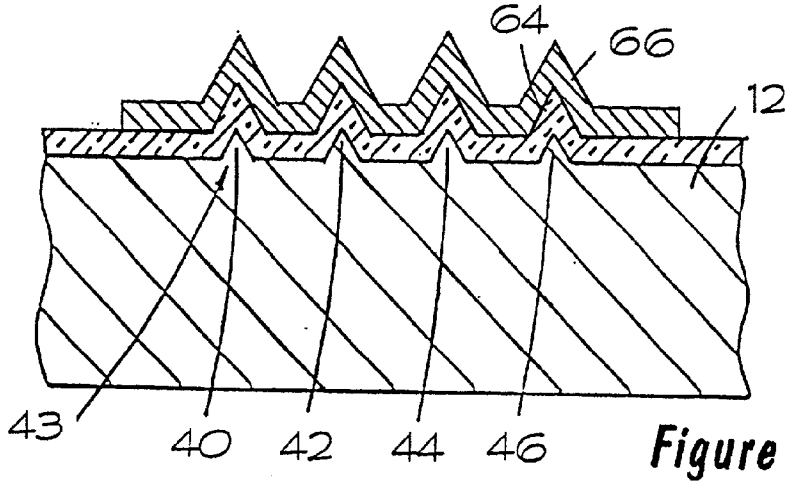

Figure 8

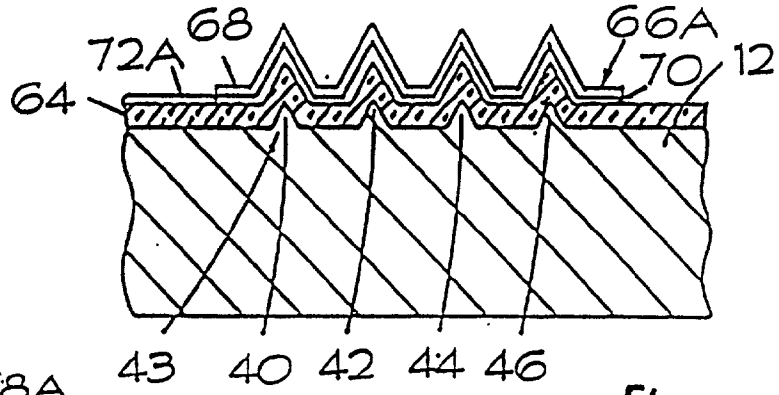

Figure 8A

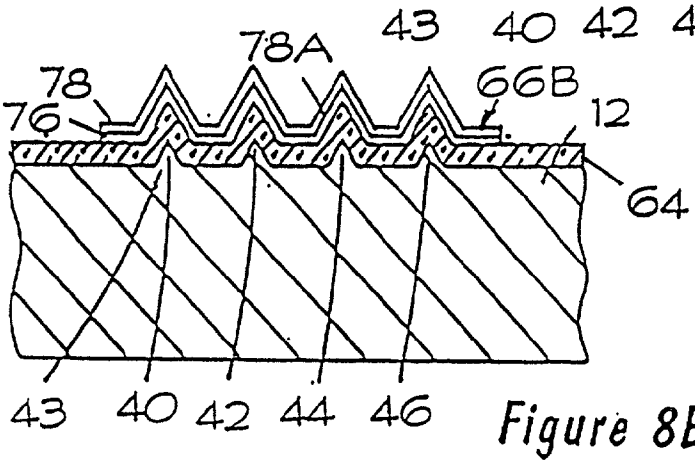

Figure 8B

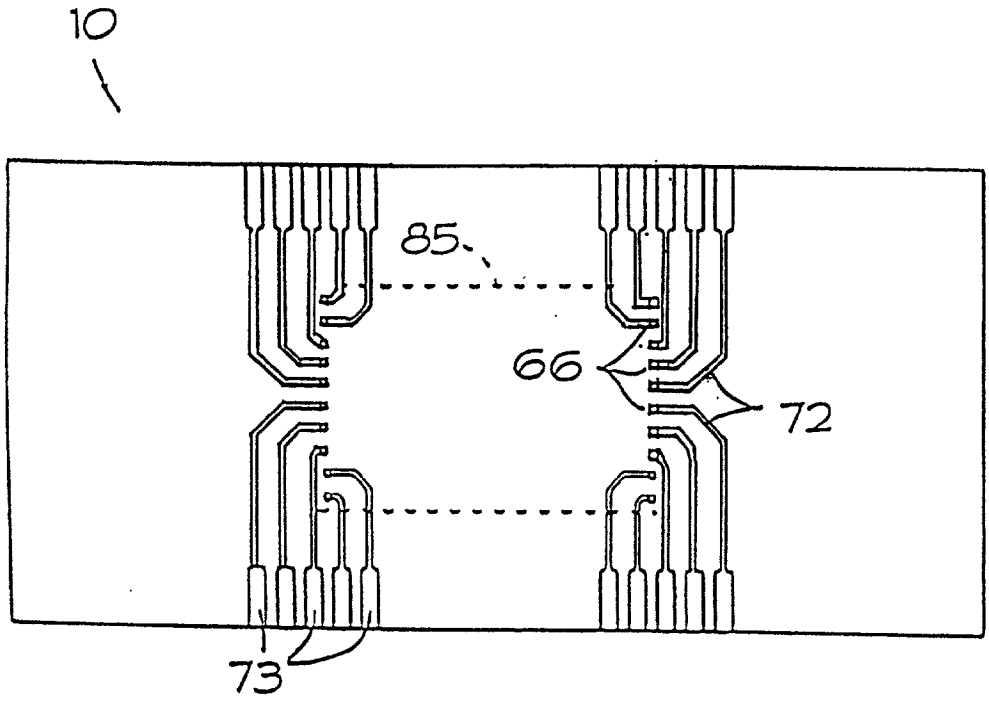

Figure 9

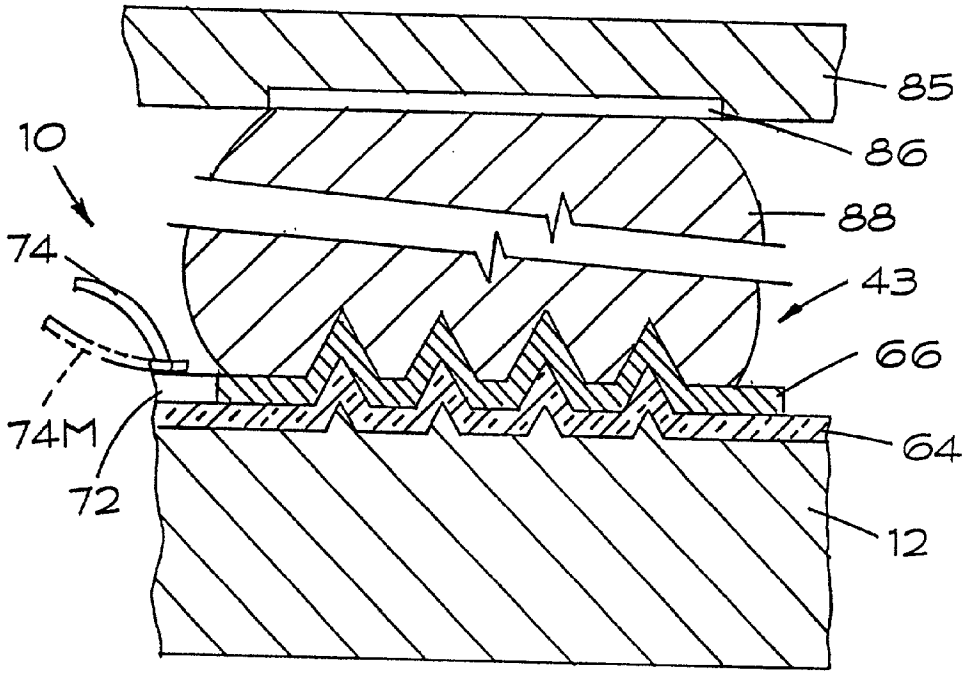

Figure 10

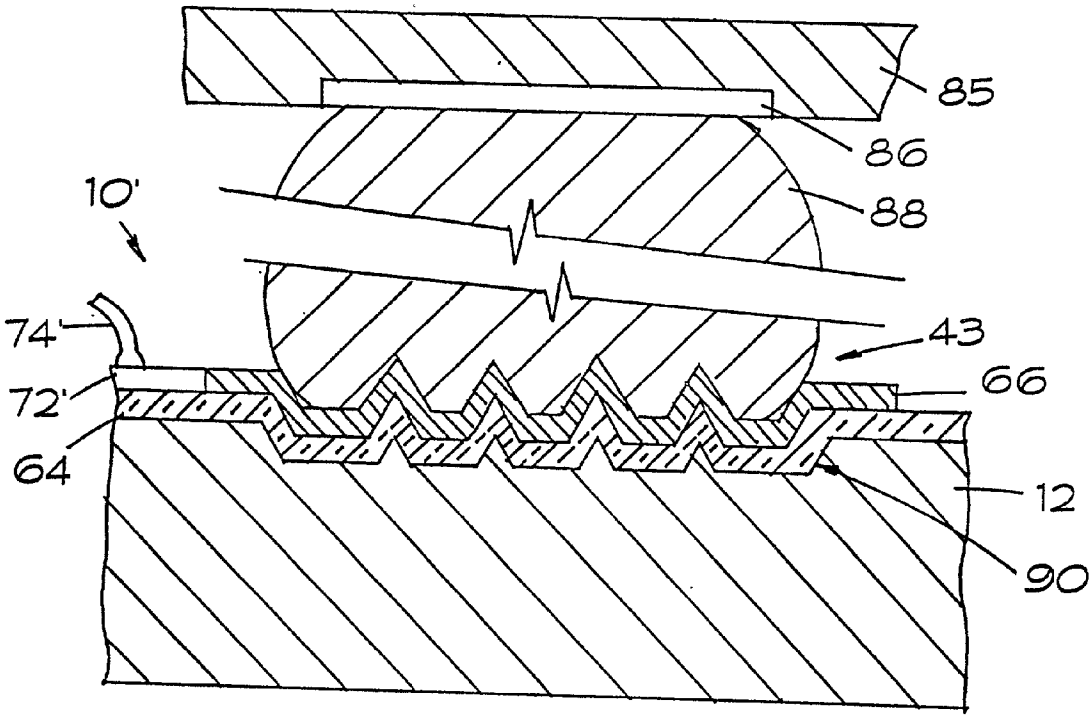

Figure 10A

INTERCONNECT FOR TESTING SEMICONDUCTOR DICE HAVING RAISED BOND PADS

BACKGROUND OF THE INVENTION

[0001] Because of a trend towards multi-chip modules, semiconductor manufacturers are required to supply unpackaged dice that have been tested and certified as known good die (KGD). Known good die is a collective term that denotes unpackaged die having the same reliability as the equivalent packaged die.

[0002] The need for known good die has led to the development of test apparatus in the form of temporary carriers suitable for testing discrete, unpackaged semiconductor dice. As an example, test apparatus for conducting burn-in tests for discrete die are disclosed in U.S. Pat. No. 4,899,107 to Corbett et al. and U.S. Pat. No. 5,302,891 to Wood et al., which are assigned to Micron Technology, Inc. Other test apparatus for discrete die are disclosed in U.S. Pat. No. 5,123,850 to Elder et al., and U.S. Pat. No. 5,073,117 to Malhi et al., which are assigned to Texas Instruments.

[0003] With this type of test apparatus, a non-permanent electrical connection must be made between contact locations on the die, such as bond pads, and external test circuitry associated with the test apparatus. The bond pads provide a connection point for testing the integrated circuitry formed on the die.

[0004] In making this temporary electrical connection, it is desirable to effect a connection that causes as little damage as possible to the bond pad. If the temporary connection to a bond pad damages the pad, the entire die may be rendered as unusable. This is difficult to accomplish because the connection must also produce a low resistance or ohmic contact with the bond pad. A bond pad typically includes a metal oxide layer that must be penetrated to make an ohmic contact.

[0005] Some prior art contact structures, such as probe cards, scrape the bond pads which wipes away the oxide layer and causes excessive damage to the bond pads. Other interconnect structures such as probe tips may pierce both the oxide layer and the metal bond pad and leave a deep gouge. Still other interconnect structures, such as microbumps, may not even pierce the oxide layer preventing the formation of an ohmic contact.

[0006] Another important consideration in testing of known good die is the effect of thermal expansion during the test procedure. As an example, during burn-in testing, a die is heated to an elevated temperature and maintained at temperature for a prolonged period. This causes thermal expansion of the die and temporary interconnect. If the die and the temporary interconnect expand by a different amount, stress may develop at the connection point and adversely effect the electrical connection. This may also lead to excessive damage of bond pads.

[0007] One type of semiconductor dice having a raised topology is referred to as a "bumped" die. A "bumped" semiconductor die includes bond pads formed with a bump of solderable material such as a lead-tin alloy. Bumped dice are often used for flip chip bonding wherein the die is mounted face down on a substrate, such as a printed circuit board, and then attached to the substrate by welding or soldering. Typically the bumps are formed as balls of material that are circular in a cross sectional plane parallel to the face of the die. The bumps typically have a diameter of from 50 μm to 100 μm. The sides of the bump typically bow or curve outwardly from a flat top surface. The flat top surface forms the actual region of contact with a mating electrode on the printed circuit board or other substrate.

[0008] In the past, following testing of a bumped die, it has been necessary to reflow the bumps, which are typically damaged by the test procedure. This is an additional process step which adds to the expense and complexity of the testing process. Furthermore, it requires heating the tested die which can adversely affect the integrated circuitry formed on the die.

OBJECTS OF THE INVENTION

[0009] In view of the need in the art for improved methods for testing unpackaged, bumped, semiconductor dice, it is an object of the present invention to provide an improved method of testing unpackaged semiconductor dice having raised or bumped bond pads.

[0010] It is a further object of the present invention to provide an improved method for forming a temporary interconnect adapted to test semiconductor die having raised or bumped bond pads.

[0011] It is a further object of the present invention to provide an improved method for fabricating temporary interconnects for bumped semiconductor dice that uses semiconductor manufacturing techniques and that provides an improved contact structure.

[0012] Other objects, advantages and capabilities of the present invention will become more apparent as the description proceeds.

SUMMARY OF THE INVENTION

[0013] In accordance with the present invention, an improved method of testing, and an improved method for fabricating a temporary interconnect for testing unpackaged semiconductor dice having raised contact locations (e.g., bumped bond pads) are provided. The improved method of testing includes a temporary interconnect adapted to establish an electrical connection with raised contact locations on the die without damage to the contact locations. The interconnect includes a substrate (e.g., silicon) having contact members formed in a pattern that matches the size and spacing of the contact locations on the die. The contact members on the interconnect include one or more sharpened projections. The sharpened projections are adapted to penetrate the raised contact locations on the die and to pierce any residual insulating material to establish an ohmic connection.

[0014] The sharpened projections are formed integrally with the substrate using an etching process or using an oxidation growth process. The sharpened projections are formed either on a surface of the substrate, or in a recess in the substrate which is sized to retain the raised contact locations on the die. In addition, the sharpened projections are formed with a size and shape which permits penetration into the contact locations but with a self-limiting penetration depth. In an illustrative embodiment, the sharpened projec-

tions are formed as an array of parallel elongated blades. Depending on the method of formation, the elongated blades can be formed in a variety of cross sectional configurations (e.g., triangular, rounded profile, flat tops). In addition, the elongated blades can be formed in a spaced array or with no spaces therebetween.

[0015] The sharpened projections are formed on an insulating layer of the interconnect substrate and are covered with a conductive layer. The conductive layer can be formed as a single layer of a highly conductive metal such as aluminum or iridium, or a conductive material such as polysilicon. Conductive traces or runners are formed in electrical contact with the conductive layer to establish an electrical pathway to and from the contact members of the interconnect.

[0016] The conductive layer for the contact members can also be formed as a stack comprising two different layers of material. An outer layer of the stack is preferably a metal such as platinum, which is chemically inert and provides a barrier layer that will not react with the raised material (e.g., bump) at the contact location on the die. The inner layer of the stack can be a metal such as aluminum or titanium which can be easily bonded to conductive traces. The inner layer and conductive traces can also be formed of a same material.

[0017] The conductive layer can also be formed as a metal silicide. A metal silicide can be formed by depositing a silicon containing layer and a metal layer on the sharpened projections and reacting these layers to form a metal silicide. The unreacted portions of the silicon containing layer and metal layer are then etched selective to the metal silicide using a salicide process.

[0018] A method for fabricating a temporary interconnect in accordance with the invention, includes the steps of: forming a substrate; forming an array of contact members on the substrate as one or more elongated sharpened projections adapted to penetrate a raised contact location (e.g., bump) on a die to a limited penetration depth; forming an insulating layer (e.g., SiO_2, Si_3N_4) over the entire substrate including the sharpened projections; forming a conductive layer over the sharpened projections; and then forming conductive traces on the substrate in electrical communication with the conductive layer. Optionally, the sharpened projections can be mounted within an indentation formed in the substrate that is adapted to retain the raised contact location on the die.

[0019] Preferably a large number of interconnects are formed on a single substrate or wafer. This substrate can then be diced (e.g., saw cut) to singulate the interconnects. In use, the temporary interconnect is placed in a temporary carrier (i.e., test apparatus) along with the die, and an electrical path is established between the conductive traces on the interconnect and external test circuitry associated with the test apparatus.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] **FIG. 1** is a schematic cross sectional view illustrating a substrate and a mask layer during an initial process step for forming an interconnect in accordance with the invention;

[0021] **FIG. 2** is a schematic cross sectional view of the substrate taken along section line **2-2** of **FIG. 3** showing the mask layer after patterning and etching to form a mask having solid areas and openings;

[0022] **FIG. 3** is a perspective view of **FIG. 2**;

[0023] **FIG. 4** is a cross sectional view showing formation of the sharpened projections on the substrate using the mask layer and an etch process;

[0024] **FIG. 5A** is a cross sectional view taken along section line **5A-5A** of **FIG. 6** showing the sharpened projections formed on the substrate with a triangular cross section using an anisotropic etch process;

[0025] **FIG. 5B** is a cross sectional view, equivalent to **FIG. 5A**, showing the sharpened projections formed on the substrate with a rounded profile using an isotropic etch process;

[0026] **FIG. 5C** is a cross sectional view equivalent to **FIG. 5A** showing the sharpened projections formed on the substrate with a truncated pyramidal cross section, using an anisotropic etch process;

[0027] **FIG. 5D** is a cross sectional view equivalent to **FIG. 5A** showing the sharpened projections formed on the substrate using an anisotropic etch with no spaces in between the projections;

[0028] **FIG. 5E** is a cross sectional view showing the sharpened projections formed on the substrate using an oxidation growth process;

[0029] **FIG. 6** is a perspective view of the substrate and sharpened projections shown in **FIG. 5**;

[0030] **FIG. 7** is a cross sectional view of the substrate and sharpened projections showing the formation of an insulating layer over the substrate;

[0031] **FIG. 8** is a cross sectional view of the substrate and sharpened projections showing the formation of a conductive layer on the sharpened projections;

[0032] **FIG. 8A** is a cross sectional view of the substrate and sharpened projections showing the formation of a conductive layer on the sharpened projections comprising a stack of two different metal layers;

[0033] **FIG. 8B** is a cross sectional view of the substrate and sharpened projections showing the formation of a conductive layer on the projections formed of a metal silicide;

[0034] **FIG. 9** is a plan view of an interconnect formed in accordance with the invention;

[0035] **FIG. 10** is a cross sectional view illustrating testing of an unpackaged semiconductor die using an interconnect formed in accordance with the invention and showing the sharpened projections electrically engaging a bumped contact location of the die; and

[0036] **FIG. 10A** is a cross sectional view illustrating testing of an unpackaged semiconductor die in accordance with the invention using an alternate embodiment contact structure in which the sharpened projections are mounted within an indentation formed in the substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0037] Referring now to **FIG. 1, a** process for forming an interconnect **10** for testing unpackaged semiconductor dice having raised contact locations, such as bumped bond pads, is shown. The interconnect **10** includes a substrate **12** formed of a material having a coefficient of thermal expan-

sion (CTE) that closely matches the CTE of a silicon die. Suitable materials for the substrate include monocrystalline silicon, silicon-on-glass, silicon-on-sapphire, germanium, or ceramic.

[0038] The substrate **12** includes a planar outer surface **14** having a mask layer **16** of a material such as silicon nitride (Si_3N_4) formed thereon. A typical thickness for the mask layer **16** is about 500 Å to 3000 Å. The mask layer **16** may be formed using a suitable deposition process such as CVD.

[0039] Next, as shown in **FIG. 2**, the mask layer **16** is patterned and etched selective to the substrate **12** to form a hard mask that includes masking blocks **18, 20, 24, 26** and openings therebetween. Depending on the materials used for the mask layer **16**, this etch step may be performed using a wet or dry etch. As an example, a layer of silicon nitride may be etched with a pattern of openings using hot (e.g., 180° C.) phosphoric acid.

[0040] As shown in the perspective view of **FIG. 3**, the masking blocks **18, 20, 24, 26** are elongated rectangular blocks. In addition, the masking blocks **18, 20, 24, 26** are formed in a parallel spaced array. The peripheral dimensions of the array are selected to accommodate the dimensions of a raised contact location on a semiconductor die. As an example, the raised contact location can be a bond pad having a metal bump with a diameter of from 1 μm-500 μm. As is apparent however, such a parallel spaced array is merely exemplary and other configurations are possible. Other suitable arrangements for the masking blocks include enclosed rectangles, squares, triangles, T-shapes and X-shapes.

[0041] Next, as shown in **FIG. 4**, elongated sharpened projections **40, 42, 44, 46** are formed on the substrate **12**. The sharpened projections **40, 42, 44, 46** can be formed using an etching process (anisotropic or isotropic), using an oxidation process, or using a deposition process.

[0042] With etching, a wet or dry isotropic, or anisotropic, etch process is used to form the sharpened projections **40, 42, 44, 46** as the material under the masking blocks **18, 20, 24, 26** is undercut by the etchant reacting with the substrate **12**. In other words, the exposed substrate **12** between the masking blocks **18, 20, 24, 26** etches faster than the covered substrate **12** under the blocks **18, 20, 24, 26**.

[0043] Following the etching process the masking blocks **18, 20, 24, 26** are stripped using a wet etchant such as H_3PO_4 that is selective to the substrate **12**. For an anisotropic etch, in which the etch rate is different in different directions, an etchant solution containing a mixture of KOH and H_2O can be utilized. As shown in **FIG. 5**A, this results in the formation of triangular shaped sharpened projections **40, 42, 44, 46**. This triangular shape is a function of the different etch rates of monocrystalline silicon along the different crystalline orientations. The surface of the substrate **12** represents the (100) planes of the silicon which etches faster than the sloped sidewalls that represent the **(110)** plane. For a silicon substrate **12**, the slope of the sidewalls of the sharpened projections is about 54° with the horizontal. For forming the triangular shaped sharpened projections **40, 42, 44, 46** the width of the masking blocks **18, 20, 24, 26** and the parameters of the etch process are controlled to form a pointed tip **58** on each projection **40, 42, 44, 46**.

[0044] For an isotropic etch, in which the etch rate is the same in all directions, an etchant solution containing a mixture of HF, HNO_3 and H_2O can be utilized. As shown in **FIG. 5**B, this results in sharpened projections **40**B, **42**B, **44**B, **46**B having a pointed tip **58**B and a rounded sidewall contour. In this embodiment the sidewalls of the sharpened projections **40**B, **42**B, **44**B, **46**B are undercut below the masking blocks **18, 20, 24, 26 (FIG. 4)** with a radius "r". The value of the radius "r" is controlled by the etch parameters (i.e., time, temperature, concentration of etchant) and by the width of the masking blocks **18, 20, 24, 26 (FIG. 4)**.

[0045] **FIG. 5C** illustrates another embodiment wherein the sharpened projections **40**C, **42**C, **44**C, **46**C are formed with a cross section of a truncated pyramid with a flat tip **58**C. In this embodiment an anisotropic etch is used. In addition, the width of the masking blocks **18, 20, 24, 26** and parameters of the etch process (e.g., time, temperature, concentration of etchant) are controlled to form the flat tip **58**C.

[0046] **FIG. 5D** illustrates another embodiment wherein the sharpened projections **40**D, **42**D, **44**D, **46**D are formed in a saw tooth array with no spaces between the base portions. In this embodiment an anisotropic etch is used and the process parameters, including the etch time and width of the masking blocks **18, 20, 24, 26** are controlled to provide a desired height and tip **58**D to tip **58**D spacing.

[0047] Alternately, in place of an isotropic or anisotropic etch process, the sharpened projections can be formed using an oxidizing process. This is shown in **FIG. 5E**. With an oxidizing process the substrate **12**E may be subjected to an oxidizing atmosphere to oxidize exposed portions of the substrate **12** not covered by the masking blocks **18**E, **20**E, **24**E, **26**E. As an example, the oxidizing atmosphere may comprise steam and **02** at an elevated temperature (e.g., 950° C). The oxidizing atmosphere oxidizes the exposed portions of the substrate **12** and forms an oxide layer **49** (e.g., silicon dioxide). At the same time, sharpened projections **40**E, **42**E, **44**E and **46**E are formed under the masking blocks **18**E, **20**E, **24**E, **26**E. With an oxidizing process, the oxide layer **49** can also be stripped using a suitable wet etchant such as HF.

[0048] The sharpened projections can also be formed by a deposition process out of a different material than the substrate **12**. As an example, a CVD process can be used to form the sharpened projections out of a deposited metal.

[0049] Referring now to **FIG. 6**, which represents the structure after completion of the process illustrated by **FIG. 5**A, the sharpened projections **40, 42, 44, 46** are formed in an array of parallel spaced, elongated, knife edges which form a contact member **43**. The contact member **43** has an overall peripheral dimension adapted to accommodate the size of a raised contact location (e.g., bumped bond pad) on a semiconductor die. Although multiple sharpened projections are formed for each contact member **43**, it is to be understood that a single sharpened projection per contact member **43** would also be suitable.

[0050] The sharpened projections **40, 42, 44, 46** project from a surface **56** of the substrate **12** and include pointed tips **58** and bases **60**. The bases **60** of adjacent sharpened projections **40, 42, 44, 46** are spaced from one another a distance sufficient to define a penetration stop plane **62** there between. The function of the penetration stop plane **62** will be apparent from the continuing discussion. Example spacing between bases **60** would be 10 μm, while an example

length of the bases **60** and tips **58** would be from 3 to 10 μm. The height of each sharpened projections **40**, **42**, **44**, **46** is preferably about one-thousandth ($\frac{1}{1000}$) to one-quarter (**1**;**4**) the diameter of a bumped bond pad on a semiconductor die. This height is selected to allow good electrical contact and at the same time provide minimum damage to raised contact locations (e.g., bumps) on dice that are typically tested using the interconnect **10** and then used for flip chip bonding. As an example, this projecting distance of the sharpened projections **40**, **42**, **44**, **46**, from the substrate **12** will be on the order of 1 to 3 μm. Subsequent to formation of the sharpened projections **40**, **42**, **44**, **46**, additional etching may be used to further sharpen the tips **58**.

[**0051**] Following the formation of the sharpened projections **40**, **42**, **44**, **46** and as shown in **FIG. 7**, an insulating layer **64** is formed over the entire substrate **12** including the contact member **43**. The insulating layer **64** can be formed of a material such as SiO_2 by exposing the substrate **12** to an oxidizing atmosphere for a short time or by using a CVD process. The insulating layer **64** can also be formed of a material such as Si_3N_4.

[**0052**] Next, as shown in **FIG. 8, a** conductive layer **66** is formed on the insulating layer **64** and in an area of the substrate overlying each contact member **43**. The conductive layer **66** can be formed of a highly conductive metal, such as aluminum (Al), iridium (Ir), copper (Cu), titanium (Ti), tungsten (W), tantalum (Ta), molybdenum (Mo) or alloys of these metals. A suitable metallization process to form the conductive layer **66** can include the steps of deposition (e.g., sputter, CVD), patterning (e.g., photopatterning) and etching (e.g., wet or dry etch).

[**0053**] The conductive layer **66** can also be formed of a conductive material such as doped polysilicon. As an example, an LPCVD process can be used to form a conductive layer **66** out of polysilicon doped with phosphorus.

[**0054**] As shown in **FIG. 8A, a** conductive layer **66**A can also be formed as a stack of two materials. The stacked conductive layer **66**A includes a barrier layer **68** and a bonding layer **70**. The barrier layer **68** is formulated to prevent formation of an oxide layer that would change the resistivity of the contact member **43**. In addition, the barrier layer **68** is formulated to prevent reaction of the conductive layer **66**A with the contact location (e.g., metal bump **88**—**FIG. 10**) on the die and prevent the diffusion of impurities from the contact location on the die to the bonding layer **70** and vice versa.

[**0055**] The barrier layer **68** is preferably a metal that will not easily form a "permanent" or "chemical" bond with a raised metal contact location on the die even under a large mechanical force (e.g., 10 lb./interconnect) and at high temperatures. In addition, this metal must be chemically stable (i.e., non reactive) for temperatures up to about 200° C. By way of example, the barrier layer **68** can be formed of a metal such as platinum (Pt), titanium (Ti) or a titanium alloy (e.g., TiN, TiW).

[**0056**] The bonding layer **70** is formulated to provide a good mechanical bond with conductive traces **72**A that are subsequently formed on the substrate **12** out of a highly conductive material. By way of example, the bonding layer **70** can be formed of aluminum (Al), tungsten (W) or titanium (Ti). In some applications the bonding layer **70** can be formed of a same material as the conductive traces **72**A using a single masking step.

[**0057**] As shown in **FIG. 8B, a** conductive layer **66**B can also be formed by depositing a silicon containing layer **76** (e.g., polysilicon, amorphous silicon) and a metal layer **78**, and reacting these layers to form a metal silicide **78**A. A typical thickness of the silicon containing layer **76** would be from about 500 Å to 3000 Å

[**0058**] The metal layer **78** is formed of a metal that will react with the silicon containing layer **76** to form a metal silicide. Suitable metals include the refractory metals, such as titanium (Ti), tungsten (W), tantalum (Ta), platinum (Pt) and molybdenum (Mo). In general, silicides of these metals (WSi_2, $TaSi_2$, $MoSi_2$, $PtSi_2$ and $TiSi_2$) are formed by alloying with a silicon surface. Other suitable metals include cobalt (Co), nickel (Ni), molybdenum (Mo), copper (Cu), gold (Au) and iridium (Ir).

[**0059**] Following deposition of the metal layer **78**, a sintering process is performed in which the metal layer **78** is heated and reacts with the silicon containing layer **76** to form a silicide layer **78**A. This type of sintering process is also known in the art as silicide sintering. Such a sintering step can be performed by heating the silicon containing layer **76** and metal layer **78** to a temperature of about 650° to 820° C. for typical thicknesses in thousands of angstroms (e.g., 2000 Å-3000 Å). This sintering process can be performed in one single step or using multiple temperature steps. A silicide layer **78**A forms at the interface of the metal layer **78** and the silicon containing layer **76**.

[**0060**] The unreacted portions of the metal layer **78** and the silicon containing layer **76** are removed while the silicide layer **78**A is left intact. This process is known in the art as a salicide process. This can be done by etching the metal layer **78** and silicon containing layer **76** selective to the silicide layer **78**A. By way of example, for a $TiSi_2$ silicide layer **78**A, the unreacted titanium can be removed with a wet etchant such as a solution of ammonia and hydrogen peroxide, or a H_2SO_4/H_2O_2 mixture, that will attack the metal layer **78** and not the silicide layer **78**A. Alternately, a dry etch process with an etchant species such as Cl_2 or BCl_3 can be used to etch the metal layer **78** selective to the silicide layer **78**A.

[**0061**] For etching the unreacted portion of the silicon containing layer **76** selective to the silicide layer **78**A, a wet etchant such as an $HF:HNO_3:H_2O$ acid mixture (typical ratios of 1:10:10) can be used to remove the unreacted silicon. A wet isotropic etchant can also be used for this purpose. Alternately the silicon containing layer **76** can be etched selective to the silicide layer **78**A using a dry etch process and an etchant such as NF_3 at low pressures (typically 30 m torr) or CL_2 and HBr at 130 m torr.

[**0062**] Following formation of the silicide layer **78**A, the resistivity of the silicide layer **78**A may be lowered using an annealing process. This may be accomplished by heating the substrate **10** and silicide layer **78**A to a temperature of between about 780° C. to 850° C. for several minutes.

[**0063**] **FIG. 9** is a plan view of the completed interconnect **10** with a semiconductor die **85** superimposed. As shown in **FIG. 9**, conductive traces **72** are formed on the interconnect **10** in electrical communication with the conductive layer **66** (or **66**A-**FIG. 8**A, **66**B-**FIG. 8B**). As also shown in **FIG. 9**, the conductive traces **72** extend to an edge of the interconnect **10** and include bond sites **73**. The bond sites **73** are used

for wire bonding a bond wire **74** (**FIG. 10**) to provide an electrical pathway from external test circuitry to the conductive layer **66**. This electrical pathway can also be established using a mechanical connectors **74**M (e.g., slide contacts, clip contacts) adapted to provide a temporary electrical connection with the conductive traces **72**.

[**0064**] Referring now to **FIG. 10, a** cross section of the interconnect **10** during testing of a semiconductor die **85** is shown. The semiconductor die **85** is an unpackaged die having a bond pad **86** formed with a metal bump **88**. For testing the die **85**, the interconnect **10** and die **85** are mounted within a temporary carrier suitable for testing discrete unpackaged semiconductor die. By way of example, a temporary carrier is described in previously cited U.S. Pat. No. 5,302,891 entitled "Discrete Die Burn-In For Non-Packaged Die", which is incorporated herein by reference. Other suitable carriers are disclosed in related application Ser. No. 08/345,064 filed Nov. 14, 1994 and entitled "Carrier For Testing An Unpackaged Semiconductor Die", which is also incorporated herein by reference. With such a carrier the interconnect **10** is used to establish a temporary electrical connection with the die **85**. The interconnect **10** and die **85** are temporarily biased together by the carrier and are separated following the test procedure.

[**0065**] Initially, the interconnect **10** is mounted within the carrier and wire **74** is wire bonded to the bond sites **73** (**FIG. 9**). (Alternately mechanical connectors **74**M-**FIG. 10** can be used.) This places the wire **74** in electrical communication with the conductive layer **66** at one end. An opposite end of the wire **74** is placed in electrical communication with external connectors (not shown) located on the carrier. This can also be accomplished by wire bonding.

[**0066**] The external connectors on the carrier are connectable to external test circuitry. The test circuitry is adapted to generate test signals for testing the operability of the integrated circuits formed on the die **85**. The carrier includes provision for aligning the die **85** and interconnect **10** and biasing the die **85** and interconnect **10** together.

[**0067**] The interconnect **10** and die **85** are biased together such that the sharpened projections **40**, **42**, **44**, **46** penetrate into the metal bump **88**. The sharpened projections **40**, **42**, **44**, **46** completely penetrate any oxide layer covering the bump **88** to establish an ohmic connection. At the same time, a penetration depth of the sharpened projections **40**, **42**, **44**, **46** into the bump **88** is limited by the stop plane **62** (**FIG. 6**) provided by the flat top surface of the conductive layer **66**.

[**0068**] Additionally, the sharpened projections **40**, **42**, **44**, **46** are dimensioned to penetrate to a predetermined depth that is less than the height of the bump **88**. Preferably the sharpened projections have a height which is much less than the diameter of the bump **88** (e.g., 1/100) to prevent excessive surface damage and spreading of the bump **88**. The bumps **88** are typically used later for flip chip bonding the die **85** to a printed circuit board. If damage to the bump **88** is minimized during testing, the bump **88** will not require a subsequent reflow process.

[**0069**] Referring now to **FIG. 10**A, an alternate embodiment interconnect **10'** is shown. The interconnect **10'** functions substantially the same as interconnect **10** but includes an indentation **90** formed in the substrate **12'** for retaining the bump **88**. The indentation **90** can be formed during formation of the sharpened projections for the contact member **43'** using an etching process. The same etch mask used to form the sharpened projections can also include an opening for forming the indentation **90**. The indentation **90** is sized to abut and retain the bump **88** during the testing procedure. This centers the bump **88** over the contact member **43'**. In addition the indentation **90** helps to prevent spreading of the bump **88** due to the penetration of the sharpened projections of the contact member **43'**.

[**0070**] Following formation of the indentation **90** and contact member **43'** an insulating layer **64'** is formed on the substrate **12'** and a conductive layer **66'** is formed over the contact member **43'** substantially as previously described. The conductive layer **66'** can be formed to overlap the indentation **90** as shown in **FIG. 10A**. In addition the conductive layer **66'** can be formed as a stack of dissimilar metals (e.g., **FIG. 8A**), as a silicide (e.g., **FIG. 8B**) or as a layer of polysilicon. Conductive traces **72'** equivalent to traces **72** (**FIG. 9**) are formed on the substrate **12'** in electrical communication with the conductive layer **66'**. Wire bonding or mechanical connectors, as previously described, can then be used to establish an electrical pathway to the conductive layer **66'**.

[**0071**] Thus the invention provides an improved method for testing a discrete, unpackaged semiconductor die having raised bond pads and an improved method for forming an interconnect for testing this type of die. Although preferred materials have been described, it is to be understood that other materials may also be utilized. Furthermore, although the method of the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.

What is claimed is:

1. A method for testing an unpackaged semiconductor die having a raised contact location electrically connected to integrated circuitry formed on the die, said method comprising:

providing a temporary carrier for the die;

providing a temporary interconnect mountable within the carrier, said interconnect having a substrate formed with a contact member, said contact member comprising at least one sharpened projection, said sharpened projection formed on an insulating layer of the substrate and dimensioned to penetrate the contact location to a limited penetration depth, said sharpened projection covered with a conductive layer in electrical communication with a conductive trace formed on the substrate;

mounting the die and interconnect within the carrier with the sharpened projection penetrating into the raised contact location on the die to the limited penetration depth to establish a temporary electrical connection therewith;

establishing an electrical path between the conductive trace and test circuitry; and

testing the integrated circuitry by applying test signals through the raised bond pad.

2. The method as claimed in claim 1 and wherein the contact member on the substrate includes a plurality of elongated sharpened projections.

3. The method as claimed in claim 2 and wherein the sharpened projections are formed as elongated blades.

4. The method as claimed in claim 1 and wherein the substrate is formed of a material selected from the group consisting of silicon, germanium, a ceramic, silicon-on-sapphire, and silicon-on-glass.

5. The method as claimed in claim 1 and wherein the sharpened projection is formed in an indentation in the substrate, said indentation adapted to contact and retain the raised contact location.

6. The method as claimed in claim 5 and wherein the indentation is formed by etching the substrate.

7. The method as claimed in claim 1 and wherein the sharpened projection is formed by forming a mask on the substrate and etching the substrate through openings in the mask.

8. The method as claimed in claim 1 and wherein the sharpened projection is formed by forming a mask on the substrate, growing an oxide on the substrate in areas of the substrate exposed by the mask and then removing the oxide.

9. The method as claimed in claim 1 and wherein the conductive layer is formed as a stack of metals including a barrier metal adjacent to the insulating layer and a bonding metal for connection to the conductive traces.

10. The method as claimed in claim 1 and wherein the conductive layer is formed as a silicide.

11. The method as claimed in claim 1 and wherein the conductive layer is formed of polysilicon.

12. A method for fabricating an interconnect suitable for establishing a temporary electrical connection with a semiconductor die having a raised contact location, said method comprising:

forming a substrate;

forming a contact member on the substrate including at least one elongated sharpened projection, said sharpened projection formed and dimensioned to penetrate into the raised contact location to a limited penetration depth;

forming an insulating layer on the substrate and sharpened projection;

forming a conductive layer on the sharpened projection; and

forming a conductive trace on the substrate in electrical communication with the conductive layer.

13. The method as claimed in claim 12 and wherein the contact member includes a plurality of sharpened projections arranged in a spaced array.

14. The method as claimed in claim 12 and wherein the sharpened projection is formed by an etching process in which a mask is formed on the substrate and the substrate is etched through openings in the mask.

15. The method as claimed in claim 14 and wherein the etch process is an anisotropic etch.

16. The method as claimed in claim 14 and wherein the etch process is an isotropic etch.

17. The method as claimed in claim 12 and wherein the sharpened projection is formed by an oxidation process in which a mask is formed on the substrate, an oxide is grown on the substrate in openings in the mask and then the oxide is removed.

18. The method as claimed in claim 12 and wherein the conductive layer is formed as a stack of metals.

19. The method as claimed in claim 12 and wherein the conductive layer is formed of a metal silicide.

20. The method as claimed in claim 12 and wherein the conductive layer and conductive traces are formed by depositing a metal layer on the substrate, patterning the metal layer and then etching the metal layer.

21. The method as claimed in claim 12 and wherein the sharpened projection is formed in an indentation formed in the substrate and adapted to contact and retain the indentation.

22. The method as claimed in claim 21 and wherein the indentation is formed by etching the substrate.

23. A method for fabricating an interconnect suitable for establishing a temporary electrical connection with a semiconductor die having a raised contact location, said method comprising:

providing a substrate;

forming a mask on the substrate and etching the substrate through exposed areas of the mask to form an array of elongated sharpened projections on the substrate, said sharpened projections dimensioned to penetrate into the raised contact location to a limited penetration depth;

forming an insulating layer over the substrate and sharpened projections;

forming a conductive layer on the insulating layer and over the sharpened projections; and

forming a conductive trace on the substrate in electrical communication with the conductive layer.

24. The method as claimed in claim 23 and wherein the conductive layer and conductive trace are formed by depositing a conductive metal on the substrate and etching the conductive metal.

25. The method as claimed in claim 23 and wherein the conductive layer is a metal silicide layer formed by forming a silicon containing layer on the substrate, depositing a metal layer on the silicon containing layer, reacting the metal layer and silicon containing layer to form the metal silicide layer, and then etching an unreacted portion of the metal layer and the silicon containing layer selective to the metal silicide layer.

26. The method as claimed in claim 23 and further comprising annealing the metal silicide layer to lowers its resistivity.

27. The method as claimed in claim 23 and wherein the conductive layer is a stack of metals formed by depositing a first metal layer and a second metal layer on the substrate and then etching through the first and second metal layers.

28. The method as claimed in claim 27 and wherein the first metal layer is formed of a metal which functions as a barrier layer to prevent reaction with the contact location and formation of an oxide and the second metal layer is formed of a metal which functions as a bonding layer for the conductive traces

29. The method as claimed in claim 27 and wherein the first metal layer is selected from the group consisting of platinum and titanium.

30. The method as claimed in claim 29 and wherein the second metal layer is selected from the group consisting of aluminum and tungsten.

31. The method as claimed in claim 23 and wherein each array of sharpened projections is formed in an indentation in the substrate sized to support and retain the raised contact location.

32. The method as claimed in claim 31 and wherein the indentation are formed by etching the substrate.

33. The method as claimed in claim 31 and wherein during etching of the substrate to form the sharpened projections, the indentations are formed in the substrate and support each array of sharpened projections is located within an indentation.

34. The method as claimed in claim 23 and wherein the conductive layer is formed of a first metal and the conductive traces are formed of a second metal.

35. The method as claimed in claim 23 and wherein the raised contact location on the die is a conductive bump.

36. The method as claimed in claim 23 and wherein the substrate is formed of a material selected from the group consisting of silicon, silicon-on-sapphire, silicon-on-glass and germanium.

37. The method as claimed in claim 23 and wherein the conductive layer is formed of polysilicon.

38. The method as claimed in claim 23 and wherein the sharpened projections are formed by an anisotropic etch process as elongated blades having a sharp edge.

39. The method as claimed in claim 23 and wherein the sharpened projections are formed by an isotropic etch process with radiused sidewalls.

40. The method as claimed in claim 23 and wherein the sharpened projections are formed by an anisotropic etch and have a truncated pyramidal cross section with a flat tip portion.

41. The method as claimed in claim 23 and wherein the sharpened projections are formed by an anisotropic etch in a saw tooth array with base portions that abut one another.

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