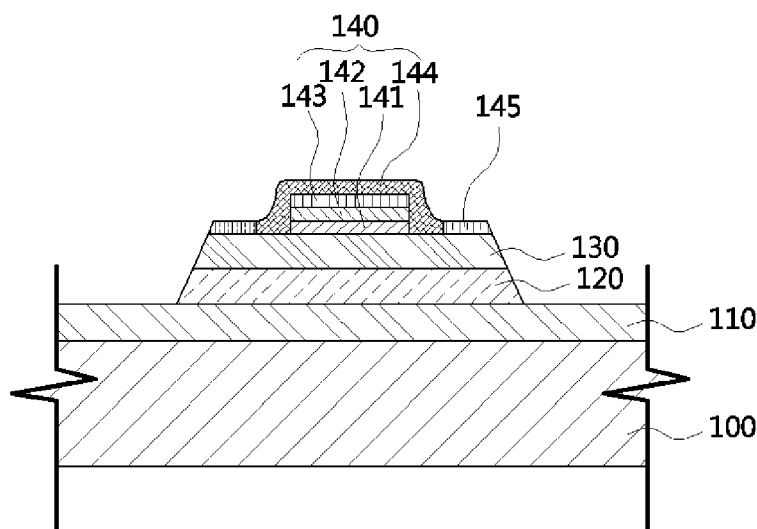




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- (71) **Applicant:** SEOUL OPTO DEVICE CO., LTD.
[KR/KR]; #36, 1Block, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR).
- (72) **Inventors:** CHAE, Jong Hyeon; #36, 1Block, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR). JANG, Jong Min; #36, 1Block, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR). ROH, Won Young; #36, 1Block, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR). SUH, Dae Woong; #36, 1Block, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR). KANG, Min Woo; #36, 1Block, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR). LEE, Joon Sub; #36, 1Block, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR). KIM, Hyun A; #36, 1Block, 727-5, Wonsi-dong, Danwon-gu, Ansan-si, Gyeonggi-do 425-851 (KR).
- (74) **Agent:** E-SANG PATENT & TRADEMARK LAW FIRM; 3F., Woodo Bldg., 82-2 Yangjae-dong, Seocho-gu, Seoul 137-890 (KR).
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(54) **Title:** LIGHT EMITTING DIODE FOR SURFACE MOUNT TECHNOLOGY, METHOD OF MANUFACTURING THE SAME, AND METHOD OF MANUFACTURING LIGHT EMITTING DIODE MODULE



(57) **Abstract:** Provided are a light emitting diode (LED) in which a conductive barrier layer configured to surround a reflective metal layer is defined by a protective insulating layer, and a method of manufacturing the same. A reflection pattern including a reflective metal layer and a conductive barrier layer is formed on an emission structure in which a first semiconductor layer, an active layer, and a second semiconductor layer are formed. The conductive barrier layer prevents diffusion of a reflective metal layer and extends to a protective insulating layer recessed under a photoresist pattern having an overhang structure during a forming process. Accordingly, a phenomenon where the conductive barrier layer is in contact with sidewalls of the photoresist pattern having an overhang structure and the reflective metal layer forms points is prevented. Thus, LED modules having various shapes may be manufactured.

Description

Title of Invention: LIGHT EMITTING DIODE FOR SURFACE MOUNT TECHNOLOGY, METHOD OF MANUFACTURING THE SAME, AND METHOD OF MANUFACTURING LIGHT EMITTING DIODE MODULE

Technical Field

- [1] The present invention relates to a light emitting diode (LED), and more particularly, to an LED for surface mounting.

Background Art

- [2] A light emitting diode (LED) is a device including an n-type semiconductor layer, a p type semiconductor layer, and an active layer interposed between the n type and p type semiconductor layers. When a forward electric field is applied to the n type and p type semiconductor layers, electrons and holes may be injected into the active layer and re-combine in the active layer to emit light.
- [3] In addition, an LED may include a reflection layer according to the type of a chip. That is, a flip-chip type is characterized by emitting light through a substrate. Accordingly, after a semiconductor layer is formed on the substrate, a reflection layer formed of a metal is introduced on the semiconductor layer or a current spreading layer, and light is reflected by the reflection layer. Also, a barrier layer is provided on the reflection layer. The barrier layer is provided to prevent diffusion of the metal forming the reflection layer.
- [4] Figs. 1 and 2 are cross-sectional views of a conventional LED including a reflection layer and a barrier layer.
- [5] Referring to Fig. 1, a first semiconductor layer 20, an active layer 30, a second semiconductor layer 40, a reflection layer 50, and a barrier layer 60 are formed on a substrate 10.
- [6] The substrate 10 is generally formed of a sapphire material, and the first semiconductor layer 20 is an n type. The active layer 30 having a typical multi-quantum well (MQW) structure is formed on the first semiconductor layer 20. Also, the p type second semiconductor layer 40 is formed on the active layer 30.
- [7] The LED having the above-described structure is mesa-etched to expose a top surface of the first semiconductor layer 20. Also, photoresist patterns 70 having an overhang structure is formed on the top surface of the first semiconductor layer 20, which is exposed by mesa-etching.
- [8] The second semiconductor layer 40 is exposed in a space in which the photoresist

patterns 70 are spaced apart from each other, and the reflection layer 50 is formed on the exposed surface of the second semiconductor layer 40. The reflection layer 50 is formed using a typical process, such as a sputtering process, on the surface of the second semiconductor layer 40 through the space in which the photoresist patterns 70 are spaced apart from each other. Furthermore, an ohmic contact layer may be additionally formed under the reflection layer 50. The ohmic contact layer may be formed of a material selected so as to form an ohmic contact between the reflection layer 50 and the second semiconductor layer 40.

[9] Thereafter, the barrier layer 60 is formed to surround top and side surfaces of the reflection layer 50. The barrier layer 60 may be formed using a sputtering process. The barrier layer 60 functions to prevent diffusion of metal atoms forming the reflection layer 50, and is formed of a conductive metal. Since the barrier layer 60 has predetermined diffusivity or isotropic diffusivity due to the sputtering process, the barrier layer 60 surrounds the top and side surfaces of the reflection layer 50 and is also formed on the exposed surface of the second semiconductor layer 40. Also, the barrier layer 60 is accumulated on edge portions of the photoresist patterns 70 having an overhang structure. The barrier layer 60 is adhered to sidewalls of the photoresist pattern 70 and deposited in pointed shapes on the edge portions of the photoresist patterns 70.

[10] Referring to Fig. 2, the photoresist patterns disclosed in Fig. 1 are removed to perform subsequent processes. By removing the photoresist patterns, points 80 of the barrier layer 60 having the pointed shapes are exposed. The exposed points 80 of the barrier layer 60 form fine particles during subsequent processes. Metallic particles increase contamination during subsequent processes and reduce yield.

[11] Accordingly, a technique of removing the points 80 during the formation of the barrier layer 60 and increasing yield is required.

Disclosure of Invention

Technical Problem

[12] The present invention is directed to a light emitting diode (LED) having a conductive barrier layer defined by a protective insulating layer.

[13] The present invention is also directed to a method of manufacturing an LED, which is used to attain the first objective.

[14] Furthermore, the present invention is directed to a method of manufacturing an LED module using the LED provided by attaining the first objective.

Solution to Problem

[15] A first aspect of the present invention provides an LED including: a substrate, a first semiconductor layer formed on the substrate, an active layer formed on the first semi-

conductor layer and configured to generate light, a second semiconductor layer formed on the active layer and having a complementary conductive type to the first semiconductor layer, and a reflection pattern formed between protective insulating layers formed on the second semiconductor layer and configured to reflect light generated in the active layer, the reflection pattern having a conductive barrier layer contacting the protective insulating layer.

- [16] A second aspect of the present invention provides, a method of manufacturing an LED including: sequentially forming a first semiconductor layer, an active layer, a second semiconductor layer, and a protective insulating layer on a substrate, etching the protective insulating layer, the second semiconductor layer, and the active layer and forming a mesa region exposing a surface of the first semiconductor layer, forming photoresist patterns having an overhang structure on the mesa region and etching the protective insulating layer exposed through a space between the photoresist patterns, forming a reflective metal layer on a surface of the second semiconductor layer that is exposed by etching the protective insulating layer, and forming a conductive barrier layer on the reflective metal layer, the conductive barrier layer extending to the protective insulating layer remaining under the photoresist pattern.
- [17] A third aspect of the present invention provide a method of manufacturing an LED including: sequentially forming a first semiconductor layer, an active layer, and a second semiconductor layer on a substrate, etching the second semiconductor layer and the active layer and forming a mesa region exposing a surface of the first semiconductor layer, forming a protective insulating layer on the mesa region and the exposed second semiconductor layer, forming photoresist patterns having an overhang structure on the mesa region and etching the protective insulating layer exposed through a space between the photoresist patterns, forming a reflective metal layer on a surface of the second semiconductor layer that is exposed by etching the protective insulating layer, and forming a conductive barrier layer on the reflective metal layer, the conductive barrier layer extending to the protective insulating layer remaining under the photoresist pattern.
- [18] A fourth aspect of the present invention provides a method of manufacturing an LED module including: coating a first insulating layer on a structure in which a first semiconductor layer, an active layer, a second semiconductor layer, and a reflection pattern are formed on a substrate and exposing the reflection pattern and the first semiconductor layer, forming a conductive reflection layer and a reflective barrier layer on the first insulating layer, the reflective barrier layer electrically connected to the first semiconductor layer through the conductive reflection layer and configured to expose the reflection pattern, coating a second insulating layer on the reflective barrier layer to expose the reflection pattern and exposing the reflective barrier layer electrically

connected to the first semiconductor layer, and forming a first pad on the reflective barrier layer and forming a second pad on the reflection pattern.

Advantageous Effects of Invention

- [19] According to the present invention, protective insulating layers are formed on an emission structure including a first semiconductor layer, an active layer, and a second semiconductor layer, and a reflection pattern including a conductive barrier layer is formed between protective insulating layers.
- [20] The reflection pattern includes a reflective metal layer, a stress relaxation layer, and a conductive barrier layer. The conductive barrier layer penetrates into a lower portion of a photoresist pattern having an overhang structure during a forming process. Accordingly, the conductive barrier layer is in contact with a protective insulating layer recessed to a portion of the lower portion of the photoresist pattern. Thus, protrusion of the conductive barrier layer is prevented. Thus, process contamination caused by generation of metal particles and a drop in yield can be prevented.
- [21] In addition, a reflective barrier layer configured to prevent diffusion of a metallic substance formed on a conductive reflection layer during manufacture of an LED module. The reflective barrier layer is electrically connected to a first semiconductor layer and electrically connected to a first pad that will be subsequently formed.
- [22] Furthermore, a pad barrier layer is formed on each of pads. Accordingly, permeation or diffusion of metal atoms during a soldering process or a bonding process is inhibited, and the pads can ensure a high conductivity.
- [23] Aspects of the present invention should not be limited by the above description, and other unmentioned aspects will be clearly understood by one of ordinary skill in the art from exemplary embodiments described herein.

Brief Description of Drawings

- [24] Figs. 1 and 2 are cross-sectional views of a conventional light emitting diode (LED) including a reflection layer and a barrier layer.
- [25] Fig. 3 is a cross-sectional view of an LED according to a first exemplary embodiment of the present invention.
- [26] Figs. 4 through 9 are cross-sectional views illustrating a method of manufacturing the LED of Fig. 3, according to the first exemplary embodiment of the present invention.
- [27] Fig. 10 is a cross-sectional view of an LED according to a second exemplary embodiment of the present invention.
- [28] Figs. 11 through 16 are cross-sectional views illustrating a method of manufacturing the LED of Fig. 10, according to the second exemplary embodiment of the present invention.
- [29] Fig. 17 is a cross-sectional view of an LED according to a third exemplary em-

bodiment of the present invention.

[30] Figs. 18 through 22 are cross-sectional views illustrating a method of manufacturing the LED of Fig. 17, according to the third exemplary embodiment of the present invention.

[31] Figs. 23 through 27 illustrate plan views and cross-sectional views of LED modules to which the structure of Fig. 3 or Fig. 10 is applied, according to a fourth exemplary embodiment of the present invention.

[32] Figs. 28 through 30 illustrate plan views and cross-sectional views of LED modules to which the structure of Fig. 3 or Fig. 10 is applied, according to a fifth exemplary embodiment of the present invention.

Mode for the Invention

[33] Hereinafter, exemplary embodiments of the present invention will be described in detail. It should be understood, however, that there is no intent to limit the invention to the particular forms disclosed.

[34] It will be understood that when a layer is referred to as being on another layer or substrate, it can be directly on the other layer or substrate or intervening layers may also be present. Terms that describe spatial relationships, such as "on", "upper", "top surface", "under", "lower", "bottom surface" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the Figures. It will be understood that such terms are intended to encompass different orientations of the device in use or operation in addition to the orientation(s) depicted in the Figures. For example, if the device in the Figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the term "below" can encompass both an orientation of above and below. The orientation of the device may be changed in other ways (e.g., rotated 90 degrees or some other angle) and spatial relationships described herein should be interpreted within the context of the changed orientation.

[35] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms.

[36] In the drawings, the thicknesses of layers and regions may be exaggerated for clarity. Like reference numerals refer to like elements throughout.

[37]

Embodiment 1

[39] Fig. 3 is a cross-sectional view of a light emitting diode (LED) according to a first exemplary embodiment of the present invention.

[40] Referring to Fig. 3, a first semiconductor layer 110, an active layer 120, a second

semiconductor layer 130, and a reflection pattern 140 are formed on a substrate 100.

[41] The substrate 100 may be formed of any material capable of inducing the first semiconductor layer 110 to be grown. Accordingly, the substrate 100 may include sapphire (Al_2O_3), silicon carbide (SiC), gallium nitride (GaN), indium gallium nitride (InGaN), aluminum gallium nitride (AlGaN), aluminum nitride (AlN), gallium oxide (Ga_2O_3), or silicon. Specifically, the substrate 100 may be a sapphire substrate.

[42] Also, the substrate 100 may be a substrate on which surface treatment is not performed. The substrate 100 may be a patterned substrate.

[43] In addition, the first semiconductor layer 110 is provided on the substrate 100. The first semiconductor layer 110 preferably is an n type.

[44] Furthermore, the active layer 120 formed on the first semiconductor layer 110 may have a single quantum well (SQW) structure in which a well layer and a barrier layer are stacked, or an MQW structure in which well layers and barrier layers are alternately stacked.

[45] The second semiconductor layer 130 is provided on the active layer 120. The second semiconductor layer 130 preferably is a p type.

[46] Furthermore, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 may include Si, GaN, AlN, InGaN, or AlInGaN. When the first semiconductor layer 110 includes GaN, the active layer 120 and the second semiconductor layer 130 preferably include GaN. However, since the second semiconductor layer 130 has a complementary conductivity type to the first semiconductor layer 110, a different dopant from that of the first semiconductor layer 110 is introduced into the second semiconductor layer 130. That is, when a dopant serving as a donor is introduced into the first semiconductor layer 110, a dopant serving as an acceptor is introduced into the second semiconductor layer 130. Also, the active layer 120 preferably includes a material on which bandgap engineering is performed to form barrier layers and well layers.

[47] The reflection pattern 140 is formed on the second semiconductor layer 130.

[48] The reflection pattern 140 includes an ohmic contact layer 141, a reflective metal layer 142, a stress relaxation layer 143, or a conductive barrier layer 144.

[49] The ohmic contact layer 141 may be formed of any material capable of enabling an ohmic contact between the reflective metal layer 142 and the second semiconductor layer 130. Accordingly, the ohmic contact layer 141 may include a metal including nickel (Ni) or platinum (Pt), or include a conductive oxide, such as indium tin oxide (ITO) or zinc oxide (ZnO). However, the ohmic contact layer 141 may be omitted in some embodiments.

[50] The reflective metal layer 142 is formed on the ohmic contact layer 141. The reflective metal layer 142 reflects light generated by the active layer 120. Accordingly,

the reflective metal layer 142 is formed by selecting a material having conductivity and a high optical reflectance. The reflective metal layer 142 includes Ag, an Ag alloy, Al, or an Al alloy.

- [51] In addition, the stress relaxation layer 143 may be formed on the reflective metal layer 142. The stress relaxation layer 143 preferably has a coefficient of thermal expansion equal to or higher than that of the conductive barrier layer 144, and equal to or lower than that of the reflective metal layer 142. Thus, stress caused due to a difference in coefficient of thermal expansion between the reflective metal layer 142 and the conductive barrier layer 144 may be reduced. Accordingly, a material forming the stress relaxation layer 143 may be differently selected according to selected materials forming the reflective metal layer 142 and the conductive barrier layer 144.
- [52] However, the ohmic contact layer 141 or the stress relaxation layer 143 may be omitted in some embodiments.
- [53] A conductive barrier layer 144 is formed on the reflective metal layer 142 or the stress relaxation layer 143. For example, when the stress relaxation layer 143 is omitted, the conductive barrier layer 144 is formed on the reflective metal layer 142. When the stress relaxation layer 143 is formed, the conductive barrier layer 144 is formed on the stress relaxation layer 143. The conductive barrier layer 144 is formed to surround at least side surfaces of the reflective metal layer 142 and top and side surfaces of the stress relaxation layer 143. Accordingly, diffusion of metal atoms or ions constituting the reflective metal layer 142 is prevented. Also, stress caused due to a difference in coefficient of thermal expansion between the conductive barrier layer 144 and the reflective metal layer 142 is absorbed in the stress relaxation layer 143.
- [54] For example, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes tungsten (W), titanium tungsten (TiW), or molybdenum (Mo), the stress relaxation layer 143 may be a single layer formed of silver (Ag), copper (Cu), nickel (Ni), platinum (Pt), titanium (Ti), rhodium (Rh), palladium (Pd), or chromium (Cr), or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd or Au. Also, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes Cr, Pt, Rh, Pd, or Ni, the stress relaxation layer 143 may be a single layer formed of Ag or Cu, or a combination formed of Ni, Au, Cu, or Ag.
- [55] Furthermore, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd, Cr, or Au. Also, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes Cr or Ni, the stress relaxation layer 143 may be a single layer formed of Cu, Cr, Rh, Pd, TiW, or Ti, or a

combination formed of Ni, Au, or Cu.

- [56] In addition, the conductive barrier layer 144 is formed to coat a surface of the second semiconductor layer 130 and extend to side surfaces of a protective insulating layer 145. However, the conductive barrier layer 144 is preferably formed to contact the side surfaces of the protective insulating layer 145 but not in such a shape as to coat a top surface of the protective insulating layer 145.
- [57] Figs. 4 through 9 are cross-sectional views illustrating a method of manufacturing the LED of Fig. 3, according to a first exemplary embodiment of the present invention.
- [58] Referring to Fig. 4, a first semiconductor layer 110, an active layer 120, a second semiconductor layer 130, and a protective insulating layer 145 are sequentially formed on a substrate 100.
- [59] The substrate 100 may include sapphire (Al_2O_3), silicon carbide (SiC), gallium nitride (GaN), indium gallium nitride (InGaN), aluminum gallium nitride (AlGaN), aluminum nitride (AlN), gallium oxide (Ga_2O_3), or silicon. Specifically, the substrate 100 may be a sapphire substrate. Also, the substrate 100 may be a patterned substrate.
- [60] Also, the first semiconductor layer 110 is provided on the substrate 100. The first semiconductor layer 110 preferably has an n conductivity type.
- [61] In addition, the active layer 120 formed on the first semiconductor layer 110 may have an SQW structure in which a well layer and a barrier layer are stacked, or an MQW structure in which well layers and barrier layers are alternately stacked.
- [62] The second semiconductor layer 130 is provided on the active layer 120. The second semiconductor layer 130 preferably has a p conductivity type.
- [63] Furthermore, materials and constructions of the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 are the same as described with reference to Fig. 3, and thus a description thereof is omitted.
- [64] In addition, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 are formed using an epitaxial growth process. Accordingly, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 are preferably formed using a metal organic chemical vapor deposition (MOCVD) process.
- [65] Also, the protective insulating layer 145 is formed on the second semiconductor layer. The protective insulating layer may be formed of any insulating material. Accordingly, the protective insulating layer 145 may be formed of silicon oxide or silicon nitride. In addition, the protective insulating layer 145 may be formed of any insulating material having an etch selectivity with respect to the underlying second semiconductor layer 130, active layer 120, or first semiconductor layer 110 and an insulating characteristic.
- [66] In addition, the protective insulating layer 145 may be formed using various

methods, such as a spin coating process, a physical vapor deposition (PVD) process, a CVD process, or an atomic layer deposition (ALD) process.

[67] Referring to Fig. 5, portions of the active layer 120, the second semiconductor layer 130, and the protective insulating layer 145 are removed using an ordinary etching process. Thus, a portion of the first semiconductor layer 110 is exposed. Due to the etching process, a top surface of the first semiconductor layer 110 is exposed, side surfaces of the active layer 120 and the second semiconductor layer 130 are exposed, and top and side surfaces of the active layer 120 and the second semiconductor layer 130 are exposed, and top and side surfaces of the protective insulating layer 145 are exposed. Accordingly, a trench or a hole may be formed by removing the portions of the active layer 120, the second semiconductor layer 130, and the protective insulating layer 145 using the etching process. That is, a mesa region 150 etched from the surface of the protective insulating layer 145 of Fig. 5 to the surface of the first semiconductor layer 110 may be a stripe type having a trench shape or a hole type.

[68] In addition, when the mesa region 150 is the stripe type, the mesa region 150 may have a vertical profile or inclined profile with respect to the surface of the first semiconductor layer 110. Preferably, the mesa region 150 has a profile inclined at an angle of about 20° to about 70° with respect to the surface of the first semiconductor layer 110. Also, when the mesa region 150 is a hole type having a roughly circular shape, the mesa region 150 may have a vertical profile or inclined profile with respect to the surface of the first semiconductor layer 110. Preferably, the mesa region 150 has a profile inclined at an angle of about 20° to about 70° with respect to the surface of the first semiconductor layer 110. When the profile is inclined at an angle of less than 20° , a width of the mesa region 150 greatly increases upward. Accordingly, convergence of light generated is degraded due to an emission structure. Also, when the profile is inclined at an angle of more than 70° , the mesa region 150 has an approximately vertical profile. Accordingly, the effect of reflection of generated light by sidewalls of layers become immaterial.

[69] Referring to Fig. 6, a photoresist pattern 160 is formed on the first semiconductor layer 110 exposed by forming a bottom surface of the mesa region 150. The photoresist pattern 160 may have a vertical profile with respect to the surface of the first semiconductor layer 110. In some embodiments, the photoresist pattern 160 may be formed to have an overhang structure having a bottom surface with a smaller width than a top surface thereof. The photoresist pattern 160 is preferably a negative type. Accordingly, exposed portions are cross-linked. To form the overhang structure, the photoresist pattern 160 is preferably exposed at a predetermined angle. In the case of the overhang structure, a distance between bottom surfaces of the photoresist patterns 160 is preferably set to be at least about 1 μm greater than a distance between top

surfaces thereof.

- [70] Furthermore, the photoresist pattern 160 is preferably provided to cover a portion of the surface of the protective insulating layer 145. Accordingly, the portion of the top surface of the protective insulating layer 145 may remain shielded by the photoresist pattern 160.
- [71] Referring to Fig. 7, an etching process is performed on the protective insulating layer 145 exposed by a space between the photoresist patterns 160. Although the etching process may be performed using a wet process or a dry process, the etching process is preferably performed using a wet etching process. Also, due to the etching process, a large portion of the protective insulating layer 145 formed on the surface of the second semiconductor layer 130 may be removed, and a portion of the surface of the second semiconductor layer 130 is exposed. However, the protective insulating layer 145 formed at corners disposed under the photoresist pattern 160 remains. Accordingly, a space is formed between a lower portion of the photoresist pattern 160 and the second semiconductor layer 130 due to the etching process, and the protective insulating layer 145 remains at an end of the space. Since the wet etching process has isotropic etching characteristics, it may take a considerable amount of time or be troublesome to etch the protective insulating layer 145 formed on the corners disposed under the photoresist pattern 160. Accordingly, the protective insulating layer 145 exposed by the photoresist pattern 160 due to the anisotropic etching process is mostly removed, while only the protective insulating layer 145 recessed under the photoresist pattern 160 remains.
- [72] Referring to Fig. 8, a reflective metal layer 142 and a stress relaxation layer 143 are sequentially stacked on the second semiconductor layer 130.
- [73] The reflective metal layer 142 includes Al, an Al alloy, Ag, or an Ag alloy. The reflective metal layer 142 may be formed using an ordinary metal deposition process. However, the reflective metal layer 142 is preferably formed using an electronic beam (e-beam) evaporation process capable of moving most metal atoms or ions onto the surface of the second semiconductor layer 130 in a vertical direction. Thus, the metal atoms or ions may have anisotropic etching characteristics and enter a space between the photoresist patterns 160 to form the reflective metal layer 142.
- [74] The reflective metal layer 142 preferably has a thickness of about 100 nm to about 1 μ m. When the reflective metal layer 142 has a thickness of less than about 100 nm, light generated by the active layer 120 is not smoothly reflected. Also, when the reflective metal layer 142 has a thickness of more than about 1 μ m, process loss may occur due to an excessive process time.
- [75] The ohmic contact layer 141 may be formed before forming the reflective metal layer 142, as needed. The ohmic contact layer 141 may include Ni, Pt, ITO, or ZnO. Also,

the ohmic contact layer 141 is preferably formed to a thickness of about 0.1 nm to about 20 nm. When the ohmic contact layer 141 has a thickness of less than about 0.1 nm, sufficient ohmic characteristics cannot be ensured due to a very small layer thickness. Also, when the ohmic contact layer 141 has a thickness of more than about 20 nm, the transmitted amount of light is reduced to reduce the quantity of light reflected by the reflective metal layer 142 disposed on the ohmic contact layer 141.

[76] The stress relaxation layer 143 is formed on the reflective metal layer 142.

[77] The stress relaxation layer 143 may be formed using an ordinary metal deposition process, but is preferably formed using an e-beam evaporation method having a high directionality during a deposition process. That is, metal atoms or ions evaporated due to e-beams may have directionality and have anisotropy in a space between the photoresist patterns 160, and the stress relaxation layer 143 may be formed of a metal layer. Also, the stress relaxation layer 143 may have a lower coefficient of thermal expansion than the reflective metal layer 142 and a higher coefficient of thermal expansion than the conductive barrier layer 144 of Fig. 3. Accordingly, a material forming the stress relaxation layer 143 may be differently selected according to selected materials forming the reflective metal layer 142 and the conductive barrier layer 144. The material forming the stress relaxation layer 143 will be described later.

[78] When the reflective metal layer 142 and the stress relaxation layer 143 are formed using an e-beam evaporation method, a side surface of the reflective metal layer 142 and a side surface of the stress relaxation layer 143 are exposed. Also, the reflective metal layer 142 and the stress relaxation layer 143 corresponding to an open upper region of the photoresist pattern 160 are formed using an anisotropic deposition process.

[79] Subsequently, a conductive barrier layer 144 is formed through the opened region of the photoresist pattern 160.

[80] The conductive barrier layer 144 includes W, TiW, Mo, Cr, Ni, Pt, Rh, Pd, or Ti. In particular, a material forming the conductive barrier layer 144 may be differently selected according to selected materials forming the reflective metal layer 142 and the stress relaxation layer 143.

[81] The conductive barrier layer 144 is formed on the stress relaxation layer 143 and shields side surfaces of the reflective metal layer 142 and the stress relaxation layer 143. Accordingly, a metal forming the reflective metal layer 142 is prevented from diffusing into the second semiconductor layer 130 due to lateral diffusion. The formation of the conductive barrier layer 144 is performed using an ordinary metal deposition process. However, the conductive barrier layer 144 is preferably formed using an isotropic etching process. This is because the conductive barrier layer 144 is configured to surround the side surfaces of the stress relaxation layer 143 and the re-

reflective metal layer 142. For example, the conductive barrier layer 144 may be formed using a sputtering process.

- [82] In addition, the conductive barrier layer 144 may be a single layer formed to a thickness of about 100 nm or more by selecting a specific metal. Also, the conductive barrier layer 144 may be formed by alternately selecting at least two metal materials, and each of layers forming the conductive barrier layer 144 may be formed to a thickness of about 20 nm or more. For example, the conductive barrier layer 144 may be formed by alternately depositing a TiW layer having a thickness of about 50 nm and a Ni layer or Ti layer having a thickness of about 50 nm.
- [83] Furthermore, a Ni/Au/Ti layer may be additionally formed on the conductive barrier layer 144 to enable a stable contact of the conductive barrier layer 144 with a subsequent material.
- [84] As described above, a material forming the stress relaxation layer 143 may be selected according to materials forming the reflective metal layer 142 and the conductive barrier layer 144. This is because a coefficient of thermal expansion of the stress relaxation layer 143 is higher than that of the conductive barrier layer 144 and lower than that of the reflective metal layer 142. Accordingly, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Ag, Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd or Au. Also, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes Ti, Cr, Pt, Rh, Pd, or Ni, the stress relaxation layer 143 may be a single layer formed of Ag or Cu, or a combination formed of Ni, Au, Cu, or Ag.
- [85] Furthermore, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd, Cr, or Au. Also, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes Cr or Ni, the stress relaxation layer 143 may be a single layer formed of Cu, Cr, Rh, Pd, TiW, or Ti, or a combination formed of Ni, Au, or Cu.
- [86] In addition, since the conductive barrier layer 144 is formed using a deposition process, such as a sputtering process, the conductive barrier layer 144 is formed to fill an edge region of the photoresist pattern 160. That is, the conductive barrier layer 144 is formed to fill a space between the photoresist pattern 160 and the second semiconductor layer 130. By filling the space, the protective insulating layer 145 and the conductive barrier layer 144 are physically in contact with each other. Also, due to the deposition process, the conductive barrier layer 144 may be formed along shapes of surfaces of the second semiconductor layer 130, the reflective metal layer 142, and the

stress relaxation layer 143.

[87] The ohmic contact layer 141, the reflective metal layer 142, the stress relaxation layer 143, and the conductive barrier layer 144 may be formed also on the photoresist pattern 160.

[88] Referring to Fig. 9, a lift-off process is performed on the photoresist pattern 160 to remove the photoresist pattern 160 and the layers disposed thereon. Accordingly, the underlying second semiconductor layer 130 and the reflection pattern 140 disposed thereon are exposed. Also, the mesa region 150 is exposed by removing the photoresist pattern 160. As described above, the mesa region 150 may be a stripe type or a hole type. Also, a protective insulating layer 145 is provided on side surfaces of the reflection pattern 140. The conductive barrier layer 144 of the reflection pattern 140 may be defined by the protective insulating layer 145.

[89] Due to the above-described processes, the reflection pattern 140 is formed on the second semiconductor layer 130. The reflection pattern 140 includes a reflective metal layer 142, a stress relaxation layer 143, and a conductive barrier layer 144. The stress relaxation layer 143 has a lower coefficient of thermal expansion than the reflective metal layer 142 and a higher coefficient of thermal expansion than the conductive barrier layer 144. Accordingly, stress caused due to a difference in coefficient of thermal expansion between the reflective metal layer 142 and the conductive barrier layer 144 is absorbed in the stress relaxation layer 143.

[90] In addition, formation of protruding points shown in Figs. 1 and 2 is excluded from the conductive barrier layer 144 formed on the reflective metal layer 142 or the stress relaxation layer 143. Accordingly, generation of metal particles is inhibited in subsequent processes to maintain a high yield.

[91]

[92] Embodiment 2

[93] Fig. 10 is a cross-sectional view of an LED according to a second exemplary embodiment of the present invention.

[94] Referring to Fig. 10, a first semiconductor layer 110, an active layer 120, a second semiconductor layer 130, a reflection pattern 140, and a protective insulating layer 145 are formed on a substrate 100.

[95] The substrate 100 may be formed of any material capable of inducing the first semiconductor layer 110 to be grown. Accordingly, the substrate 100 may include sapphire (Al_2O_3), silicon carbide (SiC), gallium nitride (GaN), indium gallium nitride (InGaN), aluminum gallium nitride (AlGaN), aluminum nitride (AlN), gallium oxide (Ga_2O_3), or silicon. Specifically, the substrate 100 may be a sapphire substrate.

[96] Also, the substrate 100 may be a substrate on which surface treatment is not performed. The substrate 100 may be a patterned substrate.

- [97] In addition, the first semiconductor layer 110 is provided on the substrate 100. The first semiconductor layer 110 preferably has an n conductivity type.
- [98] Furthermore, the active layer 120 formed on the first semiconductor layer 110 may have an SQW structure in which a well layer and a barrier layer are stacked, or an MQW structure in which well layers and barrier layers are alternately stacked.
- [99] The second semiconductor layer 130 is provided on the active layer 120. The second semiconductor layer 130 preferably has a p conductivity type.
- [100] Furthermore, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 may include Si, GaN, AlN, InGaN, or AlInGaN. When the first semiconductor layer 110 includes GaN, the active layer 120 and the second semiconductor layer 130 preferably include GaN. However, since the second semiconductor layer 130 has a complementary conductivity type to the first semiconductor layer 110, a different dopant from that of the first semiconductor layer 110 is introduced into the second semiconductor layer 130. That is, when a dopant serving as a donor is introduced into the first semiconductor layer 110, a dopant serving as an acceptor is introduced into the second semiconductor layer 130. Also, the active layer 120 preferably includes a material on which bandgap engineering is performed to form barrier layers and well layers.
- [101] The reflection pattern 140 is formed on the second semiconductor layer 130.
- [102] The reflection pattern 140 includes an ohmic contact layer 141, a reflective metal layer 142, a stress relaxation layer 143, or a conductive barrier layer 144.
- [103] The ohmic contact layer 141 may be formed of any material capable of enabling an ohmic contact between the reflective metal layer 142 and the second semiconductor layer 130. Accordingly, the ohmic contact layer 141 may include a metal including nickel (Ni) or platinum (Pt) or include a conductive oxide, such as indium tin oxide (ITO) or zinc oxide (ZnO). However, the ohmic contact layer 141 may be omitted in some embodiments.
- [104] The reflective metal layer 142 is formed on the ohmic contact layer 141. The reflective metal layer 142 reflects light generated by the active layer 120. Accordingly, the reflective metal layer 142 is formed by selecting a material having conductivity and a high optical reflectance. The reflective metal layer 142 includes Ag, an Ag alloy, Al, or an Al alloy.
- [105] In addition, the stress relaxation layer 143 may be formed on the reflective metal layer 142. The stress relaxation layer 143 preferably has a coefficient of thermal expansion equal to or higher than that of the conductive barrier layer 144, and equal to or lower than that of the reflective metal layer 142. Thus, stress caused due to a difference in coefficient of thermal expansion between the reflective metal layer 142 and the conductive barrier layer 144 may be reduced. Accordingly, a material forming

the stress relaxation layer 143 may be differently selected according to selected materials forming the reflective metal layer 142 and the conductive barrier layer 144.

[106] However, the ohmic contact layer 141 or the stress relaxation layer 143 may be omitted in some embodiments.

[107] A conductive barrier layer 144 is formed on the reflective metal layer 142 or the stress relaxation layer 143. For example, when the stress relaxation layer 143 is omitted, the conductive barrier layer 144 is formed on the reflective metal layer 142. When the stress relaxation layer 143 is formed, the conductive barrier layer 144 is formed on the stress relaxation layer 143. The conductive barrier layer 144 is formed to surround at least side surfaces of the reflective metal layer 142 and top and side surfaces of the stress relaxation layer 143. Accordingly, diffusion of metal atoms or ions constituting the reflective metal layer 142 is prevented. Also, stress caused due to a difference in coefficient of thermal expansion between the conductive barrier layer 144 and the reflective metal layer 142 is absorbed in the stress relaxation layer 143.

[108] For example, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Ag, Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd or Au. Also, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes Cr, Pt, Rh, Pd, or Ni, the stress relaxation layer 143 may be a single layer formed of Ag or Cu, or a combination formed of Ni, Au, Cu, or Ag.

[109] Furthermore, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd, Cr, or Au. Also, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes Cr or Ni, the stress relaxation layer 143 may be a single layer formed of Cu, Cr, Rh, Pd, TiW, or Ti, or a combination formed of Ni, Au, or Cu.

[110] In addition, the conductive barrier layer 144 is formed to coat a surface of the second semiconductor layer 130 and extend to side surfaces of a protective insulating layer 145. However, the conductive barrier layer 144 is preferably formed to contact the side surfaces of the protective insulating layer 145 but not in such a shape as to coat a top surface of the protective insulating layer 145.

[111] In Fig. 10, the protective insulating layer 145 is formed to completely coat a portion of a top surface of the second semiconductor layer 130 and the mesa region 150. That is, the protective insulating layer 145 coats a surface of the first semiconductor layer 110 and portions of side and top surfaces of the active layer 120 and the second semiconductor layer 130, which are exposed by mesa-etching.

- [112] Figs. 11 through 16 are cross-sectional views illustrating a method of manufacturing the LED of Fig. 10, according to a second exemplary embodiment of the present invention.
- [113] Referring to Fig. 11, a first semiconductor layer 110, an active layer 120, and a second semiconductor layer 130 are sequentially formed on a substrate 100.
- [114] Furthermore, materials and forming methods of the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 are the same as described in Embodiment 1, and thus a description thereof is omitted.
- [115] Referring to Fig. 12, portions of the active layer 120 and the second semiconductor layer 130 are removed using an ordinary etching process. Thus, a portion of the first semiconductor layer 110 is exposed. Due to the etching process, a top surface of the first semiconductor layer 110 is exposed, and side surfaces of the active layer 120 and the second semiconductor layer 130 are exposed. Accordingly, a mesa region 150 or a hole may be formed by removing the portions of the active layer 120 and the second semiconductor layer 130 using the etching process. That is, the mesa region 150 etched from the surface of the second semiconductor layer 130 of Fig. 11 to the surface of the first semiconductor layer 110 may be a stripe type having a trench shape or a hole type.
- [116] In addition, when the mesa region 150 is the stripe type, the mesa region 150 may have a vertical profile or inclined profile with respect to the surface of the first semiconductor layer 110. Preferably, the mesa region 150 has a profile inclined at an angle of about 20° to about 70° with respect to the surface of the first semiconductor layer 110. Also, when the mesa region 150 is a hole type having a roughly circular shape, the mesa region 150 may have a vertical profile or inclined profile with respect to the surface of the first semiconductor layer 110. Preferably, the mesa region 150 has a profile inclined at an angle of about 20° to about 70° with respect to the surface of the first semiconductor layer 110. When the profile is inclined at an angle of less than 20°, a width of the mesa region 150 greatly increases upward. Accordingly, convergence of light generated is degraded due to an emission structure. Also, when the profile is inclined at an angle of more than 70°, the mesa region 150 has an approximately vertical profile. Accordingly, the effect of reflection of generated light by sidewalls of layers become immaterial.
- [117] Referring to Fig. 13, a protective insulating layer 145 is formed on the entire surface of the resultant structure shown in Fig. 12.
- [118] The protective insulating layer 145 may be formed of any insulating material. Accordingly, the protective insulating layer 145 may be formed of silicon oxide or silicon nitride. In addition, the protective insulating layer 145 may be formed of any insulating material having an etch selectivity with respect to the underlying second semiconductor layer 130, active layer 120, or first semiconductor layer 110 and an in-

ulating characteristic.

- [119] The protective insulating layer 145 may be formed using a spin coating process, a PVD process, a CVD process, or an ALD process according to a used material.
- [120] Referring to Fig. 14, a photoresist pattern 160 is formed on the exposed protective insulating layer 145, which forms a bottom surface of the mesa region 150. The photoresist pattern 160 may have a vertical profile with respect to the surface of the protective insulating layer 145 disposed on the mesa region. In some embodiments, the photoresist pattern 160 may be formed to have an overhang structure having a bottom surface with a smaller width than a top surface thereof. The photoresist pattern 160 is preferably a negative type. Accordingly, exposed portions are cross-linked. To form the overhang structure, the photoresist pattern 160 is preferably exposed at a predetermined angle. In the case of the overhang structure, a distance between bottom surfaces of the photoresist patterns 160 is preferably set to be at least about 1 μm greater than a distance between top surfaces thereof.
- [121] Furthermore, the protective insulating layer 145 disposed on the second semiconductor layer is exposed through the space between the photoresist patterns 160. Subsequently, an etching process is performed on the protective insulating layer 145 exposed through the space between the photoresist patterns 160.
- [122] Although the etching process may be performed using a wet process or a dry process, the etching process is preferably performed using a wet etching process. Also, due to the etching process, a large portion of the protective insulating layer 145 formed on the surface of the second semiconductor layer 130 may be removed, and a portion of the surface of the second semiconductor layer 130 is exposed. However, the protective insulating layer 145 formed at corners disposed under the photoresist pattern 160 remains. Accordingly, a space is formed between a lower portion of the photoresist pattern 160 and the second semiconductor layer 130 due to the etching process, and the protective insulating layer 145 remains at an end of the space. Since the wet etching process has isotropic etching characteristics, it may take a considerable amount of time or be troublesome to etch the protective insulating layer 145 formed on the corners disposed under the photoresist pattern 160. Accordingly, the protective insulating layer 145 exposed by the photoresist pattern 160 due to the anisotropic etching process is mostly removed, while only the protective insulating layer 145 recessed under the photoresist pattern 160 remains.
- [123] Referring to Fig. 15, a reflective metal layer 142, a stress relaxation layer 143, and a conductive barrier layer 144 are sequentially stacked on the second semiconductor layer 130 exposed by etching.
- [124] The reflective metal layer 142 includes Al, an Al alloy, Ag, or an Ag alloy. The reflective metal layer 142 may be formed using an ordinary metal deposition process.

However, the reflective metal layer 142 is preferably formed using an electronic beam (e-beam) evaporation process capable of moving most metal atoms or ions onto the surface of the second semiconductor layer 130 in a vertical direction. Thus, the metal atoms or ions may have anisotropic etching characteristics and enter a space between the photoresist patterns 160 to form the reflective metal layer 142.

- [125] The reflective metal layer 142 preferably has a thickness of about 100 nm to about 1 μ m. When the reflective metal layer 142 has a thickness of less than about 100 nm, light generated by the active layer 120 is not smoothly reflected. Also, when the reflective metal layer 142 has a thickness of more than about 1 μ m, process loss may occur due to an excessive process time.
- [126] The ohmic contact layer 141 may be formed before forming the reflective metal layer 142, as needed. The ohmic contact layer 141 may include Ni, Pt, ITO, or ZnO. Also, the ohmic contact layer 141 is preferably formed to a thickness of about 0.1 nm to about 20 nm. When the ohmic contact layer 141 has a thickness of less than about 0.1 nm, sufficient ohmic characteristics cannot be ensured due to a very small layer thickness. Also, when the ohmic contact layer 141 has a thickness of more than about 20 nm, the transmitted amount of light is reduced to reduce the quantity of light reflected by the reflective metal layer 142 disposed on the ohmic contact layer 141.
- [127] The stress relaxation layer 143 is formed on the reflective metal layer 142.
- [128] The stress relaxation layer 143 may be formed using an ordinary metal deposition process, but is preferably formed using an e-beam evaporation method having a high directionality during a deposition process. That is, metal atoms or ions evaporated due to e-beams may have directionality and have anisotropy in a space between the photoresist patterns 160, and the stress relaxation layer 143 may be formed of a metal layer. Also, the stress relaxation layer 143 may have a lower coefficient of thermal expansion than the reflective metal layer 142 and a higher coefficient of thermal expansion than the conductive barrier layer 144 of Fig. 3. Accordingly, a material forming the stress relaxation layer 143 may be differently selected according to selected materials forming the reflective metal layer 142 and the conductive barrier layer 144. The material forming the stress relaxation layer 143 will be described later.
- [129] When the reflective metal layer 142 and the stress relaxation layer 143 are formed using an e-beam evaporation method, a side surface of the reflective metal layer 142 and a side surface of the stress relaxation layer 143 are exposed. Also, the reflective metal layer 142 and the stress relaxation layer 143 corresponding to an open upper region of the photoresist pattern 160 are formed using an anisotropic deposition process.
- [130] Subsequently, a conductive barrier layer 144 is formed through the opened region of the photoresist pattern 160.

- [131] The conductive barrier layer 144 includes W, TiW, Mo, Cr, Ni, Pt, Rh, Pd, or Ti. In particular, a material forming the conductive barrier layer 144 may be differently selected according to selected materials forming the reflective metal layer 142 and the stress relaxation layer 143.
- [132] The conductive barrier layer 144 is formed on the stress relaxation layer 143 and shields side surfaces of the reflective metal layer 142 and the stress relaxation layer 143. Accordingly, a metal forming the reflective metal layer 142 is prevented from diffusing into the second semiconductor layer 130 due to lateral diffusion. The formation of the conductive barrier layer 144 is performed using an ordinary metal deposition process. However, the conductive barrier layer 144 is preferably formed using an isotropic etching process. This is because the conductive barrier layer 144 is configured to surround the side surfaces of the stress relaxation layer 143 and the reflective metal layer 142. For example, the conductive barrier layer 144 may be formed using a sputtering process.
- [133] In addition, the conductive barrier layer 144 may be a single layer formed to a thickness of about 100 nm or more by selecting a specific metal. Also, the conductive barrier layer 144 may be formed by alternately selecting at least two metal materials, and each of layers forming the conductive barrier layer 144 may be formed to a thickness of about 20 nm or more. For example, the conductive barrier layer 144 may be formed by alternately depositing a TiW layer having a thickness of about 50 nm and a Ni layer or Ti layer having a thickness of about 50 nm.
- [134] Furthermore, a Ni/Au/Ti layer may be additionally formed on the conductive barrier layer 144 to enable a stable contact of the conductive barrier layer 144 with a subsequent material.
- [135] As described above, a material forming the stress relaxation layer 143 may be selected according to materials forming the reflective metal layer 142 and the conductive barrier layer 144. This is because a coefficient of thermal expansion of the stress relaxation layer 143 is higher than that of the conductive barrier layer 144 and lower than that of the reflective metal layer 142. Accordingly, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Ag, Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd or Au. Also, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes Ti, Cr, Pt, Rh, Pd, or Ni, the stress relaxation layer 143 may be a single layer formed of Ag or Cu, or a combination formed of Ni, Au, Cu, or Ag. Furthermore, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni,

Pt, Ti, Rh, Pd, Cr, or Au. Also, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes Pt or Ni, the stress relaxation layer 143 may be a single layer formed of Cu, Cr, Rh, Pd, TiW, or Ti, or a combination formed of Ni, Au, or Cu.

- [136] In addition, since the conductive barrier layer 144 is formed using a deposition process, such as a sputtering process, the conductive barrier layer 144 is formed to fill an edge region of the photoresist pattern 160. That is, the conductive barrier layer 144 is formed to fill a space between the photoresist pattern 160 and the second semiconductor layer 130. By filling the space, the protective insulating layer 145 and the conductive barrier layer 144 are physically in contact with each other. Also, due to the deposition process, the conductive barrier layer 144 may be formed along shapes of surfaces of the second semiconductor layer 130, the reflective metal layer 142, and the stress relaxation layer 143.
- [137] The ohmic contact layer 141, the reflective metal layer 142, the stress relaxation layer 143, and the conductive barrier layer 144 may be formed also on the photoresist pattern 160.
- [138] Referring to Fig. 16, a lift-off process is performed on the photoresist pattern 160 to remove the photoresist pattern and the layers disposed thereon. Accordingly, the protective insulating layer 145 coated on the mesa region and the reflection pattern 140 disposed thereon are exposed. As described above, the mesa region 150 may be a stripe type or a hole type. Also, a protective insulating layer 145 is provided on side surfaces of the reflection pattern 140 and the mesa region 150. The conductive barrier layer 144 of the reflection pattern 140 may be defined by the protective insulating layer 145.
- [139] Due to the above-described processes, the reflection pattern 140 is formed on the second semiconductor layer 130. The reflection pattern 140 includes a reflective metal layer 142, a stress relaxation layer 143, and a conductive barrier layer 144. The stress relaxation layer 143 has a lower coefficient of thermal expansion than the reflective metal layer 142 and a higher coefficient of thermal expansion than the conductive barrier layer 144. Accordingly, stress caused due to a difference in coefficient of thermal expansion between the reflective metal layer 142 and the conductive barrier layer 144 is absorbed in the stress relaxation layer 143.
- [140] In addition, formation of protruding points shown in Figs. 1 and 2 is excluded from the conductive barrier layer 144 formed on the reflective metal layer 142 or the stress relaxation layer 143. Accordingly, generation of metal particles is inhibited in subsequent processes to maintain a high yield.

[141]

[142] Embodiment 3

[143] Fig. 17 is a cross-sectional view of an LED according to a third exemplary em-

bodiment of the present invention.

[144] Referring to Fig. 17, a first semiconductor layer 110, an active layer 120, a second semiconductor layer 130, and a reflection pattern 140 are formed on a substrate 100.

[145] The substrate 100 may be formed of any material capable of inducing the first semiconductor layer 110 to be grown. Accordingly, the substrate 100 may include sapphire (Al_2O_3), silicon carbide (SiC), gallium nitride (GaN), indium gallium nitride (InGaN), aluminum gallium nitride (AlGaN), aluminum nitride (AlN), gallium oxide (Ga_2O_3), or silicon. Specifically, the substrate 100 may be a sapphire substrate.

[146] Also, the substrate 100 may be a substrate on which surface treatment is not performed. The substrate 100 may be a patterned substrate. Also, the substrate 100 may have a surface having a moth-eye structure. For example, the substrate may have a protrusion protruding in a roughly hemispherical shape, and pointed structures may be densely disposed on the protrusion.

[147] In addition, the first semiconductor layer 110 is provided on the substrate 100. The first semiconductor layer 110 preferably has an n conductivity type.

[148] Furthermore, the active layer 120 formed on the first semiconductor layer 110 may have an SQW structure in which a well layer and a barrier layer are stacked, or an MQW structure in which well layers and barrier layers are alternately stacked.

[149] The second semiconductor layer 130 is provided on the active layer 120. The second semiconductor layer 130 preferably has a p conductivity type.

[150] Furthermore, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 may include Si, GaN, AlN, InGaN, or AlInGaN. When the first semiconductor layer 110 includes GaN, the active layer 120 and the second semiconductor layer 130 preferably include GaN. However, since the second semiconductor layer 130 has a complementary conductivity type to the first semiconductor layer 110, a different dopant from that of the first semiconductor layer 110 is introduced into the second semiconductor layer 130. That is, when a dopant serving as a donor is introduced into the first semiconductor layer 110, a dopant serving as an acceptor is introduced into the second semiconductor layer 130. Also, the active layer 120 preferably includes a material on which bandgap engineering is performed to form barrier layers and well layers.

[151] The reflection pattern 140 is formed on the second semiconductor layer 130.

[152] The reflection pattern 140 includes a reflective metal layer 142 and a conductive barrier layer 144. Also, in some embodiments, an ohmic contact layer (not shown) may be formed under the reflective metal layer 142, and a stress relaxation layer (not shown) may be additionally formed between the reflective metal layer 142 and the conductive barrier layer 144.

[153] An ohmic contact layer may be formed of any material capable of enabling an ohmic

contact between the reflective metal layer 142 and the second semiconductor layer 130. Accordingly, the ohmic contact layer may include a metal including Ni or Pt or include a conductive oxide, such as ITO or ZnO. However, the ohmic contact layer may be omitted in some embodiments.

- [154] The reflective metal layer 142 is formed on the ohmic contact layer. The reflective metal layer 142 reflects light generated by the active layer 120. Accordingly, the reflective metal layer 142 is formed by selecting a material having conductivity and a high optical reflectance. The reflective metal layer 142 includes Ag, an Ag alloy, Al, or an Al alloy.
- [155] In addition, a stress relaxation layer may be formed on the reflective metal layer 142. The stress relaxation layer preferably has a coefficient of thermal expansion equal to or higher than that of the conductive barrier layer 144, and equal to or lower than that of the reflective metal layer 142. Thus, stress caused due to a difference in coefficient of thermal expansion between the reflective metal layer 142 and the conductive barrier layer 144 may be reduced. Accordingly, a material forming the stress relaxation layer may be differently selected according to selected materials forming the reflective metal layer 142 and the conductive barrier layer 144.
- [156] However, the ohmic contact layer or the stress relaxation layer may be omitted in some embodiments.
- [157] In addition, an angle α formed by the reflective metal layer 142 with a plane surface of the underlying second semiconductor layer 130 preferably ranges from about 5° to about 45°. When an angle α formed by a side surface of the reflective metal layer 142 is less than about 5°, it is difficult to ensure a sufficient thickness of the reflective metal layer 142. When an angle α formed by the side surface of the reflective metal layer 142 is more than about 45°, cracks occur in a side profile of the conductive barrier layer 144 formed on the reflective metal layer 142. When an ohmic contact layer is introduced, an inclination angle formed by the ohmic contact layer with the side surface of the reflective metal layer 142 should be within the above-described angle range.
- [158] The conductive barrier layer 144 is formed on the reflective metal layer 142 or the stress relaxation layer 143. For example, when a stress relaxation layer is omitted, the conductive barrier layer 144 is formed on the reflective metal layer 142, and when the stress relaxation layer is formed, the conductive barrier layer 144 is formed on the stress relaxation layer. The conductive barrier layer 144 is formed to surround at least the side surface of the reflective metal layer 142 and surround top and side surfaces of the stress relaxation layer. Accordingly, diffusion of metal atoms or ions constituting the reflective metal layer 142 is prevented. Also, stress caused due to a difference in coefficient of thermal expansion between the conductive barrier layer 144 and the re-

reflective metal layer 142 may be absorbed in the stress relaxation layer. In particular, the conductive barrier layer 144 may be formed to a different thickness according to a surface state of the underlying reflective metal layer or stress relaxation layer. For example, assuming that the thickness of the conductive barrier layer 144 formed on a top surface of the reflective metal layer 142 is t_1 , the thickness of the conductive barrier layer 144 formed on the side surface of the reflective metal layer 142 is t_2 , and the thickness of the conductive barrier layer 144 formed on the surface of the second semiconductor layer 130 is t_3 , a relationship of $t_1 > t_3 > t_2$ is preferably set.

- [159] In addition, the conductive barrier layer 144 is formed to completely shield the reflective metal layer 142 or the stress relaxation layer and extend to the surface of the second semiconductor layer 130.
- [160] In addition, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer may be a single layer formed of Ag, Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd or Au. Also, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes Ti, Cr, Pt, Rh, Pd, or Ni, the stress relaxation layer may be a single layer formed of Ag or Cu, or a combination formed of Ni, Au, Cu, or Ag.
- [161] Furthermore, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer may be a single layer formed of Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd, Cr, or Au. Also, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes Cr or Ni, the stress relaxation layer may be a single layer formed of Cu, Cr, Rh, Pd, TiW, or Ti, or a combination formed of Ni, Au, or Cu.
- [162] In addition, the conductive barrier layer 144 coats the surface of the second semiconductor layer 130.
- [163] Figs. 18 through 22 are cross-sectional views illustrating a method of manufacturing the LED of Fig. 17, according to a third exemplary embodiment of the present invention.
- [164] Referring to Fig. 18, a first semiconductor layer 110, an active layer 120, and a second semiconductor layer 130 are sequentially formed on a substrate 100.
- [165] The substrate 100 may include sapphire (Al_2O_3), silicon carbide (SiC), gallium nitride (GaN), indium gallium nitride (InGaN), aluminum gallium nitride (AlGaN), aluminum nitride (AlN), gallium oxide (Ga_2O_3), or silicon. Specifically, the substrate 100 may be a sapphire substrate. Also, the substrate 100 may be a patterned substrate or a substrate having a surface with a moth-eye structure.
- [166] Also, the first semiconductor layer 110 is provided on the substrate 100. The first

semiconductor layer 110 preferably has an n conductivity type.

[167] In addition, the active layer 120 formed on the first semiconductor layer 110 may have an SQW structure in which a well layer and a barrier layer are stacked, or an MQW structure in which well layers and barrier layers are alternately stacked.

[168] The second semiconductor layer 130 is provided on the active layer 120. The second semiconductor layer 130 preferably has a p conductivity type.

[169] Furthermore, materials and constructions of the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 are the same as described with reference to Fig. 3, and thus a description thereof is omitted.

[170] In addition, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 are formed using an epitaxial growth process. Accordingly, the first semiconductor layer 110, the active layer 120, and the second semiconductor layer 130 are preferably formed using an MOCVD process.

[171] Referring to Fig. 19, portions of the active layer 120 and the second semiconductor layer 130 are removed using an ordinary etching process. Thus, a portion of the first semiconductor layer 110 is exposed. Due to the etching process, a top surface of the first semiconductor layer 110 is exposed, and side surfaces of the active layer 120 and the second semiconductor layer 130 are exposed. Accordingly, a trench or a hole may be formed by removing the portions of the active layer 120 and the second semiconductor layer 130 using the etching process. That is, a mesa region 150 etched from the surface of the second semiconductor layer 130 of Fig. 5 to the surface of the first semiconductor layer 110 may be a stripe type having a trench shape or a hole type.

[172] In addition, when the mesa region is the stripe type, the mesa region may have a vertical profile or inclined profile with respect to the surface of the first semiconductor layer 110. Preferably, the mesa region has a profile inclined at an angle of about 20° to about 70° with respect to the surface of the first semiconductor layer 110. Also, when the mesa region 150 is a hole type having a roughly circular shape, the mesa region 150 may have a vertical profile or inclined profile with respect to the surface of the first semiconductor layer 110. Preferably, the mesa region 150 has a profile inclined at an angle of about 20° to about 70° with respect to the surface of the first semiconductor layer 110. When the profile is inclined at an angle of less than 20°, a width of the mesa region 150 greatly increases upward. Accordingly, convergence of light generated is degraded due to an emission structure. Also, when the profile is inclined at an angle of more than 70°, the mesa region 150 has an approximately vertical profile. Accordingly, the effect of reflection of generated light by sidewalls of layers become immaterial.

[173] Referring to Fig. 20, a photoresist pattern 160 is formed on the first semiconductor layer 110 exposed by forming a bottom surface of the mesa region. The photoresist

pattern 160 may have a vertical profile with respect to the surface of the first semiconductor layer 110. In some embodiments, the photoresist pattern 160 may be formed to have an overhang structure having a bottom surface with a smaller width than a top surface thereof. The photoresist pattern 160 is preferably a negative type. Accordingly, exposed portions are cross-linked. To form the overhang structure, the photoresist pattern 160 is preferably exposed at a predetermined angle. In the case of the overhang structure, a distance between bottom surfaces of the photoresist patterns 160 is preferably set to be at least about 1 μm greater than a distance between top surfaces thereof.

- [174] Furthermore, the photoresist pattern 160 is preferably provided to cover a portion of the surface of the second semiconductor layer 130. Accordingly, the portion of the top surface of the second semiconductor layer 130 may remain shielded by the photoresist pattern 160.
- [175] Referring to Fig. 21, a reflective metal layer 142 and a conductive barrier layer 144 are sequentially stacked on the second semiconductor layer 130 to form a reflection pattern 140. Also, in some embodiments, an ohmic contact layer 141 may be formed under the reflective metal layer 142, and a stress relaxation layer 143 may be additionally formed between the reflective metal layer 142 and the conductive barrier layer 144.
- [176] The reflective metal layer 142 includes Al, an Al alloy, Ag, or an Ag alloy. The reflective metal layer 142 may be formed using an ordinary metal deposition process. However, the reflective metal layer 142 is preferably formed using an electronic beam (e-beam) evaporation process capable of moving most metal atoms or ions onto the surface of the second semiconductor layer 130 in a vertical direction. Thus, the metal atoms or ions may have anisotropic etching characteristics and enter a space between the photoresist patterns 160 to form the reflective metal layer 142.
- [177] The reflective metal layer 142 preferably has a thickness of about 100 nm to about 1 μm . When the reflective metal layer 142 has a thickness of less than about 100 nm, light generated by the active layer 120 is not smoothly reflected. Also, when the reflective metal layer 142 has a thickness of more than about 1 μm , process loss may occur due to an excessive process time.
- [178] The ohmic contact layer 141 may be formed before forming the reflective metal layer 142, as needed. The ohmic contact layer 141 may include Ni, Pt, ITO, or ZnO. Also, the ohmic contact layer 141 is preferably formed to a thickness of about 0.1 nm to about 20 nm. When the ohmic contact layer 141 has a thickness of less than about 0.1 nm, sufficient ohmic characteristics cannot be ensured due to a very small layer thickness. Also, when the ohmic contact layer 141 has a thickness of more than about 20 nm, the transmitted amount of light is reduced to reduce the quantity of light

reflected by the reflective metal layer 142 disposed on the ohmic contact layer 141.

[179] The stress relaxation layer 143 is formed on the reflective metal layer 142.

[180] The stress relaxation layer 143 may be formed using an ordinary metal deposition process, but is preferably formed using an e-beam evaporation method having a high directionality during a deposition process. That is, metal atoms or ions evaporated due to e-beams may have directionality and have anisotropy in a space between the photoresist patterns 160, and the stress relaxation layer 143 may be formed of a metal layer. Also, the stress relaxation layer 143 may have a lower coefficient of thermal expansion than the reflective metal layer 142 and a higher coefficient of thermal expansion than the conductive barrier layer 144 of Fig. 3. Accordingly, a material forming the stress relaxation layer 143 may be differently selected according to selected materials forming the reflective metal layer 142 and the conductive barrier layer 144.

[181] When the reflective metal layer 142 and the stress relaxation layer 143 are formed using an e-beam evaporation method, a side surface of the reflective metal layer 142 and a side surface of the stress relaxation layer 143 are exposed. Also, the reflective metal layer 142 and the stress relaxation layer 143 corresponding to an open upper region of the photoresist pattern 160 are formed using an anisotropic deposition process.

[182] Also, in an e-beam evaporation process, upper layers are formed along a profile of a side surface of the stress relaxation layer 143, but the upper layers are provided to cover or shield lower layers. A side surface of a structure including the stress relaxation layer 143 or the reflective metal layer 142 formed using the e-beam evaporation process is preferably inclined at an angle α of about 5° to about 45° . To embody the above-described angle α of the side surface, the substrate 100 may be in an inclined direction with respect to an e-beam source during a deposition process using the e-beam evaporation process. During the deposition process, the substrate 100 may rotate (i.e., revolve) around the e-beam source and also rotate on its own axis.

[183] Subsequently, a conductive barrier layer 144 is formed through the opened region of the photoresist pattern 160.

[184] The conductive barrier layer 144 includes W, TiW, Mo, Cr, Ni, Pt, Rh, Pd, or Ti. In particular, a material forming the conductive barrier layer 144 may vary according to selected materials forming the reflective metal layer 142 and the stress relaxation layer 143.

[185] The conductive barrier layer 144 is formed on the stress relaxation layer 143 and shields side surfaces of the reflective metal layer 142 or the stress relaxation layer 143. Accordingly, a metal forming the reflective metal layer 142 is prevented from diffusing into the second semiconductor layer 130 due to lateral diffusion. The

formation of the conductive barrier layer 144 is performed using an ordinary metal deposition process. However, the conductive barrier layer 144 is preferably formed using an isotropic etching process. This is because the conductive barrier layer 144 is configured to surround the side surfaces of the stress relaxation layer 143 and the reflective metal layer 142. For example, the conductive barrier layer 144 may be formed using a sputtering process.

- [186] In addition, the conductive barrier layer 144 may be a single layer formed to a thickness of about 100 nm or more by selecting a specific metal. Also, the conductive barrier layer 144 may be formed by alternately selecting at least two metal materials, and each of layers forming the conductive barrier layer 144 may be formed to a thickness of about 20 nm or more. For example, the conductive barrier layer 144 may be formed by alternately depositing a TiW layer having a thickness of about 50 nm and a Ni layer or Ti layer having a thickness of about 50 nm.
- [187] In particular, the conductive barrier layer 144 has a different thickness according to a state or gradient of an underlying layer, and is formed to extend to an upper portion of the second semiconductor layer 130. Since a gradient of a side surface of the underlying layer has an angle of about 45° or less, occurrence of cracks in the conductive barrier layer 144 due to sharp gradient is prevented.
- [188] Furthermore, a Ni/Au/Ti layer may be additionally formed on the conductive barrier layer 144 to enable a stable contact of the conductive barrier layer 144 with a subsequent material.
- [189] As described above, a material forming the stress relaxation layer 143 may be selected according materials forming the reflective metal layer 142 and the conductive barrier layer 144. This is because a coefficient of thermal expansion of the stress relaxation layer 143 is higher than that of the conductive barrier layer 144 and lower than that of the reflective metal layer 142. Accordingly, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Ag, Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd or Au. Also, when the reflective metal layer 142 includes Al or an Al alloy, and the conductive barrier layer 144 includes Ti, Cr, Pt, Rh, Pd, or Ni, the stress relaxation layer 143 may be a single layer formed of Ag or Cu, or a combination formed of Ni, Au, Cu, or Ag. Furthermore, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes W, TiW, or Mo, the stress relaxation layer 143 may be a single layer formed of Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd, Cr, or Au. Also, when the reflective metal layer 142 includes Ag or an Ag alloy, and the conductive barrier layer 144 includes Pt or Ni, the stress relaxation layer 143 may be a single layer formed of Cu, Cr, Rh, Pd, TiW, or Ti, or a combination

formed of Ni, Au, or Cu.

- [190] The ohmic contact layer 141, the reflective metal layer 142, the stress relaxation layer 143, and the conductive barrier layer 144 may be formed also on the photoresist pattern 160.
- [191] Referring to Fig. 22, the photoresist pattern 160 and the layers thereon are removed. Accordingly, the underlying second semiconductor layer 130 and the reflection pattern 140 disposed thereon are exposed. Also, the mesa region 150 is exposed by removing the photoresist pattern 160. This is the same as described with reference to Fig. 17.
- [192] Due to the above-described processes, the reflection pattern 140 is formed on the second semiconductor layer 130. The reflection pattern 140 includes a reflective metal layer 142, a stress relaxation layer 143, and a conductive barrier layer 144. The stress relaxation layer 143 has a lower coefficient of thermal expansion than the reflective metal layer 142 and a higher coefficient of thermal expansion than the conductive barrier layer 144. Accordingly, stress caused due to a difference in coefficient of thermal expansion between the reflective metal layer 142 and the conductive barrier layer 144 is absorbed in the stress relaxation layer 143.
- [193] In addition, the conductive barrier layer 144 formed on the reflective metal layer 142 or the stress relaxation layer 143 has a different thickness according to the shape and kind of an underlying layer. For example, a thickness t_1 of the conductive barrier layer 144 formed on the surface of the reflective metal layer 142 or the stress relaxation layer 143 is greater than a thickness t_3 of the conductive barrier layer 144 formed on the surface of the second semiconductor layer 130. Also, the thickness t_3 is greater than a thickness t_2 of the conductive barrier layer 144 formed on side surfaces of the reflective metal layer 142 or the stress relaxation layer 143.
- [194] The difference in thickness is a result obtained by performing an isotropic deposition process after a photoresist pattern having an overhang structure is formed. That is, deposition is performed to the highest extent on a top surface of the reflective metal layer 142 or stress relaxation layer 144, which is opened by the photoresist pattern, and deposition may be performed to a relatively high extent on a surface of the second semiconductor layer 130 because the second semiconductor layer 130 has a planar structure. In contrast, since a side surface of the reflective metal layer 142 or the stress relaxation layer 143 has a predetermined inclination and a deposited metal should be adhered to sidewalls of the reflective metal layer 142 or the stress relaxation layer 143, deposition is performed to a relatively low extent on the side surface of the reflective metal layer 142 or the stress relaxation layer 143.
- [195] Furthermore, the side surface of the reflective metal layer 142 or the stress relaxation layer 143 is formed at an inclination angle α of about 5° to about 45° . A required inclination angle may be formed by controlling an angle of a substrate during an e-beam

evaporation process. That is, by orienting the substrate at a predetermined angle with respect to an imaginary direction in which metal ions or particles are predicted to proceed, the inclination angle α of the side surface of the reflective metal layer 142 or the stress relaxation layer 143 may be controlled. By setting the inclination angle α of the side surface, occurrence of cracks in a conductive barrier layer 144 that will be formed subsequently is prevented.

[196]

[197] Embodiment 4

[198] Figs. 23 through 27 are plan views and cross-sectional views of LED modules to which the structure of Fig. 3 or Fig. 10 is applied, according to a fourth exemplary embodiment of the present invention.

[199] Referring to Fig. 23, it is assumed that the mesa region 150 of Fig. 3 or Fig. 10 is a region etched in a stripe shape. Subsequently, a first insulating layer 200 is formed on the entire surface of the structure of Fig. 3 or Fig. 10. The first insulating layer 200 exposes a portion of a top surface of the reflection pattern 140 and exposes a surface of the first semiconductor layer 110. Accordingly, a surface of a conductive barrier layer 144 is exposed.

[200] Also, the coating of the first insulating layer 200 is performed by coating an insulating material on the entire surface of the structure of Fig. 3 or Fig. 10. However, the coated insulating material and the protective insulating layer 145 of Fig. 3 or Fig. 10 will be referred to as the first insulating layer 200. This is because an insulating layer and the protective insulating layer 145 have the same or similar electrical properties. That is, the insulating layer and the protective insulating layer 145 have the same insulating characteristics. Accordingly, the insulating layer and the protective insulating layer 145 coated for brevity will be referred to as one first insulating layer 200. Accordingly, by etching the first insulating layer 200, the surface of the first semiconductor layer 110 is exposed, and a reflection pattern 140 disposed on the surface of the first semiconductor layer 110 is exposed.

[201] To form the first insulating layer 200, an oxide layer (e.g., a SiO_2 layer), a nitride layer (e.g., a SiN layer), an insulating layer (e.g., a MgF_2 layer), or a de-bragg reflector (DBR) layer (e.g., a $\text{SiO}_2/\text{TiO}_2$ layer) is formed on the resultant structure of Fig. 23. Thereafter, a portion of the reflection pattern 140 and the surface of the first semiconductor layer 110 are exposed using an ordinary photolithography process.

[202] A view disposed under the plan view of Fig. 23 is a cross-sectional view obtained by cutting the plan view of Fig. 13 along direction A-A'. In the cross-sectional view, line A-A' is discontinuous, and a dotted line is not reflected in the cross-sectional view. However, it is assumed that the discontinuous line is continuous in the cross-sectional view. Hereinafter, this assumption will be applied likewise.

- [203] Also, although the present embodiment describes an example in which three reflection patterns 140 are exposed, the present invention is not limited to the example, and the number of exposed reflection patterns 140 may be changed.
- [204] The reflection pattern 140 is exposed in a partial region, and the first semiconductor layer 110 is exposed in the mesa region 150. Also, the first insulating layer 200 completely shields the reflection pattern 140 in a region in which the reflection pattern 140 is not exposed.
- [205] Referring to Fig. 24, a conductive reflection layer 210 and a reflective barrier layer 220 are formed on the first insulating layer 200.
- [206] The conductive reflection layer 210 is formed of a conductive material. Also, the conductive reflection layer 210 exposes a portion of the reflection pattern 140.
- [207] The conductive reflection layer 210 includes Al. Accordingly, the first semiconductor layer 110 and the conductive reflection layer 210 are electrically connected to each other, and the reflection pattern 140 is electrically insulated from the conductive reflection layer 210 by the first insulating layer 200.
- [208] In addition, a reflective barrier layer 220 is formed on the conductive reflection layer 210. The reflective barrier layer 220 prevents diffusion of a metal forming the conductive reflection layer 210. The reflective barrier layer 220 may be a single layer formed of Ni, Cr, or Au, or a combination thereof. The reflective barrier layer 220 is preferably a combination formed of Ti/Al/Ti/Ni/Au. Also, an adhesive layer (not shown) may be further provided under the conductive reflection layer 210. The adhesive layer may include Ti, Cr, or Ni.
- [209] The formation of the conductive reflection layer 210 and the reflective barrier layer 220 may be performed by sequentially stacking the conductive reflection layer 210 and the reflective barrier layer 220 and patterning the conductive reflection layer 210 and the reflective barrier layer 220 using an etching process. In addition, the conductive reflection layer 210 and the reflective barrier layer 220 may be formed using a lift-off process. That is, photoresist is coated on the reflection pattern 140, and the conductive reflection layer 210 and the reflective barrier layer 220 are formed using an ordinary deposition process. Subsequently, by removing the photoresist from the reflection pattern 140, the conductive reflection layer 210 and the reflective barrier layer 220 are formed to expose the reflection pattern 140.
- [210] The above descriptions will be understood with reference to a lower cross-sectional view of Fig. 24. That is, the reflection pattern 140 is exposed in a cross-section through two exposed reflection patterns 140 in line A-A', while the first insulating layer 200 is formed on the reflection pattern 140, and the conductive reflection layer 210 and the reflective barrier layer 220 are formed on the first insulating layer 200 in a cross-section through a region filled with only the conductive reflection layer 210 and the re-

flective barrier layer 220.

- [211] Since the conductive reflection layer 210 includes an Al material, the conductive reflection layer 210 may reflect light generated by an active layer. Accordingly, the conductive reflection layer 210 is in electrical contact with the first semiconductor layer 110 and serves as a reflection layer configured to reflect light. Also, the reflective barrier layer 220 formed on the conductive reflection layer 210 prevents diffusion of metal particles forming the conductive reflection layer 210.
- [212] In addition, by interposing a contact layer, an ohmic contact between the conductive reflection layer 210 and the first semiconductor layer 110 may be easily formed.
- [213] Referring to Fig. 25, a second insulating layer 230 is formed on the resultant structure of Fig. 24. A portion of the reflective barrier layer 220 is exposed through the second insulating layer 230, and a portion of the reflection pattern 140 is also exposed. The reflection pattern 140 remains electrically connected to the second semiconductor layer 130, and the reflective barrier layer 220 remains electrically connected to the first semiconductor layer 110 through the conductive reflection layer 210.
- [214] The second insulating layer 230 may be formed of any insulating material. Accordingly, an oxide-based insulating material, a nitride-based insulating material, a polymer (e.g., polyimide, Teflon, or parylene) may be used to form the second insulating layer 230.
- [215] Referring to Fig. 26, a first pad 240 and a second pad 250 are formed on the resultant structure of Fig. 25. The first pad 240 is electrically connected to the conductive reflection layer 210 through the exposed reflective barrier layer 220 in Fig. 25. Accordingly, the first pad 240 and the first semiconductor layer 110 are electrically connected to each other. This indicates that the first semiconductor layer 110 is electrically connected to an external power source or power supply line through the first pad 240. Also, the second pad 250 is electrically connected to the exposed reflection pattern 140 in Fig. 25. Accordingly, the second pad 250 and the second semiconductor layer 130 are electrically connected. This indicates that the second semiconductor layer 130 is electrically connected to an external power source or power supply line through the second pad 250.
- [216] The first pad 240 and the second pad 250 may have a double structure including a layer including Ti, Cr, or Ni and a layer including Al, Cu, Ag, or Au. Also, the first pad 240 and the second pad 250 may be formed by patterning photoresist, depositing a metal material between patterned spaces, and removing the deposited metal material using a lift-off process. Also, a double or single metal layer is formed, and then a pattern is formed using an ordinary photolithography process, and the first and second pads 240 and 250 may be formed by means of a dry etching process or wet etching process using the pattern. Here, an etchant used during the dry or wet etching process

may be differently determined according to characteristics of an etched metal material.

- [217] In addition, a pad barrier layer 260 or 270 formed of a conductive material may be formed on the first pad 240 or the second pad 250. The pad barrier layer 260 or 270 is provided to prevent diffusion of a metal during a process of bonding or soldering the pads 240 and 250. For example, during the bonding or soldering process, tin (Sn) atoms contained in a bonding metal or soldering material are prevented from diffusing into the pads 240 and 250 and increasing the resistivity of the pads 240 and 250. To this end, the pad barrier layer 260 or 270 may include Cr, Ni, Ti W, TiW, Mo, Pt, or a combination thereof.
- [218] Fig. 27 illustrates cross-sectional views taken along lines B-B' and C-C' of Fig. 26.
- [219] To begin with, line B-B' cuts through a region in which the first pad 240 is formed. The first pad 240 is electrically connected to the exposed reflective barrier layer 220. Also, a first pad barrier layer 260 is formed on the first pad 240.
- [220] In addition, line C-C' cuts through a region in which the second pad 250 is formed. The second pad 250 is electrically connected to the exposed reflection pattern 140. Also, a second pad barrier layer 270 is formed on the second pad.
- [221] The first pad barrier layer 260 and the second pad barrier layer 270 are electrically isolated from each other.
- [222] As a result, it can be seen that the first pad 240 is electrically connected to the first semiconductor layer 110, and the second pad 250 is electrically connected to the second semiconductor layer 130.
- [223] Due to the above-described process, the conductive barrier layer 144 of the reflection pattern 140 is defined by the protective insulating layer 145. Accordingly, the conductive barrier layer 144 is coated on a space between protective insulating layers 145 and formed to surround top and side surfaces of the reflective metal layer 142 or the stress relaxation layer 143. Accordingly, a phenomenon where the conductive barrier layer 144 is formed on sidewalls of a photoresist pattern using a sputtering process to form points is prevented. Also, in an LED module using the above-described advantage, the first semiconductor layer 110 is exposed as a stripe type and in electrical contact with the first pad 240 through the conductive reflection layer 210 and the reflective barrier layer 220. Diffusion of a metal is prevented by the reflective barrier layer 220 provided between the conductive reflection layer 210 and the first pad 240. For instance, a metal forming the conductive reflection layer 210 is prevented from moving to the first pad 240 and increasing the resistivity of the first pad 240. Also, the second semiconductor layer 130 is electrically connected to the second pad 250. A pad barrier layer 260 or 270 is formed on each of the pads. The pad barrier layer 260 or 270 prevents diffusion of a generated metal during a bonding or soldering process so that the first pad 240 or the second pad 250 can have a high conductivity

and be in electrical contact with the outside.

[224]

[225] Embodiment 5

[226] Figs. 28 through 30 illustrate plan views and cross-sectional views of LED modules to which the structure of Fig. 3 or Fig. 10 is applied, according to a fifth exemplary embodiment of the present invention.

[227] Referring to Fig. 28, a mesa region 150 is formed as a hole type shown in Figs. 3 and 10. Accordingly, a first semiconductor layer 110 is exposed in a roughly circular shape.

[228] Subsequently, a first insulating layer 200 is formed on the entire surface of the structure of Fig. 28. The first insulating layer 200 exposes a portion of a top surface of the reflection pattern 140 and exposes the surface of the first semiconductor layer 110. The formation of the first insulating layer 200 is the same as described in Embodiment 4 with reference to Fig. 23, and thus a description thereof is omitted.

[229] A view disposed under the plan view of Fig. 28 is a cross-sectional view obtained by cutting the plan view of Fig. 28 along direction D-D'. In the cross-sectional view, line D-D' is discontinuous on a dotted line and formed by connecting solid lines to the dotted line. Accordingly, only the solid lines, and not the dotted line, are reflected in the cross-sectional view.

[230] The reflection pattern 140 is exposed in a partial region, and the first semiconductor layer 110 is exposed in the mesa region 150. Also, the first insulating layer 200 completely shields the reflection pattern 140 in a region in which the reflection pattern 140 is not exposed.

[231] Furthermore, the hole-type mesa region 150 is exaggerated for clarity in Fig. 28. Accordingly, the number and shape of hole-type mesa regions 150 may be sufficiently changed in some embodiments.

[232] Referring to Fig. 29, a conductive reflection layer 210 and a reflective barrier layer 220 are formed on the first insulating layer 200. Materials and forming processes of the conductive reflection layer 210 and the reflective barrier layer 220 are the same as described with reference to Fig. 24. Also, the conductive reflection layer 210 and the reflective barrier layer 220 expose a portion of the reflection pattern 140.

[233] Accordingly, the first semiconductor layer 110 and the reflective barrier layer 220 are electrically connected through the conductive reflection layer 210, and the reflection pattern 140 is electrically insulated from the conductive reflection layer 210 by the first insulating layer 200.

[234] The above descriptions will be understood with reference to a lower cross-sectional view of Fig. 29. That is, the reflection pattern 140 is exposed in a cross-section through two exposed reflection patterns 140 in line D-D', while the first insulating layer 200 is

formed on the reflection pattern 140, and the conductive reflection layer 210 and the reflective barrier layer 220 are formed on the first insulating layer 200 in a cross-section through a region filled with only the conductive reflection layer 210 and the reflective barrier layer 220. Also, the conductive reflection layer 210 and the reflective barrier layer 220 are formed on a surface of the first semiconductor layer 110 exposed as a hole type in Fig. 29.

[235] Since the conductive reflection layer 210 includes an Al material, the conductive reflection layer 210 may reflect light generated by the active layer 120. Accordingly, the conductive reflection layer 210 is in electrical contact with the first semiconductor layer 110 and serves as a reflection layer configured to reflect light.

[236] Before forming the conductive reflection layer 210, a contact layer having the same shape as the conductive reflection layer 210 may be additionally formed. The contact layer includes Ti, Cr, or Ni. By interposing the contact layer, an ohmic contact may be easily formed between the conductive reflection layer 210 and the first semiconductor layer 110.

[237] Furthermore, the reflective barrier layer 220 formed on the conductive reflection layer 210 may be a single layer formed of Ni, Cr, or Au, or a combination thereof. The reflective barrier layer 220 is preferably a combination formed of Ti/Al/Ti/Ni/Au.

[238] Referring to Fig. 30, a second insulating layer 230 is formed. A portion of the reflective barrier layer 220 is exposed through the second insulating layer 230, and a portion of the reflection pattern 140 is exposed. The reflection pattern 140 remains electrically connected to the second semiconductor layer 130, and the conductive reflection layer 210 remains electrically connected to the first semiconductor layer 110. Accordingly, an electrical path between the first semiconductor layer 110 and the second semiconductor layer 130 is opened by the second insulating layer 230.

[239] A material and formation of the second insulating layer 230 are the same as described with reference to Fig. 25, and thus a description thereof is omitted.

[240] Subsequently, a first pad (not shown) and a second pad (not shown) are formed as described with reference to Fig. 26. The first pad is electrically connected to the exposed conductive reflection layer 210 in Fig. 30. Accordingly, the first pad and the first semiconductor layer 110 are electrically connected to each other. This indicates that the first semiconductor layer 110 is electrically connected to an external power source or power supply line through the first pad. Also, the second pad is electrically connected to the exposed reflection pattern 140 in Fig. 30. Accordingly, the second pad and the second semiconductor layer 130 are electrically connected. This indicates that the second semiconductor layer 130 is electrically connected to an external power source or power supply line through the second pad.

[241] In addition, a pad barrier layer formed of a conductive material may be formed on the

first pad or the second pad. The pad barrier layer is provided to prevent diffusion of a metal during a process of bonding or soldering the pads. For example, during the bonding or soldering process, tin (Sn) atoms contained in a bonding metal or soldering material are prevented from diffusing into the pads and increasing the resistivity of the pads. To this end, the pad barrier layer may include Cr, Ni, Ti W, TiW, Mo, Pt, or a combination thereof.

[242] Due to the above-described process, the conductive barrier layer 144 of the reflection pattern 140 is defined by the protective insulating layer 145. Accordingly, the conductive barrier layer 144 is coated on a space between protective insulating layers 145 and formed to surround top and side surfaces of the reflective metal layer 142 or the stress relaxation layer 143. Accordingly, a phenomenon where the conductive barrier layer 144 is formed on sidewalls of a photoresist pattern using a sputtering process to form points is prevented. Also, in an LED module using the above-described advantage, the first semiconductor layer 110 is exposed as a stripe type and in electrical contact with the first pad through the conductive reflection layer 210 and the reflective barrier layer 220. Diffusion of a metal is prevented by the reflective barrier layer 220 provided between the conductive reflection layer 210 and the first pad 240. For instance, a metal forming the conductive reflection layer 210 is prevented from moving to the first pad and increasing the resistivity of the first pad. Also, the second semiconductor layer 130 is electrically connected to the second pad. A pad barrier layer is formed on each of the pads. The pad barrier layer prevents diffusion of a generated metal during a bonding or soldering process so that the first pad or the second pad can have a high conductivity and be in electrical contact with the outside.

[243] While the invention has been shown and described with reference to m certain exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

[244] *Description of Major Symbols in the above Figures

[245] 100: Substrate 110: First semiconductor layer

[246] 120: Active layer 130: Second semiconductor layer

[247] 140: Reflection pattern 141: Ohmic contact layer

[248] 142: Reflective metal layer 143: Stress relaxation layer

[249] 144: Conductive barrier layer 145: Protective insulating layer

[250] 150: Mesa region 200: First insulating layer

[251] 210: Conductive reflection layer 220: Reflective barrier layer

[252] 230: Second insulating layer 240: First pad

[253] 250: Second pad 260: First pad barrier layer

[254] 270: Second pad barrier layer

Claims

- [Claim 1] A light emitting diode (LED) comprising:
a substrate;
a first semiconductor layer formed on the substrate;
an active layer formed on the first semiconductor layer and configured to generate light;
a second semiconductor layer formed on the active layer and having a complementary conductive type to the first semiconductor layer; and
a reflection pattern formed between protective insulating layers formed on the second semiconductor layer and configured to reflect light generated in the active layer, the reflection pattern having a conductive barrier layer contacting the protective insulating layer.
- [Claim 2] The LED of claim 1, wherein the reflection pattern further comprises a reflective metal layer formed on the second semiconductor layer and configured to reflect light, and the conductive barrier layer shields top and side surfaces of the reflective metal layer.
- [Claim 3] The LED of claim 2, wherein the reflection pattern further comprises a stress relaxation layer formed between the reflective metal layer and the conductive barrier layer and configured to absorb stress caused by a difference in coefficient of thermal expansion between the reflective metal layer and the conductive barrier layer.
- [Claim 4] The LED of claim 3, wherein a coefficient of thermal expansion of the stress relaxation layer is equal to or higher than a coefficient of thermal expansion of the conductive barrier layer and equal to or lower than a coefficient of thermal expansion of the reflective metal layer.
- [Claim 5] The LED of claim 3, wherein the reflective metal layer includes aluminum (Al), an Al alloy, silver (Ag), or an Ag alloy.
- [Claim 6] The LED of claim 5, wherein the conductive barrier layer includes tungsten (W), titanium tungsten (TiW), molybdenum (Mo), titanium (Ti), chromium (Cr), platinum (Pt), rhodium (Rh), palladium (Pd), or nickel (Ni).
- [Claim 7] The LED of claim 6, wherein when the reflective metal layer includes Al or an Al alloy and the conductive barrier layer includes W, TiW, or Mo, the stress relaxation layer is a single layer formed of Ag, Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd or Au.
- [Claim 8] The LED of claim 6, wherein when the reflective metal layer includes

- Al or an Al alloy and the conductive barrier layer includes Ti, Cr, Pt, Rh, Pd, or Ni, the stress relaxation layer is a single layer formed of Ag or Cu, or a combination formed of Ni, Au, Cu, or Ag.
- [Claim 9] The LED of claim 6, wherein when the reflective metal layer includes Ag or an Ag alloy and the conductive barrier layer includes W, TiW, or Mo, the stress relaxation layer is a single layer formed of Cu, Ni, Pt, Ti, Rh, Pd, or Cr, or a combination formed of Cu, Ni, Pt, Ti, Rh, Pd, Cr, or Au.
- [Claim 10] The LED of claim 6, wherein when the reflective metal layer includes Ag or an Ag alloy and the conductive barrier layer includes Pt or Ni, the stress relaxation layer is a single layer formed of Cu, Cr, Rh, Pd, TiW, or Ti, or a combination formed of Ni, Au, or Cu.
- [Claim 11] A method of manufacturing a light emitting diode (LED), comprising:
 sequentially forming a first semiconductor layer, an active layer, a second semiconductor layer, and a protective insulating layer on a substrate;
 etching the protective insulating layer, the second semiconductor layer, and the active layer and forming a mesa region exposing a surface of the first semiconductor layer;
 forming photoresist patterns having an overhang structure on the mesa region and etching the protective insulating layer exposed through a space between the photoresist patterns;
 forming a reflective metal layer on a surface of the second semiconductor layer that is exposed by etching the protective insulating layer; and
 forming a conductive barrier layer on the reflective metal layer, the conductive barrier layer extending to the protective insulating layer remaining under the photoresist pattern.
- [Claim 12] The method of claim 11, wherein the etching of the protective insulating layer comprises etching a region opened by the photoresist pattern and etching a partial region shielded by a lower portion of the photoresist pattern to leave a portion of the protective insulating layer under the photoresist pattern.
- [Claim 13] The method of claim 11, further comprising, after forming the reflective metal layer, forming a stress relaxation layer on the reflective metal layer to absorb stress caused by a difference in coefficient of thermal expansion.
- [Claim 14] The method of claim 11, wherein the etching of the protective in-

- insulating layer is performed using an isotropic wet etching process.
- [Claim 15] A method of manufacturing a light emitting diode (LED), comprising:
sequentially forming a first semiconductor layer, an active layer, and a second semiconductor layer on a substrate;
etching the second semiconductor layer and the active layer and forming a mesa region exposing a surface of the first semiconductor layer;
forming a protective insulating layer on the mesa region and the exposed second semiconductor layer;
forming photoresist patterns having an overhang structure on the mesa region and etching the protective insulating layer exposed through a space between the photoresist patterns;
forming a reflective metal layer on a surface of the second semiconductor layer that is exposed by etching the protective insulating layer; and
forming a conductive barrier layer on the reflective metal layer, the conductive barrier layer extending to the protective insulating layer remaining under the photoresist pattern.
- [Claim 16] A method of manufacturing a light emitting diode (LED) module, comprising:
coating a first insulating layer on a structure in which a first semiconductor layer, an active layer, a second semiconductor layer, and a reflection pattern are formed on a substrate and exposing the reflection pattern and the first semiconductor layer;
forming a conductive reflection layer and a reflective barrier layer on the first insulating layer, the reflective barrier layer electrically connected to the first semiconductor layer through the conductive reflection layer and configured to expose the reflection pattern;
coating a second insulating layer on the reflective barrier layer to expose the reflection pattern and exposing the reflective barrier layer electrically connected to the first semiconductor layer; and
forming a first pad on the reflective barrier layer and forming a second pad on the reflection pattern.
- [Claim 17] The method of claim 16, wherein the forming of the structure in which the first semiconductor layer, the active layer, the second semiconductor layer, and the reflection pattern are formed comprises:
sequentially forming the first semiconductor layer, the active layer, the second semiconductor layer, and a protective insulating layer on the

substrate;

etching the protective insulating layer, the second semiconductor layer, and the active layer and forming a mesa region exposing a surface of the first semiconductor layer;

forming photoresist patterns having an overhang structure on the mesa region and etching the protective insulating layer exposed through a space between the photoresist patterns;

forming a reflective metal layer on a surface of the second semiconductor layer that is exposed by etching the protective insulating layer; and

forming a conductive barrier layer on the reflective metal layer, the conductive barrier layer extending to the protective insulating layer remaining under the photoresist pattern.

[Claim 18]

The method of claim 16, wherein the forming of the structure in which the first semiconductor layer, the active layer, the second semiconductor layer, and the reflection pattern are formed comprises: sequentially forming the first semiconductor layer, the active layer, and the second semiconductor layer on the substrate;

etching the second semiconductor layer and the active layer and forming a mesa region exposing a surface of the first semiconductor layer;

forming a protective insulating layer on the mesa region and the exposed second semiconductor layer;

forming photoresist patterns having an overhang structure on the mesa region and etching the protective insulating layer exposed through a space between the photoresist patterns;

forming a reflective metal layer on a surface of the second semiconductor layer that is exposed by etching the protective insulating layer; and

forming a conductive barrier layer on the reflective metal layer, the conductive barrier layer extending to the protective insulating layer remaining under the photoresist pattern.

[Claim 19]

The method of claim 16, wherein the reflective barrier layer is a single layer formed of Ni, Cr, or Au, or a combination thereof.

[Claim 20]

The method of claim 16, wherein the reflective barrier layer is a combination formed of Ti/Al/Ti/Ni/Au.

[Claim 21]

The method of claim 16, further comprising, after forming the first pad and the second pad, forming a pad barrier layer on at least one of the

first and second pads, the pad barrier layer configured to prevent diffusion of metal atoms during a bonding process or a soldering process.

[Claim 22] The method of claim 21, wherein the pad barrier layer includes Cr, Ni, Ti W, TiW, Mo, Pt, or a combination thereof.

[Claim 23] A light emitting diode (LED) comprising:
a substrate;
a first semiconductor layer formed on the substrate;
an active layer formed on the first semiconductor layer and configured to generate light;
a second semiconductor layer formed on the active layer and having a complementary conductivity type to the first semiconductor layer; and
a reflection pattern formed on the second semiconductor layer and having a conductive barrier layer having a different thickness according to an underlying layer.

[Claim 24] The LED of claim 23, wherein the reflection pattern further comprises a reflective metal layer formed on the second semiconductor layer and configured to reflect light, and the conductive barrier layer shields top and side surfaces of the reflective metal layer.

[Claim 25] The LED of claim 24, wherein a side surface of the reflective metal layer is inclined at an angle of about 5° to about 45° with respect to a surface of the second semiconductor layer.

[Claim 26] The LED of claim 25, wherein the reflection pattern further comprises a stress relaxation layer formed between the reflective metal layer and the conductive barrier layer and configured to absorb stress caused by a difference in coefficient of thermal expansion between the reflective metal layer and the conductive barrier layer.

[Claim 27] The LED of claim 26, wherein a coefficient of thermal expansion of the stress relaxation layer is equal to or higher than a coefficient of thermal expansion of the conductive barrier layer and equal to or lower than a coefficient of thermal expansion of the reflective metal layer.

[Claim 28] The LED of claim 26, wherein the reflective metal layer includes Al, an Al alloy, Ag, or an Ag alloy.

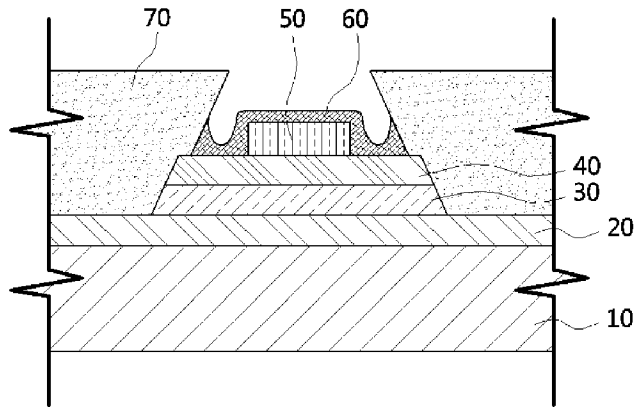
[Claim 29] The LED of claim 28, wherein the conductive barrier layer includes W, TiW, Mo, Ti, Cr, Pt, Rh, Pd, or Ni.

[Claim 30] The LED of claim 25, wherein the conductive barrier layer shields the reflective metal layer and continuously extends to the surface of the second semiconductor layer.

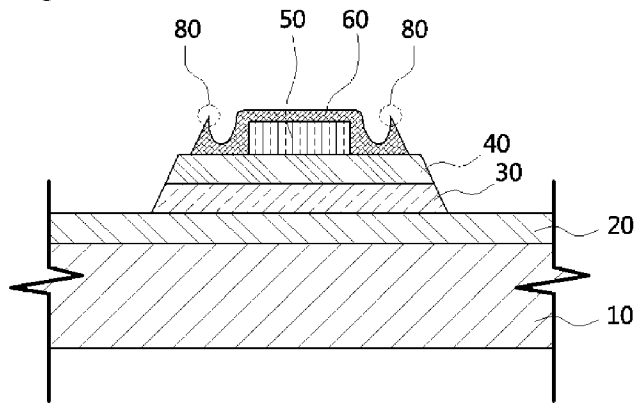
[Claim 31]

The LED of claim 30, wherein a thickness of the conductive barrier layer formed on the reflective metal layer is greater than a thickness of the conductive barrier layer formed on the second semiconductor layer, and the thickness of the conductive barrier layer formed on the second semiconductor layer is greater than a thickness of the conductive barrier layer formed on a side surface of the reflective metal layer.

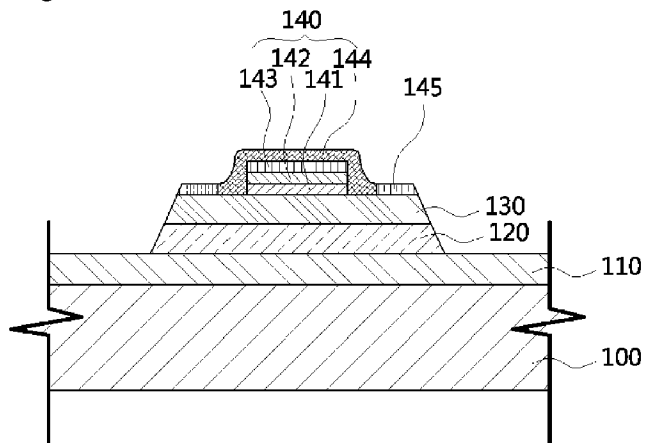
[Fig. 1]



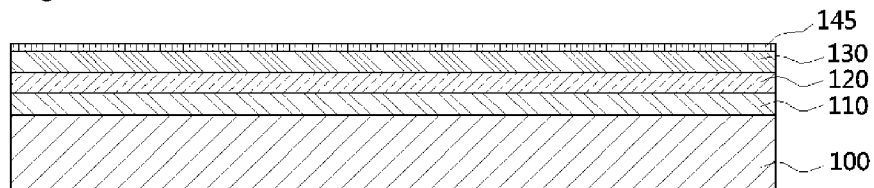
[Fig. 2]



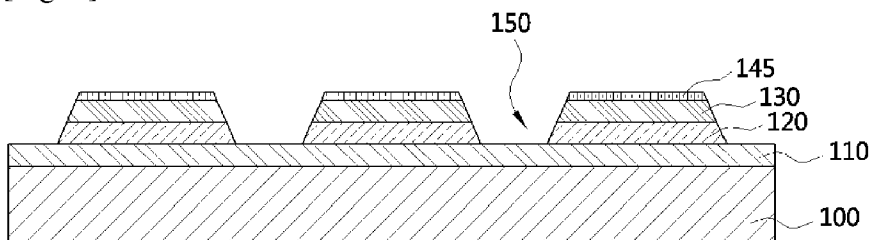
[Fig. 3]



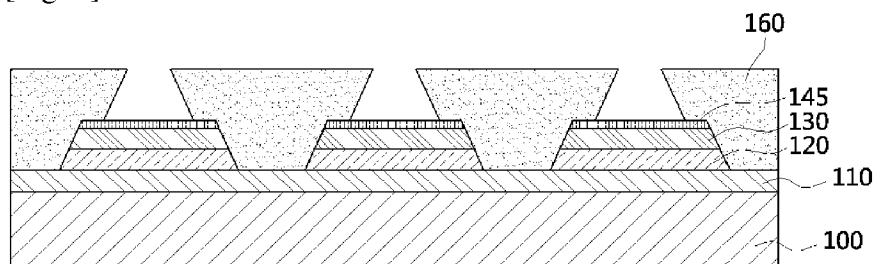
[Fig. 4]



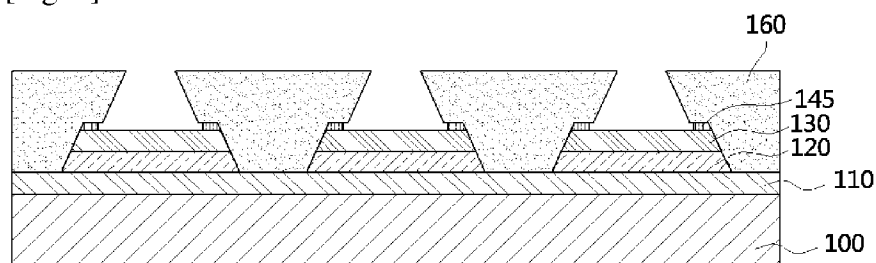
[Fig. 5]



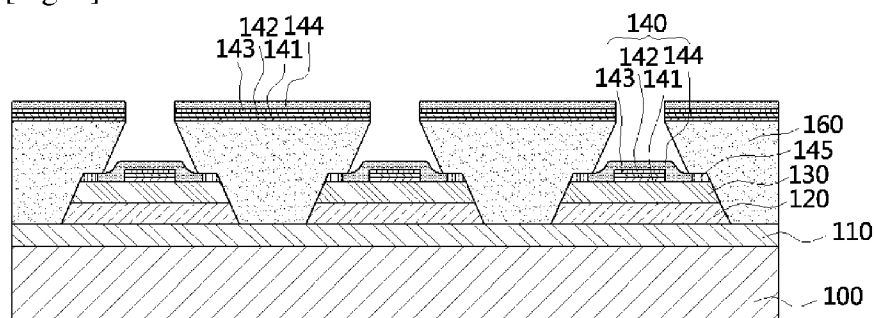
[Fig. 6]



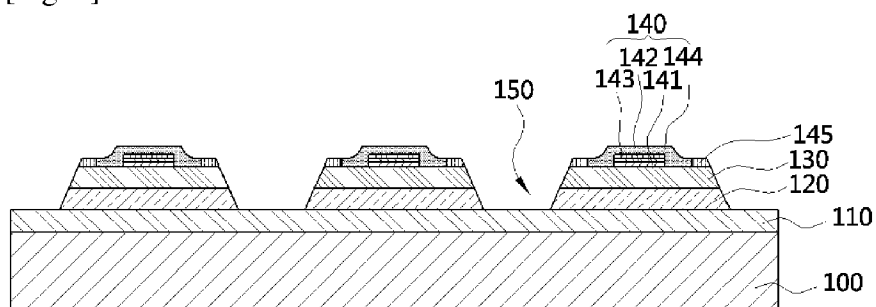
[Fig. 7]



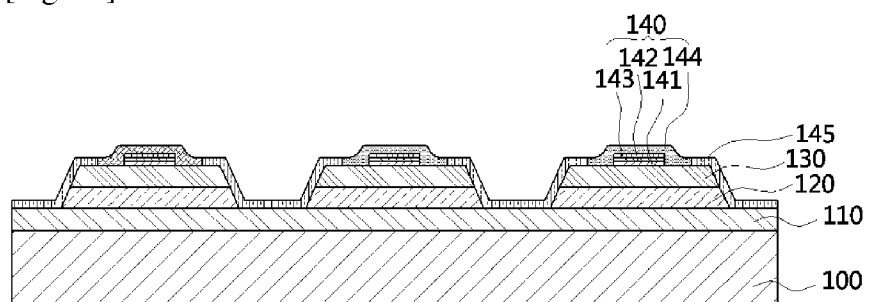
[Fig. 8]



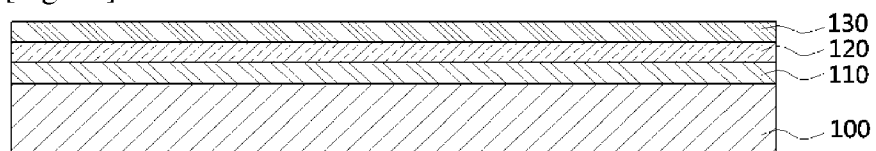
[Fig. 9]



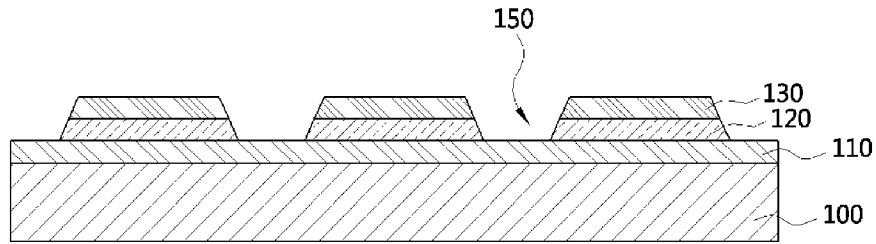
[Fig. 10]



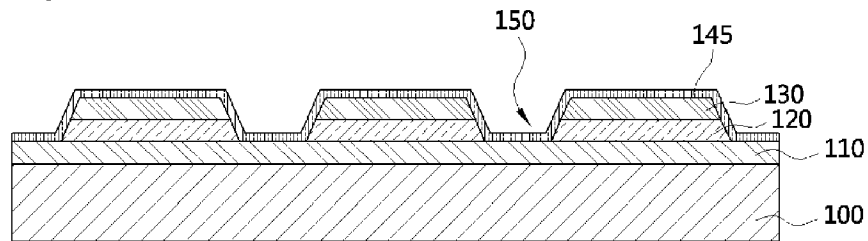
[Fig. 11]



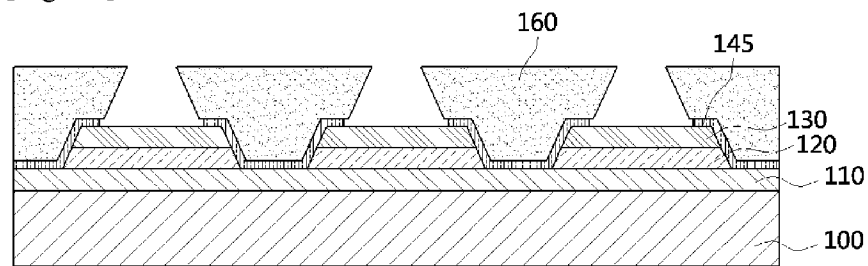
[Fig. 12]



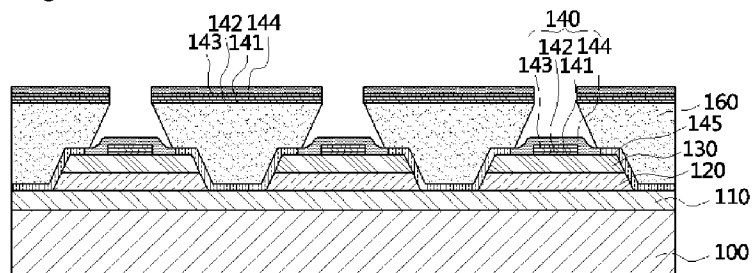
[Fig. 13]



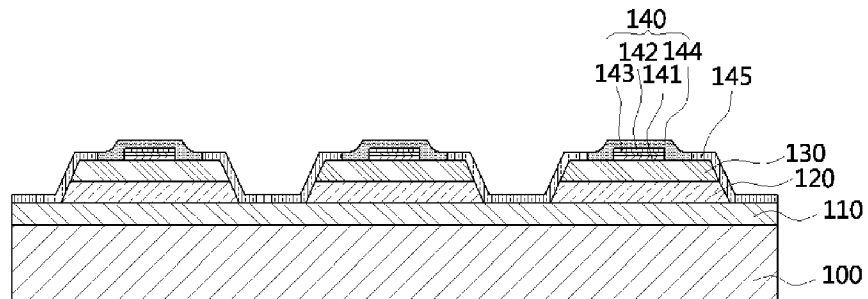
[Fig. 14]



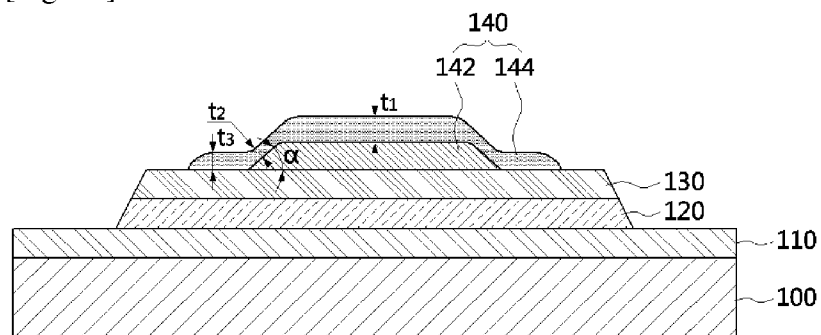
[Fig. 15]



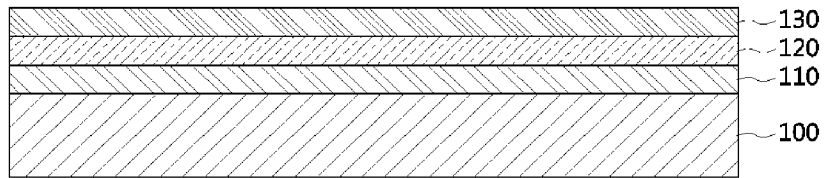
[Fig. 16]



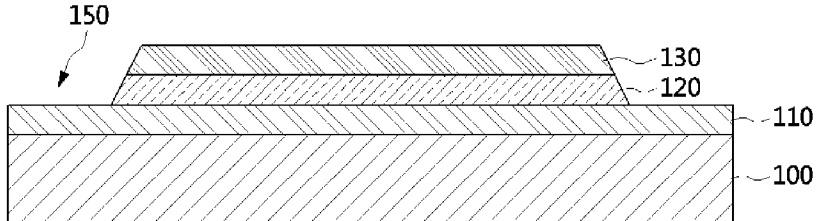
[Fig. 17]



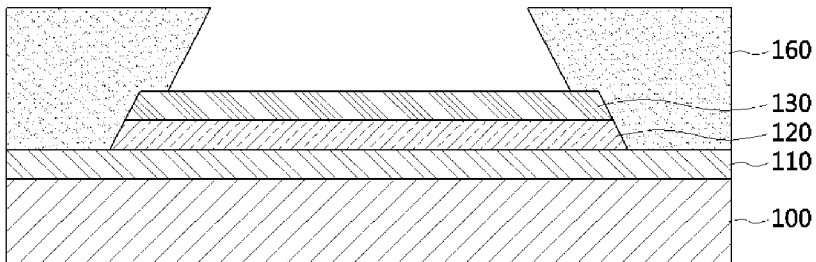
[Fig. 18]



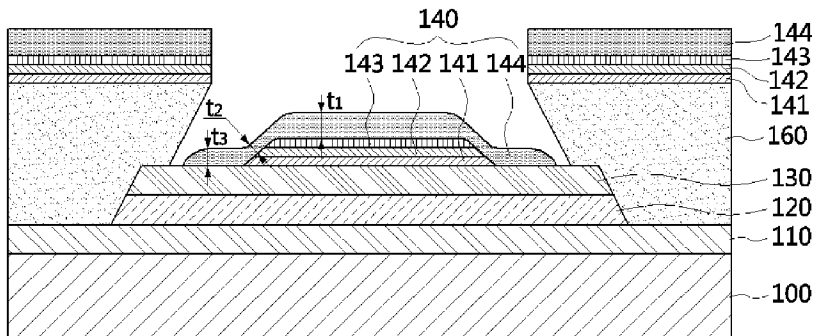
[Fig. 19]



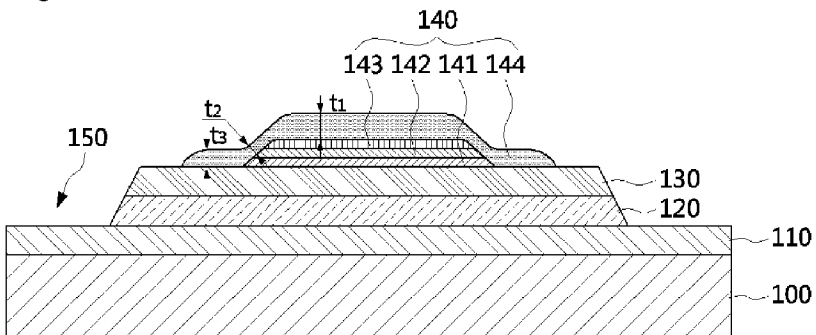
[Fig. 20]



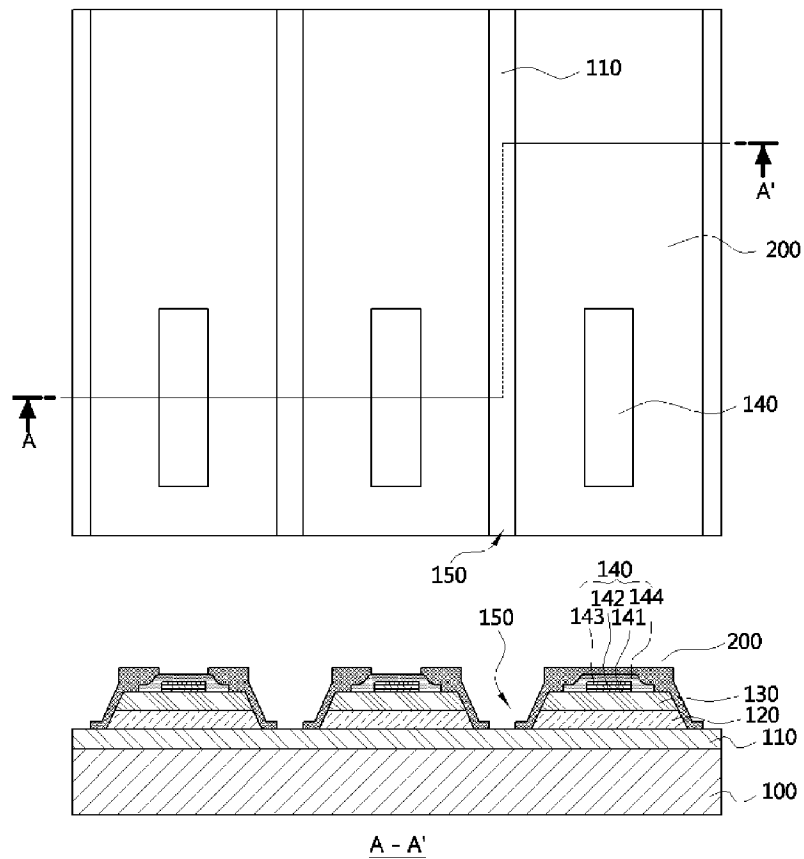
[Fig. 21]



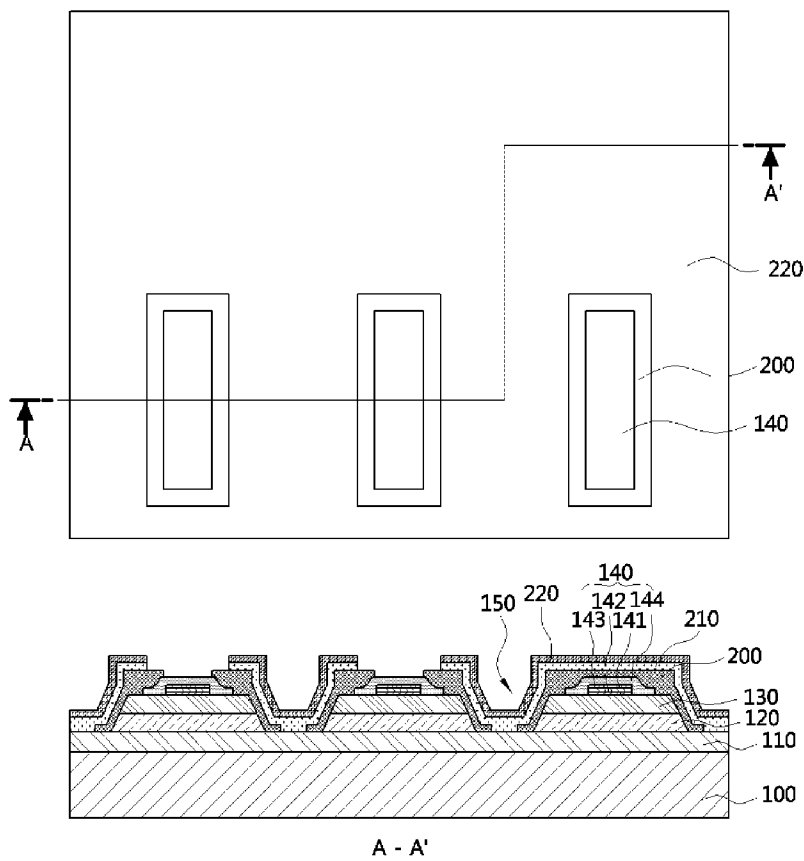
[Fig. 22]



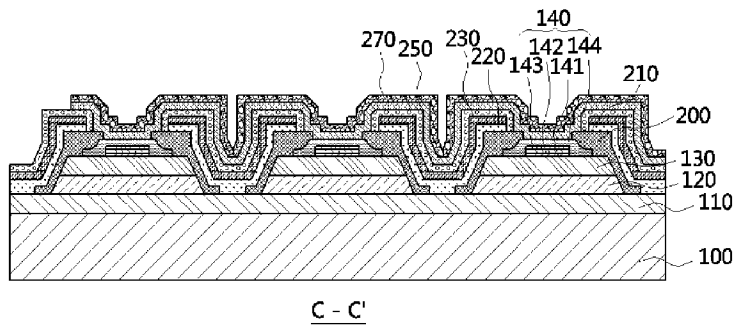
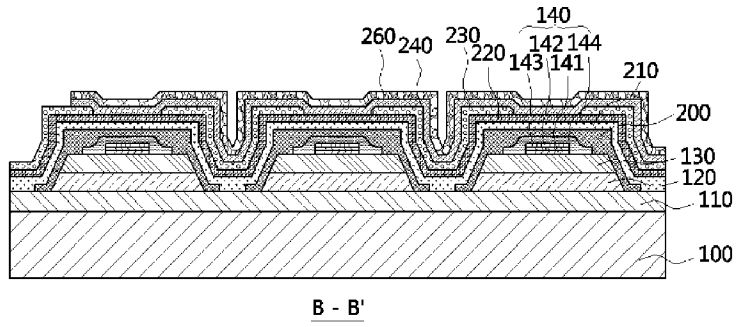
[Fig. 23]



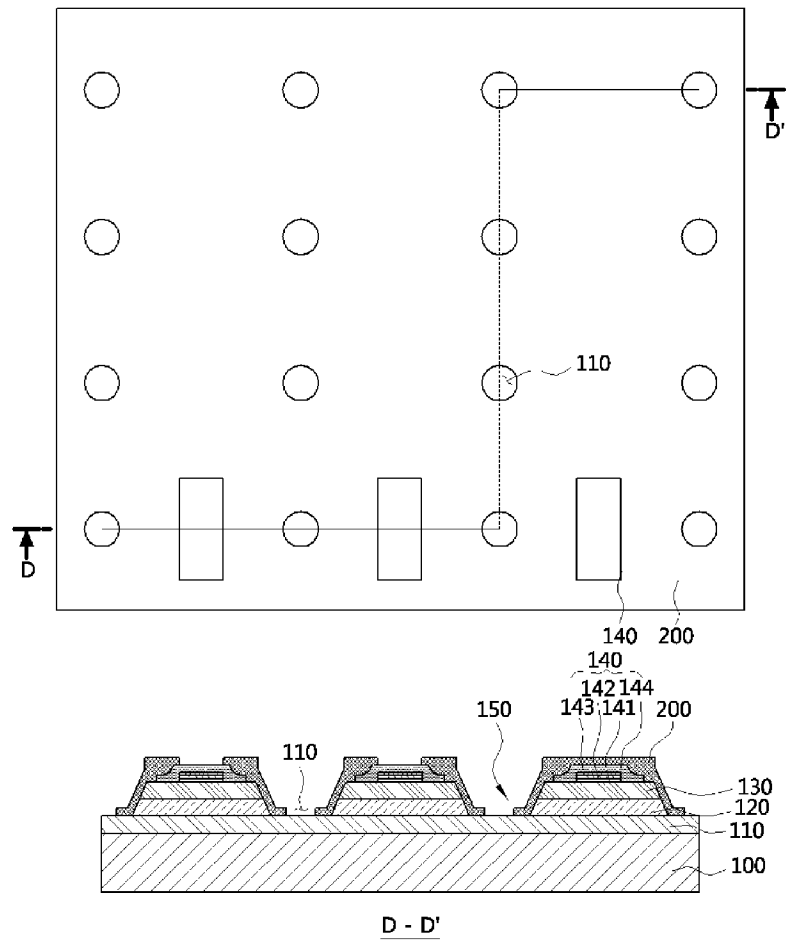
[Fig. 24]



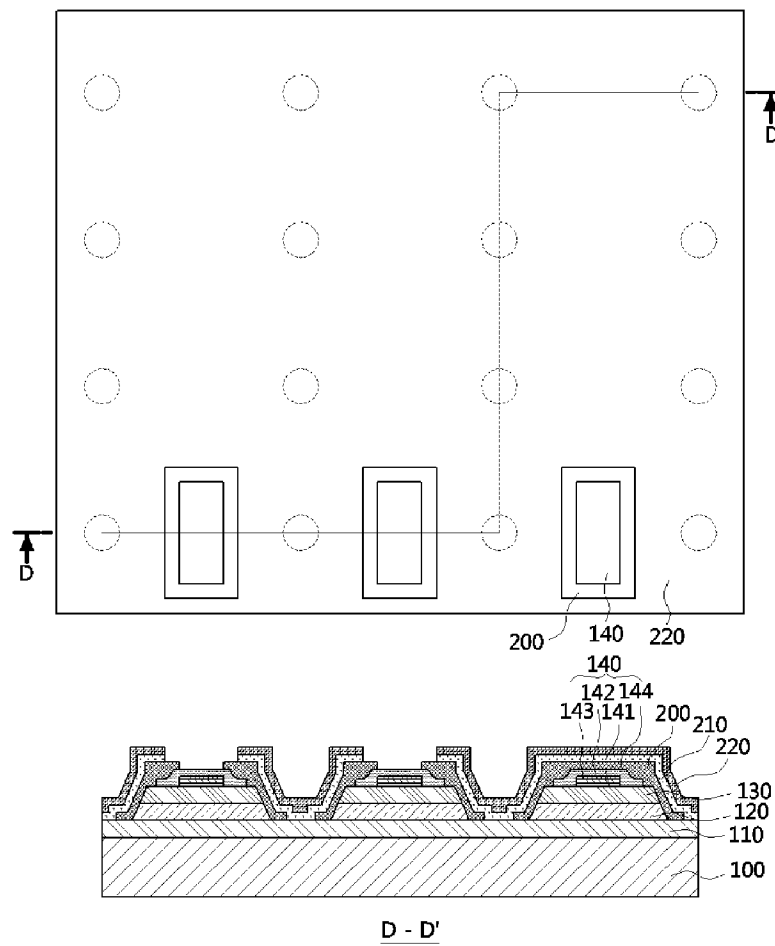
[Fig. 27]



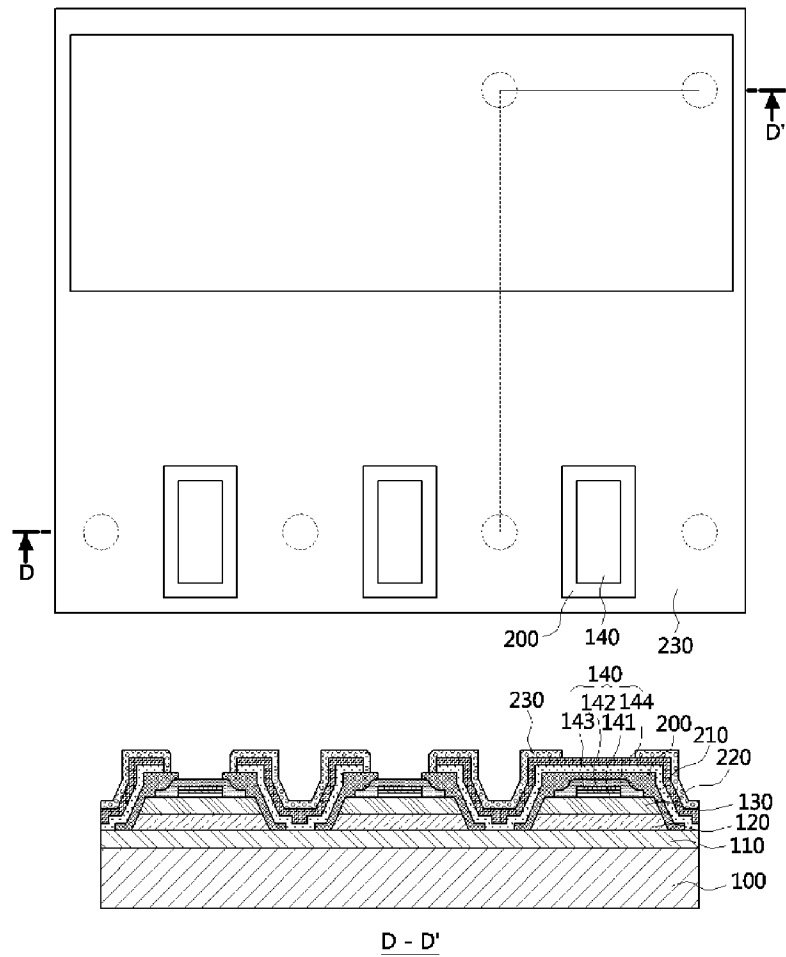
[Fig. 28]



[Fig. 29]



[Fig. 30]



A. CLASSIFICATION OF SUBJECT MATTER**H01L 33/44(2010.01)i, H01L 33/46(2010.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/44; H01L 33/00; H01L 33/36; H01L 33/46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: LED, reflection pattern, photoresist pattern, electrode, protective insulating layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006-0249736 A1 (JAE HOON LEE et al.) 09 November 2006 See paragraphs [0070]-[0081] and figure 5f.	1
A		2-31
A	US 2006-0071228 A1 (DECAI SUN) 06 April 2006 See paragraph [0028] and figure 5D.	1-31
A	JP 2007-234918 A (TOYODA GOSEI CO., LTD.) 13 September 2007 See paragraphs [0016]-[0028] and figure 1.	1-31
A	JP 2007-019467 A (SONY CORP.) 25 January 2007 See paragraphs [0044]-[0051] and figures 14-16.	1-31
A	JP 2010-263016 A (SHOWA DENKO K.K.) 18 November 2010 See paragraphs [0080]-[0094] and figures 7-10.	1-31
A	JP 2009-188422 A (STANLEY ELECTRIC CO., LTD.) 20 August 2009 See paragraphs [0031]-[0034] and figures 1(A), 12(A).	1-31



Further documents are listed in the continuation of Box C.



See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

27 August 2013 (27.08.2013)

Date of mailing of the international search report

28 August 2013 (28.08.2013)

Name and mailing address of the ISA/KR

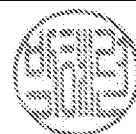
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2013/005254

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