US 20090065772A1

(19) United States

(12) Patent Application Publication

PARK

(10) Pub. No.: US 2009/0065772 A1

(43) Pub. Date: Mar. 12, 2009

(54) **APPARATUS FOR DETECTING PATTERN ALIGNMENT ERROR**

(76) Inventor: **Jeong Hyun PARK**, Seoul (KR)

Correspondence Address:
LADAS & PARRY LLP
224 SOUTH MICHIGAN AVENUE, SUITE 1600
CHICAGO, IL 60604 (US)

(21) Appl. No.: **11/868,561**

(22) Filed: **Oct. 8, 2007**

(30) **Foreign Application Priority Data**

Sep. 10, 2007 (KR) 10-2007-0091798

Publication Classification

(51) **Int. Cl.**
G01R 31/26 (2006.01)

(52) **U.S. Cl.** **257/48**; 257/E21.522

(57) **ABSTRACT**

An apparatus for detecting pattern alignment error includes a first conductive pattern disposed over a first insulation member with a power source applied to the first conductive pattern; a second insulation member for covering the first conductive pattern; a second conductive pattern disposed on the second insulation member; a conductive via connected to the second conductive pattern and passing through the second insulation member; and an insulation pattern disposed in the first conductive pattern for detecting an alignment error in response to a position of the conductive via. The apparatus for detecting pattern alignment error can detect the alignment of lower wiring in a device with multi-layer wiring

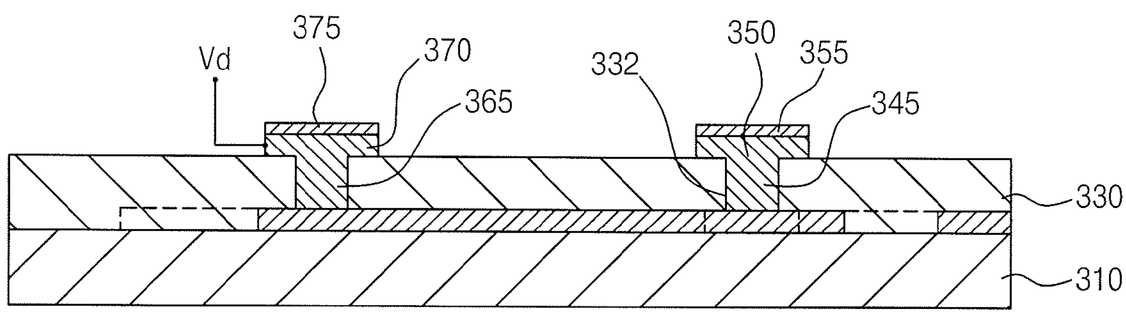


FIG.1

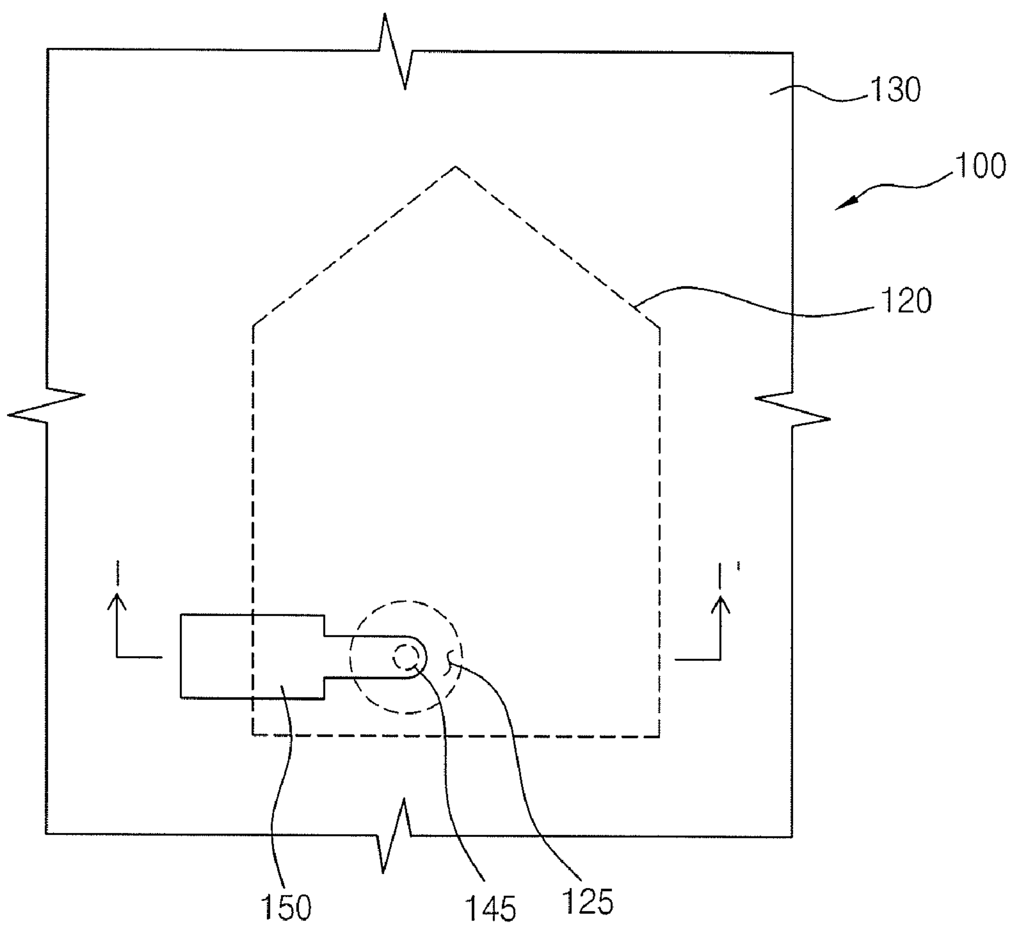


FIG.2

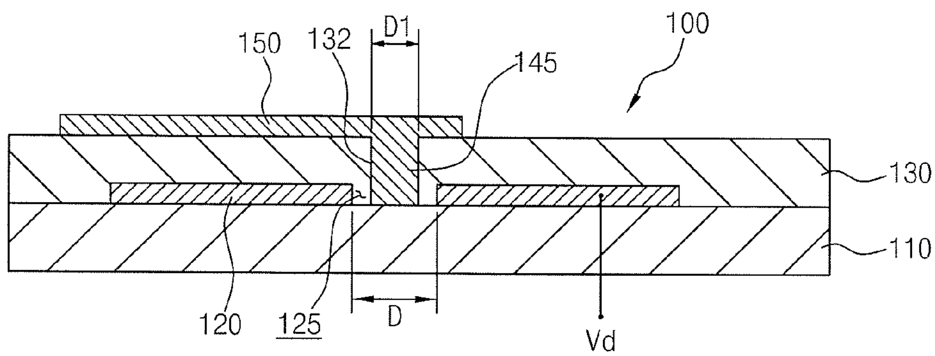

150
132
D1
145
100
130
110
120
125
D
Vd

FIG.3

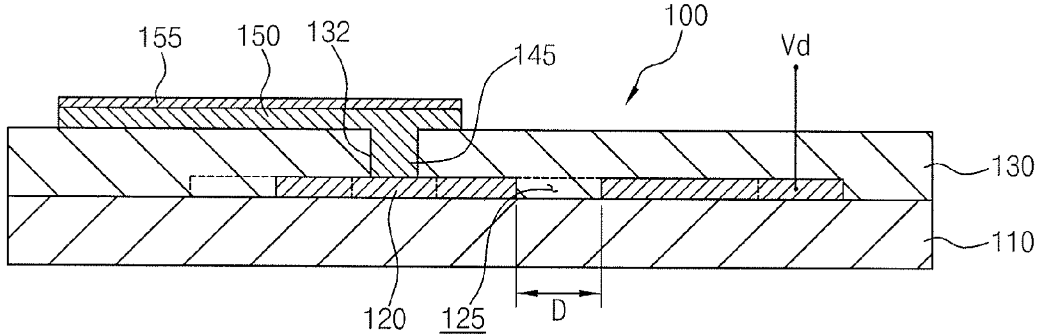

155
150
132
145
100
Vd
130
110
120
125
D

FIG.4

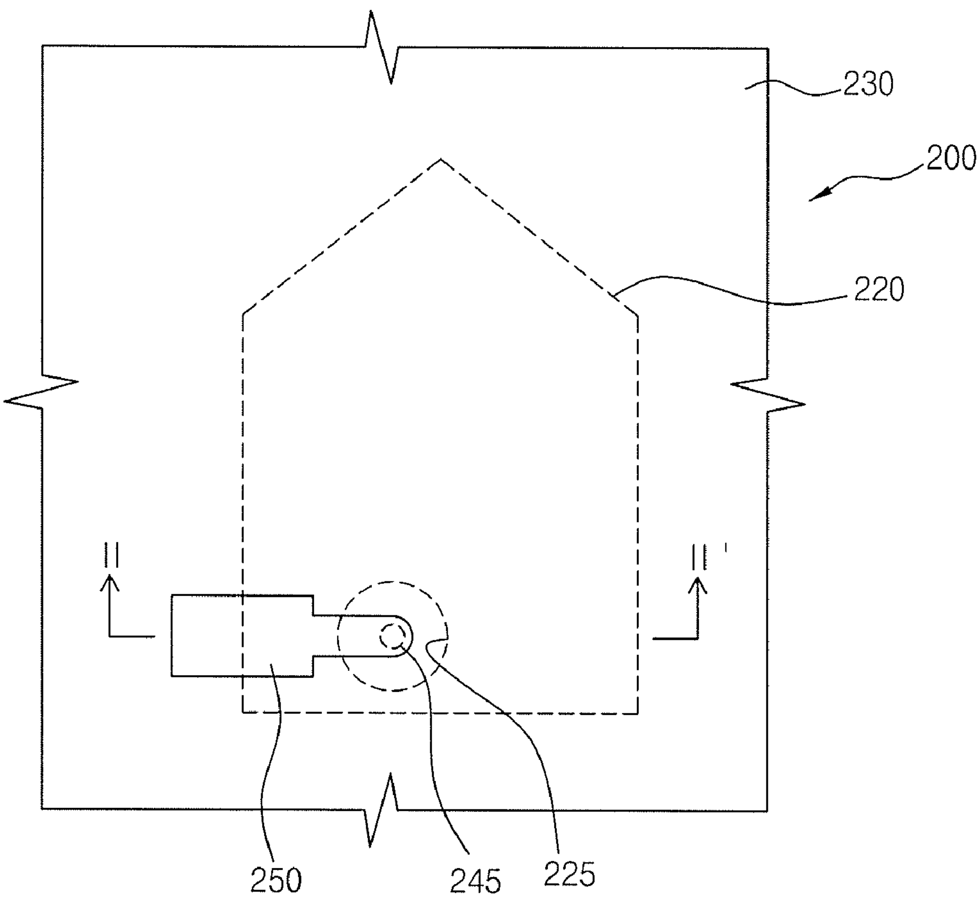


FIG.5

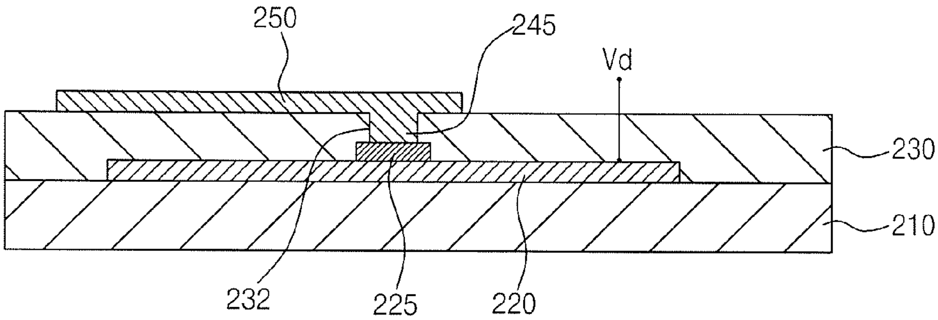


FIG.6

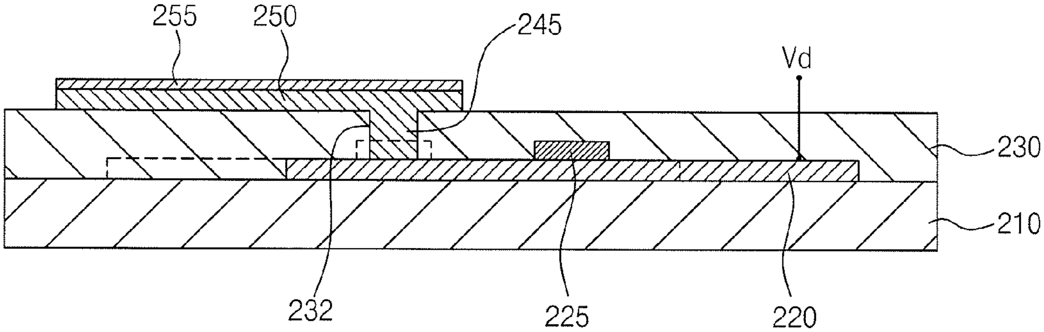


FIG.7

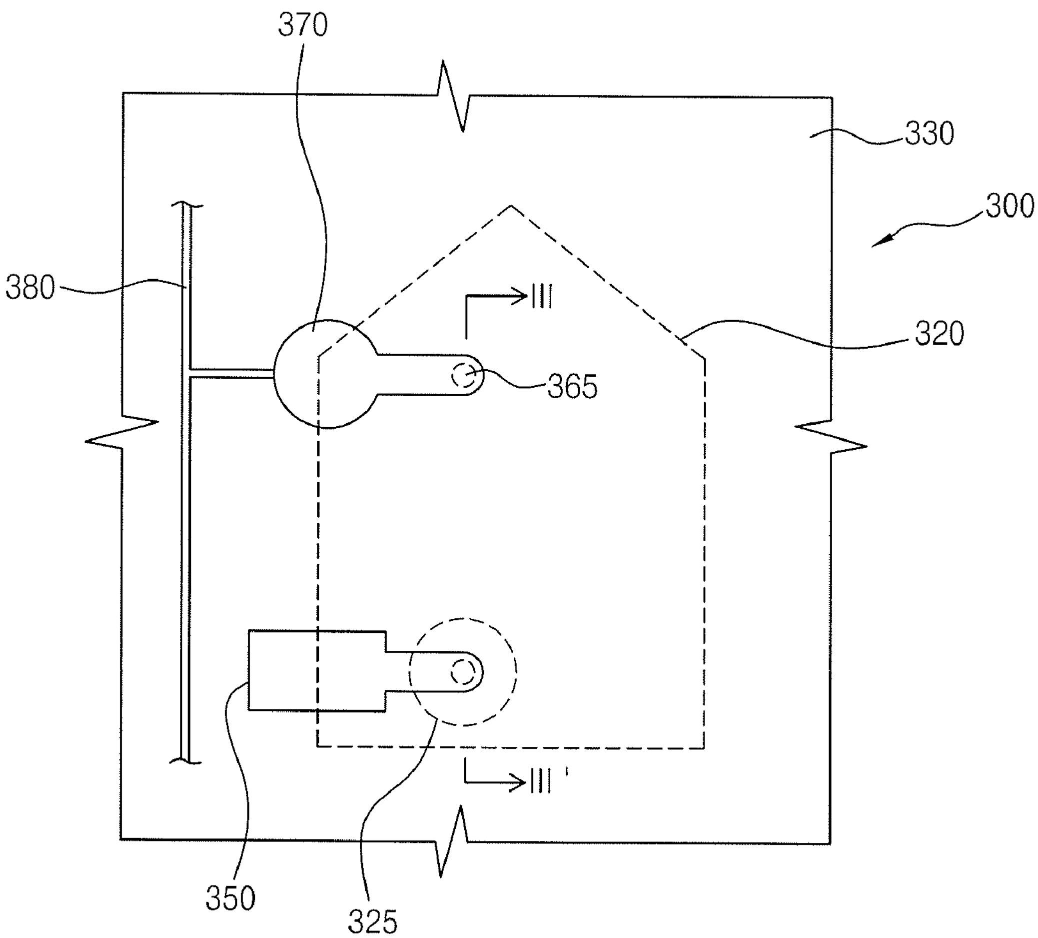


FIG.8

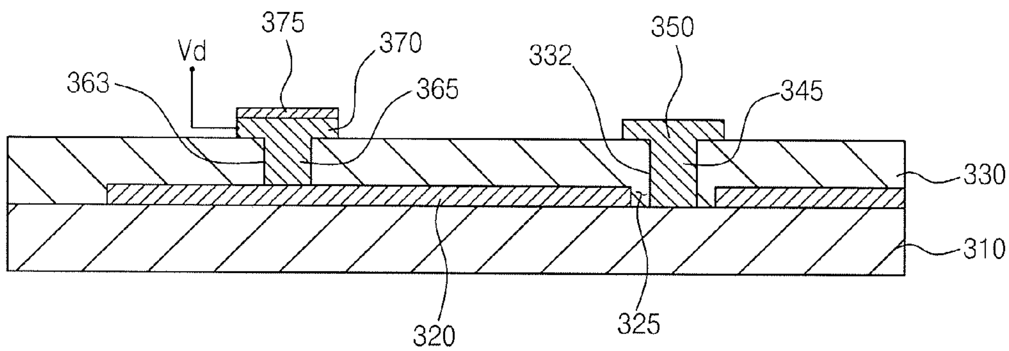

375
370
Vd
363
365
332
350
345
330
310
320
325

FIG.9

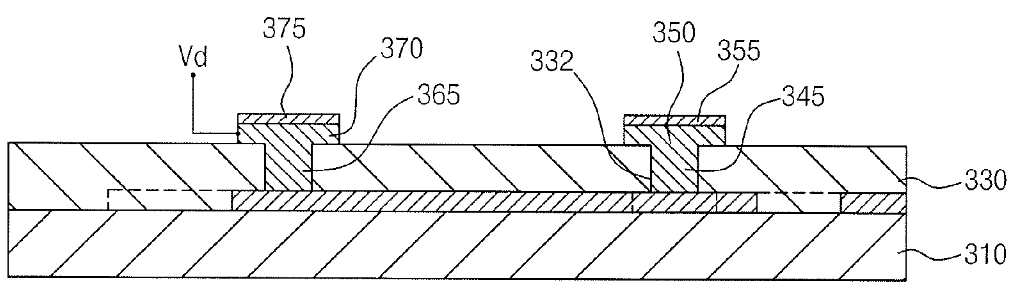

375
370
Vd
365
332
350
355
345
330
310

FIG.10

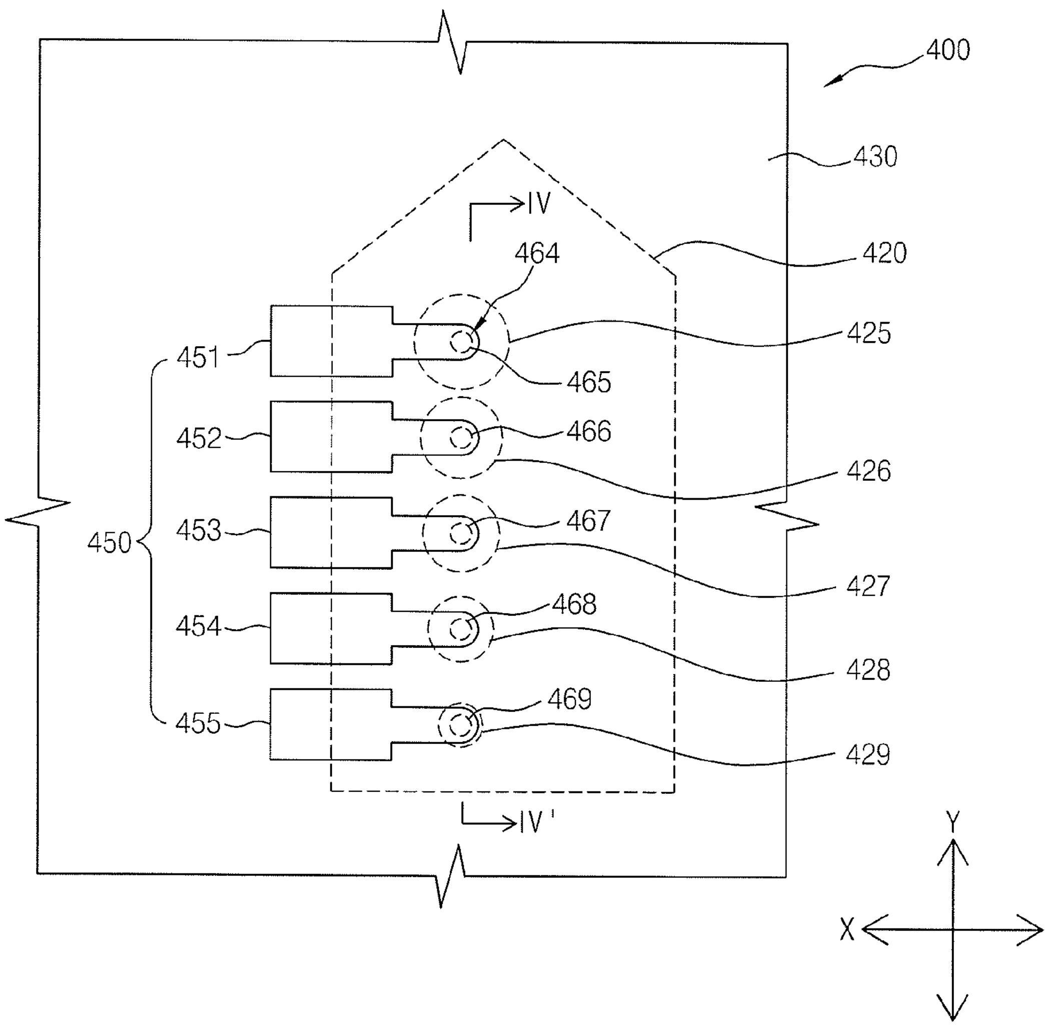

400
430
IV
464
420
425
451
465
452
466
426
450
453
467
427
454
468
428
455
469
429
IV'
Y
X

FIG. 11

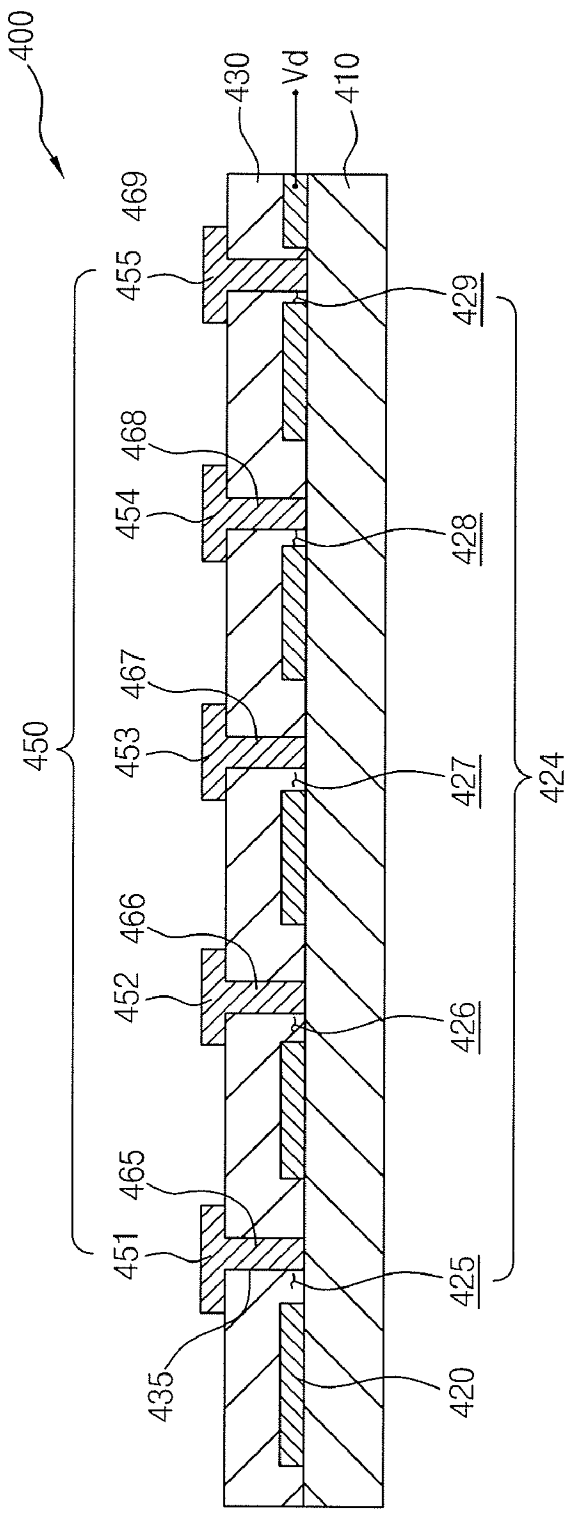
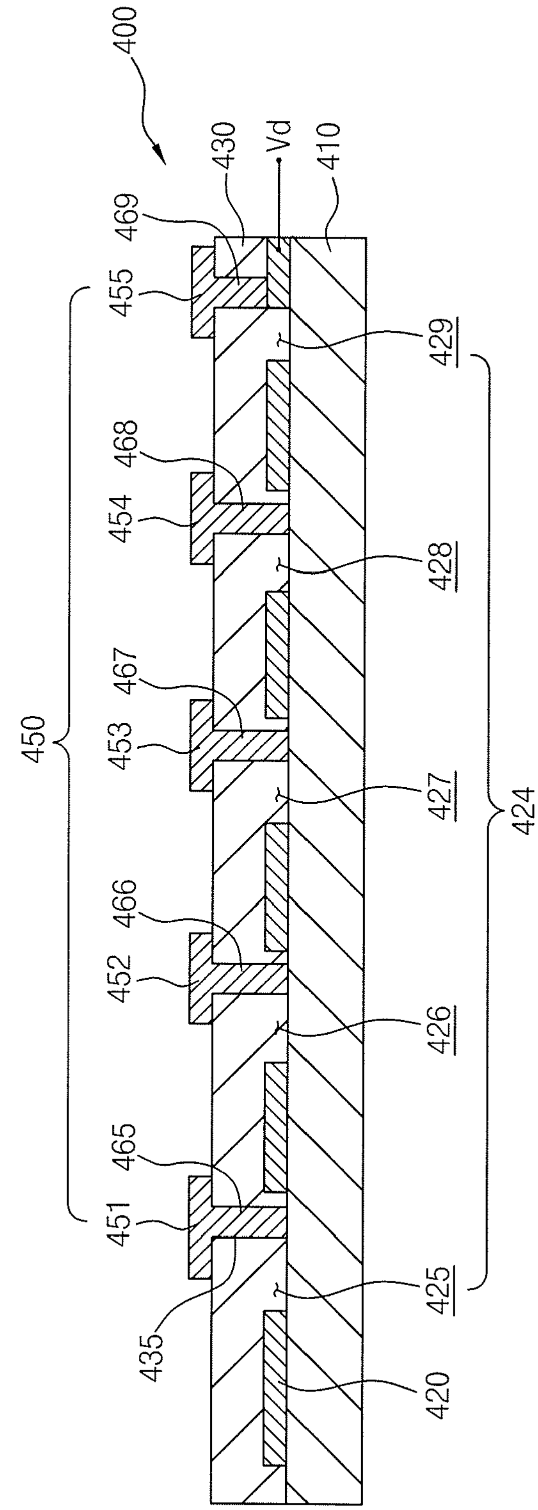

400
430
Vd
410
469
455
429
468
454
428
467
453
450
427
424
466
452
426
465
451
425
435
420

FIG. 12


400
430
Vd
410
469
455
429
468
454
428
467
453
450
427
424
466
452
426
465
451
425
435
420

APPARATUS FOR DETECTING PATTERN ALIGNMENT ERROR

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority to Korean patent application number 10-2007-91798 filed on Sep. 10, 2007, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to an apparatus for detecting a pattern alignment error.

[0003] Recent, developments in semiconductor device fabrication have led to a technology for fabricating a semiconductor package with a semiconductor device and a circuit board on which the semiconductor package is mounted.

[0004] In the development, the semiconductor device, semiconductor package and circuit board may have a multi-layered wiring structure.

[0005] For example, a circuit board may include wirings disposed on different layers in order to input or output various types of signals.

[0006] In this technology, in order to form the wirings in different layers, a lower wiring is formed on a lower insulation member, and the lower wiring is insulated by an upper insulation member. Subsequently, an upper wiring is formed on the upper insulation member, and the upper wiring is then electrically connected to the lower wiring through a conductive via.

[0007] However, when the wirings are disposed on different layers, they are often not aligned accurately, and the upper wiring and lower wiring end up not being connected to each other through the conductive via.

[0008] An alignment error of the upper wiring can be easily recognized through a visual test while, but an alignment error of the lower wiring is hard to recognized through a visual test because the lower wiring has been covered by the upper insulation member.

BRIEF SUMMARY OF THE INVENTION

[0009] Embodiments of the present invention are directed to an apparatus for detecting pattern alignment error, and more specifically to an apparatus that is adapted to detect the alignment of the lower wiring of a device with multi-layered wiring.

[0010] In one embodiment, an apparatus for detecting pattern alignment error may comprise a first conductive pattern disposed over a first insulation member with a power source applied to the first conductive pattern; a second insulation member covering the first conductive pattern; a second conductive pattern disposed on the second insulation layer; a conductive via connected to the second conductive pattern and passing through the second insulation member; and an insulation pattern disposed in the first conductive pattern for detecting an alignment error in response to a position of the conductive via.

[0011] The insulation pattern may be a through hole passing through the first conductive pattern. Alternatively, the insulation pattern may be disposed over the first conductive pattern.

[0012] The power source is a DC voltage. An area of the insulation pattern is about 105 to 200% of the area of the conductive via. The insulation pattern may have a circular shape when viewed from above with a diameter of 50 μm to 200 μm.

[0013] The apparatus for detecting pattern alignment error may further comprise a third conductive pattern disposed over the second insulation member and an additional conductive via passing through the second insulation member that connects the third conductive pattern to the first conductive pattern; and a power line that is electrically connected to the third conductive pattern rather than the first conductive pattern and a power source applied to the power line.

[0014] A plated layer may be formed on the second and third conductive patterns in a case where the conductive via is disposed over the first conductive pattern.

[0015] The plated layer will be formed only on the third conductive pattern in a case where the conductive via is disposed over the insulation pattern rather than the first conductive pattern.

[0016] The apparatus for detecting a pattern alignment error may include a number of second conductive patterns and insulation patterns corresponding to each second conductive pattern, and the insulation patterns may all be different sizes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. **1** is a plan view illustrating an apparatus for detecting pattern alignment error in accordance with a first embodiment of the present invention.

[0018] FIG. **2** is a cross-sectional view taken along line I-I' in FIG. **1**.

[0019] FIG. **3** is a cross-sectional view illustrating that a first conductive pattern shown in FIG. **2** is disposed out of the alignment error range.

[0020] FIG. **4** is a plan view illustrating an apparatus for detecting pattern alignment error in accordance with a second embodiment of the present invention.

[0021] FIG. **5** is a cross-sectional view taken along line II-II' in FIG. **4**.

[0022] FIG. **6** is a cross-sectional view illustrating that a first conductive pattern shown in FIG. **5** is disposed out of the alignment error range.

[0023] FIG. **7** is a plan view illustrating an apparatus for detecting pattern alignment error in accordance with a third embodiment of the present invention.

[0024] FIG. **8** is a cross-sectional view taken along line III-III' in FIG. **7**.

[0025] FIG. **9** is a cross-sectional view illustrating that a first conductive pattern shown in FIG. **8** is disposed out of the alignment error range.

[0026] FIG. **10** is a plan view illustrating an apparatus for detecting pattern alignment error in accordance with a fourth embodiment of the present invention.

[0027] FIG. **11** is a cross-sectional view taken along line IV-IV' in FIG. **9**.

[0028] FIG. **12** is a cross-sectional view illustrating that a first conductive pattern shown in FIG. **11** is disposed out of the alignment error range.

DESCRIPTION OF SPECIFIC EMBODIMENTS

[0029] Hereafter, an apparatus for detecting a pattern alignment error in accordance with embodiments of the present invention will be described with reference to the attached drawings.

[0030] The apparatus for detecting a pattern alignment error to be described herein after is disposed at a periphery of an active area on which a multi-layered wiring is formed. Also, a first conductive pattern of the apparatus for detecting a pattern alignment error is formed simultaneously with the lower wiring disposed at the active area. A second pattern is formed simultaneously with the upper wiring disposed at the active area.

[0031] FIG. **1** is a plan view illustrating an apparatus for detecting pattern alignment error in accordance with a first embodiment of the present invention. FIG. **2** is a cross-sectional view taken along line I-I' in FIG. **1** showing a case where the first conductive layer is formed within the alignment error range. FIG. **3** shows a case where the first conductive layer is formed outside of the alignment error range.

[0032] Referring to FIGS. **1**, **2**, and **3**, the pattern alignment error detecting apparatus **100** includes a first insulation member **110**, a first conductive pattern **120** having an insulation pattern **125**, a second insulation member **130**, and a second conductive pattern **150** having a conductive via **145**.

[0033] The first conductive pattern **120** is disposed over the first insulation member **110** which includes insulation material. The first conductive pattern **120** may be electrically connected, for example, to a power line (not shown) through which a DC power source Vd is applied.

[0034] In the present embodiment, an example of material which may be used as the first conductive pattern **120** and the power line include aluminum, aluminum alloy, copper, cooper alloy, metal alloy, etc.

[0035] The first conductive pattern **120** includes the insulation pattern **125**. The insulation pattern **125** may be disposed, for example, in the center part of the first conductive pattern **120**. In the present embodiment, the insulation pattern **125** may be a through hole that is formed in a portion of the first conductive pattern **120**. The insulation pattern **125** has a circular shape when viewed from above with a diameter D. For example, the diameter D of the insulation pattern **125** may be about 50 μm to about 200 μm The diameter D of the insulation pattern **125** may otherwise vary within the alignment error range.

[0036] The second insulation member **130** is disposed over the first insulation member **110** and consequently covers the first conductive pattern **120**. The second insulation member **130** includes insulation material.

[0037] A via hole **132** passes through the second insulation member **130**. In the present embodiment, when the first conductive pattern **120** is formed within the alignment error range, the via hole **132** is located at the portion corresponding to the insulation pattern **125** of the first conductive pattern **120** (as shown in FIG. **2**). When the first conductive pattern **120** is formed outside of the alignment error range, the via hole **132** will be located at a portion of the first conductive pattern **120** adjacent to the insulation pattern **125** (as shown in FIG. **3**).

[0038] A conductive via **145** is placed inside the via hole **132** formed in the second insulation member **130**. In the present embodiment, the conductive via **145** may have a cylindrical shape. The conductive via **145** having a cylindrical shape has a diameter D1 that is smaller than the diameter D of the insulation pattern **125**. In the present embodiment, the area of the insulation pattern **125** may be about 105 to 200% of the area of the conductive via **145**.

[0039] The second conductive pattern **150** is disposed over the second insulation member **130**. In the present embodiment, the conductive via **145** and the second conductive pattern **150** may be formed integrally.

[0040] An examples of material that may be used as the conductive via **145** and the second conductive pattern **150** include aluminum, aluminum alloy, copper, cooper alloy, and metal alloy, etc.

[0041] Hereinafter, the operation of the pattern alignment error detecting apparatus in accordance with the first embodiments of the present invention will be described with reference to the attached drawings.

[0042] FIG. **2** shows the case where the first conductive pattern **120** is disposed within the alignment error range. A plating solution may be applied to the second conductive pattern **150**. The conductive via **145** and the first conductive pattern **120** are spaced apart from each other (i.e. they don't connect) and thus the DC voltage Vd applied to the first conductive pattern **120** does not reach the second conductive pattern **150** through the conductive via **145**.

[0043] Therefore, when the first conductive pattern **120** is disposed within the alignment error range, the second conductive pattern **150** does not receive DC voltage Vd, and consequently a plated layer is not formed over the second conductive pattern **150** even when the second conductive pattern **150** comes into contact with a plating solution. When the plating area is not formed, the fact that the first conductive pattern **120** is disposed within the alignment error range is confirmed. Alternatively, it is possible to confirm that the first conductive pattern **120** is disposed within the alignment error range, by measuring the voltage of the second conductive pattern **150** rather than applying a plating solution.

[0044] FIG. **3** is a cross-sectional view illustrating that the first conductive pattern shown in FIG. **2** is disposed out of the alignment error range.

[0045] FIG. **3** shows a case where the first conductive pattern **120** is disposed out of the alignment error range. In FIG. **3**, the conductive via **145** is electrically connected to the first conductive pattern **120**. Therefore, the DC voltage Vd applied to the first conductive pattern **120** is reaches the second conductive pattern **150** through the conductive via **145**.

[0046] Therefore, when the plating solution is applied to the second conductive pattern **150** and the first conductive pattern **120** is out of the alignment error range, the second conductive pattern **150** receives DC voltage Vd and a plated layer **155** is formed over the second conductive pattern **150**. Alternatively, it is possible to confirm easily that the disposition of the first conductive pattern **120** is out of the alignment error range by measuring the voltage of the second conductive pattern **150** rather than applying the plating solution.

[0047] FIG. **4** is a plan view illustrating an apparatus for detecting pattern alignment error in accordance with a second embodiment of the present invention. FIG. **5** is a cross-sectional view taken along line II-II' in FIG. **4** showing a case where the first conductive layer is formed within the alignment error range. FIG. **6** shows a case where the first conductive layer is formed outside of the alignment error range.

[0048] Referring to FIGS. **4**, **5**, and **6**, the pattern alignment error detecting apparatus **200** includes a first insulation member **210**, a first conductive pattern **220** having an insulation pattern **225**, a second insulation member **230**, and a second conductive pattern **250** having a conductive via **245**.

[0049] The first conductive pattern **220** is disposed over the first insulation member **210**. The insulation member includes an insulation material. The first conductive pattern **220** is electrically connected, for example, to a power line (not shown) through which a DC power source Vd is applied.

[0050] In the present embodiment, examples of material that may be used as the first conductive pattern **220** and the power line include aluminum, aluminum alloy, copper, cooper alloy, metal alloy, etc.

[0051] The first conductive pattern **220** includes the insulation pattern **225**. The insulation pattern **225** may be disposed, for example, on the center part of the first conductive pattern **220**.

[0052] In the present embodiment, the insulation pattern **225** may be disposed over the first conductive pattern **220**. The insulation pattern **225** may be an insulation layer disposed over the first conductive pattern **220**, or alternatively, the insulation pattern **225** may be a photoresist pattern disposed over the first conductive pattern **220**.

[0053] The insulation pattern **225** disposed over the first conductive pattern **220** has a disc shape with a diameter D when viewed from above. The diameter D of the insulation pattern **225** may be about 50 μm to about 200 μm. The diameter D of the insulation pattern **225** may otherwise vary within an alignment error range.

[0054] The second insulation member **230** is disposed over the first insulation member **210** and consequently covers the first conductive pattern **220**. The second insulation member **230** includes insulation material.

[0055] A via hole **232** is located in the second insulation member **230**. The via hole **232** passes through the second insulation member **230**. In the present embodiment, when the first conductive pattern is formed within the alignment error range (as shown in FIG. **5**), the via hole **232** is formed in the area of the second insulation layer that corresponds to the insulation pattern **225** disposed over the first conductive pattern **220**. When the first conductive pattern is formed outside of the alignment error range (as shown in FIG. **6**), the via hole **232** is formed on a portion of the first conductive pattern **220** adjacent to the insulation pattern **225**.

[0056] A conductive via **245** is placed inside the via hole **232** formed in the second insulation member **230**. In the present embodiment, the conductive via **245** may have a cylindrical shape. The conductive via **245** having a cylindrical shape has a diameter D**1** that is smaller than the diameter D of the insulation pattern **225** disposed over the first conductive pattern **220**. In the present embodiment, the area of the insulation pattern **225** may be about 105 to 200% of the area of the conductive via **245**.

[0057] The second conductive pattern **250** is disposed over the second insulation member **230**. In the present embodiment, the conductive via **245** and the second conductive pattern **250** may be formed integrally.

[0058] Examples of material that may be used as the conductive via **245** and the second conductive pattern **250** include aluminum, aluminum alloy, copper, cooper alloy, metal alloy, etc.

[0059] Hereinafter, the operation of the pattern alignment error detecting apparatus in accordance with the second embodiments of the present invention will be described with reference to the attached drawings.

[0060] FIG. **5** shows the case where the first conductive pattern **220** is disposed within the alignment error range. In the pattern alignment error device, a plating solution may be applied to the second conductive pattern. When the first conductive pattern **220** is disposed within the alignment error range, the conductive via **245** is disposed over the insulation pattern **225** of the first conductive pattern **220**, and thus the DC voltage Vd applied to the first conductive pattern **220** does not reach the second conductive pattern **250** through the conductive via **245** due to the insulation pattern **225**.

[0061] Therefore, when the first conductive pattern **220** is disposed within an alignment error range, the second conductive pattern **250** does not receive the DC voltage Vd and consequently a plated layer does not form over the second conductive pattern **250** even when the second conductive pattern **250** comes into contact with a plating solution. When the plating area is not formed, the fact that the first conductive pattern **120** is disposed within the alignment error range is confirmed. Alternatively, it is possible to confirm that the first conductive pattern **220** is disposed within the alignment error range by measuring the voltage of the second conductive pattern **250** rather than applying a plating solution.

[0062] FIG. **6** is a cross-sectional view illustrating that the first conductive pattern shown in FIG. **5** is disposed out of the alignment error range.

[0063] FIG. **6** shows a case where the first conductive pattern **220** is disposed out of the alignment error range. The conductive via **245** is electrically connected to the first conductive pattern **220**. Therefore, the DC voltage Vd applied to the first conductive pattern reaches the second conductive pattern **250** through the conductive via **245**.

[0064] Therefore, when the plating solution is applied to the second conductive pattern and the the first conductive pattern **220** is out of the alignment error range, the second conductive pattern **250** receives DC voltage Vd and thus a plated layer **255** is formed over the second conductive pattern **250**. Alternatively, it is possible to confirm easily that the disposition of the first conductive pattern **220** is out of the alignment error range by measuring the voltage of the second conductive pattern **250** rather than applying the plating solution.

[0065] FIG. **7** is a plan view illustrating an apparatus for detecting pattern alignment error in accordance with a third embodiment of the present invention. FIG. **8** is a cross-sectional view taken along line III-III' in FIG. **7** showing a case where the first conductive layer is formed within the alignment error range. FIG. **9** shows a case where the first conductive layer is formed outside of the alignment error range.

[0066] Referring to FIGS. **7**, **8**, and **9**, the pattern alignment error detecting apparatus **300** includes a first insulation member **310**, a first conductive pattern **320** having an insulation pattern **325**, a second insulation member **330**, a second conductive pattern **350** having a conductive via **345**, and a third conductive pattern **370** having an additional conductive via **365**.

[0067] The first conductive pattern **320** is disposed over the first insulation member **310**. The first insulation member **310** includes insulation material.

[0068] The first conductive pattern **320** includes the insulation pattern **325**. The insulation pattern **325** may be disposed, for example, at a center part of the first conductive pattern **320**. In the present embodiment, the insulation pattern **325** may be a through hole that is formed in a portion of the first conductive pattern **320**. The insulation pattern **325** has a circular shape with a diameter D when view from above. The diameter D of the insulation pattern **325** may be about 50 μm to 200 μm. The diameter D of the insulation pattern **125** may otherwise vary within the alignment error range. Alternatively, the insulation pattern may instead be an insulation layer or a photoresist pattern disposed over the first conductive pattern **320**.

[0069] The second insulation member **330** is disposed over the first insulation member **310** and consequently covers the first conductive pattern **320**. The second insulation member **330** includes insulation material.

[0070] A via hole **332** passes through the second insulation member **330**. In the present embodiment, when the first conductive pattern **320** is formed within the alignment error range, the via hole **332** is formed at a portion corresponding to the insulation pattern **325** of the first conductive pattern **320**. When the first conductive pattern **320** is formed outside of the alignment error range, the via hole **332** will be formed at a portion of the first conductive pattern **320** adjacent to the insulation pattern **325** (as shown in FIG. **9**).

[0071] A conductive via **345** is placed inside the via hole **332** formed in the second insulation member **330**. In the present embodiment, the conductive via **345** may have a cylindrical shape. The conductive via **345** having a cylindrical shape has a diameter D**1** that is smaller than the diameter D of the insulation pattern **325**. In the present embodiment, the area of the insulation pattern **325** may be about 105 to 200% of the area of the conductive via **345**.

[0072] The second conductive pattern **350** is disposed over the second insulation member **330**. In the present embodiment, the conductive via **345** and the second conductive pattern **350** may be formed integrally.

[0073] An examples of material that may be used as the conductive via **345** and the second conductive pattern **350** include aluminum, aluminum alloy, copper, cooper alloy, and metal alloy, etc.

[0074] The second insulation member **330** includes an additional via hole **363** that passes through the second insulation member **330**. In the present embodiment, the additional via hole **363** is disposed at a portion of the first conductive pattern **320** adjacent to the insulation pattern **325**. The additional conductive via **363** is placed inside the additional via hole **363**, and the conductive via **363** contacts the first conductive pattern **320**.

[0075] The third conductive pattern **370** is disposed over the second insulation member **330**. In the present embodiment, the third conductive pattern **370** and the additional conductive via **365** may be formed integrally. The third conductive pattern **370** is electrically connected to a power line **380** that provides a DC voltage Vd to the third conductive pattern **370**.

[0076] Hereinafter, the operation of the pattern alignment error detecting apparatus in accordance with the third embodiments of the present invention will be described with reference to the attached drawings.

[0077] FIG. **8** shows the case where the first conductive pattern **320** is disposed within the alignment error range. A plating solution may be applied to the second conductive pattern **350** and the third conductive pattern **375**. The third conductive pattern **370** is electrically connected to the first conductive pattern **320** by the additional conductive via **365**. However, the conductive via **345** is spaced apart from the first conductive pattern **120**. Therefore, the DC voltage Vd applied to the third conductive pattern **370** by the power line **380**, which in turn flows through the additional conductive via **365** and the first conductive pattern **320**, does not reach the second conductive pattern **350** through the conductive via **345**.

[0078] Therefore, when the first conductive pattern **320** is disposed within the alignment error range, the second conductive pattern **350** does not receive the DC voltage Vd, and consequently a plated layer is not formed over the second conductive pattern **350** even when the second conductive pattern **350** comes into contact with a plating solution. When the plating area is not formed, the fact that the first conductive pattern **120** is disposed within the alignment error range is confirmed. Alternatively, it is possible to confirm that the first conductive pattern **320** is disposed within the alignment error range by measuring the voltage of the second conductive pattern **150**, rather than applying a plating solution. When the plating solution is applied to the second and third conductive patterns **350** and **370**, although a plated layer will not form over the second conductive pattern when the first conductive pattern is disposed within the alignment error range, a plated layer **375** will form over the third conductive pattern **370**.

[0079] FIG. **9** is a cross-sectional view illustrating that the first conductive pattern shown in FIG. **8** is disposed out of the alignment error range.

[0080] FIG. **9** shows a case where the first conductive pattern **320** is disposed out of the alignment error range. In FIG. **9**, the conductive via **345** is electrically connected to the first conductive pattern **320**. Therefore, the DC voltage Vd applied to the third conductive pattern **370** by the power line **380**, which then travels through the additional conductive via **365** and the first conductive pattern, reaches the second conductive pattern **350** through the conductive via **345**.

[0081] Therefore, when the plating solution is applied to the second conductive pattern, and the first conductive pattern **320** is out of the alignment error range, the second conductive pattern **350** received DC voltage Vd and a plated layer **355** is formed over the second conductive pattern **350**. Alternatively, it is possible to confirm easily that the the first conductive pattern **320** is out of the alignment error range by measuring a voltage applied to the second conductive pattern **350** rather than applying the plating solution.

[0082] FIG. **10** is a plan view illustrating an apparatus for detecting pattern alignment error in accordance with a fourth embodiment of the present invention. FIG. **11** is a cross-sectional view taken along line IV-IV' in FIG. **9** showing a case where the first conductive layer is formed within the alignment error range. FIG. **3** shows a case where the first conductive layer is formed outside of the alignment error range.

[0083] Referring to FIGS. **10**, **11**, and **12**, the pattern alignment error detecting apparatus **400** includes a first insulation member **410**, a first conductive pattern **420** having a plurality of insulation patterns **424**, a second insulation member **430**, and a second conductive pattern **450** having a plurality of conductive vias **464**.

[0084] The first conductive pattern **420** is disposed over the first insulation member **410**. The first insulation member **410** includes insulation material. The first conductive pattern **420** is electrically connected, for example, to a power line (not shown) through which a DC power source Vd is applied.

[0085] In the present embodiment, an example of materials that may be used as the first conductive pattern **420** and the power line include aluminum, aluminum alloy, copper, cooper alloy, metal alloy, etc.

[0086] The first conductive pattern **420** includes the insulation patterns **424**. In the present embodiment, the insulation patterns **424** may be, for example, through holes that are formed in the first conductive pattern **420**. The insulation pattern **125** has a circular shape when view from above. For example, the diameter of each insulation pattern **424** may be 50 μm to 200 μm. The diameter of the insulation pattern **424** may otherwise vary within the alignment error range.

[0087] The insulation patterns **424** are disposed along the Y-axis shown in FIG. **10**. In the present embodiment, the number of the insulation patterns **424** is five. Hereinafter, the five insulation patterns are referred to as a first insulation pattern **425**, a second insulation pattern **426**, a third insulation pattern **427**, a fourth insulation pattern **428**, and a fifth insulation pattern **429**.

[0088] In the present embodiment, the first to fifth insulation patterns **425** to **429** each have different sizes. For example, the first insulation pattern **425** has a first size, the second insulation pattern **426** has a second size, the third insulation pattern **427** has a third size, the fourth insulation pattern **428** has a fourth size, and the fifth insulation pattern **429** has a fifth size.

[0089] The second insulation member **430** is disposed over the first insulation member **410** and consequently covers the first conductive pattern **420**. The second insulation member **430** includes insulation material.

[0090] The second insulation member **430** includes a plurality of via holes **435** that each pass through the second insulation member **430**. In the present embodiment, when the first conductive pattern **420** is formed within the alignment error range, the via holes **435** are formed at portions of the second insulation member corresponding to the respective insulation patterns **425** to **429**. When the first conductive pattern **420** is formed outside of the alignment error range, the via holes **435** may be formed at portions of the first conductive pattern **420** adjacent to the insulation patterns **425** to **429**.

[0091] The conductive vias **465**, **466**, **467**, **468** and **469** are placed respectively inside the via holes **435** formed in the second insulation member **430**. In the present embodiment, the conductive vias **465** to **469** may have, for example, a cylindrical shape.

[0092] The conductive vias **465** to **469** having the cylindrical shape have the same diameters. The diameter of the conductive vias **465** to **469** is smaller than the diameter of the insulation patterns **425** to **429**. In the present embodiment, areas of the insulation patterns **425** to **429** may be 105 to 200% of the areas of the conductive vias **465** to **469** respectively.

[0093] The second conductive patterns **451**, **452**, **453**, **454**, **455** are disposed over the second insulation member **430**. In the present embodiment, the conductive patterns **450** are formed integrally with the corresponding conductive via **465** to **469**.

[0094] Hereinafter, the operation of the pattern alignment error detecting apparatus in accordance with the fourth embodiments of the present invention will be described with reference to the attached drawings.

[0095] FIG. **11** shows the case where the first conductive pattern **420** is disposed within an alignment error range. A plating solution may be applied to the second conductive patterns **450**. The conductive vias **145** and the first conductive pattern **420** are spaced apart from each other (i.e. they don't connect) and thus the DC voltage Vd applied to the first conductive pattern **420** does not reach the second conductive patterns **450** through the conductive vias **465** to **469**.

[0096] Therefore, when the first conductive pattern **420** is disposed within the alignment error range, the second conductive pattern **450** does not receive DC voltage Vd and consequently a plated layer is not formed over each second conductive pattern **450** even when the second conductive pattern **450** comes into contact with a plating solution. When the plating area is not formed, the fact that the first conductive pattern **420** is disposed within the alignment error range is confirmed. Alternatively, it is possible to confirm that the first conductive pattern **420** is disposed within the alignment error range by measuring the voltage of each second conductive pattern **450**, rather than applying the plating solution.

[0097] FIG. **12** is a cross-sectional view illustrating that a first conductive pattern shown in FIG. **11** is disposed out of an alignment error range.

[0098] FIG. **12** shows a case where the first conductive pattern **420** is disposed out of the alignment error range. When the first conductive pattern **420** is disposed out of the alignment error range, some of the conductive vias **465** to **469** may be electrically connected to the first conductive pattern **420**. For example, the conductive via **469** corresponding to the fifth insulation pattern **429** has a relatively small area, and thus is electrically connected to the first conductive pattern **420**.

[0099] Therefore, when the plating solution is applied to the second conductive patterns **450**, and the DC voltage Vd applied to the first conductive pattern **420** reaches the second conductive pattern **455** through the conductive via **469**, a plated layer **480** is formed over the second conductive pattern **455**. Alternatively, it is possible to confirm easily that the disposition of the first conductive pattern **420** is out of the alignment error range by measuring a voltage applied to the second conductive patterns **451** to **455** rather than applying the plating solution.

[0100] In a case where the alignment error range of the first conductive pattern **420** is small, the number of the second conductive patterns **451** to **455** on which the plated layer is formed is small. In contrast, in a case that the alignment error range of the first conductive pattern **420** is large, the number of the second conductive patterns **451** to **455** on which the plated layer is formed increases.

[0101] The pattern alignment error detecting apparatus described above can be applied to various devices having multi-layered wiring. For example, the pattern alignment error detecting apparatus may be applied to a printed circuit board having multi-layered wiring, a semiconductor chip having multi-layered wiring, a semiconductor package having multi-layered wiring, etc.

[0102] As is apparent from the above description, there is a major advantage in using the present invention, in that the alignment error of the lower wiring of a multi-layered wiring can be easily recognized.

[0103] Although specific embodiments of the present invention have been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and the spirit of the invention as disclosed in the accompanying claims.

What is claimed is:

1. An apparatus for detecting a pattern alignment error, comprising:

a first conductive pattern disposed over a first insulation member, wherein a power source is applied to the first conductive pattern;

a second insulation member covering the first conductive pattern;

a second conductive pattern disposed on the second insulation layer;

a conductive via electrically connected to the second conductive pattern and passing through the second insulation member; and

an insulation pattern disposed in the first conductive pattern for detecting an alignment error in response to a position of the conductive via.

2. The apparatus for detecting a pattern alignment error according to claim **1**, wherein the insulation pattern is a through hole passing through the first conductive pattern.

3. The apparatus for detecting a pattern alignment error according to claim **1**, wherein the insulation pattern is disposed over the first conductive pattern.

4. The apparatus for detecting a pattern alignment error according to claim **1**, wherein the power source is a DC voltage.

5. The apparatus for detecting a pattern alignment error according to claim **1**, wherein an area of the insulation pattern is 105% to 200% of an area of the conductive via.

6. The apparatus for detecting a pattern alignment error according to claim **5**, wherein the insulation pattern has a circular shape when viewed from above and a diameter of the insulation pattern is 50 μm to 200 μm.

7. The apparatus for detecting a pattern alignment error according to claim **1**, further comprising:

a third conductive pattern disposed over the second insulation member;

an additional conductive via passing through the second insulation member, wherein the additional conductive via is electrically connected to the third conductive pattern and the first conductive pattern;

wherein the power source is electrically connected to the third conductive pattern rather than the first conductive pattern.

8. The apparatus for detecting a pattern alignment error according to claim **7**, wherein a plated layer is formed over the second and third conductive patterns when when the position of the conductive via is such that the conductive via is on the first conductive pattern.

9. The apparatus for detecting a pattern alignment error according to claim **7**, wherein a plating layer is formed over only the third conductive pattern when the position of the conductive via is such that the conductive via is over the insulation pattern.

10. The apparatus for detecting a pattern alignment error according to claim **1**, wherein a number of the second conductive pattern is at least two, and each insulation pattern corresponds to each second conductive pattern, and the insulation patterns have different sizes.

* * * * *