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U1S S2204

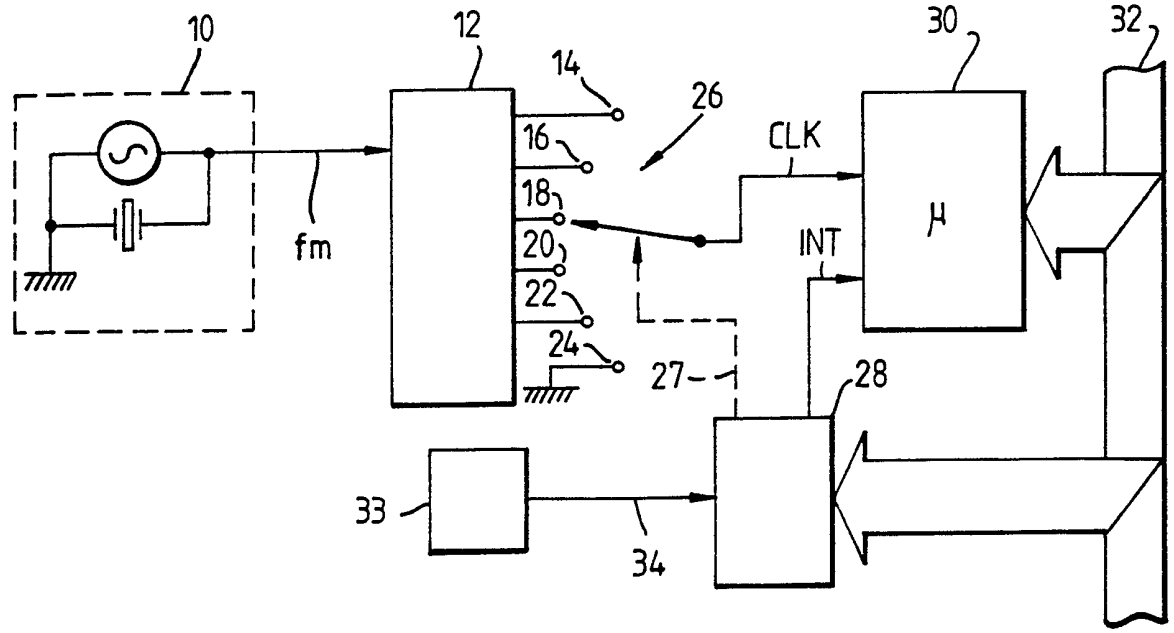
(56) Documents cited
GB 2194082 A **GB 2192295 A** **GB 1450324 A**
GB 1447637 A **EP 0242010 A1** **EP 0229692 A2**
WO 85/02275 A1

(58) Field of search
UK CL (Edition K) **G4A AFT**
INT CL[5] **G06F**

(54) Altering the rate at which digital circuitry operates

(57) The output of a clock (10) is divided (12) to give signal outputs (14, 16, 18, 20, 22) at a number of different frequencies which can be selected one at a time by means of a switch (26). The variable rate signal at the output of the switch (26) is used as the clock input (CLK) for clocked digital circuitry such as a microprocessor (30). Generally the microprocessor (30) alters the clock frequency to be commensurate with its current processing load by means of a decoding and control means (28). However in an interrupt driven system the microprocessor can be switched to its lowest possible rate which may, for example, be a zero clock frequency or a ground signal (24), and upon receipt of an interrupt (34) the decoding and control means (28) increases the processing power of the microprocessor (30) by increasing the rate of the clock signal (CLK) and then passes the interrupt to the microprocessor (30) for processing in the normal manner.

Fig.1.



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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Fig.1.

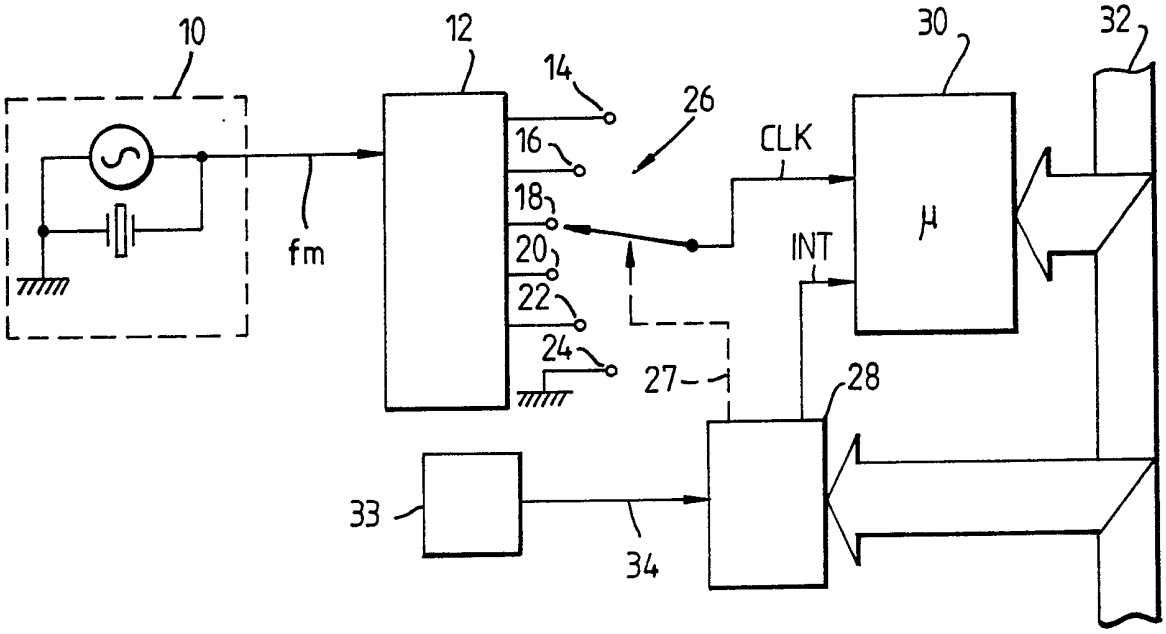
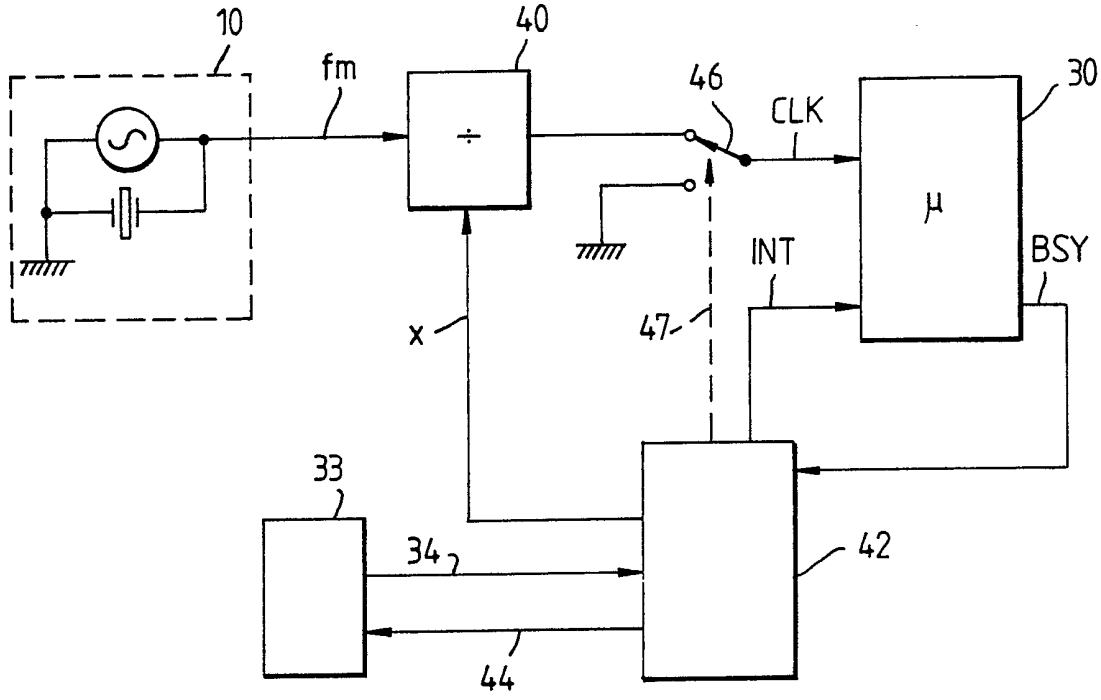

10
12
14
26
30
32
16
CLK
18
fm
μ
20
INT
22
24
27
28
33
34

Fig.2.


10
40
fm
46
CLK
30
÷
μ
INT
BSY
x
47
33
34
42
44

DESCRIPTION

A METHOD OF, AND SYSTEM FOR, ALTERING THE RATE AT WHICH DIGITAL CIRCUITRY OPERATES

The present invention relates to method of, and system for, altering the rate of the clock signal applied to clocked, digital circuitry, having particular, but not exclusive application to a microprocessor circuit operating in a noise sensitive environment.

United Kingdom Patent Application GB 2 212 030 A (PHN 12314) discloses a digital transceiver including both a data processor and a microcontroller constructed as CMOS devices. The data processor is clocked at 1.2 MHz and performs relatively mundane tasks which can be carried out at a relatively low speed and the microcontroller is clocked at 9.6 MHz to perform higher level tasks within the transceiver. The microcontroller is only activated at times when the processing required within the transceiver demands it, with the result that current consumption and r.f. interference which are related to the frequency of operation of the data processing elements are reduced. The transceiver architecture described thus has two constituents that are capable of processing data, the more powerful of which is idle for a considerable proportion of the time that the transceiver is active. Also during periods of very low transceiver activity, even the more modest data processor may be operating at well below its maximum capability although it is possible that it is operating under some form of current saving regime.

It is an aim of the present invention to provide low levels of r.f. interference and low current consumption in a clocked digital logic circuit without the need to divide the data processing operations between two processing elements.

According to a first aspect of the present invention there is provided a variable rate digital data processing system comprising

a clock, digital logic circuitry driven by the clock and a means of varying the frequency of the clock output, wherein said means maintains the frequency of the clock signals supplied to the logic circuitry at a value which is determined by the prevailing processing demand upon the logic circuitry.

By altering the clock rate of the data processing system in this manner the current consumption and rf interference generated may be reduced to values approaching the lowest levels possible for any given processing load, without the provision of extra data processing elements.

According to a second aspect of the present invention there is provided a method of altering the rate at which clocked, digital circuitry operates comprising providing a clock signal to the digital circuitry, monitoring the processing load upon the circuitry and altering the frequency of the clock signal to the lowest rate commensurate with the prevailing processing load.

In one embodiment of the invention, the rate at which a microprocessor is clocked is determined by the microprocessor itself but the alteration of the clock signals has to be performed in a phase continuous manner so as not to crash the processor by introducing spurious signals onto its clock line. Alternatively, some means external to the microprocessor can be provided to determine and alter the clock rate.

The invention will now be explained and described, by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a block schematic diagram of a first embodiment of the present invention, including a clock, a microprocessor and a frequency divider,

Figure 2 is a block schematic diagram of a second embodiment of the present invention, including a clock, a microprocessor and a frequency divider.

In the Figures, corresponding elements have been identified using the same reference numerals.

Figure 1 shows a system for the adjustment of the clock frequency of a microprocessor 30. The output of a master clock oscillator 10, which may comprise a crystal oscillator, is a square wave with a fixed frequency of fm and is fed to an input of a frequency divider 12. The outputs 14,16,18,20 of the frequency divider are each at half of the frequency of the preceding output and the output 22 has a greater division coefficient to provide an especially low output frequency. All five outputs are fed to a single pole, six way switch 26 so that the switch can select any one of these outputs or a ground connection 24. The operation of the switch 26 is controlled by a decoding and control circuit 28 which is itself connected to the microprocessor's address and data buses 32. For example, if fm is set to 8 MHz, the frequency divider outputs 14,16,18,20,22 could provide frequencies of 8 MHz, 4 MHz, 2 MHz, 1 MHz and 126 kHz respectively. The output of the switch 26 is fed to the clock input CLK of the microprocessor 30. The decoding and control circuit 28 also comprises an interrupt input line 34 which is connected to a source of interrupts 33 and an output line which is connected to an interrupt line INT of the microprocessor 30.

In operation the microprocessor 30 regularly executes a simple routine to calculate its current processing load and the minimum clock frequency required to meet that processing load. If an alteration of its clock rate is required a signal will be sent to the decoding and control circuit 28 via the bus 32 which will effect the alteration by means of the switch 26 via a control line 27. If no processing is required the microprocessor is switched to the lowest acceptable frequency which may be zero if the application permits and can be achieved by the selection of the ground connection 24 by the switch 26. In certain applications it is preferred not to turn off the microprocessor completely because it includes a delay between being powered up (or a clock signal being applied) and the start of execution of the software. In an interrupt driven system this delay will usually be unacceptable.

If an interrupt 33 occurs within the equipment it is fed to

the decoding and control circuit 28 on the line 34 which immediately causes the switch 26 to select the highest operating frequency available, in this case the 8 MHz signal on the switch output 14, and passes the interrupt to the microprocessor on the line INT. The microprocessor can then operate in one of two modes. It can service the interrupt at the full speed and then demand a reduction in the clock frequency, or it can determine the lowest permissible clock frequency required to perform the interrupt handling and demand that frequency prior to performing the processing. In either case the microprocessor will not usually be operating at full speed for more than 1ms and in many situations not for more than 200-300μs (remember that at 8 MHz, 200μs corresponds to 1600 clock cycles). In a situation where the microprocessor cooperates with other circuitry which is clocked in synchronism with the microprocessor, the clock signal(s) for this circuitry can usually be derived from the variable frequency signal CLK.

In such a situation, the operating frequencies and the processing loads of this circuitry need to be considered. Additionally, any software timers within the microprocessor will not keep a linear record of elapsed time. If this is likely to cause difficulties an external real time clock which is driven directly from the clock 10 can be provided.

Figure 2 shows another embodiment of the present invention which has two differences from the embodiment shown in Figure 1. The optimum clock rate is no longer calculated by the microprocessor and the clock rate selected on the receipt of a interrupt is no longer necessarily the highest rate available. The output of a clock 10 is a square wave with a frequency of fm which is fed to a counter/divider 40, the output of which counter is fed to a first input of a switch 46. The output of the switch 46 is fed to the clock input CLK of a microprocessor 30. A second input of the switch 46 is connected to ground. The switch 46 is controlled by a calculating and control means 42 via a control line 47. The output of a source of interrupts 33 is fed to the control

means 42 on a line 34. The control means 42 can also interrogate the source of interrupts using a line 44 to determine the urgency of any given interrupt. An output x of the control means 42 controls the division parameter of the counter 40. The control means 42 is also fed from a busy line BSY of the microprocessor and has an interrupt output INT which is fed to the microprocessor 30.

In operation the rate of the output of the counter 40 is determined by the control means 42 using information from the busy line BSY of the microprocessor. The busy line gives an indication of whether the microprocessor is currently active, for example, if the busy line is an active low line and is high for the majority of the time, the microprocessor is under utilised. If the line BSY shows that the microprocessor has been idle for greater than a given proportion of a time interval then the clock rate division parameter x is increased and the clock rate fed to the microprocessor is reduced. Conversely if the microprocessor line BSY shows that it is constantly active or very nearly so then it will decrease x to increase the rate of the clock signal fed to the microprocessor.

The control means 42 contains an integrating means which operates on the output of the line BSY to prevent the clock rate from being altered very frequently causing the throughput of the processor to be degraded. It may also be desirable to include some means of hysteresis in the decision making process to increase or decrease the clock rate CLK so that the clock rate does not fluctuate in response to only small changes in processing demand.

When an interrupt is generated it is fed from the interrupt means 33 to the control means 42 on the line 34. The control means 42 then interrogates the interrupt means 33 on the line 44 to determine the source of the interrupt. The control means 42 then determines how much of an increase in processor speed will be required to deal with the interrupt and makes the necessary adjustments to the division parameter x. This decision could be made using a simple look-up table with an entry for every interrupt type. The interrupt is then fed on the line INT to the

microprocessor 30. Once the interrupt is dealt with, the busy line BSY will indicate that the clock rate is excessive for the current processing demand and the control means 42 will take the necessary steps to reduce it.

Since the frequency of the signals on the clock line CLK in this embodiment is controlled by the control means 42 without direct control from the microprocessor 30, any software timers within the microprocessor, or external timers driven by the clock line CLK, will not maintain a linear record of elapsed time. Again, one solution is the provision of a separate timer or timers driven directly from the clock 10.

Obviously the decision based upon the busy line condition could be used with a clock rate adjustment technique as shown in Figure 1 and vice versa. The embodiment shown in Figure 2 could be adapted to cause the clock rate to be a maximum upon receipt of any interrupt and thus not require the interrogation line 44 or the calculation of the increase in clock rate required.

From reading the present disclosure, other variations will be apparent to persons skilled in the art. Such variations may involve other features which are already known in the design, manufacture and use of clocked digital systems and component parts thereof and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present application also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

CLAIMS

1. A variable rate digital data processing system comprising a clock, digital logic circuitry driven by the clock and a means of varying the frequency of the clock output, wherein said means maintains the frequency of the clock signals supplied to the logic circuitry at a value which is determined by the prevailing processing demand upon the logic circuitry.

2. A system as claimed in Claim 1, wherein the means of varying the frequency of the clock output is a divider having a plurality of outputs at different frequencies connected to a switching means interposed between the clock and the logic circuitry which selects the appropriate divided clock output to be fed to the logic circuitry.

3. A system as claimed in Claim 1, wherein the means of varying the frequency of the clock output is a counter/divider having a variable division parameter.

4. A system as claimed in Claim 1, Claim 2 or Claim 3, wherein said means of varying the frequency of the clock output is governed by the digital logic circuitry and this logic circuitry has means to calculate a clock frequency commensurate with the prevailing processing demand upon the logic circuitry.

5. A system as claimed in Claim 1, Claim 2 or Claim 3, wherein the system further comprises a means of monitoring the activity of the digital logic circuitry, whereby said monitoring means is operable to reduce the frequency of the clock output if the circuitry is active for less than a first predetermined portion of a time period and said monitoring means is operable to increase the frequency of the clock output if the circuitry is active for more than a second predetermined portion of the said time period.

6. A system as claimed in any one of Claims 1 to 5, wherein the means of varying the frequency of the clock output carries out any alterations in the clock output frequency in a phase continuous manner.

7. A system as claimed in any one of Claims 1 to 6, wherein the digital logic circuitry includes a microprocessor.

8. A system as claimed in Claim 5, wherein the digital logic circuitry includes a microprocessor and the means of monitoring the activity of the digital logic circuitry is connected to the busy line of the microprocessor.

9. A data processing system constructed and arranged to operate substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

10. A method of altering the rate at which clocked, digital circuitry operates comprising providing a clock signal to the digital circuitry, monitoring the processing load upon the circuitry and altering the frequency of the clock signal to the lowest rate commensurate with the prevailing processing load.

11. A method as claimed in Claim 10, wherein the clock signal has a lowest permissible rate of zero.

12. A method as claimed in Claim 10 or Claim 11, wherein the frequency of the clock is increased in response to the receipt of an interrupt by the clocked, digital circuitry.

13. A method of altering the rate at which clocked, digital circuitry operates substantially as hereinbefore described with reference to the accompanying drawings.

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