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(54) Title: NON-RECTANGULAR ELECTRONIC DEVICE COMPONENTS

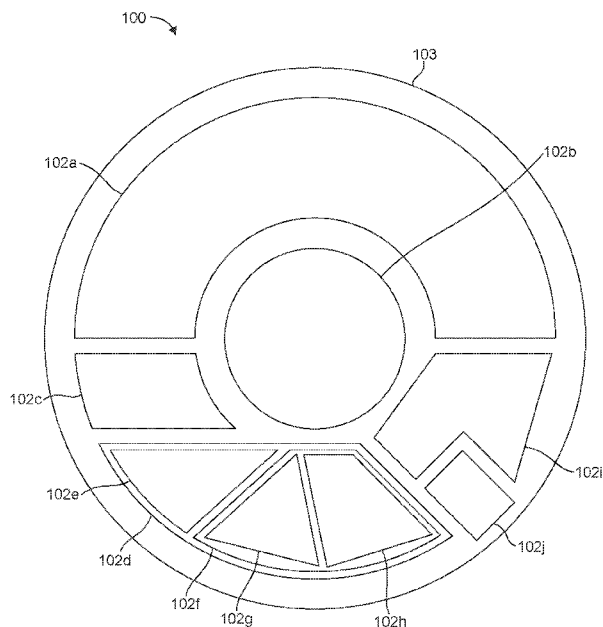


FIG. 1

(57) Abstract: Electronic device shape configuration technology is disclosed. In an example, an electronic device substrate is provided that can comprise a top surface, and a bottom surface opposing the top surface. The top surface and/or the bottom surface can have a non-rectangular shaped perimeter. An electronic device die is also provided that can comprise a top surface, and a bottom surface opposing the top surface. The top surface and/or the bottom surface can have a non-rectangular shaped perimeter. In addition, an electronic device package is provided that can comprise a substrate having a top surface configured to receive a die and a bottom surface opposing the top surface. The package can also include a die having a top surface and a bottom surface opposing the top surface. The die can be coupled to the top surface of the substrate. The top surface and/or the bottom surface of either the substrate, or the die, or both can have a non-rectangular shaped perimeter.



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NON-RECTANGULAR ELECTRONIC DEVICE COMPONENTS

Technical Field

[0001] Embodiments described herein relate generally to electronic devices.

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Background

[0002] As personal computing devices continue to develop, new device form factors are being introduced. For example, wearable computing technology is providing new shapes for users to facilitate use of the devices on or about a human body. In addition, smartphones and tablets may take on non-traditional shapes as these technologies develop.

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Brief Description of the Drawings

[0003] Invention features and advantages will be apparent from the detailed description which follows, taken in conjunction with the accompanying drawings, which together illustrate, by way of example, various invention embodiments; and, wherein:

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[0004] FIG. 1 illustrates a schematic plan view representation of an exemplary electronic device;

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[0005] FIG. 2A illustrates a side view of an item or component of an exemplary electronic device;

[0006] FIG. 2B illustrates a top view of the item or component of an exemplary electronic device;

[0007] FIG. 3 illustrates a top view of an item or component of an exemplary electronic device;

25

[0008] FIGS. 4A-4I illustrate shapes of items or components that can be incorporated into an exemplary electronic devices;

[0009] FIG. 5 illustrates an exemplary electronic device package;

[0010] FIG. 6 illustrates an exemplary electronic device package;

[0011] FIG. 7 illustrates a typical square or rectangular die experiencing warpage due to heat during the mounting or coupling process to a substrate;

[0012] FIG. 8 illustrates an exemplary electronic device die;

5 [0013] FIG. 9A illustrates a non-rectangular shaped exemplary electronic device die;

[0014] FIG. 9B illustrates a typical rectangular shaped electronic device die;

[0015] FIG. 10A illustrates a exemplary configuration for forming units of the non-rectangular shaped electronic device die from a round wafer;

10 [0016] FIG. 10B illustrates an exemplary configuration for forming units of the typical rectangular shaped electronic device die from a round wafer;

[0017] FIG. 11A illustrates an exemplary configuration for forming units of the non-rectangular shaped electronic device die from a round wafer; and

[0018] FIG. 11B illustrates another exemplary configuration for forming units of the typical rectangular shaped electronic device die from a round wafer.

15 [0019] Reference will now be made to the exemplary embodiments illustrated, and specific language will be used herein to describe the same. It will nevertheless be understood that no limitation of the scope or to specific invention embodiments is thereby intended.

20 **Description of Embodiments**

[0020] Before invention embodiments are disclosed and described, it is to be understood that no limitation to the particular structures, process steps, or materials disclosed herein is intended, but also includes equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should
25 also be understood that terminology employed herein is used for the purpose of describing particular examples only and is not intended to be limiting. The same reference numerals in different drawings represent the same element. Numbers provided in flow charts and processes are provided for clarity in illustrating steps and operations and do not necessarily indicate a particular
30 order or sequence. Unless defined otherwise, all technical and scientific terms

used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs.

[0021] As used in this specification and the appended claims, the singular forms “a,” “an” and “the” include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to “a die” includes a plurality of such dies.

[0022] In this application, “comprises,” “comprising,” “containing” and “having” and the like can have the meaning ascribed to them in U.S. Patent law and can mean “includes,” “including,” and the like, and are generally interpreted to be open ended terms. The terms “consisting of” or “consists of” are closed terms, and include only the components, structures, steps, or the like specifically listed in conjunction with such terms, as well as that which is in accordance with U.S. Patent law. “Consisting essentially of” or “consists essentially of” have the meaning generally ascribed to them by U.S. Patent law. In particular, such terms are generally closed terms, with the exception of allowing inclusion of additional items, materials, components, steps, or elements, that do not materially affect the basic and novel characteristics or function of the item(s) used in connection therewith. For example, trace elements present in a composition, but not affecting the composition’s nature or characteristics would be permissible if present under the “consisting essentially of” language, even though not expressly recited in a list of items following such terminology. When using an open ended term, like “comprising” or “including,” in this specification it is understood that direct support should be afforded also to “consisting essentially of” language as well as “consisting of” language as if stated explicitly and vice versa.

[0023] The terms “first,” “second,” “third,” “fourth,” and the like in the description and in the claims, if any, are used for distinguishing between similar elements and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments described herein are, for example, capable of operation in sequences other than those illustrated or

otherwise described herein. Similarly, if a method is described herein as comprising a series of steps, the order of such steps as presented herein is not necessarily the only order in which such steps may be performed, and certain of the stated steps may possibly be omitted and/or certain other steps not
5 described herein may possibly be added to the method.

[0024] The terms “left,” “right,” “front,” “back,” “top,” “bottom,” “over,” “under,” and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is to be understood that the terms so used are interchangeable under appropriate
10 circumstances such that the embodiments described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein. The term “coupled,” as used herein, is defined as directly or indirectly connected in an electrical or nonelectrical manner. Objects described herein as being “adjacent to” each other may be in physical contact with each
15 other, in close proximity to each other, or in the same general region or area as each other, as appropriate for the context in which the phrase is used. Occurrences of the phrase “in one embodiment,” or “in one aspect,” herein do not necessarily all refer to the same embodiment or aspect.

[0025] As used herein, the term “substantially” refers to the complete or nearly
20 complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is “substantially” enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally
25 speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of “substantially” is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is “substantially
30 free of” particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is “substantially free of” an

ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

[0026] As used herein, the term “about” is used to provide flexibility to a numerical range endpoint by providing that a given value may be “a little above”
5 or “a little below” the endpoint.

[0027] As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual
10 member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

[0028] Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range
15 format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of “about 1 to
20 about 5” should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

[0029] This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

[0030] Reference throughout this specification to “an example” means that a particular feature, structure, or characteristic described in connection with the
30 example is included in at least one embodiment. Thus, appearances of the

phrases “in an example” in various places throughout this specification are not necessarily all referring to the same embodiment.

Example Embodiments

5 **[0031]** An initial overview of technology embodiments is provided below and specific technology embodiments are then described in further detail. This initial summary is intended to aid readers in understanding the technology more quickly but is not intended to identify key or essential features of the technology nor is it intended to limit the scope of the claimed subject matter.

10 **[0032]** While the external form factors of many electronic devices have changed to accommodate new uses or to better meet user needs, the form factors or shapes of the internal electronic components of these devices has remained substantially the same rectangular or square shape or form factor. Fitting rectangular shaped electronic components within a non-rectangular device form
15 factor on a non-rectangular motherboard can be challenging and can result in inefficient use of the available space.

[0033] Certain invention embodiments provide electronic components that can facilitate better use of the space available associated with a non-rectangular electronic device form factor. In one aspect, an electronic device substrate is
20 provided that can comprise a top surface, and a bottom surface opposing the top surface. The top surface and/or the bottom surface can have a non-rectangular shaped perimeter. An electronic device die is also provided that can comprise a top surface, and a bottom surface opposing the top surface. The top surface and/or the bottom surface can have a non-rectangular shaped
25 perimeter. In addition, an electronic device package is provided that can comprise a substrate having a top surface configured to receive a die and a bottom surface opposing the top surface. The package can also include a die having a top surface and a bottom surface opposing the top surface. The die can be coupled to the top surface of the substrate. The top surface and/or the
30 bottom surface of either the substrate, or the die, or both can have a non-rectangular shaped perimeter. In addition to facilitating an effective use of

space, the principles of the present disclosure can also provide other advantages, such as improved I/O routing, improved reliability, and lower warpage during mounting of electronic components, which are described in more detail hereinafter.

5 **[0034]** Referring to FIG. 1, an exemplary electronic device 100 is illustrated. The electronic device 100 can include one or more generic items 102a-j. The items 102a-j can be directly or indirectly coupled to a motherboard 103 or other suitable substrate. The items 102a-j can represent any suitable device or component that can be included in an electronic device or operably coupled to
10 the motherboard 103. Such items include without limitation a processor, a memory device, a die (which can include one or more processors and/or memory devices), an electronic device package (which can include one or more dies), a radio, a heat sink, a port, a slot, an input/output (I/O), a connector, a socket, an LED, a capacitor, a resistor, a substrate (e.g., for a package or an
15 embedded multi-die interconnect bridge (EMIB)), etc. An electronic device package can be a system in a package (SiP), a package on package (PoP), and/or any other suitable package configuration. The electronic device 100 can comprise any type of electronic device, such as a computing system (e.g., a desktop computer, a laptop computer, a tablet computer, a smartphone, a
20 smartwatch, a server, etc.).

[0035] The motherboard 103 can have any suitable shape or configuration, such as a rectangular or non-rectangular shape. As illustrated in FIG.1 the motherboard 103 has a non-rectangular perimeter shape. In this case, the perimeter shape of the motherboard 103 is a circular shape, although the
25 motherboard can have any suitable non-rectangular shape, such as a semi-circular shape, an elliptical shape, a polygonal shape (e.g., a triangular shape, a quadrilateral shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, etc.), a curvilinear shape, and/or a free form shape.

[0036] Similarly, the items 102a-j can have rectangular or non-rectangular shaped perimeters of any suitable shape, such as a circular shape (e.g., item 102b), a semi-circular shape (e.g., items 102a, 102c-f), an elliptical shape, a polygonal shape (e.g., items 102g-j), a curvilinear shape (e.g., items 102a, 102c-f), and/or a free form shape. A polygonal shape can be a triangular shape, a quadrilateral shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, etc. The combination of perimeter shapes of the items 102a-j can be selected to maximize the number of items coupleable to the motherboard 103. For example, based on the size and shape of the motherboard 103, which may be rectangular or non-rectangular, the size and shape configurations of the items 102a-j can be selected to maximize the density of the items on the motherboard 103. In one aspect, the perimeter shapes of two or more of the items 102a-j can be complementary such that the shapes combine to form a shape that maximizes the density of the items on the motherboard 103 or on another item or component, as the case may be.

[0037] Generally, the motherboard 103 and the items 102a-j can be any suitable shape, and any combination of motherboard 103 and item 102a-j shapes can be used in order to arrive at a device with specific properties, such as size and overall operation. For example, any suitable item shape (e.g., a package) can be selected for a given form factor shape of the electronic device and/or the motherboard to make efficient use of the available area. The ability to select or customize the shapes of the items in an electronic device or on a motherboard can provide flexibility in meeting the space constraints of the available area. In addition, because the items or components of an electronic device can be more efficiently packaged or arranged, the form factor of the electronic device can be made smaller, which can reduce costs and provide new or better uses for the device.

[0038] Because FIG. 1 illustrates a schematic plan view representation of the electronic device 100, perimeter shapes of top and bottom surfaces of the motherboard 103 and the items 102a-j are not distinguished. Rather, the outer perimeter or boundary shapes of the motherboard 103 and the items 102a-j are

represented in this figure. It should be recognized that top and bottom surfaces of the motherboard 103 and the items 102a-j may have perimeters that match in shape and/or size, or differ in shape and/or size. For example, FIGS. 2A and 2B illustrate an item 202 or component of an electronic device, such as a
5 processor, a memory device, a die, an electronic device package, a radio, a heat sink, a port, a slot, an input/output (I/O), a connector, a socket, an LED, a capacitor, a resistor, a substrate (e.g., of a motherboard or a package), etc. The item 202 can have a top surface 204 and a bottom surface 205 opposing the top surface. The top and bottom surfaces 204, 205 can differ in size (e.g.,
10 perimeter dimension or area), as illustrated, or the top and bottom surfaces can be the same size. In this example, the top and bottom surfaces 204, 205 are similar in shape (i.e., circular). However, as shown in FIG. 3, an item 302 or component can have top and bottom surfaces 304, 305 that have different shapes (e.g., a circular top surface 304 and an elliptical bottom surface 305 as
15 illustrated, hexagonal and octagonal, etc.). The top and bottom surfaces 304, 305 can be the same size or different in size, as desired.

[0039] FIGS. 4A-4I illustrate several examples of possible shapes of items or components that can be incorporated into an electronic device as disclosed herein. For example, FIG. 4A illustrates an elliptical shape, FIG. 4B illustrates a
20 circular shape, FIGS. 4C and 4D illustrate semi-circular shapes, FIG. 4E illustrates a triangular shape, FIG. 4F illustrates a quadrilateral shape, FIG. 4G illustrates a hexagonal shape, FIG. 4H illustrates a curvilinear shape, and FIG. 4I illustrates a free form shape. The shapes shown in these figures are merely examples and are not meant to be limiting in any way, as any suitable shape or
25 configuration can be utilized.

[0040] FIG. 5 illustrates an electronic device package 401 in accordance with an example of the present disclosure. The electronic device package 401 can include a substrate 410 and a die 420. The substrate 410 can have a top surface 411 configured to receive the die 420 and the die 420 can be coupled to the top surface 411 of the substrate 410. Thus, the substrate 410 can have electronic circuitry (obscured from view by the die 420), which may be associated with the top surface 411, to electrically couple with the die 420. As discussed above and illustrated in FIGS. 2A-3, the substrate 410 and the die 420 can have rectangular or non-rectangular perimeter shapes, which can be defined by top and/or bottom surfaces of the substrate 410 and the die 420. As shown in FIG. 5, the substrate 410 and the die 420 can have non-rectangular shaped perimeters. In this case, the substrate 410 and the die 420 have matching non-rectangular shapes (e.g., a hexagonal shape). It should be recognized that either the substrate 410, the die 420, or both can have a non-rectangular shaped perimeter. It should also be recognized, as discussed above, that the perimeter shapes of either the substrate 410, the die 420, or both can comprise a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, and/or a free form shape.

[0041] The shape of the package 401, which can be defined by the substrate 410 and/or the die 420, can be configured to maximize the number of packages coupled to a substrate (e.g., a motherboard) or other component to which the package 410 may be coupled, such as another package. The shape of the electronic device package 410 can therefore be selected based on a shape of a substrate or other component to which the package 410 may be coupled. In addition, the shape of the package 410 can be based on the shapes of other components or items which may be coupled to the same substrate or component in order to arrive at a device with specific properties, such as size and overall operation.

[0042] FIG. 6 illustrates an electronic device package 501 in accordance with another example of the present disclosure. The electronic device package 501 can include a substrate 510 and multiple dies 520a-f, which are illustrated with non-rectangular shaped perimeters. The substrate 510 can have a different
5 shape than the dies 520a-f. In this case, the substrate 510 has a hexagonal shape and the dies 520a-f have triangular shapes. The geometry is such that six triangular dies 520a-f can fit on the hexagonal substrate 510. The shape of the package 501, which can be defined by the substrate 510 and/or the dies 520a-f, can be configured to maximize the number of packages coupled to a
10 substrate (e.g., a motherboard) or other component to which the package 501 may be coupled, such as another package. Thus, in one aspect, the shape of the substrate 510 can be configured to maximize the number of packages coupled to a substrate or other component. In another aspect, the shape of each of the dies 520a-f can be configured to maximize the number of dies
15 coupled to the substrate 510. As shown in FIG. 6, the shapes of the dies 520a-f can be complementary to fit on the substrate 510. In this case, the shapes of the dies 520a-f match one another. It should be recognized, however, that the shapes of the dies can be different, as discussed above with respect to FIG. 1.

[0043] In one aspect, the principles disclosed herein provide for PoP
20 arrangements. In the example illustrated in FIG. 6, for instance, the substrate 510 and the dies 520a-f can represent packages. Thus, multiple packages (triangular shaped in this case) can be mounted on or coupled to a common package (hexagonal shaped in this case) as part of an overall computing device. In general, one or more packages having a non-rectangular perimeter
25 shape can be mounted on another package also having a rectangular or a non-rectangular perimeter shape. Any combination of shapes (e.g., rectangular or non-rectangular) can be used in this regard in order to arrive at a device with specific properties, such as size and overall operation.

[0044] In one aspect, a die or an electronic device package can be configured to
30 provide lower corner solder joint stresses compared to a rectangular die or package of the same area. As illustrated in FIG. 7, a typical square or rectangular die is highly susceptible to warpage due to temperature variations.

For such square or rectangular shaped dies, solder joint failures (e.g., non-contact electrical opens or electrical disconnects) often occur in the corner regions (indicated at 630, 631) of the die during the mounting process (i.e., surface mounting process) or when subjected to shock, vibration, transient bending, or other loading conditions. These failures are due to the distance 632 from the center of the die (e.g., increased warpage) and the presence of fewer solder joints located at that distance that can provide structural support for the die. The area of these failures therefore is typically along a periphery of a die. In order to maximize surface mount (SMT) yield and effectively minimize warpage and solder joint failure or areas of lost electrical contact (i.e. electrical opens), the number of corners of a die can be increased or corners on the shape of a die can be eliminated altogether. This can reduce the distance from the center of a die to a corner or edge of the die (e.g., reduced warpage), which can provide an increased number of solder joints at corner or edge regions to distribute or share the load. Thus, for example, a hexagonal or circular shaped die can provide lower solder joint stresses at a corner or edge compared to a rectangular die of the same area, which can improve production yields (e.g., fewer failures during surface mounting processes) as well as provide increased resistance to failure under a variety of loading conditions. In one aspect, the perimeter of a die can have a shape that maximizes perimeter length for a given area. This increased perimeter length can also provide benefits for routing of traces or other electrical contacts by providing more space or options for connections.

[0045] In some cases, the overall perimeter shape of a die may be constrained by shape considerations as disclosed herein, such as to fit on a given substrate alone or with other components. In this case, corners of the die can be reduced or eliminated by rounding or chamfering in order to reduce the distance from the center of the die to the corner or an edge of the die. An example of this is illustrated in FIG. 8, where corners 733a-c of a triangular shaped die 720 are rounded. Rounding of the corners of the die 720 can reduce stress concentrations and prevent corner chipping or cracking during the assembly process. In one aspect, by eliminating the "point" of the corners 733a-c,

distances 732a-c from a center of the die 720 to the corner 733a-c, respectively, can be reduced, thereby improving solder joint reliability and performance under shock, vibration, and transient bending loading conditions, as discussed above. It should be recognized that these principles also apply to substrates and packages or any other component coupled to another component via a solder coupling.

[0046] In one aspect, invention embodiments can maximize use of a round wafer in producing dies. Once one or more non-rectangular perimeter shapes and sizes for a die have been selected as described above, a maximum number of the die units can be identified that will fit on a surface of the round wafer. This can involve orienting units of the selected shape(s) and size(s) in relation to the wafer surface. The dies can then be formed from the wafer. Similarly, in the case of substrates, which are typically made from rectangular panels, once one or more non-rectangular perimeter shapes and sizes for a substrate have been selected as described above, the maximum number of the substrate units can be identified that will fit on a surface of the rectangular panel. This can involve orienting units of the selected shape(s) and size(s) in relation to the panel surface. The substrates can then be formed from the panel.

[0047] These principles are illustrated in FIGS. 9A-11B in which a non-rectangular shaped die is compared to a typical rectangular shaped die. For example, FIG. 9A illustrates a non-rectangular shaped die 820 in the form of a triangle and FIG. 9B illustrates a rectangular shaped die 920 in the form of a square. The triangle shaped die 820 and the square shaped die 920 have the same area. FIGS. 10A and 10B show six of the triangle shaped dies 820 of the same shape and size, and four of the square shaped dies 920 of the same shape and size per wafer 840, 940, respectively. FIGS. 11A and 11B show 42 of the triangle shaped dies 820 and 37 of the square shaped dies 920 per wafer 840', 940', respectively. Thus, certain non-rectangular shaped geometries can be utilized to improve the yield of dies from a single wafer over traditional die shapes for a given die area. In one aspect, different sized and/or shaped dies can be combined to utilize even more of the wafer 840. Groups of six triangles as shown in FIGS. 10A and 11A can represent a hexagon shaped die as an

illustration of how hexagon shaped dies may fit on a wafer. As mentioned above, non-rectangular geometries such as triangles and hexagons with large perimeters for a given area can be utilized as bridge stitching elements in EMIB or other die embedding technologies where a small area is utilized and a high I/O count is desired.

Examples

[0048] The following examples pertain to further embodiments.

[0049] In one example there is provided, an electronic device substrate comprising a top surface, and a bottom surface opposing the top surface, wherein at least one of the top surface and the bottom surface has a non-rectangular shaped perimeter.

[0050] In one example of an electronic device, the electronic device substrate can further comprise electronic circuitry.

[0051] In one example of an electronic device, the non-rectangular perimeter comprises a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

[0052] In one example of an electronic device, the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

[0053] In one example of an electronic device, the polygonal shape is a triangular shape.

[0054] In one example of an electronic device, the shape minimizes areas of lost electrical contact with a motherboard to which the substrate is coupled due to thermally induced warping of the substrate.

[0055] In one example of an electronic device, the area of lost electrical contact is along a periphery of the substrate.

[0056] In one example of an electronic device, the shape of the substrate is selected in order to maximize a number of substrates harvested from a single wafer or panel.

[0057] In one example of an electronic device, the perimeters of the top and bottom surfaces match in shape and size.

[0058] In one example of an electronic device, the perimeters of the top and bottom surfaces differ in shape or size.

5 **[0059]** In one example of an electronic device, the perimeter has a shape that maximizes perimeter length for a given area.

[0060] In one example of an electronic device, the shape is a polygon.

[0061] In one example of an electronic device, the shape is an ellipse.

[0062] In one example of an electronic device, the shape is a circle.

10 **[0063]** In one example there is provided, an electronic device die comprising a top surface, and a bottom surface opposing the top surface, wherein at least one of the top surface and the bottom surface has a non-rectangular shaped perimeter.

[0064] In one example of an electronic device die, the non-rectangular perimeter
15 comprises a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

[0065] In one example of an electronic device die, the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an
20 octagonal shape, or a combination thereof.

[0066] In one example of an electronic device die, the polygonal shape is a triangular shape.

[0067] In one example of an electronic device die, the shape minimizes areas of lost electrical contact with a package substrate or motherboard to which the die is
25 coupled due to thermally induced warping of the die.

[0068] In one example of an electronic device die, the area of lost electrical contact is along a periphery of the die.

[0069] In one example of an electronic device die, the shape of the die is selected in order to maximize a number of dies harvested from a single wafer.

[0070] In one example of an electronic device die, the perimeters of the top and bottom surfaces match in shape and size.

[0071] In one example of an electronic device die, the perimeters of the top and bottom surfaces differ in shape or size.

5 **[0072]** In one example of an electronic device die, the perimeter has a shape that maximizes perimeter length for a given area.

[0073] In one example of an electronic device die, the shape is a polygon.

[0074] In one example of an electronic device die, the shape is an ellipse.

[0075] In one example of an electronic device die, the shape is a circle.

10 **[0076]** In one example, there is provided, an electronic device package comprising a substrate having a top surface configured to receive a die and a bottom surface opposing the top surface, a die having a top surface and a bottom surface opposing the top surface, said die coupled to the top surface of the substrate, wherein at least one of the top surface and the bottom surface of
15 either the substrate, or the die, or both has a non-rectangular shaped perimeter.

[0077] In one example of an electronic device package, the substrate further comprises electronic circuitry.

[0078] In one example of an electronic device package, the non-rectangular perimeter of either the substrate, the die, or both comprises a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form
20 shape, or a combination thereof.

[0079] In one example of an electronic device package, the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

25 **[0080]** In one example of an electronic device package, the polygonal shape is a triangular shape.

[0081] In one example of an electronic device package, the shape minimizes areas of lost electrical contact between the die and the substrate, or between the substrate and a motherboard to which the substrate is coupled due to thermally
30 induced warping of the die or the substrate.

[0082] In one example of an electronic device package, the area of lost electrical contact is along a periphery of the die or the substrate.

[0083] In one example of an electronic device package, the shape of the die or the substrate is selected in order to maximize a number of dies or substrates harvested
5 from a single wafer or panel.

[0084] In one example of an electronic device package, the perimeters of the top and bottom surfaces of the substrate or of the die match in shape and size.

[0085] In one example of an electronic device package, the perimeters of the top and bottom surfaces of the substrate or of the die differ in shape or size.

10 **[0086]** In one example of an electronic device package, the substrate and die have substantially matching perimeter shapes.

[0087] In one example of an electronic device package, the substrate and die have different perimeter shapes.

15 **[0088]** In one example of an electronic device package, the die comprises a plurality of dies.

[0089] In one example of an electronic device package, the non-rectangular perimeter of each die has a shape configured to maximize the number of dies coupled to the substrate or to a motherboard.

20 **[0090]** In one example of an electronic device package, the shapes of the dies are complementary.

[0091] In one example of an electronic device package, the shapes of the dies substantially match.

[0092] In one example of an electronic device package, the shapes of the dies are different.

25 **[0093]** In one example of an electronic device package, the perimeter of the substrate, or the die, or both is a shape that maximizes perimeter length for a given area.

[0094] In one example of an electronic device package, the shape is a polygon.

[0095] In one example of an electronic device package, the shape is an ellipse.

[0096] In one example of an electronic device package, the shape is a circle.

[0097] In one there is provided, an electronic device comprising an electronic device package as disclosed herein coupled to a motherboard.

[0098] In one example of an electronic device, the motherboard has a non-
5 rectangular perimeter shape.

[0099] In one example of an electronic device, the non-rectangular perimeter of the motherboard comprises a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

[00100] In one example of an electronic device, the polygonal shape of the
10 motherboard comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

[00101] In one example of an electronic device, the electronic device package comprises a plurality of electronic device packages.

[00102] In one example of an electronic device, the non-rectangular perimeter of
15 the substrate of each electronic device package has a shape configured to maximize the number of electronic device packages coupleable to the motherboard.

[00103] In one example of an electronic device, the perimeter shapes of the substrates are complementary.

[00104] In one example of an electronic device, the perimeters of the top and
20 bottom surfaces match in shape and size.

[00105] In one example of an electronic device, the perimeters of the top and bottom surfaces differ in shape or size.

[00106] In one example of an electronic device, the electronic device can further
25 comprise a processor, a memory, an input/output (I/O), a connector, a socket, or a combination thereof.

[00107] In one example of an electronic device, the electronic device comprises a desktop computer, a laptop computer, a tablet computer, a smartphone, a smartwatch, a server, or a combination thereof.

[00108] In one example there is provided, a method of maximizing use of a
30 rectangular panel or a round wafer in producing electronic device substrates or

dies comprising selecting at least one non-rectangular perimeter shape and size for the substrates or dies that is sufficient for use in an electronic device package into which the substrate or die is to be incorporated, identifying a maximum number of the substrate units that fit on a surface of the rectangular panel or a maximum number of the die units that fit on a surface of the round wafer, and forming the substrates from the panel or the dies from the wafer.

[00109] In one example of a method for maximizing use of a wafer, the non-rectangular perimeter shape comprises a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

[00110] In one example of a method for maximizing use of a wafer, the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

[00111] In one example of a method for maximizing use of a wafer, the polygonal shape is a triangle.

[00112] In one example of a method for maximizing use of a wafer, the substrate or die units have a substantially same shape or size, or both shape and size.

[00113] In one example of a method for maximizing use of a wafer, the substrate or die units have substantially different shapes, or sizes, or both shapes and sizes.

[00114] In one example of a method for maximizing use of a wafer, identifying a maximum number of substrate units that fit on a surface of the rectangular panel or a maximum number of die units that fit on a surface of the round wafer comprises orienting units of the selected shape(s) and size(s) in relation to the panel or wafer surface.

[00115] In one example of a method for maximizing use of a wafer, at least one substrate unit is suitable for use as an embedded multi-die interconnect bridge (EMIB).

[00116] In one example there is provided, a method of making an electronic device package can comprise providing a die, providing a substrate, and coupling the die to the substrate, wherein either the die, the substrate, or both have a non-rectangular shaped perimeter.

[00117] In one example of a method of making an electronic device package, the method of claim 68, wherein the non-rectangular shaped perimeter comprises a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

[00118] In one example of a method of making an electronic device package, the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

[00119] In one example of a method of making an electronic device package, the polygonal shape is a triangle.

[00120] In one example of a method of making an electronic device package, the die has a non-rectangular perimeter shape.

[00121] In one example of a method of making an electronic device package, the substrate has a non-rectangular perimeter shape.

[00122] In one example of a method of making an electronic device package, both the die and the substrate have a non-rectangular perimeter shape.

[00123] In one example of a method of making an electronic device package, the die comprises a plurality of dies and the non-rectangular shaped perimeter of each die is configured to maximize the number of dies coupled to the substrate.

[00124] In one example there is provided, a method of maximizing a number of electronic device packages on a motherboard comprising selecting a size and shape for the motherboard, selecting electronic device package configurations with non-rectangular shaped perimeters having complementary shapes that combine to form a shape that maximizes a density of the electronic device packages on the motherboard, and mounting the electronic device packages on the motherboard.

[00125] In one example of a method of making an electronic device package, the non-rectangular perimeter of the electronic device package configurations can comprise a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

[00126] In one example of a method of making an electronic device package, the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

[00127] In one example of a method of making an electronic device package,
5 the motherboard has a rectangular perimeter shape.

[00128] In one example of a method of making an electronic device package, the motherboard has a non-rectangular perimeter shape.

[00129] Circuitry used in electronic components or devices (e.g. a die) of an electronic device package can include hardware, firmware, program code, executable
10 code, computer instructions, and/or software. Electronic components and devices can include a non-transitory computer readable storage medium which can be a computer readable storage medium that does not include signal. In the case of program code execution on programmable computers, the computing devices recited herein may include a processor, a storage medium readable by the processor (including volatile
15 and non-volatile memory and/or storage elements), at least one input device, and at least one output device. Volatile and non-volatile memory and/or storage elements may be a RAM, EPROM, flash drive, optical drive, magnetic hard drive, solid state drive, or other medium for storing electronic data. Node and wireless devices may also include a transceiver module, a counter module, a processing module, and/or a clock module
20 or timer module. One or more programs that may implement or utilize any techniques described herein may use an application programming interface (API), reusable controls, and the like. Such programs may be implemented in a high level procedural or object oriented programming language to communicate with a computer system. However, the program(s) may be implemented in assembly or machine language, if
25 desired. In any case, the language may be a compiled or interpreted language, and combined with hardware implementations.

[00130] While the forgoing examples are illustrative of the specific embodiments in one or more particular applications, it will be apparent to those of ordinary skill in the art that numerous modifications in form, usage and details of implementation can be made
30 without departing from the principles and concepts articulated herein.

Claims

What is claimed is:

1. An electronic device substrate, comprising:
5 a top surface; and
a bottom surface opposing the top surface, wherein at least one of the
top surface and the bottom surface has a non-rectangular shaped
perimeter.
- 10 2. The electronic device substrate of claim 1, further comprising electronic
circuitry.
3. The electronic device substrate of claim 1, wherein the non-rectangular
perimeter comprises a circular shape, a semi-circular shape, an elliptical shape,
15 a polygonal shape, a curvilinear shape, a free form shape, or a combination
thereof.
4. The electronic device substrate of claim 3, wherein the polygonal shape
comprises a triangular shape, a pentagonal shape, a hexagonal shape, a
20 heptagonal shape, an octagonal shape, or a combination thereof.
5. The electronic device substrate of claim 4, wherein the polygonal shape
is a triangular shape.
- 25 6. The electronic device substrate of claim 1, wherein the shape minimizes
areas of lost electrical contact with a motherboard to which the substrate is
coupled due to thermally induced warping of the substrate.
7. The electronic device substrate of claim 6, wherein the area of lost
30 electrical contact is along a periphery of the substrate.

8. The electronic device substrate of claim 1, wherein the shape of the substrate is selected in order to maximize a number of substrates harvested from a single wafer or panel.
- 5 9. The electronic device substrate of claim 1, wherein the perimeters of the top and bottom surfaces match in shape and size.
10. The electronic device substrate of claim 1, wherein the perimeters of the top and bottom surfaces differ in shape or size.
- 10 11. The electronic device substrate of claim 1, wherein the perimeter has a shape that maximizes perimeter length for a given area.
12. The electronic device substrate of claim 11, wherein the shape is a
15 polygon.
13. The electronic device substrate of claim 11, wherein the shape is an ellipse.
- 20 14. The electronic device substrate of claim 13, wherein the shape is a circle.
15. An electronic device die, comprising:
a top surface; and
a bottom surface opposing the top surface, wherein at least one of the
25 top surface and the bottom surface has a non-rectangular shaped perimeter.
16. The electronic device die of claim 15, wherein the non-rectangular perimeter comprises a circular shape, a semi-circular shape, an elliptical shape,
30 a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

17. The electronic device die of claim 16, wherein the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

5 18. The electronic device die of claim 17, wherein the polygonal shape is a triangular shape.

19. The electronic device die of claim 15, wherein the shape minimizes areas of lost electrical contact with a package substrate or motherboard to which the
10 die is coupled due to thermally induced warping of the die.

20. The electronic device die of claim 19, wherein the area of lost electrical contact is along a periphery of the die.

15 21. The electronic device die of claim 15, wherein the shape of the die is selected in order to maximize a number of dies harvested from a single wafer.

22. The electronic device die of claim 15, wherein the perimeters of the top and bottom surfaces match in shape and size.

20

23. The electronic device die of claim 15, wherein the perimeters of the top and bottom surfaces differ in shape or size.

24. The electronic device die of claim 15, wherein the perimeter has a shape
25 that maximizes perimeter length for a given area.

25. The electronic device die of claim 24, wherein the shape is a polygon.

26. The electronic device die of claim 25, wherein the shape is an ellipse.
30

27. The electronic device die of claim 26, wherein the shape is a circle.

28. An electronic device package, comprising:
a substrate having a top surface configured to receive a die and a bottom
surface opposing the top surface;
a die having a top surface and a bottom surface opposing the top
5 surface, said die coupled to the top surface of the substrate;
wherein at least one of the top surface and the bottom surface of either
the substrate, or the die, or both has a non-rectangular shaped
perimeter.
- 10 29. The electronic device package of claim 28, wherein the substrate further
comprises electronic circuitry.
30. The electronic device package of claim 28, wherein the non-rectangular
perimeter of either the substrate, the die, or both comprises a circular shape, a
15 semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape,
a free form shape, or a combination thereof.
31. The electronic device package of claim 30, wherein the polygonal shape
comprises a triangular shape, a pentagonal shape, a hexagonal shape, a
20 heptagonal shape, an octagonal shape, or a combination thereof.
32. The electronic device package of claim 31, wherein the polygonal shape
is a triangular shape.
- 25 33. The electronic device package of claim 28, wherein the shape minimizes
areas of lost electrical contact between the die and the substrate, or between
the substrate and a motherboard to which the substrate is coupled due to
thermally induced warping of the die or the substrate.
- 30 34. The electronic device package of claim 33, wherein the area of lost
electrical contact is along a periphery of the die or the substrate.

35. The electronic device package of claim 28, wherein the shape of the die or the substrate is selected in order to maximize a number of dies or substrates harvested from a single wafer or panel.

5 36. The electronic device package of claim 28, wherein the perimeters of the top and bottom surfaces of the substrate or of the die match in shape and size.

37. The electronic device package of claim 28, wherein the perimeters of the top and bottom surfaces of the substrate or of the die differ in shape or size.

10

38. The electronic device package of claim 28, wherein the substrate and die have substantially matching perimeter shapes.

15 39. The electronic device package of claim 28, wherein the substrate and die have different perimeter shapes.

40. The electronic device package of claim 28, wherein the die comprises a plurality of dies.

20 41. The electronic device package of claim 40, wherein the non-rectangular perimeter of each die has a shape configured to maximize the number of dies coupled to the substrate or to a motherboard.

25 42. The electronic device package of claim 41, wherein the shapes of the dies are complementary.

43. The electronic device package of claim 41, wherein the shapes of the dies substantially match.

30 44. The electronic device package of claim 41, wherein the shapes of the dies are different.

45. The electronic device die of claim 28, wherein the perimeter of the substrate, or the die, or both is a shape that maximizes perimeter length for a given area.

5 46. The electronic device package of claim 45, wherein the shape is a polygon.

47. The electronic device package of claim 45, wherein the shape is an ellipse.

10

48. The electronic device package of claim 47, wherein the shape is a circle.

49. An electronic device, comprising:
an electronic device package as recited in any of claims 28-48 coupled to a
15 motherboard.

50. The electronic device of claim 49, wherein the motherboard has a non-rectangular perimeter shape.

20 51. The electronic device of claim 50, wherein the non-rectangular perimeter of the motherboard comprises a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

25 52. The electronic device of claim 51, wherein the polygonal shape of the motherboard comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

53. The electronic device of claim 50, wherein the electronic device package
30 comprises a plurality of electronic device packages.

54. The electronic device of claim 53, wherein the non-rectangular perimeter of the substrate of each electronic device package has a shape configured to maximize the number of electronic device packages coupleable to the motherboard.

5

55. The electronic device of claim 54, wherein the perimeter shapes of the substrates are complementary.

56. The electronic device of claim 54, wherein the perimeters of the top and bottom surfaces match in shape and size.

10

57. The electronic device of claim 54, wherein the perimeters of the top and bottom surfaces differ in shape or size.

58. The electronic device of claim 49, further comprising a processor, a memory, an input/output (I/O), a connector, a socket, or a combination thereof.

15

59. The electronic device of claim 49, wherein the electronic device comprises a desktop computer, a laptop computer, a tablet computer, a smartphone, a smartwatch, a server, or a combination thereof.

20

60. A method of maximizing use of a rectangular panel or a round wafer in producing electronic device substrates or dies, comprising:

25

selecting at least one non-rectangular perimeter shape and size for the substrates or dies that is sufficient for use in an electronic device package into which the substrate or die is to be incorporated;

identifying a maximum number of the substrate units that fit on a surface of the rectangular panel or a maximum number of the die units that fit on a surface of the round wafer; and

30

forming the substrates from the panel or the dies from the wafer.

61. The method of claim 60, wherein the non-rectangular perimeter shape comprises a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

5

62. The method of claim 61, wherein the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

10 63. The method of claim 62, wherein the polygonal shape is a triangle.

64. The method of claim 60, wherein the substrate or die units have a substantially same shape or size, or both shape and size.

15 65. The method of claim 60, wherein the substrate or die units have substantially different shapes, or sizes, or both shapes and sizes.

66. The method of claim 60, wherein identifying a maximum number of substrate units that fit on a surface of the rectangular panel or a maximum
20 number of die units that fit on a surface of the round wafer comprises orienting units of the selected shape(s) and size(s) in relation to the panel or wafer surface.

67. The method of claim 60, wherein at least one substrate unit is suitable for
25 use as an embedded multi-die interconnect bridge (EMIB).

68. A method of making an electronic device package, comprising:
providing a die;
providing a substrate; and
30 coupling the die to the substrate, wherein either the die, the substrate, or both have a non-rectangular shaped perimeter.

69. The method of claim 68, wherein the non-rectangular shaped perimeter comprises a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free form shape, or a combination thereof.

5

70. The method of claim 69, wherein the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.

10 71. The method of claim 70, wherein the polygonal shape is a triangle.

72. The method of claim 68, wherein the die has a non-rectangular perimeter shape.

15 73. The method of claim 68, wherein the substrate has a non-rectangular perimeter shape.

74. The method of claim 68, wherein both the die and the substrate have a non-rectangular perimeter shape.

20

75. The method of claim 68, wherein the die comprises a plurality of dies and the non-rectangular shaped perimeter of each die is configured to maximize the number of dies coupled to the substrate.

25 76. A method of maximizing a number of electronic device packages on a motherboard, comprising:

selecting a size and shape for the motherboard;

selecting electronic device package configurations with non-rectangular shaped perimeters having complementary shapes that combine to form a shape that maximizes a density of the electronic device packages on the motherboard; and

30

mounting the electronic device packages on the motherboard.

77. The method of claim 76, wherein the non-rectangular perimeter of the electronic device package configurations comprise a circular shape, a semi-circular shape, an elliptical shape, a polygonal shape, a curvilinear shape, a free
5 form shape, or a combination thereof.

78. The method of claim 77, wherein the polygonal shape comprises a triangular shape, a pentagonal shape, a hexagonal shape, a heptagonal shape, an octagonal shape, or a combination thereof.
10

79. The method of claim 76, wherein the motherboard has a rectangular perimeter shape.

80. The method of claim 76, wherein the motherboard has a non-rectangular
15 perimeter shape.

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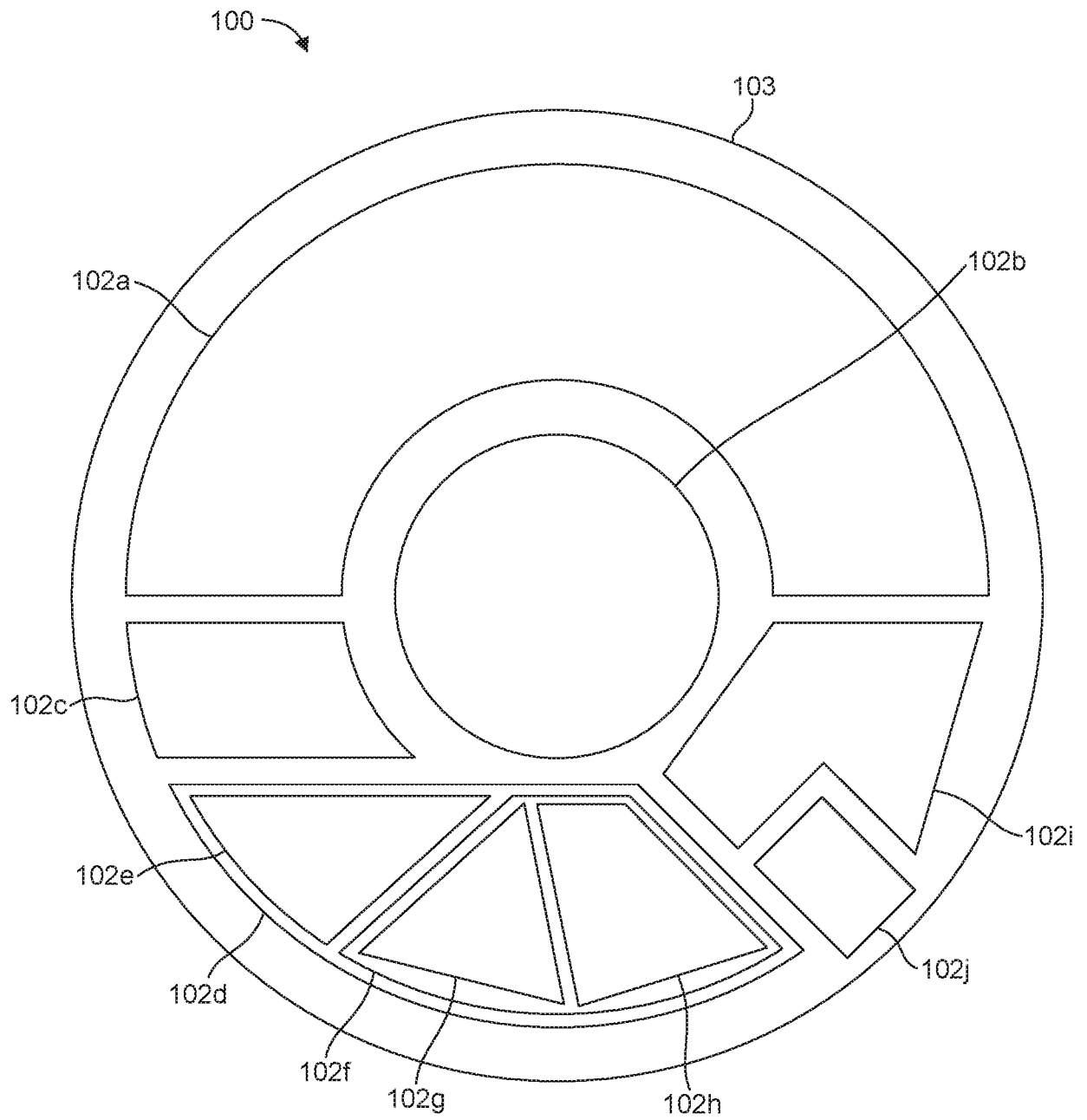


FIG. 1

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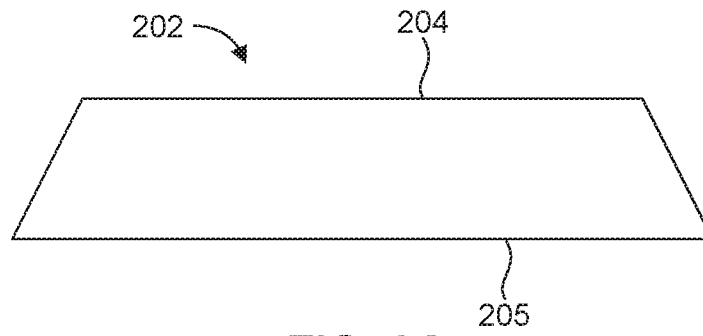


FIG. 2A

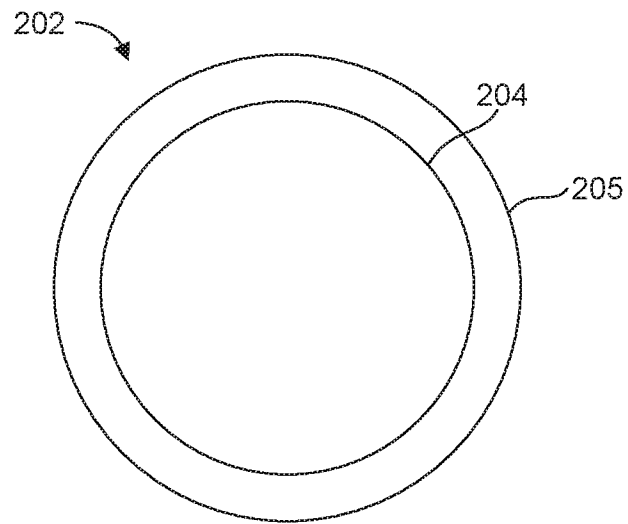


FIG. 2B

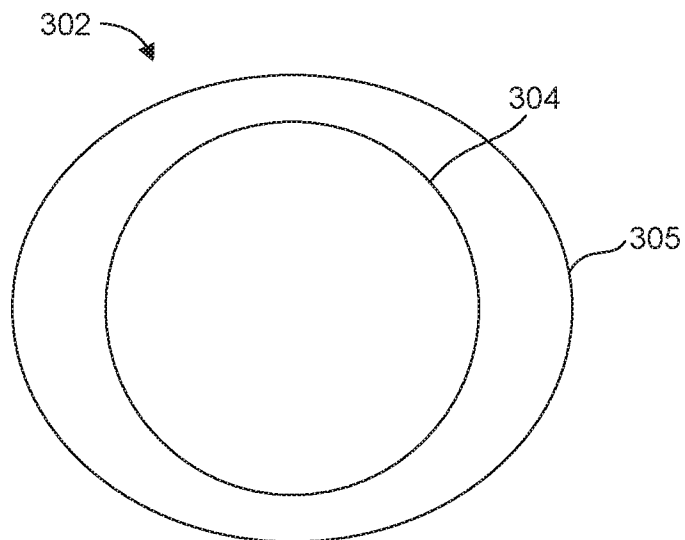


FIG. 3

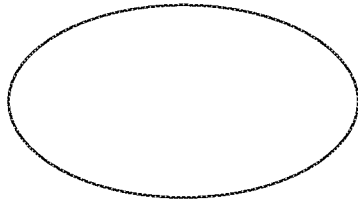


FIG. 4A

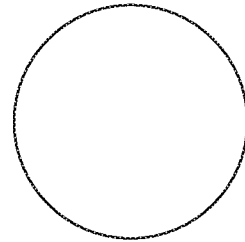


FIG. 4B

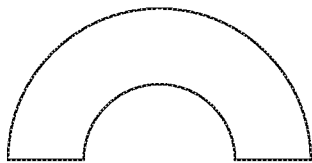


FIG. 4C



FIG. 4D

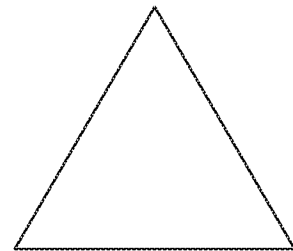


FIG. 4E



FIG. 4F

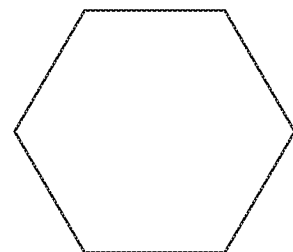


FIG. 4G



FIG. 4H

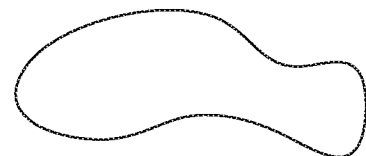


FIG. 4I

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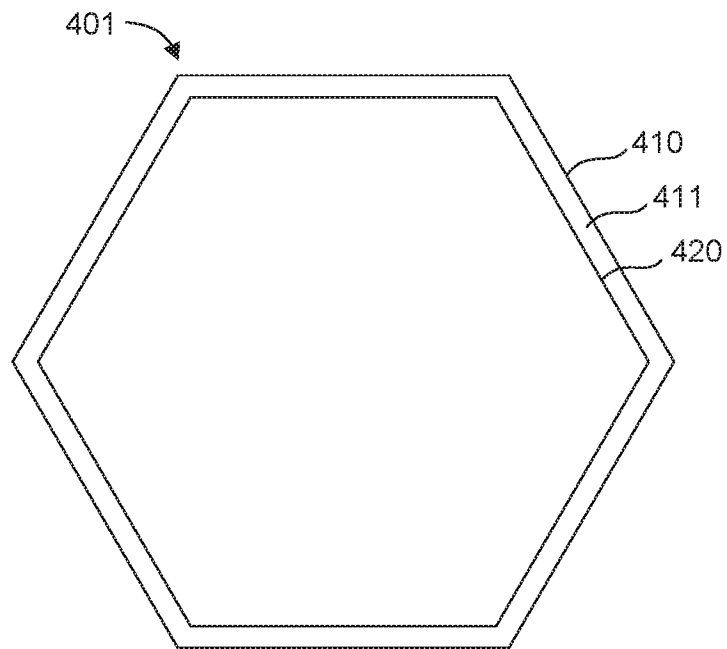


FIG. 5

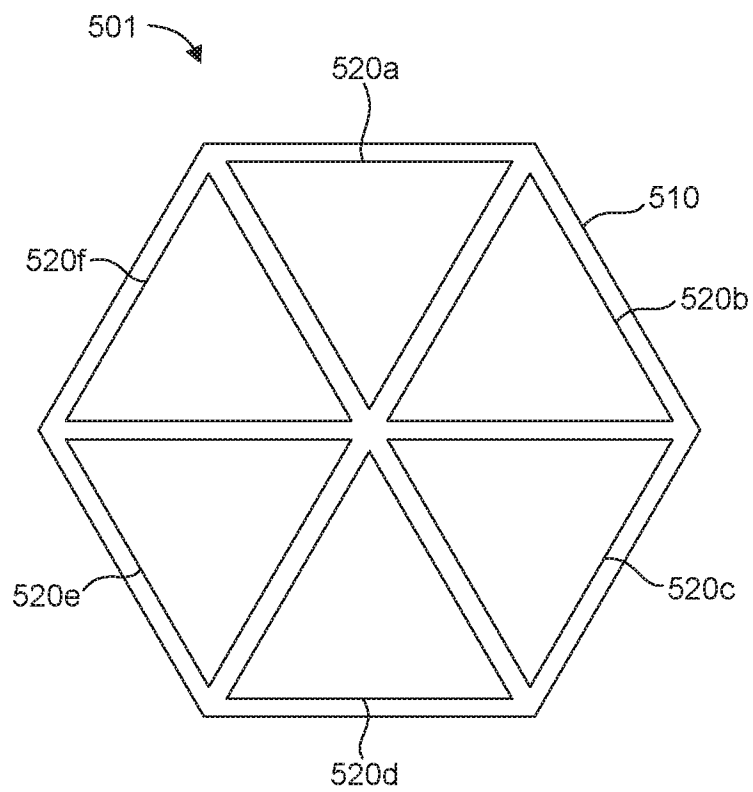


FIG. 6

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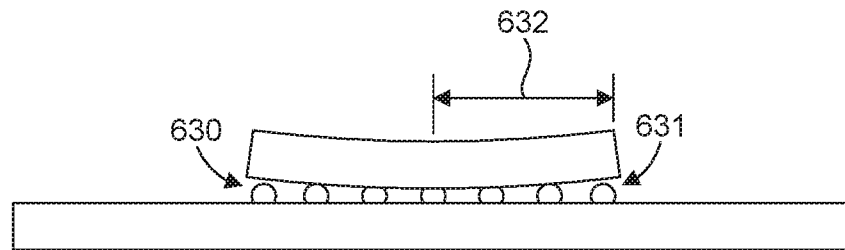


FIG. 7

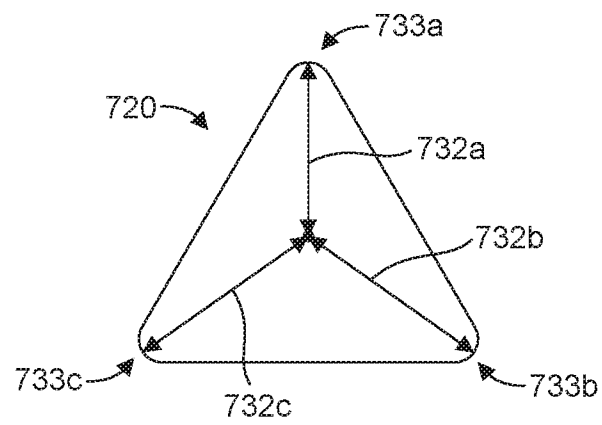


FIG. 8

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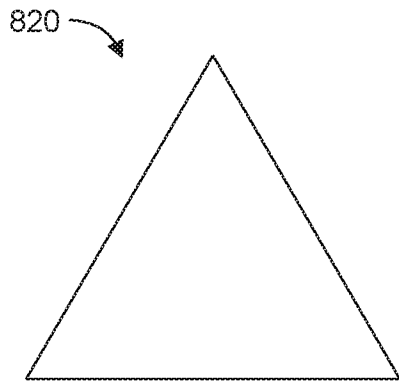


FIG. 9A

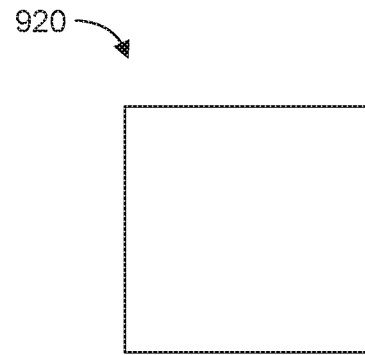


FIG. 9B

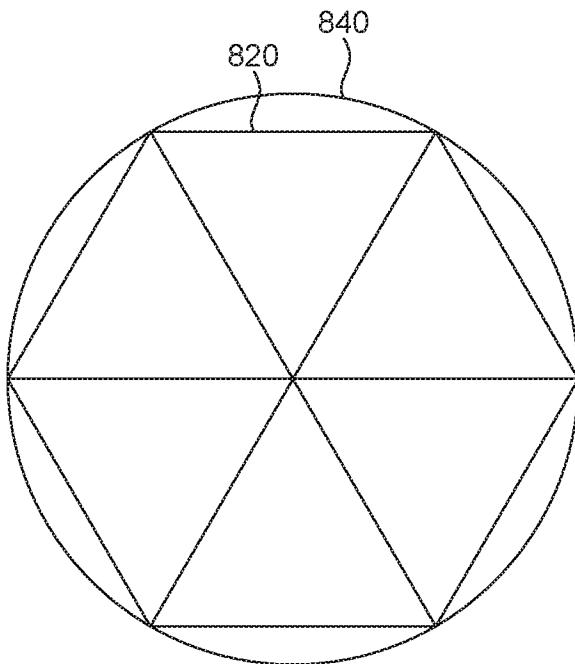


FIG. 10A

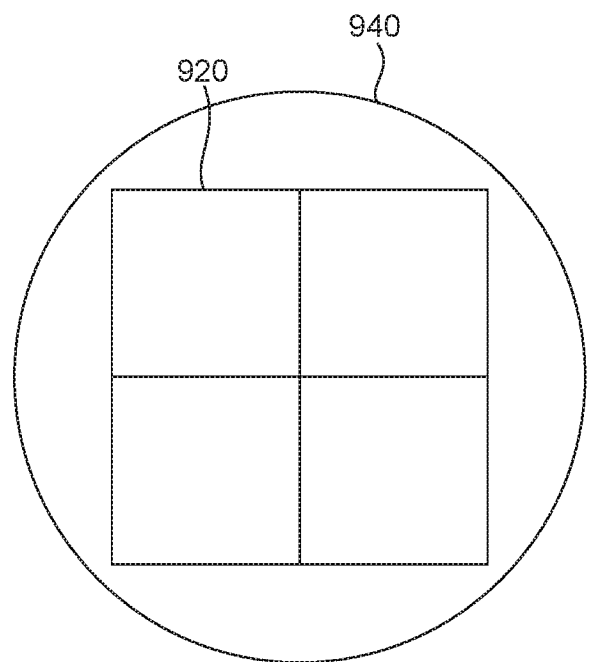


FIG. 10B

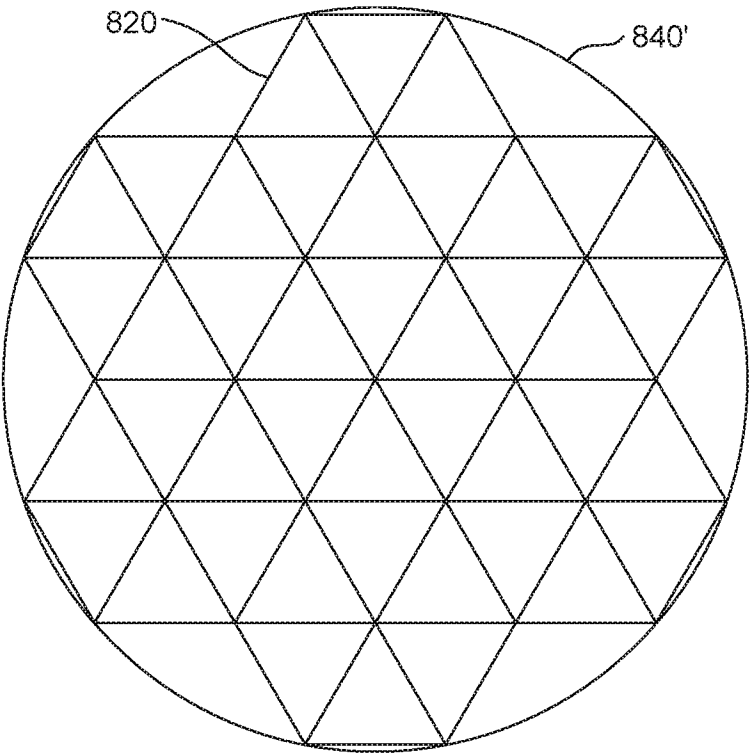


FIG. 11A

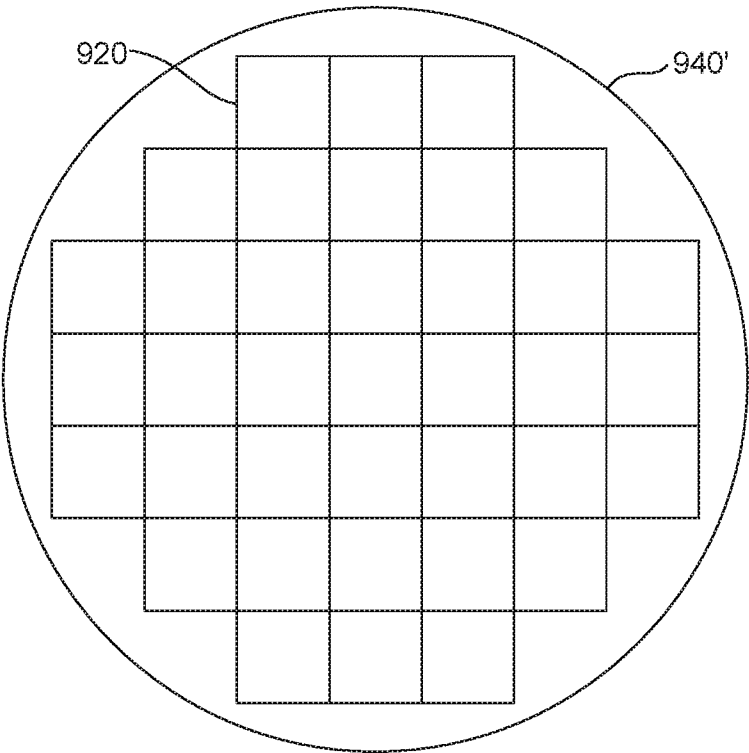


FIG. 11B

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2016/063799

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/02 H01L23/13 H01L29/06 H05K13/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 532 934 A (ROSTOKER MICHAEL D [US]) 2 July 1996 (1996-07-02)	1-9,11, 12, 15-22, 24,25, 60-67
Y	figures	23,26, 27,39-59
X	US 5 434 750 A (ROSTOKER MICHAEL D [US] ET AL) 18 July 1995 (1995-07-18)	28-36, 38,68-75
Y	abstract; figures	39-59
X	US 2007/018335 A1 (CHO SEUNG-HYUN [KR] ET AL) 25 January 2007 (2007-01-25)	28-31, 68-73
	abstract; figures 4-6	
	----- -/-	



Further documents are listed in the continuation of Box C.



See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/323469 A1 (BORTHAKUR SWARNAL [US] ET AL) 23 December 2010 (2010-12-23) figure 11 -----	10,13, 14,26,27
X	JP 2001 358369 A (ENOMOTO CO LTD) 26 December 2001 (2001-12-26) figures 2, 4 -----	10,13, 14,26,27 23,26,27
Y		

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5532934	A	02-07-1996	NONE
US 5434750	A	18-07-1995	US 5434750 A 18-07-1995
		US 5594626	A 14-01-1997
US 2007018335	A1	25-01-2007	CN 1897263 A 17-01-2007
		JP 2007027699	A 01-02-2007
		TW I307550	B 11-03-2009
		US 2007018335	A1 25-01-2007
US 2010323469	A1	23-12-2010	NONE
JP 2001358369	A	26-12-2001	NONE