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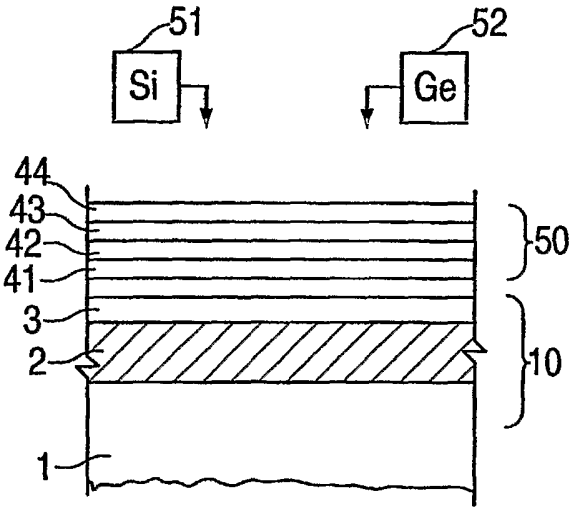
(54) **Title:** METHOD OF FORMING STRAINED SILICON MATERIALS WITH IMPROVED THERMAL CONDUCTIVITY



(57) **Abstract:** A method is disclosed for forming a strained Si layer on SiGe, where the SiGe layer has improved thermal conductivity. A first layer (41) of Si or Ge is deposited on a substrate (10) in a first depositing step; a second layer (42) of the other element is deposited on the first layer in a second depositing step; and the first and second depositing steps are repeated so as to form a combined SiGe layer (50) having a plurality of Si layers and a plurality of Ge layers (41-44). The respective thicknesses of the Si layers and Ge layers are in accordance with a desired composition ratio of the combined SiGe layer. The combined SiGe layer (50) is characterized as a digital alloy of Si and Ge having a thermal conductivity greater than that of a random alloy of Si and Ge. This method may further include the step of depositing a Si layer (61) on the combined SiGe layer (50); the combined SiGe layer is characterized as a relaxed SiGe layer, and the Si layer (61) is a strained Si layer. For still greater thermal conductivity in the SiGe layer, the first layer and second layer may be deposited so that each layer consists essentially of a single isotope.

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Method of Forming Strained Silicon Materials With Improved Thermal Conductivity

Technical Field

This invention relates to the fabrication of electronic devices, and more particularly to processes for forming strained Si and SiGe alloy films where the SiGe alloy has improved thermal conductivity.

Background Art

Silicon layers that possess tensile strain are of interest for use in high-performance CMOS devices. Improved charge carrier mobilities in strained Si layers permit enhanced FET performance (higher on-state current) without the need for geometric scaling in the device. A strained Si layer is typically formed by growing a Si layer on a relaxed silicon-germanium (SiGe) layer. Depending on the device application, the SiGe layer may be grown either on a bulk Si substrate or formed on top of an insulating layer to create a silicon-germanium-on-insulator (SGOI) wafer. The strained Si on a relaxed SiGe layer may be viewed as a Si/SiGe bilayer structure.

Regardless of how the substrates are made, a substantial obstacle to device fabrication in a Si/SiGe bilayer structure is the poor thermal conductivity of the SiGe alloy material. This has been shown to degrade the electrical characteristics of transistors fabricated on the bilayer structure. Since heat cannot be transported away as quickly as in the case of pure Si, the temperature in the channel region of the device increases, thereby degrading the mobility of the charge carriers.

In general, a variation in mass of the constituent atoms in a lattice reduces the phonon lifetime within the crystal, which in turn leads to reduced thermal conductivity. In the case of a SiGe random alloy, variation in mass between Si and Ge atoms, and among the various isotopes of Si and Ge, leads to reduced thermal conductivity. In a typical random SiGe alloy with naturally occurring Si and Ge, Si has three isotopes ^{28}Si, ^{29}Si and ^{30}Si, and Ge has five isotopes ^{70}Ge, ^{72}Ge, ^{73}Ge, ^{74}Ge and ^{76}Ge. The thermal conductivity of the SiGe material can be improved by using isotopically enriched gas sources for SiGe formation, which minimizes the isotopic mass variance of the Si and Ge respectively. U.S. Published Patent Application 2004/0004271 (Fukuda et al.) proposes that a SiGe layer be formed by deposition using

silane (SiH_4) and germane (GeH_4) gases where the isotope concentration of ^{28}Si and ^{70}Ge are both greater than 95%. A layer of Si (which may also be isotopically enriched) is deposited over this SiGe layer. This technique results in a bilayer structure of strained Si on a relaxed SiGe alloy layer having reduced isotopic mass variance, on a bulk Si substrate or an SOI substrate. Figures 1 and 2 show application of this technique on an SOI substrate. A typical SOI substrate 10 has an insulator layer 2 and a substrate layer 3 on a Si substrate 1 (Figure 1). Source gases 21, 22 for isotopically enriched Si and Ge are used in a deposition process to form a random SiGe alloy layer 4 (Figure 2). The isotopic enrichment serves to lower the mass variance of the SiGe layer, thereby improving its thermal conductivity.

A thermal mixing process (as described in U.S. Patent Application No. 10/055,138 of Bedell et al., assigned to the same assignee as the present application) may be employed to mix substrate layer 3 with reduced-mass-variance SiGe layer 4, to produce a relaxed SiGe layer 5 on insulator 2 (Figure 3). This structure may thus be viewed as a relaxed SiGe-on-insulator (SGOI) substrate, on which a Si layer 6 may be formed to provide a strained Si layer, as shown in Figure 4.

In order to realize the advantages of strained Si layers in CMOS devices, there is a need to provide Si/SiGe bilayer structures with improved thermal conductivity in the SiGe alloy layer. It is desirable to form relaxed SiGe layers with reduced mass variance, without the added complexity and expense of using isotopically enriched source gases for the Si and Ge.

Disclosure of Invention

The present invention provides a method of forming a SiGe layer on a substrate, where the SiGe layer has greater thermal conductivity than that of a random alloy of SiGe. In this method, a first layer of Si or Ge is deposited on a substrate in a first depositing step; a second layer of the other element is deposited on the first layer in a second depositing step; and the first and second depositing steps are repeated so as to form a combined SiGe layer having a plurality of Si layers and a plurality of Ge layers. The respective thicknesses of the Si layers and Ge layers are in accordance with a desired composition ratio of the combined SiGe layer (for example, a 1:1 ratio typically is realized with Si and Ge layers each about 10 Å thick to form a $Si_{0.5}Ge_{0.5}$ layer). Although the Si and Ge layers are strained, they are thin enough so that strain relieving dislocations are not formed therein. The combined SiGe layer

is characterized as a digital alloy of Si and Ge having a thermal conductivity greater than that of a random alloy of Si and Ge. This method may further include the step of depositing a Si layer on the combined SiGe layer; the combined SiGe layer is characterized as a relaxed SiGe layer, and the Si layer is a strained Si layer. For still greater thermal conductivity in the SiGe layer, the first layer and second layer may be deposited so that each layer consists essentially of a single isotope.

According to another aspect of the invention, a method is provided for fabricating a semiconductor device. This method includes the steps of forming a layer of a digital alloy of SiGe on a substrate, and forming a Si layer on the digital alloy of SiGe. The digital alloy of SiGe has a thermal conductivity greater than that of a random alloy of Si and Ge. The digital alloy layer may also be characterized as a relaxed SiGe layer, with the Si layer being a strained Si layer. According to a particular embodiment of the invention, the digital alloy layer includes a plurality of alternating sublayers of Si and Ge. These sublayers are formed with thicknesses in accordance with a desired composition ratio of the digital alloy of SiGe. Each of the sublayers may consist essentially of a single isotope.

According to a further aspect of the invention, a semiconductor device is provided which includes a layer of a digital alloy of SiGe on a substrate and a Si layer on the digital alloy of SiGe, wherein the digital alloy of SiGe has a thermal conductivity greater than that of a random alloy of Si and Ge. The digital alloy layer may be characterized as a relaxed SiGe layer, and the Si layer on the SiGe layer as a strained Si layer. The digital alloy layer includes a plurality of alternating sublayers of Si and Ge. The substrate may be a bulk Si substrate, a random SiGe alloy layer grown on a bulk Si substrate, or an SOI or SGOI structure.

Brief Description of Drawings

Figure 1 is a schematic illustration of a typical SOI substrate.

Figure 2 illustrates a SiGe layer formation technique using isotopically enriched Si and Ge sources.

Figure 3 is a schematic illustration of a SiGe-on-insulator (SGOI) structure formed by thermal mixing of SiGe and Si layers.

Figure 4 illustrates a strained Si layer on a SGOI substrate.

Figure 5 is a schematic illustration of a formation process for a low-mass-variance digital SiGe alloy layer on a SOI or SGOI substrate, in accordance with the present invention.

Figure 6 illustrates a strained Si layer deposited on the SiGe alloy layer of Figure 5.

Best Mode for Carrying Out the Invention

In accordance with the present invention, a layer of SiGe alloy is formed on a substrate (typically bulk Si, SiGe grown on bulk Si, SOI or SGOI); the SiGe alloy layer has reduced mass variance and hence higher thermal conductivity than a layer of random SiGe alloy. This is accomplished by forming the SiGe layer as an ordered digital alloy, as opposed to a random alloy.

Figure 5 illustrates a SiGe digital alloy formed by the process of the present invention. The substrate 10 (here shown as an SGOI structure with substrate layer 3 and insulator 2 on bulk substrate 1) is placed in a processing chamber where layers of either Si or Ge may be deposited on the substrate using Si and Ge sources 51, 52. A variety of deposition techniques may be used, including ultrahigh-vacuum CVD (UHVCVD) and low-temperature epitaxy (LTE), preferably at temperatures less than 650 °C.

A thin layer 41 of Si is deposited on the substrate, and a thin layer 42 of Ge is deposited on layer 42. Alternating layers 43, 44, etc. of Si and Ge are deposited until a desired total thickness of Si/Ge is reached. The relative thickness of the Si and Ge layers is adjusted in accordance with the desired composition ratio. For example, if the overall SiGe layer is to be 90% Si, layers 41 and 43 of Si would each typically be 90 Å thick while layers 42, 44 of Ge would each typically be 10 Å thick. The total number of Si and Ge layers depends on the desired thickness of the combined layer 50, which may vary from a few hundred Å to as much as a micron, depending on the device application. For example, if the SiGe layer is to be 50% Si and 500 Å thick, there would typically be 50 sublayers of Si and Ge (25 of each) 10 Å thick. The optimal thickness of the sublayers depends mainly on the ability to grow these layers in a planar manner while minimizing the formation of defects. Because the Si and Ge sublayers will typically be strained, there will be a thickness above which strain relieving dislocations will form. For substrates with an in-plane lattice parameter (parallel to substrate surface) close to that of relaxed Si, the Ge sublayers should not exceed 10 to 20 Å, but the Si sublayers can be up to a few hundred Å. For substrates with an in-plane lattice parameter close to that of relaxed Ge, the Si sublayers should not exceed 10 to 20 Å,

but the Ge sublayers can be up to a few hundred Å.

It is also desirable to limit the effect of mass variance in the substrate layer 3 (for example, if the substrate is SGOI so that layer 3 is itself a SiGe layer). This may be done before deposition of the Si/Ge sublayers 41, 42, etc. by thinning layer 3 (e.g. by polishing) so that the thickness of layer 3 is only a small fraction of layer 50. In the example given above where layer 50 is 500 Å thick and includes 25 sublayers each of Si and Ge, layer 3 may be thinned to 50 Å.

The combined layer 50, including all the alternating sublayers of Si and Ge, may be viewed as a superlattice, and more particularly as an ordered alloy or digital alloy of SiGe. It should be noted that, since each sublayer has only one element present, the mass variance in the combined layer is less than in a random alloy layer. Accordingly, the thermal conductivity of Si/Ge combined layer 50 is greater than for a conventionally deposited SiGe layer.

In this embodiment, the upper layer 3 of the substrate is a SiGe layer in an SGOI structure, and the first-deposited sublayer 41 is Si. As is understood in the art, this arrangement provides the advantages of a preferred interface between the substrate and the deposited layer; specifically, silicon growth tends to reduce the amount of oxygen at the growth interface, leading to a higher quality crystal layer.

Alternatively, the first-deposited sublayer may be of Ge if desired. As noted above, Si/Ge layer 50 may also be formed on a bulk Si, an existing SiGe layer on a bulk substrate, or an SOI substrate.

Each of the sublayers 42, 43, 44, etc. will be strained due to lattice mismatch determined by the in-plane lattice parameter of substrate layer 3 which is serving as the growth template. For example, if substrate layer 3 is a fully relaxed $Si_{0.5}Ge_{0.5}$ layer, then the Si sublayer will possess about 2.0% tensile strain and the Ge sublayer will possess about 2.2% compressive strain. However, the combined layer 50 as a whole has effectively zero stress, and for the purpose of forming a strained Si layer functions as a relaxed SiGe layer. A layer of Si 61 deposited on layer 50 will thus be a strained Si layer (see Figure 6), and the Si/SiGe combination 61, 50 will have higher thermal conductivity than a Si/SiGe bilayer where the SiGe is a random alloy.

In this embodiment, the Si and Ge delivered by sources 51, 52 (e.g. SiH_4 and GeH_4 gases respectively) are not isotopically enriched. However, isotope-enriched sources may be

used to achieve very low mass variance in the individual Si and Ge sublayers, and accordingly further improve the thermal conductivity of Si/Ge layer 50.

Industrial Applicability

The present invention is applicable to the manufacture of high-performance semiconductor devices where devices are to be formed in a layer of strained Si which overlies a SiGe alloy sublayer. In particular, the invention is applicable to formation of the SiGe alloy where improvement of thermal conductivity of the SiGe is desired.

While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the following claims.

Claims

1. A method of forming a SiGe layer on a substrate (10), the method comprising the steps of:

depositing a first layer (41) of one of Si and Ge in a first depositing step;

depositing a second layer (42) of the other of Si and Ge on the first layer in a second depositing step; and

repeating said first depositing step and said second depositing step so as to form a combined SiGe layer (50) having a plurality of Si layers and a plurality of Ge layers (41-44),

wherein respective thicknesses of the Si layers and Ge layers are in accordance with a desired composition ratio of the combined SiGe layer (50), and

the combined SiGe layer (50) is characterized as a digital alloy of Si and Ge having a thermal conductivity greater than that of a random alloy of Si and Ge.

2. A method according to claim 1, wherein each of the Si layers and Ge layers has a thickness such that strain relieving dislocations are not formed therein.

3. A method according to claim 1, further comprising the step of:

depositing a Si layer (61) on the combined SiGe layer (50),

wherein the combined SiGe layer (50) is further characterized as a relaxed SiGe layer, and said Si layer (61) is a strained Si layer.

4. A method according to claim 1, wherein the substrate (10) comprises a silicon-on-insulator (SOI) structure.

5. A method according to claim 1, wherein the substrate (10) comprises a SiGe-on-insulator (SGOI) structure (1, 2, 3).

6. A method according to claim 1, wherein the substrate (10) comprises a SiGe layer overlying a Si substrate (1).

7. A method according to claim 1, characterized in that the substrate (10) has an upper layer (3), and further comprising the step of polishing said upper layer to reduce the thickness thereof, before said first depositing step.

8. A method according to claim 1, wherein at least one of the first layer and the second layer consists essentially of a single isotope.

9. A semiconductor device comprising:

a layer (50) of a digital alloy of SiGe on a substrate (10); and

a Si layer (61) on the digital alloy of SiGe,

characterized in that the digital alloy of SiGe has a thermal conductivity greater than that of a random alloy of Si and Ge.

10. A device according to claim 9, wherein the digital alloy layer (50) is characterized as a relaxed SiGe layer, and said Si layer (61) is a strained Si layer.

11. A device according to claim 9, characterized in that the digital alloy layer (50) includes a plurality of alternating sublayers (41-44) of Si and Ge.

12. A device according to claim 11, characterized in that the sublayers (41-44) are formed with thicknesses in accordance with a desired composition ratio of the digital alloy of SiGe.

13. A device according to claim 11, characterized in that each of the sublayers (41-44) is formed with a thickness such that strain relieving dislocations are not formed therein.

14. A device according to claim 11, characterized in that each of the sublayers (41-44) consists essentially of a single isotope.

15. A device according to claim 11, characterized in that a sublayer of Si (41) is disposed on the substrate (10).

16. A device according to claim 9, characterized in that the substrate (10) includes a silicon-on-insulator (SOI) structure.

17. A device according to claim 9, characterized in that the substrate (10) includes a silicon-germanium-on-insulator (SGOI) structure (1, 2, 3).

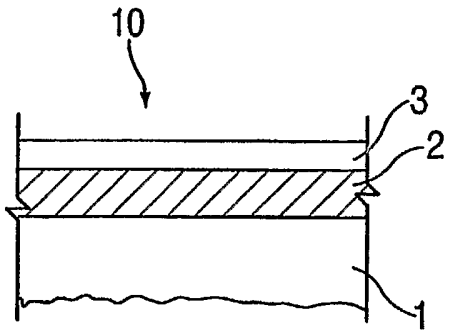

FIG. 1
(PRIOR ART)

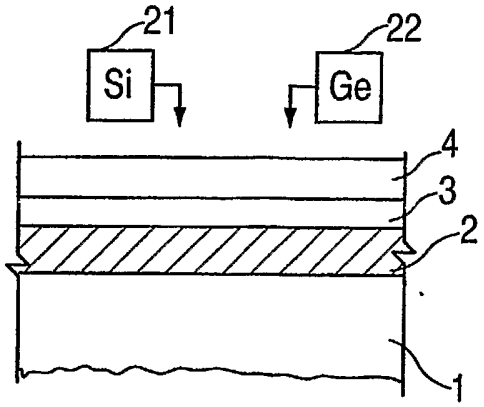

FIG. 2
(PRIOR ART)

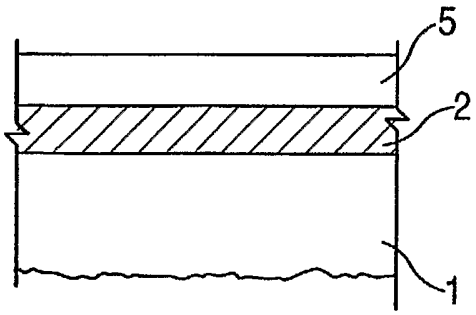

FIG. 3
(PRIOR ART)

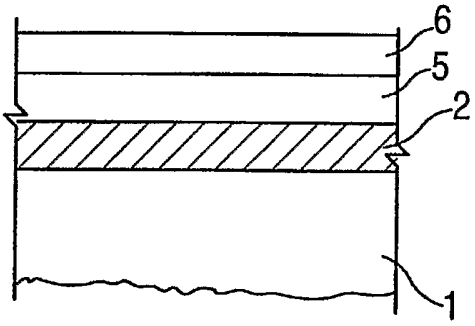

FIG. 4
(PRIOR ART)

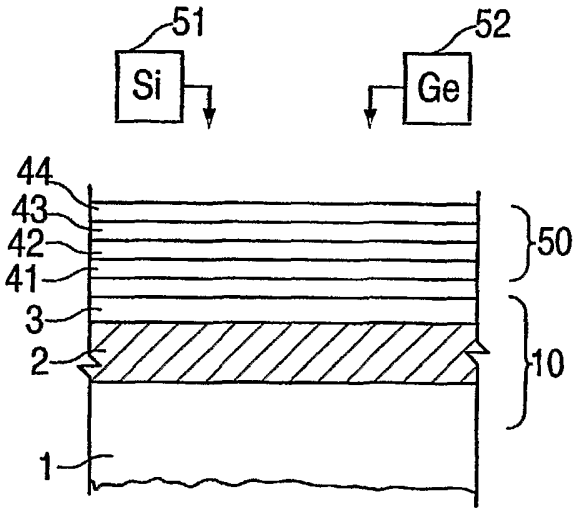

FIG. 5

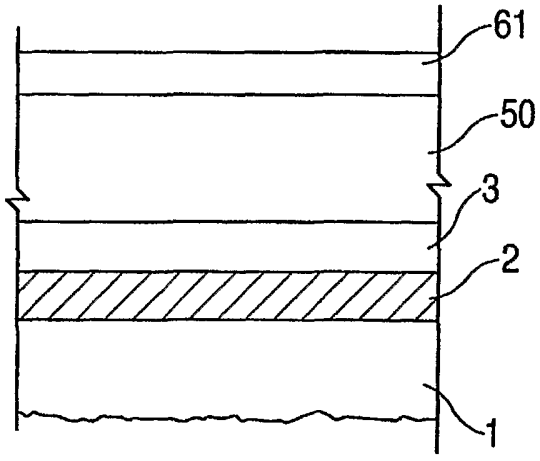

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/27691

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 21/36, 21/20, 31/117
US CL : 438/478; 257/616
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/478; 257/616

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	CHURCHILL, A.C., et al. Optical Etalon Effects and Electronic Structure in Silicon-Germanium 4 Monolayer: 4 Monolayer Strained Layer Superlattices, Semicond. Sci. Technol. 1991, Vol. 6, pages 18-26, especially pages 18-19.	1, 2, 3, 9, 10, 11, 12, 13, 15, ---------- 4, 5, 8, 14, 16, 17
X	US 6,043,517 (PRESTING et al) 28 March 2000 (28.03.2000), column 2, lines 11-19, column 2, line 64 - column 3, line 46.	1, 6, 7
Y	US 2004/0004271 A1 (FUKUDA et al) 8 January 2004 (08.01.2004), paragraphs 11, 23, and 101-113.	4, 5, 8, 14, 16, 17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
24 October 2005 (24.10.2005)	08 DEC 2005
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