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(71) Applicant (for all designated States except US): **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, MS: RNB-4-150, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **VARMA, Ankush** [IN/US]; 179 SE 49th Ct, Hillsboro, Oregon 97123 (US). **SISTLA, Krishnakanth** [IN/US]; 6000 SW Fountain Grove Terrace, Beaverton, Oregon 97007 (US). **QUIROZ, Cesar** [PE/US]; Granada Ave Unit 114, Santa Clara, California 95051 (US). **GARG, Vivek** [US/US]; 257 Oxborough Drive, Folsom, California 95630 (US). **ROWLAND, Martin** [US/US]; 6570 SW Ecola Place, Beaverton, Oregon 97007 (US). **SODHI, Inder** [US/US]; 963 Sterling Circle, Folsom, California 95630 (US). **BURNS, James** [US/US]; 19700 Alderbrook Way, Cupertino, California 95014 (US).(74) Agents: **HUNTER, Spencer K.** et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 1279 Oakmead Parkway, Sunnyvale, California 94085-4040 (US).

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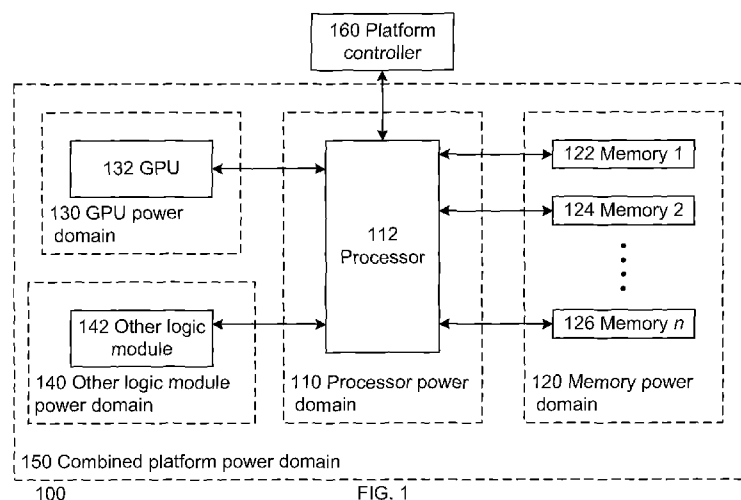


FIG. 1

(57) Abstract: A method and apparatus for dynamic power limit sharing among the modules in the platform. In one embodiment of the invention, the platform comprises a processor and memory modules. By expanding the power domain to include the processor and the memory modules, dynamic sharing of the power budget of the platform between the processor and the memory modules is enabled. For low-bandwidth workloads, the dynamic sharing of the power budget offers significant opportunity for the processor to increase its frequency by using the headroom in the memory power and vice versa. This enables higher peak performance for the same total platform power budget in one embodiment of the invention.



DYNAMIC POWER LIMIT SHARING IN A PLATFORM

FIELD OF THE INVENTION

[0001] This disclosure pertains to a platform, as well as code to execute thereon, and in particular but not exclusively, to the dynamic power limit sharing among the modules in the platform.

BACKGROUND DESCRIPTION

[0002] Traditionally, the power limit to the central processing unit (CPU) has been provided by the platform. With the advent of integrated memory controllers, the CPU or processor controls the power consumption of the memory modules in the platform as well. In a micro-processor based platform, the power consumption of the memory modules in the platform can constitute a significant portion of the total power consumed by the platform.

[0003] In many platforms, the processor and the memory modules are treated as separate power domains when the total platform power budget is allocated. When the total platform budget such as platform rating is determined, each domain is set to a realistic maximum value, which is not the worst case scenario. As such, there is a processor power limit that is obeyed by the processor and a memory power limit that is obeyed by the memory modules.

[0004] When the memory modules and the processor each have a separate power budget or limit, it limits the performance of the platform or system for low-bandwidth workloads.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The features and advantages of embodiments of the invention will become apparent from the following detailed description of the subject matter in which:

[0006] Figure 1 illustrates the block diagram of a platform in accordance with one embodiment of the invention;

[0007] Figure 2 illustrates the operations to enable dynamic power limit sharing in the platform in accordance with one embodiment of the invention; and

[0008] Figure 3 illustrates a system to implement the methods disclosed herein in accordance with one embodiment of the invention.

DETAILED DESCRIPTION

[0009] Embodiments of the invention described herein are illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the figures to indicate corresponding or analogous elements. Reference in the specification to “one embodiment” or “an embodiment” of the invention means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrase “in one embodiment” in various places throughout the specification are not necessarily all referring to the same embodiment.

[0010] Embodiments of the invention provide a method and apparatus for dynamic power limit sharing among the modules in the platform. The platform includes, but is not limited to, a desktop computer, a tablet computer, a laptop computer, a netbook, a notebook computer, a personal digital assistant (PDA), a tablet, a server, a workstation, a cellular telephone, a mobile computing device, a smart phone, an Internet appliance or any other type of computing device.

[0011] In one embodiment of the invention, the platform comprises a processor and memory modules. By expanding the power domain to include the processor and the memory modules, dynamic sharing of the power budget or limit of the platform between the processor and the memory modules is enabled. For low-bandwidth workloads, the dynamic sharing of the power budget offers significant opportunity for the processor to increase its frequency by using the headroom in the memory power and vice versa. This enables higher peak performance for the same total platform power budget in one embodiment of the invention.

[0012] In another embodiment of the invention, the platform comprises other logic modules and the platform enables dynamic sharing of the power limit among the logic modules. The logic module includes, but is not limited to, a processor, a co-processor, a digital signal processor, a graphics processing unit (GPU), a memory module and other module where the power consumption of the module can be estimated.

[0013] Figure 1 **100** illustrates the block diagram of a platform in accordance with one embodiment of the invention. In one embodiment of the

invention, the platform comprises a processor **112**, memory modules 1 **122**, 2 **124**, n **126**, the GPU **132** and the other logic module **142**. The memory module n **126** illustrates that the processor can be coupled with any number of memory modules and the other module **142** illustrates that the platform can have other logic modules coupled with the processor **112**.

[0014] In one embodiment of the invention, each module in the platform has its own power domain. For example, in one embodiment of the invention, the processor **112** is powered by the processor power domain **110**, the memory modules 1 **122**, 2 **124**, n **126** are powered by the memory power domain **120**, the GPU **132** is powered by the GPU power domain **130** and the other logic module **142** is powered by the other logic power domain **140**.

[0015] To enable dynamic sharing of the power limit among the modules in the platform, the platform creates a combined platform power domain **150** in one embodiment of the invention. The modules of the platform obey the power limit set in the combined platform power domain **150** but the individual constraints on each module can be relaxed in one embodiment of the invention. By doing so, it allows dynamic power sharing among the modules in the platform in one embodiment of the invention.

[0016] Further, with one limit for the combined platform power domain **150**, only one guard band is needed to be added for the platform and it allows minimal guard band requirements for the power consumption of each of the modules in the platform in one embodiment of the invention. This is because the modules in the

platform are dynamically sharing the power consumption limit for the combined platform power domain **150**.

[0017] For example, when the processor is executing a low bandwidth task and the memory modules do not require high memory bandwidth utilization, the power limit of the processor is dynamically increased while the power limit of the memory modules are decreased such that the power budget of the combined platform power domain is still obeyed. This enables the processor to execute faster with a higher power limit while power of the memory modules is decreased.

[0018] In one embodiment of the invention, the combined platform power domain **150** allows the platform to handle a power sensitive environment where the overall power budget or limit needs to be maintained while allowing each of the modules to execute in an efficient way.

[0019] In one embodiment of the invention, the platform has a register to store the programmable limit for the combined platform power domain **150** and another register to set the programmable platform domain time window over which the limit is enforced. In one embodiment of the invention, the limit of the combined platform power domain **150** is created in addition to the existing limits of the modules in the platform. In another embodiment of the invention, the limit of the combined platform power domain **150** replaces the power limits of the modules in the platform.

[0020] In one embodiment of the invention, the platform has logic to enforce the limit for the combined platform power domain **150** by changing the power consumption of the modules in the platform. For example, in one embodiment of

the invention, the platform executes logic such as processor-based firmware to enforce the limit of the combined platform power domain **150**. The processor-based firmware dynamically changes the behavior of each module such that the module stays within the limit of the combined platform power domain **150**.

[0021] For example, in one embodiment of the invention, in order to change the power consumption of the processor **112**, the logic in the platform changes one or more parameters of the processor **112** that include, but are not limited to, voltage input, frequency, throughput of instructions, and any other parameter that affects the power consumption of the processor **112**. In one embodiment of the invention, in order to lower the power consumption of the processor **112**, the logic in the platform switches the executing code or instructions to a lower performing code that requires less power by only using lower precision arithmetic units, but requires more iteration to build the precision.

[0022] For example, in another embodiment of the invention, in order to change the power consumption of the memory modules **1 122, 2 124, n 126**, the platform changes one or more parameters of the memory modules **1 122, 2 124, n 126** that include, but are not limited to, voltage input, frequency, number of read instructions, number of write instructions, bandwidth throttling and any other parameter that affects the power consumption of the memory modules **1 122, 2 124, n 126**. One of ordinary skill in the relevant art will readily appreciate how to use other techniques to alter the power consumption of the modules and these other techniques can be used without affecting the workings of the invention.

[0023] In one embodiment of the invention, the platform controller **160** sets the power limits for each domain and communicates them to the processor **112**. In one embodiment of the invention, the platform controller **160** is a hardware device such as a Board Management Controller (BMC) or a Manageability Engine (ME) that is connected through a dedicated hardware interface. In another embodiment of the invention, the platform controller **160** is a software entity such as a Node Manager that is in charge of the platform power management. In yet another embodiment of the invention, the platform controller **160** is integrated with the processor **112**.

[0024] In one embodiment of the invention, the platform has logic such as processor-based firmware (P-code) to observe the average power consumption of the modules in the platform over the platform domain time window. For example, in one embodiment of the invention, the platform analyzes or determines the average processor and memory power consumption over the platform domain time window and adjusts the power consumption of the processor **112** and the memory modules **122**, **124**, *n* **126** to enforce both the individual processor and memory power limits and/or the limit of the combined platform power domain **150**.

[0025] When a module has multiple power consumption limits, the lowest available limit is enforced by the platform. For example, in one embodiment of the invention, if the average processor power consumption over the platform domain time window exceeds the processor power limit, the voltage/frequency of the processor **112** is reduced. Similarly, if the average memory power consumption exceeds the memory power limit, the memory controller in the processor can be set to throttle the memory.

[0026] In addition, if the average platform power consumption exceeds the limit of the combined platform power domain **150**, the platform selects the most power consuming module to reduce its power consumption such that the limit of the combined platform power domain **150** is met. For example, the platform may select the processor **112** and reduces its voltage / frequency because it is a performance-efficient mechanism for reducing the power of the platform. If the processor **112** is set to the lower operating point that consumes the least power but the limit of the combined platform power domain **150** is not met, the platform selects another module to throttle its power consumption to meet the limit of the combined platform power domain **150**. For example, the platform may select the GPU **132** for throttling if the limit of the combined platform power domain **150** is not met.

[0027] In one embodiment of the invention, the processor-based firmware has access to the power measurements of the modules in the platform. This allows the average power consumption of each module to be determined and checked against the set threshold. For example, in one embodiment of the invention, the platform may access readings taken from the associated digital voltage regulators for the modules. In another embodiment of invention, the platform may estimate the power consumed by each module by using performance counters. One of ordinary skill in the relevant art will readily appreciate how to use other techniques of determining the power consumption of each module in the platform and these other techniques can be used without affecting the workings of the invention.

[0028] Figure 2 illustrates the operations to enable dynamic power limit sharing in the platform in accordance with one embodiment of the invention. For clarity of illustration, figure 2 is discussed with reference to figure 1. For ease of illustration, the operations illustrated in figure 2 apply to a platform with a processor power domain **110** and a memory power domain **120**. One of ordinary skill in the relevant art will readily appreciate how to extend the operations for a platform with more modules and shall not be described herein.

[0029] In step **210**, the target processor power (TARGET_CPU_power) is set to the difference between the combined platform power budget **105** (Platform budget) and the average memory power consumption (MEM_POWER). In one embodiment of the invention, the average memory power consumption is computed over the platform domain window time limit.

[0030] The step **210** allows the platform to dynamically share the power budget between the processor and the memory modules. For example, in one embodiment of the invention, when the average power consumption of the memory modules is low, a higher target processor power is given to the processor. Similarly, when the average power consumption of the memory modules is high, a lower target processor power is given to the processor.

[0031] In step **220**, the operation **200** checks if the target processor power is greater than the minimum allowed processor power. The minimum allowed processor power is the lowest allowed power rating for the processor in one embodiment of the invention. If the target processor power is greater than the

minimum allowed processor power in step **220**, the processor power limit is set to the target processor power in step **232**. In step **234**, the operation **200** disable the throttling of the memory and the operation **200** goes back to step **210**.

[0032] If the target processor power is not greater than or equal to the minimum allowed processor power in step **220**, the target memory power limit (TARGET_MEM_POWER) is set to the difference between the combined platform power budget **105** and the minimum allowed processor power in step **242**. In step **244**, the operation **200** enables the throttling of the memory to meet the target memory power limit. In step **246**, the operation **220** sets the processor power limit to the minimum allowed processor power and the operation **200** goes back to step **210**.

[0033] Figure 3 illustrates a system or platform **300** to implement the methods disclosed herein in accordance with one embodiment of the invention. The system **300** includes, but is not limited to, a desktop computer, a tablet computer, a laptop computer, a netbook, a notebook computer, a personal digital assistant (PDA), a server, a workstation, a cellular telephone, a mobile computing device, a smart phone, an Internet appliance or any other type of computing device. In another embodiment, the system **300** used to implement the methods disclosed herein may be a system on a chip (SOC) system.

[0034] The processor **310** has a processing core **312** to execute instructions of the system **300**. The processing core **312** includes, but is not limited to, fetch logic to fetch instructions, decode logic to decode the instructions, execution logic to execute

instructions and the like. The processor **310** has a cache memory **316** to cache instructions and/or data of the system **300**. In another embodiment of the invention, the cache memory **316** includes, but is not limited to, level one, level two and level three, cache memory or any other configuration of the cache memory within the processor **310**.

[0035] The memory control hub (MCH) **314** performs functions that enable the processor **310** to access and communicate with a memory **330** that includes a volatile memory **332** and/or a non-volatile memory **334**. The volatile memory **332** includes, but is not limited to, Synchronous Dynamic Random Access Memory (SDRAM), Dynamic Random Access Memory (DRAM), RAMBUS Dynamic Random Access Memory (RDRAM), and/or any other type of random access memory device. The non-volatile memory **334** includes, but is not limited to, NAND flash memory, phase change memory (PCM), read only memory (ROM), electrically erasable programmable read only memory (EEPROM), or any other type of non-volatile memory device.

[0036] The memory **330** stores information and instructions to be executed by the processor **310**. The memory **330** may also stores temporary variables or other intermediate information while the processor **310** is executing instructions. The chipset **320** connects with the processor **310** via Point-to-Point (PtP) interfaces **317** and **322**. The chipset **320** enables the processor **310** to connect to other modules in the system **300**. In another embodiment of the invention, the chipset **320** is a platform controller hub (PCH). In one embodiment of the invention, the interfaces **317** and **322** operate in accordance with a PtP communication protocol such as the Intel® QuickPath

Interconnect (QPI) or the like. The chipset **320** connects to a GPU or a display device **340** that includes, but is not limited to, liquid crystal display (LCD), cathode ray tube (CRT) display, or any other form of visual display device. In another embodiment of the invention, the GPU **340** is not connected to the chipset **320** and is part of the processor **310** (not shown).

[0037] In addition, the chipset **320** connects to one or more buses **350** and **360** that interconnect the various modules **374**, **380**, **382**, **384**, and **386**. Buses **350** and **360** may be interconnected together via a bus bridge **372** if there is a mismatch in bus speed or communication protocol. The chipset **320** couples with, but is not limited to, a non-volatile memory **380**, a mass storage device(s) **382**, a keyboard/mouse **384** and a network interface **386**. The mass storage device **382** includes, but is not limited to, a solid state drive, a hard disk drive, an universal serial bus flash memory drive, or any other form of computer data storage medium. The network interface **386** is implemented using any type of well known network interface standard including, but not limited to, an Ethernet interface, a universal serial bus (USB) interface, a Peripheral Component Interconnect (PCI) Express interface, a wireless interface and/or any other suitable type of interface. The wireless interface operates in accordance with, but is not limited to, the IEEE 802.11 standard and its related family, Home Plug AV (HPAV), Ultra Wide Band (UWB), Bluetooth, WiMax, or any form of wireless communication protocol.

[0038] While the modules shown in figure 3 are depicted as separate blocks within the system **300**, the functions performed by some of these blocks may be

integrated within a single semiconductor circuit or may be implemented using two or more separate integrated circuits. The system **300** may include more than one processor / processing core in another embodiment of the invention.

[0039] The methods disclosed herein can be implemented in hardware, software, firmware, or any other combination thereof. Although examples of the embodiments of the disclosed subject matter are described, one of ordinary skill in the relevant art will readily appreciate that many other methods of implementing the disclosed subject matter may alternatively be used. In the preceding description, various aspects of the disclosed subject matter have been described. For purposes of explanation, specific numbers, systems and configurations were set forth in order to provide a thorough understanding of the subject matter. However, it is apparent to one skilled in the relevant art having the benefit of this disclosure that the subject matter may be practiced without the specific details. In other instances, well-known features, components, or modules were omitted, simplified, combined, or split in order not to obscure the disclosed subject matter.

[0040] The term “is operable” used herein means that the device, system, protocol etc, is able to operate or is adapted to operate for its desired functionality when the device or system is in off-powered state. Various embodiments of the disclosed subject matter may be implemented in hardware, firmware, software, or combination thereof, and may be described by reference to or in conjunction with program code, such as instructions, functions, procedures, data structures, logic, application programs, design representations or formats for simulation, emulation, and fabrication of a design,

which when accessed by a machine results in the machine performing tasks, defining abstract data types or low-level hardware contexts, or producing a result.

[0041] The techniques shown in the figures can be implemented using code and data stored and executed on one or more computing devices such as general purpose computers or computing devices. Such computing devices store and communicate (internally and with other computing devices over a network) code and data using machine-readable media, such as machine readable storage media (e.g., magnetic disks; optical disks; random access memory; read only memory; flash memory devices; phase-change memory) and machine readable communication media (e.g., electrical, optical, acoustical or other form of propagated signals – such as carrier waves, infrared signals, digital signals, etc.).

[0042] While the disclosed subject matter has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the subject matter, which are apparent to persons skilled in the art to which the disclosed subject matter pertains are deemed to lie within the scope of the disclosed subject matter.

CLAIMS

What is claimed is:

1. A processor comprising:
logic to:
determine a power budget for a platform, wherein the platform comprises the processor and a memory module; and
dynamically set a power limit for the processor and another power limit for the memory module based on the power budget for the platform.
2. The processor of claim 1, wherein the logic is further to determine a time period to enforce the power budget for the platform, and wherein the logic to dynamically set the power limit for the processor and the other power limit for the memory module based on the power budget for the platform is to dynamically set the power limit for the processor and the other power limit for the memory module based on the power budget for the platform for a duration of the time period.
3. The processor of claim 1, wherein the logic to dynamically set the power limit for the processor and the other power limit for the memory module based on the power budget for the platform is to:
analyze an average power consumption of the processor to determine the power limit for the processor; and

analyze another average power consumption of the memory module to determine the other power limit for the memory module.

4. The processor of claim 3, wherein the logic to analyze the average power consumption of the processor to determine the power limit for the processor is to:
perform one or more of, determining number of stall counts of the processor, and determining characteristics of workloads executed by the processor.
5. The processor of claim 3, wherein the logic to analyze the average power consumption of the memory module to determine the other power limit for the memory module is to determine memory bandwidth utilization of the memory module.
6. The processor of claim 1, wherein the logic is further to:
adjust operations of the processor based on the dynamically set power limit of the processor; and
adjust operations of the memory module based on the other dynamically set power limit of the memory module.
7. The processor of claim 6, wherein the logic to adjust the operations of the processor based on the dynamically set power limit of the processor is to:

adjust one or more of, a voltage, a frequency, instruction throughput, and a performance level of executing code, of the processor to meet the dynamically set power limit of the processor.

8. The processor of claim 6, wherein the logic to adjust the operations of the memory module based on the other dynamically set power limit of the memory module is to:

adjust one or more of, read operations, write operations, and a voltage, of the memory module to meet the dynamically set power limit of the memory module.

9. A system comprising:

a logic module;

a processor coupled with the logic module, to:

receive a power budget for a system; and

dynamically set a power limit for the processor and another power limit for the logic module based on the power budget for the platform.

10. The system of claim 9, wherein the processor is further to determine a time period to enforce the power budget for the system, and wherein the processor to dynamically set the power limit for the processor and the other power limit for the logic module based on the power budget for the system is to dynamically set the power limit

for the processor and the other power limit for the logic module based on the power budget for the system for a duration of the time period.

11. The system of claim 9, wherein the processor to dynamically set the power limit for the processor and the other power limit for the logic module based on the power budget for the system is to:

analyze an average power consumption of the processor to determine the power limit for the processor; and

analyze another average power consumption of the logic module to determine the other power limit for the memory module.

12. The system of claim 11, wherein the processor to analyze the average power consumption of the processor to determine the power limit for the processor is to:

perform one or more of, determining number of stall counts of the processor, and determining characteristics of workloads executed by the processor.

13. The system of claim 12, wherein the processor to analyze the average power consumption of the logic module to determine the other power limit for the logic module is to determine bandwidth utilization of the logic module.

14. The system of claim 13, wherein the processor to dynamically set the power limit for the processor and the other power limit for the logic module based on the power budget for the system:

set a target processor power as a difference of the power budget and the average power consumption of the logic module; and

determine whether the target processor power is greater than a minimum allowed power consumption of the processor.

15. The system of claim 14, wherein the processor is further to:

set the power limit of the processor as the target processor power in response to a determination that the target processor power is greater than the minimum allowed power consumption of the processor; and

disable any throttling of the logic module.

16. The system of claim 14, wherein in response to a determination that the target processor power is not greater than the minimum allowed power consumption of the processor, the processor is to:

set a target logic module power as a difference of the power budget and the minimum allowed power consumption of the processor;

enable throttling of the logic module to meet the target logic module power; and

set the power limit of the processor as the minimum allowed power consumption of the processor.

17. The system of claim 9, wherein the logic module comprises one of a memory module, a graphics processor unit (GPU), and a co-processor.
18. A method comprising:
- determine a power budget for a platform, wherein the platform comprises the processor and one memory module; and
 - dynamically setting a power limit for the processor and another power limit for the logic module based on the power budget for the platform.
19. The method of claim 18, further comprising determining a time period to enforce the power budget for the platform, and wherein dynamically setting the power limit for the processor and the other power limit for the logic module based on the power budget for the platform comprises dynamically setting the power limit for the processor and the other power limit for the logic module based on the power budget for the platform for a duration of the time period.
20. The method of claim 18, wherein dynamically setting the power limit for the processor and the other power limit for the logic module based on the power budget for the platform comprises:
- analyzing an average power consumption of the processor to determine the power limit for the processor; and

analyzing another average power consumption of the logic module to determine the other power limit for the memory module.

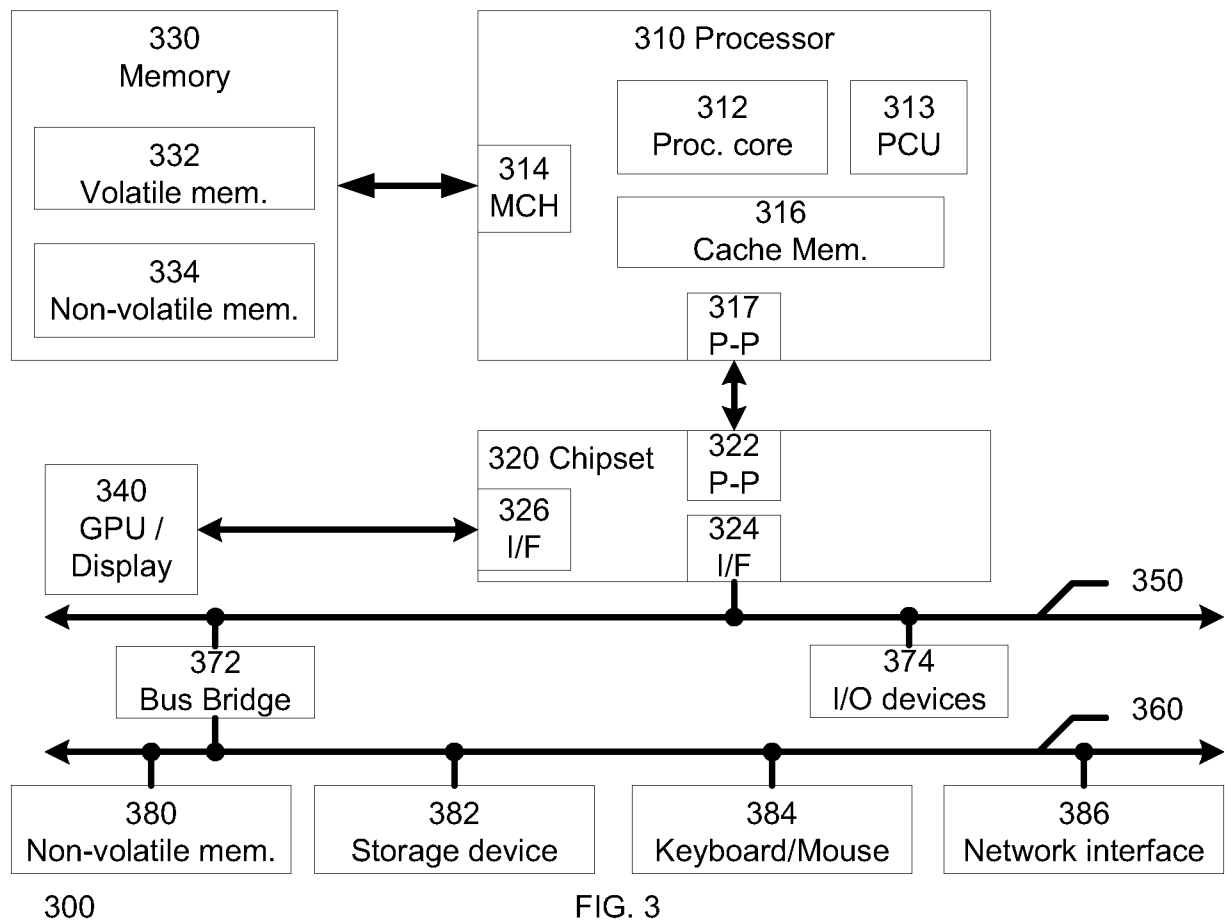
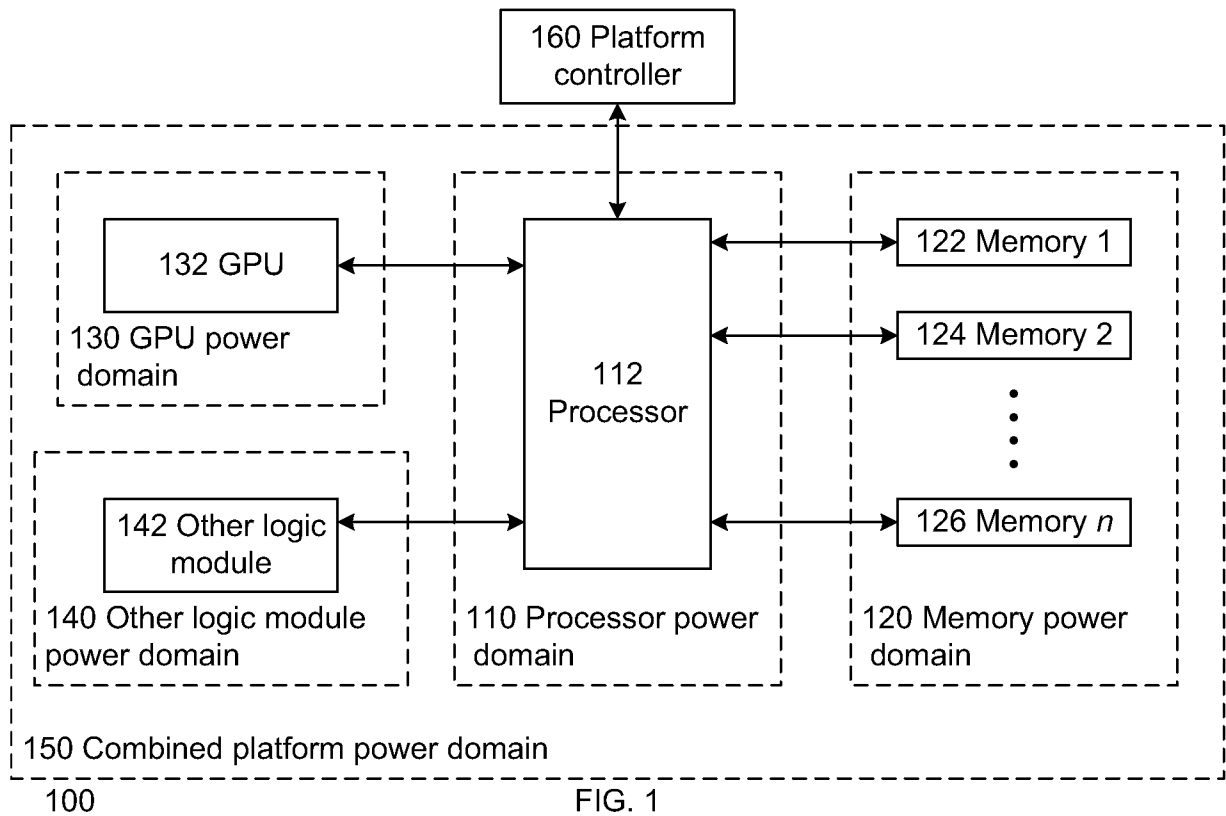
21. The method of claim 20, wherein analyzing the average power consumption of the processor to determine the power limit for the processor comprises performing one or more of, determining number of stall counts of the processor, and determining characteristics of workloads executed by the processor, and wherein analyzing the average power consumption of the logic module to determine the other power limit for the logic module comprises determining bandwidth utilization of the logic module.

22. The method of claim 18, further comprising:
adjusting operations of the processor based on the dynamically set power limit of the processor; and
adjusting operations of the logic module based on the other dynamically set power limit of the logic module.

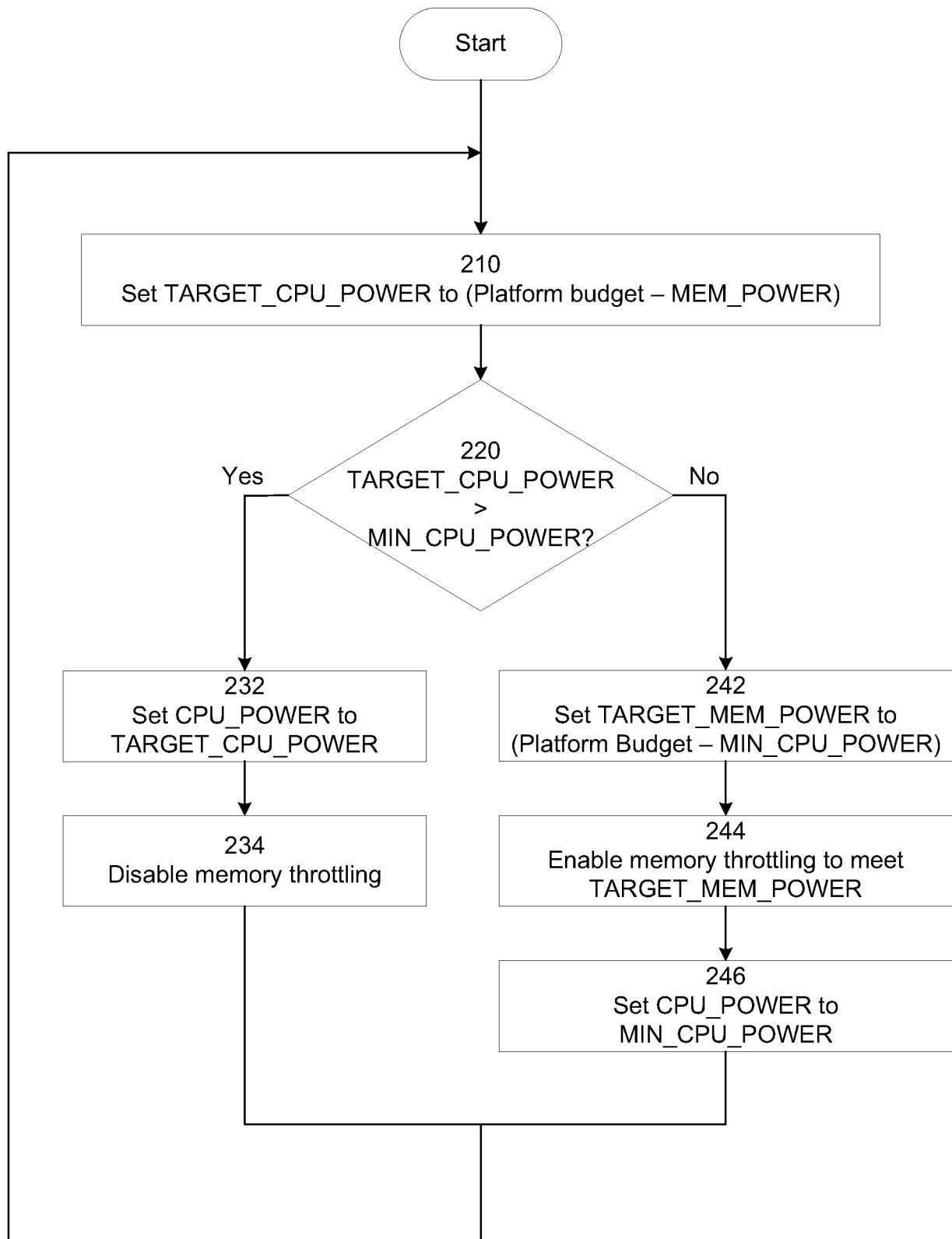
23. The method of claim 18, wherein dynamically setting the power limit for the processor and the other power limit for the logic module based on the power budget for the system comprises:
setting a target processor power as a difference of the power budget and the average power consumption of the logic module; and
determining whether the target processor power is greater than a minimum allowed power consumption of the processor.

24. The method of claim 23, further comprising:
- setting the power limit of the processor as the target processor power in response to a determination that the target processor power is greater than the minimum allowed power consumption of the processor; and
 - disabling any throttling of the logic module.
25. The method of claim 23, wherein in response to a determination that the target processor power is not greater than the minimum allowed power consumption of the processor, the method further comprising:
- setting a target logic module power as a difference of the power budget and the minimum allowed power consumption of the processor;
 - enabling throttling of the logic module to meet the target logic module power;
- and
- setting the power limit of the processor as the minimum allowed power consumption of the processor.
26. The method of claim 18, wherein the logic module comprises one of a memory module, a graphics processor unit (GPU), and a co-processor.

1/2



2/2



200

FIG. 2

A. CLASSIFICATION OF SUBJECT MATTER**G06F 1/32(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/32; G06F 1/26; G06F 1/00; G08C 17/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: platform comprising processor and memory module, power budget, power limit for processor, power limit for memory module

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 8140868 B2 (FELTER WESLEY MICHAEL et al.) 20 March 2012 See abstract, column 5, line 9 - column 6, line 50, claim 1, and figures 1-2.	1, 9, 17, 18, 26 2-8, 10-16, 19-25
A	US 2012-0023351 A1 (WAKRAT NIR J. et al.) 26 January 2012 See abstract, paragraphs [0004]-[0008], [0023]-[0025], [0060]-[0070], and figures 1, 5.	1-26
A	US 7787405 B2 (DETTINGER RICHARD D. et al.) 31 August 2010 See abstract, column 4, lines 32-63, and figure 1.	1-26
A	US 2012-0017099 A1 (DAVID HOWARD S. et al.) 19 January 2012 See abstract, paragraphs [0020]-[0021], and figure 4.	1-26



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search

09 NOVEMBER 2012 (09.11.2012)

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Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan
City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Park Ji Eun

Telephone No. 82-42-481-5696



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/031249

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 8140868 B2	20.03.2012	US 2008-0301475 A1	04.12.2008
US 2012-0023351 A1	26.01.2012	KR 10-2012-0010989 A WO 2012-018605 A1	06.02.2012 09.02.2012
US 7787405 B2	31.08.2010	US 2008-0165714 A1	10.07.2008
US 2012-0017099 A1	19.01.2012	None	