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(54) **Title**: SEMICONDUCTOR POWER DEVICE

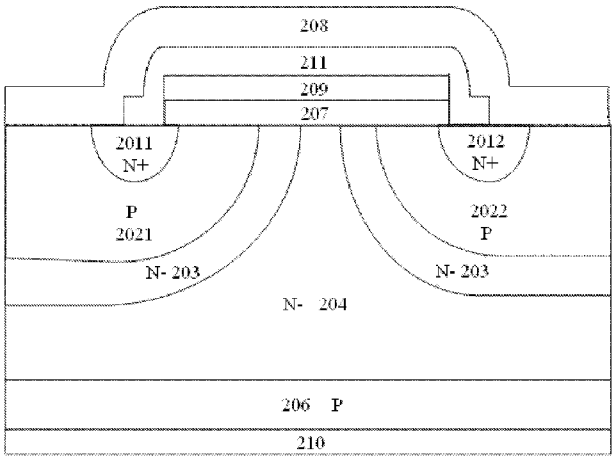

Fig. 2

(57) **Abstract**: A semiconductor power device is provided. The semiconductor power device comprises: a first semiconductor layer (204) of a first conductivity type; a first well region (2021) of a second conductivity type and a second well region (2022) of the second conductivity type; a second semiconductor layer (203) of the first conductivity type, in which a band gap of the second semiconductor layer (203) is greater than that of the first semiconductor layer (204); a first source region (2011) of the first conductivity type and a second source region (2012) of the first conductivity type; a first insulating layer (207); a polysilicon layer (209) formed on the first insulating layer (207); a second insulating layer (211); a first metal layer (208); a third semiconductor layer (206) of the second conductivity type formed below the first semiconductor layer (204); and a second metal layer (210) formed below the third semiconductor layer (206).

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SEMICONDUCTOR POWER DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to and benefits of the following applications:

1) Chinese Patent Application Serial No. 201110110252.6, filed with the State Intellectual Property Office of P. R. China on April 29, 2011; and

2) Chinese Patent Application Serial No. 201210073789.4, filed with the State Intellectual Property Office of P. R. China on March 20, 2012.

The entire contents of the above applications are incorporated herein by reference.

FIELD

The present disclosure belongs to the field of semiconductor, and more particularly relates to a semiconductor power device.

BACKGROUND

High frequency, high voltage resistance and low loss are importance performances of a semiconductor power device. The semiconductor power device has advantages of both a bipolar power device and a MOS type power device and has high frequency, high voltage resistance and low loss. With continuous development of the power electronics industry, the requirements for the performance of the semiconductor power device becomes higher and higher. In order to reduce the on-state voltage drop of the semiconductor power device so as to reduce the on-state loss, a barrier layer is introduced. As shown in Fig. 1, an n-channel insulated gate bipolar transistor (IGBT) comprises a barrier layer 103, a drift region 104, and well regions 102 and 112, in which a doping concentration of the barrier layer 103 is higher than that of the drift region 104. Due to the difference between doping concentrations of the barrier layer 103 and the drift region 104, a potential barrier is formed because of diffusion of majority carriers between the barrier layer 103 and the drift region 104, which may stop minority carriers stored in the barrier layer 103. Therefore, minority carriers may not be easily collected by a reverse-biased well-drift region junction, thus increasing the concentration of carriers near the surface of the device, enhancing the conductance modulating action near the surface of the device, effectively reducing the on-state voltage drop, and reducing the on-state loss. The barrier layer may be commonly formed by

diffusing a dopant identical with a dopant in the drift region on the surface of the entire device or in a selected region to form a doped region with a certain thickness and a high concentration.

However, the conventional method for forming the barrier layer has some defects. Particularly, because the barrier layer is formed by a highly doped region near the surface of the device, when the device is in an off state, a depletion layer of the reverse-biased well-drift region junction is extended. According to the PN junction theory, the higher the doping concentration, the more difficult the extension of the depletion layer is, thus reducing the voltage resistance of the device. One conventional solution is to shorten a space between unit cells, thus shortening the distance between well regions so as to ensure the voltage resistance. However, for the entire device, the number of the unit cells must be increased, thus bringing two following negative influences. On one hand, the increase of the number of the unit cells means the increase of the proportion of the well region area, thus increasing the area where minority carriers are collected, reducing the conductance modulating action, and weakening the function of the barrier layer. On the other hand, the increase of the number of the unit cells may cause the increase of the density of the channel, and because the density of the channel is in direct proportion to the short-circuit current, the increase of the density of the channel means the increase of the short-circuit current, thus weakening the self-current-limiting capability of the device and reducing the robustness of the device.

SUMMARY

Embodiments of the present disclosure seek to solve at least one of the problems existing in the prior art to at least some extent, particularly a problem of the conflict between the on-state loss and the voltage resistance of a conventional semiconductor power device, or to provide a consumer with a useful commercial choice.

According to embodiments of the present disclosure, there is provided a semiconductor power device. The semiconductor power device comprises: a first semiconductor layer of a first conductivity type; a first well region of a second conductivity type and a second well region of the second conductivity type which are formed above the first semiconductor layer; a second semiconductor layer of the first conductivity type formed between the first well region and the first semiconductor layer and between the second well region and the first semiconductor layer, in which a band gap of the second semiconductor layer is greater than that of the first semiconductor

layer; a first source region of the first conductivity type formed in a part of the first well region and a second source region of the first conductivity type formed in a part of the second well region; a first insulating layer formed on the second semiconductor layer and covering a part of the first source region, a part of the second source region, a part of the first well region and a part of the second well region; a polysilicon layer formed on the first insulating layer; a second insulating layer formed on the polysilicon layer and covering the polysilicon layer, a part of the first source region and a part of the second source region; a first metal layer formed on the second insulating layer and covering the second insulating layer, a part of the first source region, a part of the second source region, a part of the first well region and a part of the second well region; a third semiconductor layer of the second conductivity type formed below the first semiconductor layer; and a second metal layer formed below the third semiconductor layer.

With the semiconductor power device according to an embodiment of the present disclosure, because the band gap of the second semiconductor layer is greater than that of the first semiconductor layer, when the doping concentration of the second semiconductor layer is equal to or slightly lower than that of the first semiconductor layer, the energy level of majority carriers is substantially invariable, while the energy level of minority carriers is curved to form a potential barrier for the minority carriers. When the semiconductor power device is turned on, the potential barrier may inhibit the minority carriers diffusing from a drift region to a well region, thus effectively inhibiting the collection of the minority carriers by a well-drift region junction, increasing the concentration of carriers near the surface of the semiconductor power device, reducing the on-state loss, and ensuring that the voltage resistance of the semiconductor power device is not affected.

The above summary of the present disclosure is not intended to describe each disclosed embodiment or every implementation of the present disclosure. The Figures and the detailed description which follow more particularly exemplify illustrative embodiments.

Additional aspects and advantages of embodiments of present disclosure will be given in part in the following descriptions, become apparent in part from the following descriptions, or be learned from the practice of the embodiments of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects and advantages of embodiments of the present disclosure will

become apparent and more readily appreciated from the following descriptions made with reference to the accompanying drawings, in which:

Fig.1 is a cross-sectional view of a conventional n-channel IGBT;

Fig. 2 is a cross-sectional view of an n-channel IGBT according to a first embodiment of the present disclosure;

Fig. 3 is a cross-sectional view of an n-channel IGBT according to a second embodiment of the present disclosure;

Fig. 4 is a first band structure diagram of a barrier layer and a drift region in an n-channel IGBT according to an embodiment of the present disclosure;

Fig. 5 is a second band structure diagram of a barrier layer and a drift region in an n-channel IGBT according to an embodiment of the present disclosure;

Fig. 6 is a first band structure diagram of a barrier layer and a drift region in a p-channel IGBT according to an embodiment of the present disclosure; and

Fig. 7 is a second band structure diagram of a barrier layer and a drift region in a p-channel IGBT according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

Reference will be made in detail to embodiments of the present disclosure. The embodiments described herein with reference to drawings are explanatory, illustrative, and used to generally understand the present disclosure. The embodiments shall not be construed to limit the present disclosure. The same or similar elements and the elements having same or similar functions are denoted by like reference numerals throughout the descriptions.

According to embodiments of the present disclosure, a semiconductor power device is provided. The semiconductor power device comprises: a first semiconductor layer of a first conductivity type; a first well region of a second conductivity type and a second well region of the second conductivity type which are formed above the first semiconductor layer; a second semiconductor layer of the first conductivity type formed between the first well region and the first semiconductor layer and between the second well region and the first semiconductor layer, in which a band gap of the second semiconductor layer is greater than that of the first semiconductor layer; a first source region of the first conductivity type formed in a part of the first well region and a second source region of the first conductivity type formed in a part of the second well region; a

first insulating layer formed on the second semiconductor layer and covering a part of the first source region, a part of the second source region, a part of the first well region and a part of the second well region; a polysilicon layer formed on the first insulating layer; a second insulating layer formed on the polysilicon layer and covering the polysilicon layer, a part of the first source region and a part of the second source region; a first metal layer formed on the second insulating layer and covering the second insulating layer, a part of the first source region, a part of the second source region, a part of the first well region and a part of the second well region; a third semiconductor layer of the second conductivity type formed below the first semiconductor layer; and a second metal layer formed below the third semiconductor layer.

With the semiconductor power device according to an embodiment of the present disclosure, because the band gap of the second semiconductor layer is greater than that of the first semiconductor layer, when the doping concentration of the second semiconductor layer is equal to or slightly lower than that of the first semiconductor layer, the energy level of majority carriers is substantially invariable, while the energy level of minority carriers is curved to form a potential barrier for the minority carriers. When the semiconductor power device is turned on, the potential barrier may inhibit the minority carriers diffusing from a drift region to a well region, thus effectively inhibiting the collection of the minority carriers by a well-drift region junction, increasing the concentration of carriers near the surface of the semiconductor power device, reducing the on-state loss, and ensuring that the voltage resistance of the semiconductor power device is not affected.

The semiconductor power device according to a first embodiment of the present disclosure, i.e., an n-channel IGBT, will be described below with reference to Fig. 2. As shown in Fig. 2, the semiconductor power device comprises a first semiconductor layer 204 of a first conductivity type, and a second semiconductor layer 203 of the first conductivity type formed on the first semiconductor layer 204. The semiconductor power device further comprises a first well region 2021 of a second conductivity type formed in the second semiconductor layer 203 and a second well region 2022 of the second conductivity type spaced apart from the first well region 2021. The second semiconductor layer 203 is formed between the first well region 2021 and the first semiconductor layer 204 and between the second well region 2022 and the first semiconductor layer 204.

The semiconductor power device further comprises a first source region 2011 of the first

conductivity type formed in a part of the first well region 2021 and a second source region 2012 of the first conductivity type formed in a part of the second well region 2022. The semiconductor power device further comprises a first insulating layer 207 formed on the second semiconductor layer 203 and covering a part of the first source region 2011, a part of the second source region 2012, a part of the first well region 2021 and a part of the second well region 2022; a polysilicon layer 209 formed on the first insulating layer 207; a second insulating layer 211 formed on the polysilicon layer 209 and covering the polysilicon layer 209, a part of the first source region 2011 and a part of the second source region 2012; and a first metal layer 208 formed on the second insulating layer 211 and covering the second insulating layer 211, a part of the first source region 2011, a part of the second source region 2012, a part of the first well region 2021 and a part of the second well region 2022.

In one embodiment, a material of the first insulating layer 207 may be silicon dioxide (SiO_2). In one embodiment, a material of the second insulating layer 211 may be borophosphosilicate glass (BPSG), thus stopping outside moistures and impurities from entering into the device.

In one embodiment, the second semiconductor layer 203 surrounds a part of the first well region 2021 and a part of the second well region 2022, and the first semiconductor layer 204 is contacted with the first insulating layer 207. That is, the second semiconductor layer 203 is divided into two portions by the first semiconductor layer 204, the first well region 2021 is formed in one portion of the second semiconductor layer 203, and the second well region 2022 is formed in the other portion of the second semiconductor layer 203.

The semiconductor power device further comprises a third semiconductor layer 206 of the second conductivity type formed below the first semiconductor layer 204, and a second metal layer 210 formed below the third semiconductor layer 206.

In one embodiment, a band gap of the second semiconductor layer 203 is greater than that of the first semiconductor layer 204. In this embodiment, for the semiconductor power device, the third semiconductor layer 206 is used as a collector, the first semiconductor layer 204 is used as a drift region, the second semiconductor layer 203 is used as a barrier layer, the first metal layer 208 is used as an emitter, and the polysilicon layer 209 is used as a gate.

The semiconductor power device according to a second embodiment of the present disclosure, i.e., an n-channel IGBT, will be described below with reference to Fig. 3. As shown in Fig. 3, the semiconductor power device comprises a first semiconductor layer 304 of a first conductivity type;

a second semiconductor layer 303 of the first conductivity type formed on the first semiconductor layer 304; a first well region 3021 of a second conductivity type formed in the second semiconductor layer 303 and a second well region 3022 of the second conductivity type spaced apart from the first well region 3021; a first source region 3011 of the first conductivity type formed in a part of the first well region 3021 and a second source region 3012 of the first conductivity type formed in a part of the second well region 3022; a first insulating layer 307 formed on the second semiconductor layer 303 and covering a part of the first source region 3011, a part of the second source region 3012, a part of the first well region 3021 and a part of the second well region 3022; a polysilicon layer 309 formed on the first insulating layer 307; a second insulating layer 311 formed on the polysilicon layer 309 and covering the polysilicon layer 309, a part of the first source region 3011 and a part of the second source region 3012; a first metal layer 308 formed on the second insulating layer 311 and covering the second insulating layer 311, a part of the first source region 3011, a part of the second source region 3012, a part of the first well region 3021 and a part of the second well region 3022; a third semiconductor layer 306 of the second conductivity type formed below the first semiconductor layer 304; and a second metal layer 310 formed below the third semiconductor layer 306. In one embodiment, a band gap of the second semiconductor layer 303 is greater than that of the first semiconductor layer 304. In this embodiment, for the semiconductor power device, the third semiconductor layer 306 is used as a collector, the first semiconductor layer 304 is used as a drift region, the second semiconductor layer 303 is used as a barrier layer, the first metal layer 308 is used as an emitter, and the polysilicon layer 309 is used as a gate.

The second semiconductor layer 303 surrounds a part of the first well region 3021 and a part of the second well region 3022 and isolates the first semiconductor layer 304 from the first insulating layer 307.

In one embodiment, a doping concentration of the second semiconductor layer is lower than or equal to that of the first semiconductor layer. For example, in the semiconductor power device shown in Fig. 3, a doping concentration of the second semiconductor layer 303 is lower than or equal to that of the first semiconductor layer 304. In one embodiment, a dopant is phosphorus (P).

In another embodiment, the doping concentration of the second semiconductor layer (i.e., a barrier layer) is equal to that of the first semiconductor layer (i.e., a drift region). First and second band structure diagrams of an n-channel IGBT according to an embodiment of the present

disclosure are shown in Figs. 4-5 respectively, in which Ev is a valence band, Ef is a Fermi level, and Ec is a conduction band. As shown in Fig. 4, the conduction band of the barrier layer is substantially collinear with the conduction band of the drift region, while the top of the valence band of the barrier layer is lower than the top of the valance band of the drift region. In this way, electrons in the valence band may easily flow from the barrier layer to the drift region, while minority carriers (i.e., holes) in the drift region may enter into the barrier layer only when exceeding a potential barrier. Therefore, the barrier layer may stop holes from flowing from the first semiconductor layer (i.e., the drift region) to the second semiconductor layer (i.e., a barrier layer), thus effectively inhibiting the collection of the minority carriers (i.e., holes) by a well-drift region junction, increasing the concentration of the minority carriers near the surface of the IGBT, reducing the on-state voltage drop, and reducing the on-state loss of the semiconductor power device.

As shown in Fig. 5, the bottom of the conduction band of the barrier layer is higher than the bottom of the conduction band of the drift region, the Fermi level of the barrier layer is collinear with the Fermi level of the drift region, but electrons still tend to diffuse to the drift region, thus facilitating the increase of the electron current when the semiconductor power device is turned on. Meanwhile, the top of the valence band of the barrier layer is also lower than the top of the valance band of the drift region to form a potential barrier for holes, thus inhibiting the collection of the minority carriers (i.e., holes) by a well-drift region junction when the minority carriers diffuse from the drift region to the barrier layer, effectively increasing the concentration of the minority carriers near the surface of the IGBT, reducing the on-state voltage drop, and reducing the on-state loss of the semiconductor power device. Because the potential barrier for holes is caused by inconsistent band gap and the difference of the energy levels but not caused by carrier diffusion resulted from concentration doping, it is not required that the doping concentration of the barrier layer is higher than that of the drift region, so that the voltage resistance of the device may not be reduced. On the contrary, because the band gap of the semiconductor materials of the barrier layer is greater than that of the semiconductor materials of the drift region, the breakdown electric field of the barrier layer is higher than that of the drift region, so that the voltage resistance of the device is higher. As shown in Fig. 5, the doping concentration of the barrier layer may also be lower than that of the drift region, thus enhancing the voltage resistance of the device.

First and second band structure diagrams of a p-channel IGBT according to an embodiment

of the present disclosure are shown in Figs. 6-7 respectively, in which Ev is a valence band, Ef is a Fermi level, and Ec is a conduction band. Similar to the n-channel IGBT, as shown in Fig. 6, because the valence band of the barrier layer is substantially collinear with the valence band of the drift region, holes may easily move from the barrier layer to the drift region. For electrons, because the bottom of the conduction band of the barrier layer is higher than the bottom of the conduction band of the drift region, electrons in the drift region may enter into the barrier layer only when exceeding a certain potential barrier, that is, the electron affinity energy of the second semiconductor layer is lower than that of the first semiconductor layer. Therefore, electrons may not easily flow from the first semiconductor layer (i.e., the drift region) to the second semiconductor layer (i.e., the barrier layer), thus effectively increasing the concentration of carriers on the surface of the device and reducing the forward direction voltage drop and the loss of the device. As shown in Fig. 7, the top of the valence band of the barrier layer is lower than the top of the valence band of the drift region, the bottom of the conduction band of the barrier layer is higher than the bottom of the conduction band of the drift region, but holes still tend to diffuse from the barrier layer to the drift region, thus facilitating the flow of the hole current. However, electrons in the drift region may enter into the barrier layer only when exceeding a certain potential barrier, thus effectively increasing the concentration of carriers on the surface of the IGBT and reducing the on-state voltage drop and the loss of the device. Similarly, the band gap of the barrier layer is greater than that of the drift region, or the doping concentration of the barrier layer may be lower than that of the drift region, so that the voltage resistance of the device may not be reduced.

In some embodiments, the doping concentration of the second semiconductor layer is about $5e^{12}/cm^3$ to about $1e^{15}/cm^3$, and the doping concentration of the first semiconductor layer is about $5e^{12}/cm^3$ to about $1e^{15}/cm^3$. For example, in the embodiment shown in Fig. 2, the doping concentration of the second semiconductor layer 203 is about $1e^{14}/cm^3$, the doping concentration of the first semiconductor layer 204 is about $1e^{14}/cm^3$, the doping concentration of each of the first source region 2011 and the second source region 2012 is about $2e^{19}/cm^3$, the doping concentration of each of the first well region 2021 and the second well region 2022 is about $1e^{18}/cm^3$, and the doping concentration of the third semiconductor layer 206 is about $5e^{17}/cm^3$.

For example, in the embodiment shown in Fig. 3, the doping concentration of the second semiconductor layer 303 is about $6e^{13}/cm^3$, the doping concentration of the first semiconductor

layer 304 is about $8e^{13}/cm^3$, the doping concentration of each of the first source region 3011 and the second source region 3012 is about $2e^{19}/cm^3$, the doping concentration of each of the first well region 3021 and the second well region 3022 is about $1e^{18}/cm^3$, and the doping concentration of the third semiconductor layer 306 is about $5e^{17}/cm^3$.

In some embodiments, the band gap of the second semiconductor layer is 1eV to 5eV, and the band gap of the first semiconductor layer is 0.1eV to 3eV, thus conveniently selecting suitable semiconductor materials, ensuring that the band gap of the barrier layer is greater than that of the drift region, effectively stopping the collection of the minority carriers by the well-drift region junction, and achieving the technical effect of the present disclosure.

In some embodiments, a material of the second semiconductor layer is at least one selected from the group consisting of silicon (Si), silicon carbide (SiC), aluminum phosphide (AlP), indium phosphide (InP), and aluminum arsenide (AlAs); or may be other semiconductor materials having larger band gap.

In some embodiments, a material of the first semiconductor layer is at least one selected from the group consisting of germanium (Ge), silicon germanide ($Si_{1-x}Ge_x$), and carbon silicon germanide (SiGeC); or may be other semiconductor materials having smaller band gap.

For example, in the semiconductor power device shown in Fig. 2, a material of each of the first semiconductor layer 204 and the third semiconductor layer 206 is $Si_{1-x}Ge_x$; and a material of each of the second semiconductor layer 203, the first well region 2021, the second well region 2022, the first source region 2011 and the second source region 2012 is Si.

In some embodiments, the first conductivity type is N type, and the second conductivity type is P type, particularly see the semiconductor power devices shown in Figs. 2-3. Certainly, it would be appreciated by those skilled in the art that the first conductivity type may be P type, and the second conductivity type may be N type.

Although explanatory embodiments have been shown and described, it would be appreciated by those skilled in the art that the above embodiments can not be construed to limit the present disclosure, and changes, alternatives, and modifications can be made in the embodiments without departing from spirit, principles and scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor power device, comprising:

a first semiconductor layer of a first conductivity type;

a first well region of a second conductivity type and a second well region of the second conductivity type which are formed above the first semiconductor layer;

a second semiconductor layer of the first conductivity type formed between the first well region and the first semiconductor layer and between the second well region and the first semiconductor layer, wherein a band gap of the second semiconductor layer is greater than that of the first semiconductor layer;

a first source region of the first conductivity type formed in a part of the first well region and a second source region of the first conductivity type formed in a part of the second well region;

a first insulating layer formed on the second semiconductor layer and covering a part of the first source region, a part of the second source region, a part of the first well region and a part of the second well region;

a polysilicon layer formed on the first insulating layer;

a second insulating layer formed on the polysilicon layer and covering the polysilicon layer, a part of the first source region and a part of the second source region;

a first metal layer formed on the second insulating layer and covering the second insulating layer, a part of the first source region, a part of the second source region, a part of the first well region and a part of the second well region;

a third semiconductor layer of the second conductivity type formed below the first semiconductor layer; and

a second metal layer formed below the third semiconductor layer.

2. The semiconductor power device according to claim 1, wherein the second semiconductor layer surrounds a part of the first well region and a part of the second well region, and the first semiconductor layer is contacted with the first insulating layer.

3. The semiconductor power device according to claim 1, wherein the second semiconductor layer surrounds a part of the first well region and a part of the second well region and isolates the first semiconductor layer from the first insulating layer.

4. The semiconductor power device according to claim 1, wherein a doping concentration of the second semiconductor layer is lower than or equal to that of the first semiconductor layer.

5. The semiconductor power device according to claim 4, wherein the doping concentration of the second semiconductor layer is about $5e^{12}/cm^3$ to about $1e^{15}/cm^3$, and the doping concentration of the first semiconductor layer is about $5e^{12}/cm^3$ to about $1e^{15}/cm^3$.

6. The semiconductor power device according to claim 4, wherein an electron affinity energy of the second semiconductor layer is lower than that of the first semiconductor layer.

7. The semiconductor power device according to claim 1, wherein the band gap of the second semiconductor layer is 1eV to 5eV, and the band gap of the first semiconductor layer is 0.1eV to 3eV.

8. The semiconductor power device according to claim 1, wherein a material of the second semiconductor layer is at least one selected from a group consisting of silicon, silicon carbide, aluminum phosphide, indium phosphide, and aluminum arsenide.

9. The semiconductor power device according to claim 1, wherein a material of the first semiconductor layer is at least one selected from a group consisting of Ge, $Si_{1-x}Ge_x$, and SiGeC.

10. The semiconductor power device according to any one of claims 1-9, wherein the first conductivity type is N type, and the second conductivity type is P type; or the first conductivity type is P type, and the second conductivity type is N type.

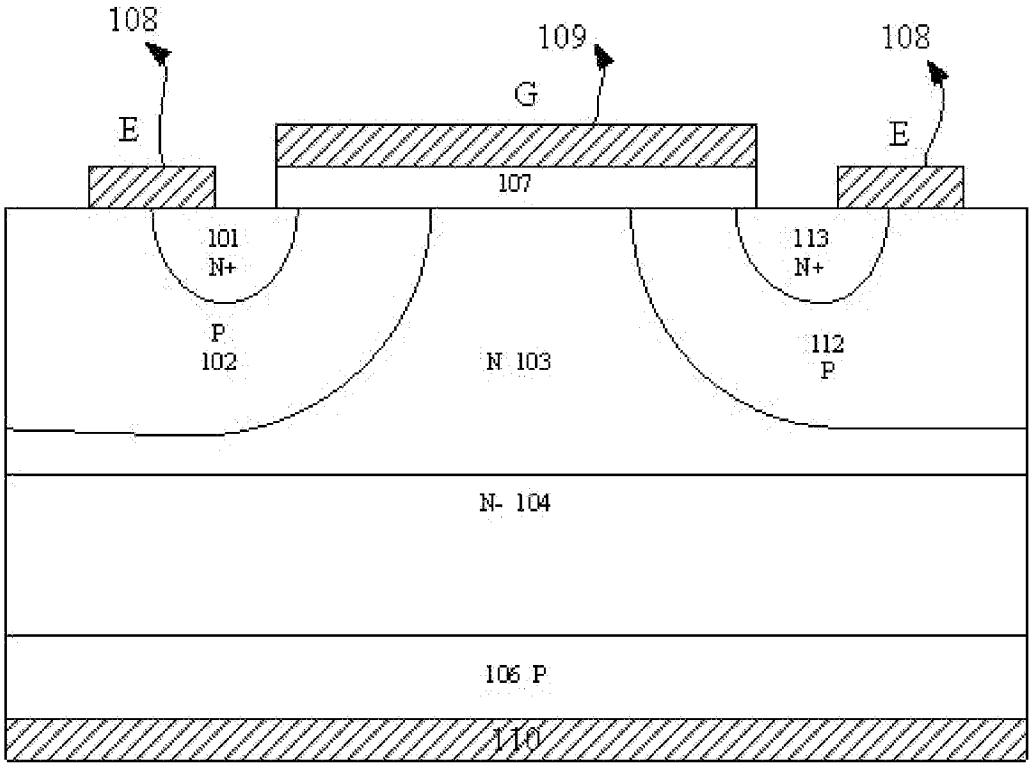
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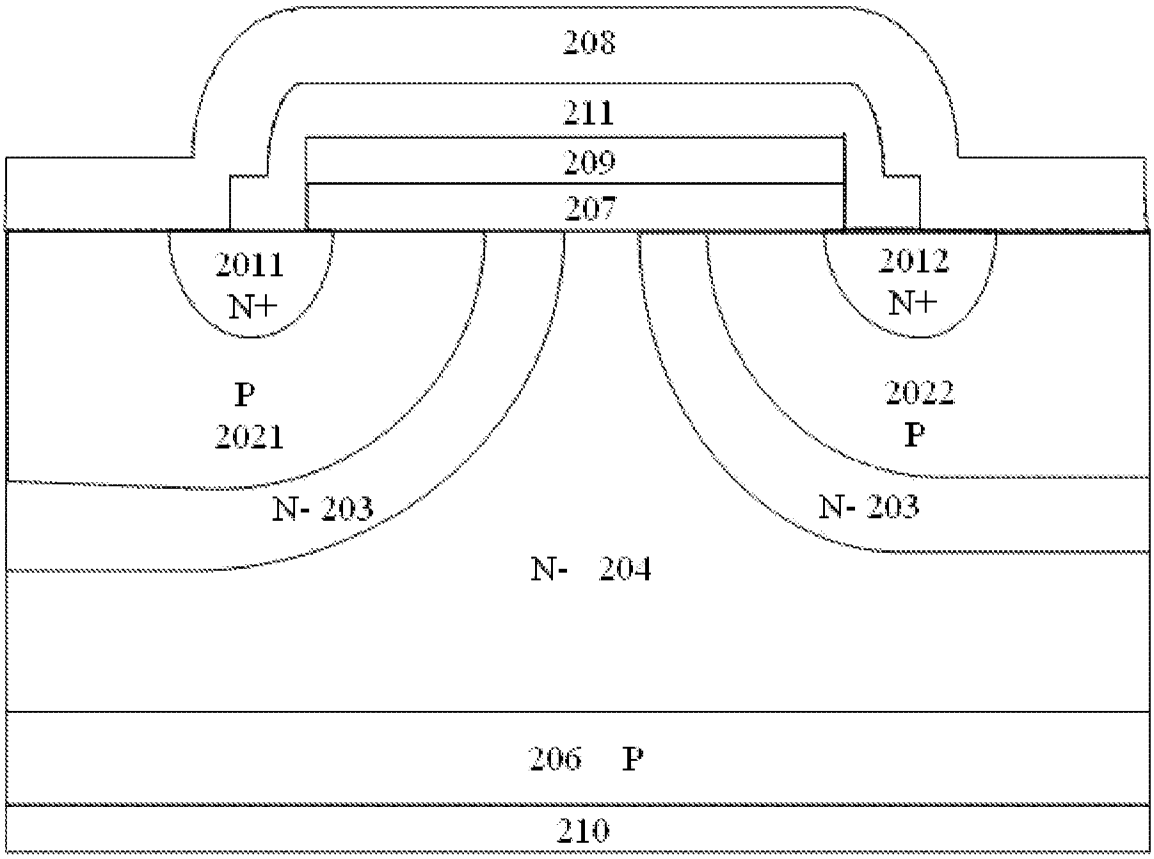
Fig. 1


208
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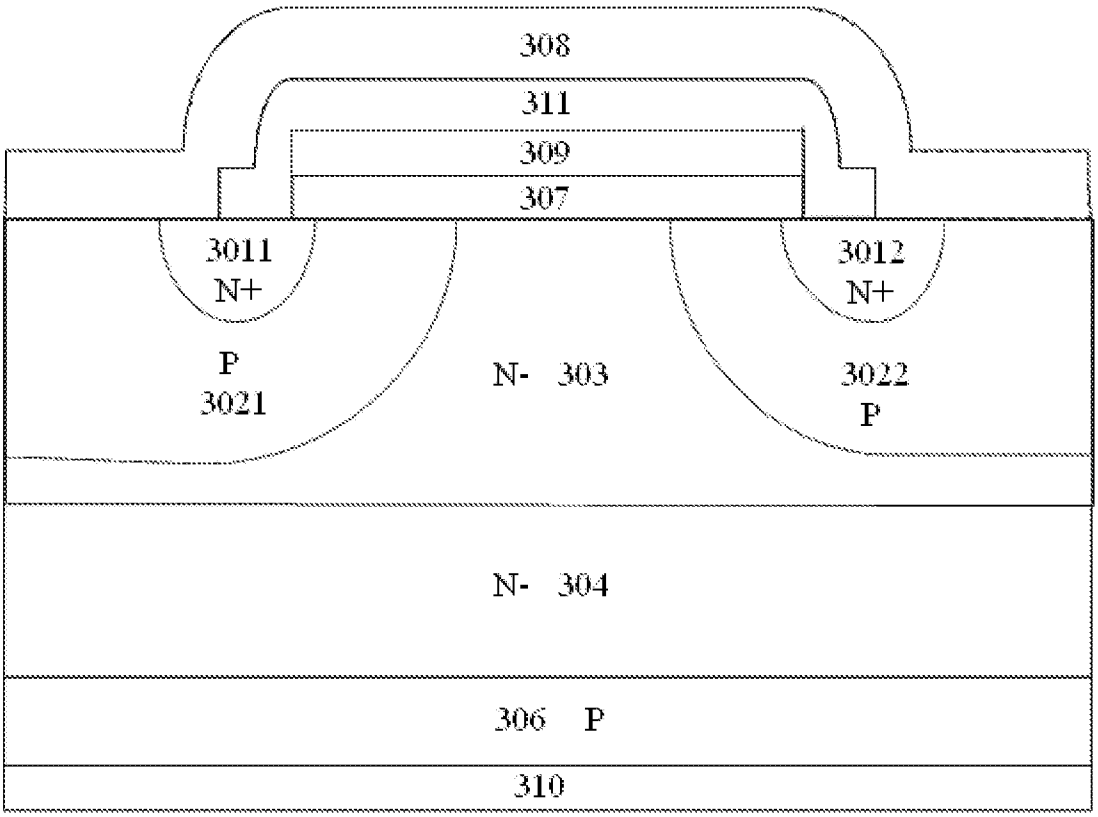
210

Fig. 2


308
311
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3012
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3022
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310

Fig. 3

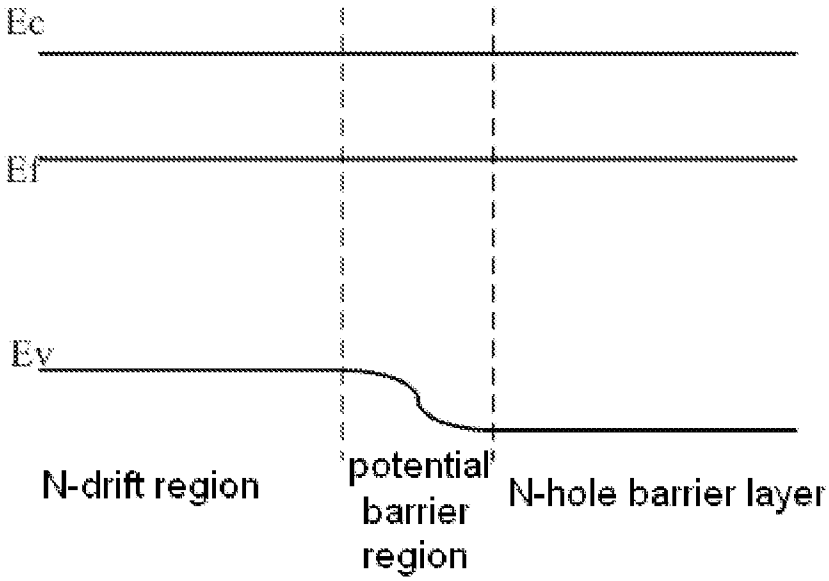
Ec
Ef
Ev
N-drift region
potential barrier region
N-hole barrier layer

Fig. 4

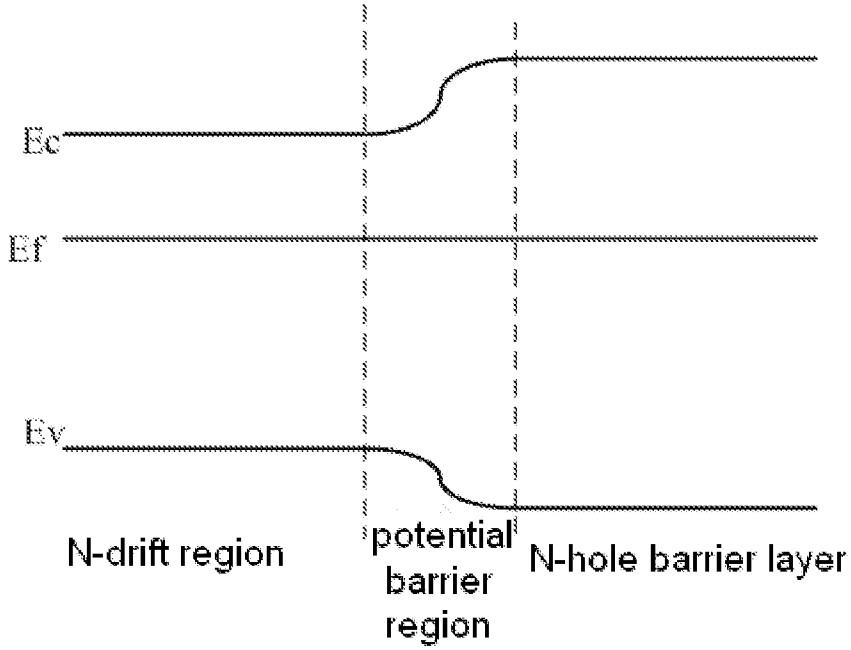
Ec
Ef
Ev
N-drift region
potential barrier region
N-hole barrier layer

Fig. 5

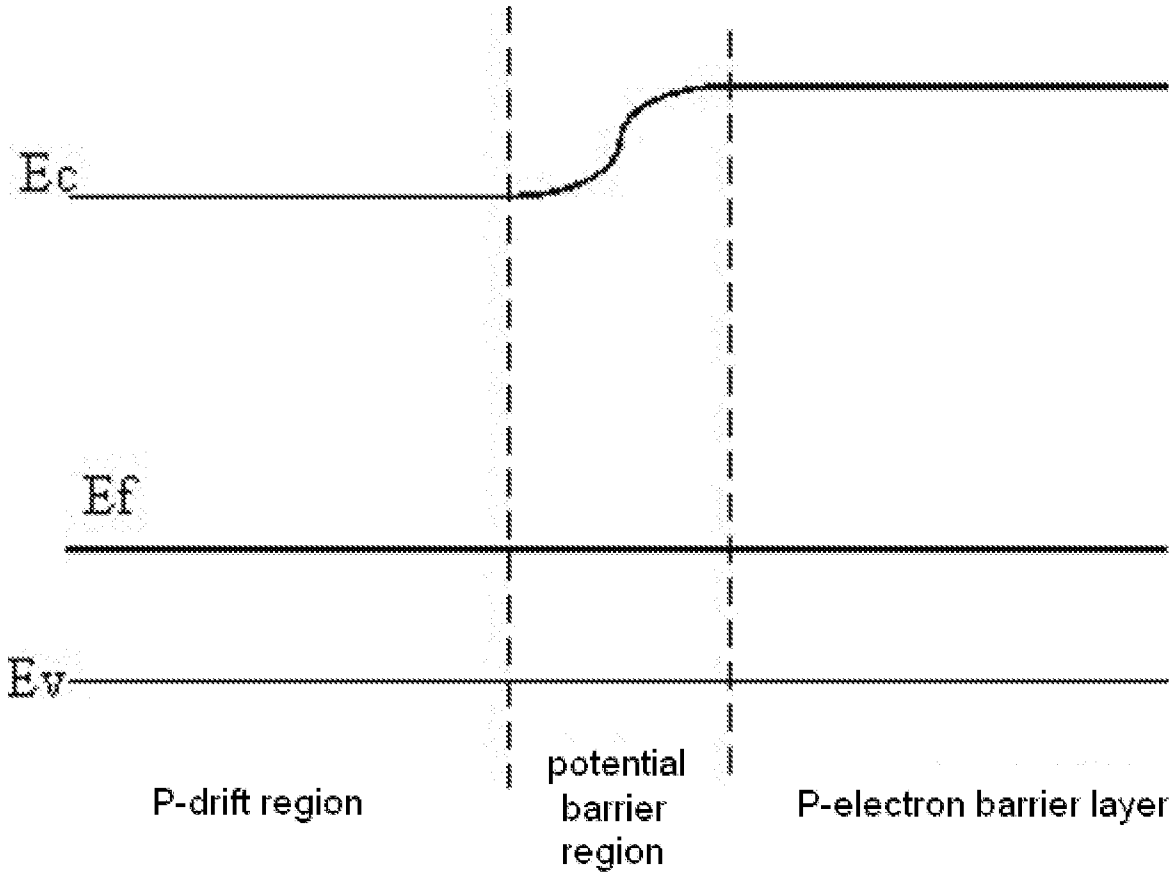
Ec
Ef
Ev
P-drift region
potential barrier region
P-electron barrier layer

Fig. 6

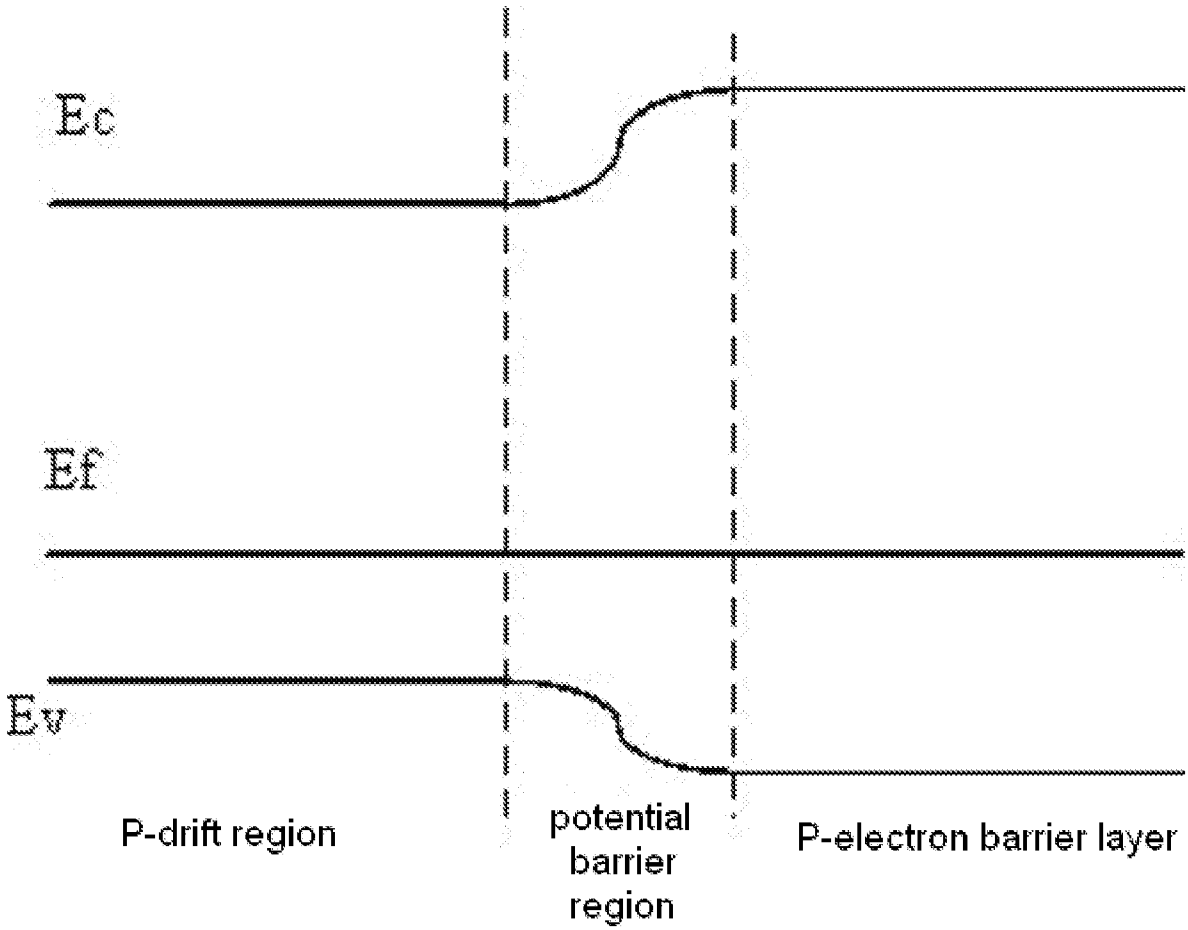
Ec
Ef
Ev
P-drift region
potential barrier region
P-electron barrier layer

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/074782

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L 29/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, CNPAT, CNKI: power, well, barrier, drift, band gap, gate, source, metal, polysilicon

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP7193232A(NISSAN MOTOR CO LTD)28 Jul. 1995(28.07.1995)	1-10
	See paragraphs 0010-0012, figures 1-2	
Y	CN102263127A(BYD Co., Ltd.)30 Nov. 2011(30.11.2011)	1-10
	See paragraphs 0030-0050, figure 5	
A	JP63157478A(NISSAN MOTOR CO LTD)30 Jun. 1988(30.06.1988) the whole document	1-10
A	US2006292805A1(TOSHIBA KK)28 Dec. 2006(28.12.2006) the whole document	1-10
A	US2009072242A1(CREE INC)19 Mar. 2009(19.03.2009) the whole document	1-10

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 Jun. 2012(29.06.2012)	**02 Aug. 2012 (02.08.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer LIU,Guoliang Telephone No. (86-10)62411893

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/074782

Box No. I Nucleotide and/or amino acid sequence(s) (Continuation of item item1.c of the first sheet)

1. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international search was carried out on the basis of:

   a. a sequence listing filed or furnished

      ☒ on paper

      ☐ in electronic form

   b. time of filing or furnishing

      ☐ contained in the applicantion as filed

      ☐ filed together with the application in electronic form

      ☐ furnished subsequently to this Authority for the purposes of search

2. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

3. Additional comments:

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2012/074782

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
JP7193232A	28.07.1995	JP3198766B2	13.08.2001
CN102263127A	30.11.2011	NONE	
JP63157478A	30.06.1988	NONE	
US2006292805A1	28.12.2006	JP2007005723A	11.01.2007
US2009072242A1	19.03.2009	WO2009038610A1	26.03.2009
		US7687825B2	30.03.2010
		EP2198460A1	23.06.2010
		JP2010539728A	16.12.2010

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2012/074782

CLASSIFICATION OF SUBJECT MATTER:

H01L 29/739(2006.01)i

H01L 29/36(2006.01)i