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Description

The invention relates to apparatus for generating a periodic resonant pulse voltage across an inductance. The invention is useful for example in a television deflection apparatus but is not exclusively concerned with that example.

A conventionally built output stage of a television deflection apparatus, includes, in general, three parallel coupled branches. The first branch includes series coupled deflection winding and a trace capacitor forming a trace resonant circuit during trace. The second branch includes a retrace capacitor that forms with the deflection winding a retrace resonant circuit during retrace. The third branch includes a switch that operates to generate trace and retrace deflection currents in the deflection winding.

When the switch is not conductive, energy is transferred, during the first half of the retrace interval, from the deflection winding into the retrace capacitor; in the second half; it is transferred from the retrace capacitor back to the deflection winding.

Energy is transferred during the first half of the trace interval from the deflection winding into the trace capacitor through a damper diode current path of the switch. In the second half of the trace interval, it is transferred from the trace capacitor back to the deflection winding through a bipolar transistor of the switch.

A circuit operating generally as described above is included in the apparatus of GB—A—2119209. Referring to Figure 1 of that document, a deflection winding L_H and trace capacitor C_S are series connected in a first parallel branch of the circuit, retrace capacitor C_{RD} forms a second branch, and transistor Q1 and damper diode D1 form the third branch.

Another known circuit is shown in Siemens-Bautelle-Informationen 9 (1971) No. 5, pages 135 to 140. This document does not disclose the generation of a periodic resonant pulse voltage and does not refer to trace and retrace capacitors. However, it does contain a switching arrangement which conducts currents in a pattern substantially as described above. In the circuit Figure 3 of this prior art document, the switching arrangement comprises the cascade arrangement of common-base transistor BU108 and common-emitter connected transistor TV58. During the second half of the trace period, current flows through the main conduction paths of the two transistors from the collector of BU108 to the emitter of TV58. At the end of the trace interval, transistor TV58 is rendered nonconductive. A brief collector to base current flows in transistor BU108, discharging the base capacitance, and then no current flows through the switching arrangement during the retrace period. However, the switching arrangement of this prior art document does not contain a damper diode. During the first half of the trace period the damping current in the switching arrangement is provided by a reverse collector current from transistor BU108, this current being partly a reverse transistor current flowing in through the emitter, and partly current flowing through the base-to-collector diode. Positive base voltage is provided to the transistor BU108 during the trace period from a 24 V voltage source and a 4 V auxiliary voltage source.

A circuit for generating voltage pulses is shown in L'Onde Electrique September/October 1984, Volume 64, No. 5 pages 21 to 28. The circuit is not resonant, and the pulses are generated in response to a control signal which turns on a switching arrangement.

A switching arrangement illustrated in Figure 2 of this prior art document comprises a cascode arrangement of a common-base connected bipolar transistor and a common-source connected field effect transistor.

According to the invention there is provided apparatus in accordance with claim 1.

In an embodiment of the invention as applied to a television deflection apparatus, the cascode switch arrangement is used to conduct the trace current during the second half of the trace interval. The cascode arrangement may include a first bipolar transistor and a second transistor that may be a majority carrier device such as an MOS field effect transistor (FET).

In carrying out the embodiment the emitter of the first transistor may, for example, be coupled to a main current terminal of the FET, such as the drain electrode. The trace current flows from the collector of the first transistor, through the drain of the FET and into the source of the FET. A switching control voltage is coupled to the gate of the FET for controlling the switching time of the switch. An attribute of the FET is that it enables fast switching that is difficult to achieve with a bipolar transistor coupled in a common emitter arrangement. This attribute of the FET makes the cascode arrangement switch of the invention particularly desirable for usage in a deflection circuit that operates at a high frequency, such as 64 kilohertz. Also, the very high input impedance of the gate permits simple drive circuitry.

During retrace, the switch is nonconductive and the high retrace voltage that is developed across the switch, resulting from the interruption in the trace current of the deflection winding caused by the switch becoming nonconductive, is developed across the base-to-collector junction of the first transistor. An attribute of the first transistor is its high breakdown voltage. Thus, using a low voltage, fast switching transistor, such as an FET, in the emitter of the high voltage first transistor, yields a combined high voltage, high speed cascode switch arrangement.

In operation of the preferred embodiment of the invention, a storage charge is supplied to the base of the first transistor during the first half of trace, when the damper diode of the switch is conductive, but the FET is not. This storage charge turns-on the first transistor. During the second half of trace, when the FET is conductive, the stored charge at the base, that was accumulated during

the first half of trace, maintains the first transistor in a conductive state so that the trace current flows from its collector through its emitter to the drain of the turned-on FET. Because the storage charge is injected to the base region prior to turning-on of the FET, the emitter current in the first transistor immediately follows the turn-on instant of the FET to provide high speed, low power switching operation. When the FET is turned off, at the end of trace, the stored charge in the base region of the first transistor is discharged quickly.

It should be understood that using the cascode switch arrangement of the invention is not limited to deflection circuits. It may be used in other applications where current of pulse producing resonating circuits is switched, such as in a power supply used for generating a high voltage.

Embodiments of the present invention, given by way of non-limiting example, will now be described with reference to the drawings, in which:

Figure 1 illustrates, by way of example, a television deflection circuit output stage and a high voltage power supply embodying an aspect of the invention;

Figures 2a—2h illustrate waveforms useful in explaining the operation of the circuit of Figure 1;

Figure 3 illustrates, by way of example, a deflection circuit output stage and a high voltage power supply embodying another aspect of the invention; and

Figures 4a—4h illustrate waveforms useful in explaining the operation of the circuit of Figure 3.

In the arrangement of Figure 1, a regulated voltage B+, filtered by a capacitor C3, is coupled to an end terminal 40 of a primary winding W1 of a flyback transformer T1. A tap terminal 41, at an intermediate point of winding W1, is coupled to a switch 35 comprising a transistor Q_1 and a damper diode D1. Each of damper diode D1 and retrace capacitor C_r is coupled between terminal 41 and ground, the common conductor.

One end terminal of a parallel arrangement of deflection windings L_{H1} and L_{H2} is coupled to an end terminal 43 of primary winding W1 of transformer T1, forming an autotransformer arrangement. The parallel arrangement of deflection windings L_{H1} and L_{H2} is coupled between terminal 43 and a terminal 46. A parallel arrangement that includes a linearity inductor L1 and a resistor R5 is coupled between terminal 46 and a terminal 47. A trace capacitor C_s is coupled between terminal 47 and ground. Capacitor C_s serves as a source of trace voltage to store energy in the inductance of deflection windings L_{H1} and L_{H2} during the latter portion of trace when switch 35 is conducting.

A zener diode Z1 is coupled from the base of transistor Q1 to ground. A terminal 42 of a secondary winding W3 of transformer T1 is coupled through a diode D2 in series with a current limiting resistor R4 to the base of transistor Q1 for providing a storage charge to the base during the first half of the trace interval, as described later on.

A resistor R3 supplies a small portion of a base current i_b for transistor Q1. Resistor R3 is coupled between a +15V source and the base. Resistor R3 provides base current i_b when deflection circuit 30 is not capable of supplying base current through resistor R4, such as during turn-on or start-up.

The emitter of transistor Q1 is coupled to the drain of an FET Q2 forming a series cascode switching arrangement.

A horizontal rate voltage V_{4fH}, obtained from a timing unit synchronized to the horizontal sync pulses of an incoming composite video signal, not shown in Figure 1, is coupled through a driver circuit 20 to one end terminal of a resistor R2 to develop a switching signal V_g. The other end terminal of resistor R2 is coupled to the gate of FET Q2. The horizontal line deflection frequency is substantially greater than the standard (NTSC) frequency fH=15.75 kilohertz. The line deflection frequency may illustratively be 4fH=63 kilohertz.

A terminal 44 of a secondary winding W4 is coupled through a series arrangement of a resistor R1 and a rectifying diode D3 to a terminal 48 of a capacitor C2. The voltage between terminal 48 and ground is coupled across a voltage divider that includes resistors R6 and R7, to provide a screen voltage S to a CRT that is not shown.

Figures 2a—2h illustrate waveforms useful in explaining the operation of deflection circuit 30 of Figure 1. Similar symbols and numerals in Figures 1 and 2a—2h indicate similar items or functions.

At time t_{br} of Figures 2e and 2h, the beginning of retrace, voltage V_g of Figure 1, that is coupled to the gate of FET Q2, turns off the current path of current i_e flowing from the drain to the source of FET Q2. As, illustrated in Figures 2e and 2d, currents i_e and i_c through the emitter and collector, respectively, of transistor Q1 of Figure 1 drop quickly toward zero immediately after time t_{br}. The sweeping out of charge at the base of transistor Q1 by reverse collector current causes breakdown conduction in zener diode Z1, as illustrated in Figure 2f. Zener diode Z1 remains in breakdown conduction thereafter due to combined effects of current flowing from R3 and the residual reverse collector electrode current. Also, due to reverse breakdown of the base-emitter junction of transistor Q1 of Figure 1, emitter voltage V_e rises abruptly, as illustrated in Figure 2g.

Retrace voltage V_c of Figure 2a is developed across capacitor C_r of Figure 1 as a result of energy transfer from deflection windings L_{H1} and L_{H2} via retrace current i_{df}. Because of the autotransformer arrangement of flyback transformer T1, the retrace voltage at terminal 43 of deflection windings L_{H1} and L_{H2} is higher than voltage V_c. On the other hand, current i_c through the collector of transistor Q1 is higher than deflection current i_{df}. This is so because of the transformer T1 windings ratio arrangement that provides windings turns ratio of $(N_1-N_2)/N_1$, where N_1 equals the number of turns between terminals 40 and 43 and N_2 equal the number of turns of winding section W2,

between tap terminal 41 and terminal 43. This transformer T1 windings ratio arrangement is used for reducing voltage V_c at the collector of transistor Q1 during retrace. This ratio is illustratively 0.64.

At time t_{er}, the end of retrace, capacitor C_r voltage V_c of Figure 2a has completely discharged through deflection windings L_{H1} and L_{H2} and transformer T1 of Figure 1. Damper diode D1 terminates the generation of the resonant pulse voltage V_c and the generation of the resonant pulse voltage developed at terminal 43 of the retrace resonant circuit formed by resonant capacitor C_r and the inductance of deflection windings L_{H1} and L_{H2}. Deflection current i_{df} in deflection windings L_{H1} and L_{H2}, continues to flow through the forward biased diode D1, in the form of current i_{D1} of Figure 2b, and through forward biased zener diode Z1 that is in series with the base-collector junction of transistor Q1, in the form of base current i_b and reverse collector current i_c of Figures 2c and 2d, respectively. Note that the base current waveform illustrated in Figure 2c is the negatively referenced current $-i_b$. Thus when positive current flows into the base of Q1, the current waveform of Figure 2c is below the 0 ampere level.

Zener diode Z1 and transistor Q1 of Figure 1 assist the slow turn-on type diode D1 in conducting deflection trace current i_{df} until a time t_d of Figure 2d. From time t_d, after diode D1 has fully turned-on, until time t_{ht}, diode D1 of Figure 1 conducts the major part of deflection trace current i_{D1}.

Near time t_{ht} of Figures 2a—2h, near the center of trace, each of deflection trace current i_{df} of Figure 1 and current i_{D1} through diode D1 becomes zero. Current begins to flow to the left from tap terminal 41 of flyback transformer primary winding W1.

In accordance with an aspect of the invention, voltage V_s across secondary winding W3 supplies storage charge to the base of transistor Q1 from, approximately, time t_{er}, the beginning of trace, until time t_{br}' of Figure 2a, at the end of trace. This is so because the trace voltage across primary winding W1, causes an induced voltage V_s in secondary winding W3 to be of a positive polarity at terminal 42. Voltage V_s turns on diode D2 to provide positive current i_s in resistor R4 that sums with the small current in resistor R3 to provide positive base current i_b.

Advantageously, the interval in which transistor Q1 is supplied with positive base current overlaps the first half of trace interval t_{er}—t_{ht} in which diode D1 is forward biased and prior to conduction of cascode arranged FET Q2. Also, in output stage 30 of the invention, the base storage charge is capable, by itself, to sustain collector current i_c of Figure 2d between times t_{ht} and t_{br}'. This arrangement avoids the use of a bootstrap capacitor between the base of transistor Q1 and ground to provide forward base to emitter conduction that initiates conventional transistor action. The coupling to the base of transistor Q1 of additional capacitance could undesirably cause trace ringing of the deflection current at the beginning of trace, after time t_{er} of Figure 2, when the base and collector electrodes of Q1 provide a path for damper current.

The amount of current that resistor R4 is required to provide during the trace interval from time t_{er} to time t_{br}' to generate sufficient stored charge in the base region of transistor Q1 is relatively small, less than, for example 250 milliampere, peak. This current is significantly smaller than would otherwise have been required, had the base of bipolar transistor Q1 been driven normally to provide saturated, forward collector-to-emitter conduction of the deflection current of nearly six amperes peak, for example, at the collector electrode.

Furthermore, the current i_s thru resistor R4 may even decrease towards the end of trace, depending on the magnitude of the trace voltage V_s relative to the base voltage V_b. As illustrated in Figures 2f and 2g the emitter voltage V_e and thus the base voltage V_b tends to increase from time t_{ht} to time t_{br}' due to increasing voltage drop across the channel resistance of FET Q2 produced by the increasing deflection current i_{df} flowing therethrough.

At the beginning of trace between time t_{er} and time t_d, before damper diode D1 becomes fully conductive, the negative deflection current i_{df} flows from ground thru zener diode Z1 into the base electrode and out of the collector electrode, providing an additional mechanism for storing charge in the base region of Q1. After time t_d until time t_{ht}, positive base electrode current still flows, obtained from resistors R3 and R4 and from the forward biased zener diode Z1 acting as a conventional diode. This result follows due to the negative voltage being developed at the collector electrode by the forward biased damper diode D1. The positive base current flowing between time t_d and time t_{ht} is relatively small and is not illustrated in Figure 2c on the current scale used.

The charge stored in the base region of transistor Q2 between times t_{er} and t_{ht} is sufficient by itself to maintain forward collector current i_c of Figure 2d during the later interval t_{ht} to t_{br}'.

During the interval t_{er} to t_{ht}, the base-collector PN junction is forward biased, producing a reverse transistor action at the emitter that generates a small negative, emitter to collector current, as illustrated in Figure 2e between time t_d and time t_{ht}. The emitter current flows from ground through the internal, oppositely poled diode, that exists in FET Q2.

At a predetermined time t_{Q2} between time t_{er} and t_{ht} of Figures 2a—2h, FET Q2 of Figure 1 is turned on by gate voltage V_g. When deflection trace current i_{df} reverses its polarity, near time t_{ht} of Figures 2b and 2d, the stored charge at the base region of transistor Q1, as supplemented slightly by the currents through resistors R4 and R3, causes that current i_{df} of Figure 1 flow through the collector of transistor Q1 in the form of forward collector current i_c of Figure 2d. Current i_c

also flows through the emitter in the form of forward emitter current i_e of Figure 2e. Because of the finite channel resistance of FET Q2 of Figure 1, both voltage V_e of Figure 2g and voltage V_b of Figure 2f increase as current i_e of Figure 2e increases from time t_{ht} to time t_{br}'. At time t_{br}', that is equivalent to time t_{br}, at the beginning of retrace, FET Q2 of Figure 1 is turned off, as described before.

In accordance with another aspect of the invention, a power supply 31 generates an ultor voltage U by rectifying the voltage at a secondary winding W2' of a high voltage flyback type of transformer T2. Power supply 31 includes a switched mode power supply 130 that is constructed similarly to deflection circuit 30 except that deflection windings L_{H1} and L_{H2} and their branch elements are omitted. Transformer T2 is analogous to flyback transformer T1 of deflection circuit 30. The inductance of transformer T2 then provides substantially the entire inductance that resonates with the resonating capacitance in power supply 130 to generate the narrow pulse voltage V_r, repeating at the 4fH rate.

Figure 3 illustrates a deflection circuit output stage 30'' embodying another aspect of the invention. Similar numbers and symbols in Figures 1 and 3 depict similar items or functions. Figures 4a—4h illustrate waveforms useful in explaining the operation of output stage 30'' of Figure 3, including a controllable switching arrangement 35'' similar to controllable switching arrangement 35 of Figure 1. Figures 4a—4h are analogous to Figures 2a—2h, respectively. Similar numbers and symbols in Figures 2a—2h and 4a—4h illustrate items or functions. Output stage 30'' of Figure 3, is similar to output stage 30 of Figure 1 except for the exceptions noted below.

The drain-source channel of a FET Q3 of Figure 3 is coupled between the base of transistor Q1 and ground. An inverter 27 provides a drive voltage to the gate of FET Q3 that is inverted from voltage V_g supplied to the gate of FET Q2. Thus, FET Q3 of Figure 3 is conductive when FET Q2 of Figure 3 is nonconductive, and vice versa.

From time t_{er} of Figures 4a—4h, and until time t_{Q2}, voltage V_b, at the base of transistor Q1 of Figure 3, is approximately zero because of the low channel resistance of FET Q3 that is turned-on. With FET Q3 turned-on, the voltage across the forward biased base-collector PN junction of transistor Q1 is approximately the same as the voltage across diode D1. Current $-i_b$ or i_e of Figures 4c and 4d, respectively, provides a current path for deflection current i_{df} that is in parallel to that through diode D1.

Because the voltage across the forward biased base-collector PN junction of transistor Q1 and across the forward bias PN junction of diode D1 is substantially the same, the switching time of the current through both immediately after time t_{er} of Figure 4a—4h is advantageously faster than if damper action is substantially provided by only one PN junction. Thus, power losses in switch 35'' of Figure 3 are lower than if damper action is substantially provided by only one PN junction. The forward biased base-collector PN junction of transistor Q1 causes that additional base charge is stored during the damper action.

At time T_{Q2} of Figures 4a—4h, FET Q3 of Figure 3 is turned off. When forward collector current commences at time t_{ht}, the charge already stored in the base region of transistor Q1 is trapped, since as indicated in Figure 4c, after time t_{Q2}, no significant base electrode current flows in transistor Q1. The base electrode current flowing when forward collector-to-emitter current flows, is insufficient, by itself, to maintain transistor Q1 in a saturated state during the later portion of conduction of FET Q2. However, the stored charge in the base region is capable of sustaining collector current i_c of Figure 4d after time t_{ht}, and of maintaining transistor Q1 of Figure 3 in a saturated, or closed, without the need for additional positive base current. Advantageously, the arrangement of winding W3, diode D2 and resistor R4, used in deflection circuit 30 of Figure 1 to provide base current is eliminated from deflection circuit 30'' of Figure 3.

Claims

1. An apparatus for generating a periodic resonant pulse voltage across an inductance, comprising:

a resonating capacitance (Cr) coupled to said inductance;

a controllable switching arrangement causing current to flow in said inductance (L_{H1}, L_{H2}); and

a source (20) of a periodic switching signal coupled to said controllable switching arrangement, each cycle of said switching signal including a turn-on portion and a turn-off portion, the initiation of said turn-off portion making said controllable switching arrangement nonconductive to enable said inductance (L_{H1}, L_{H2}) and resonating capacitance (Cr) to form a resonant circuit that generates a resonant pulse voltage at a terminal (41) of said resonant circuit during a first interval, said controllable switching arrangement providing a damper action that terminates the generation of said resonant pulse voltage at the end of said first interval, prior to the initiation of the turn-on portion of said switching signal;

characterized in that

said controlled switching arrangement includes first (Q1) and second (Q2) switching means coupled together in a series cascode arrangement, said source (20) of a periodic switching signal being coupled to said second switching means (Q2) and the initiation of said signal turn-off portion making said second switching means (Q2) nonconductive,

and further characterized by

means (T1, D2; Q3, D4) for supplying a control current to a control electrode (base) of said first switching means (Q1) during the occurrence of said damper action to enable said first switching means (Q1) to conduct current from said induc-

tance (L_{H1}, L_{H2}) during conduction of said second switching means (Q2).

2. Apparatus according to claim 1 having a source (B+) of first voltage, said cascode arrangement applying said first voltage (B+) to said inductance (L_{H1}, L_{H2}) for storing energy therein; and

means (the charge storage of Q1) coupled to the control electrode (base) of said first switching means (Q1) for storing charge during the time in which said controllable switching arrangement provides said damper action.

3. Apparatus according to claim 1 or claim 2 in which the first switching means (Q1) comprises a transistor and in which said supply of control current stores charge in the transistor during the time in which the controllable switching arrangement provides said damper action.

4. Apparatus according to any one of the preceding claims in which the second switching means (Q2) comprises a field effect transistor.

5. Apparatus according to any one of the preceding claims in which the first switching means (Q1) comprises a bipolar transistor and said control electrode comprises the base of the bipolar transistor.

6. Apparatus according to claim 5 in which the current which the first switching means (Q1) is enabled to conduct by said supply of a control current comprises forward collector current of said bipolar transistor.

7. Apparatus according to claim 5 or claim 6 in which said supply of control current stores charge on the base of said bipolar transistor (Q1) sufficient to maintain said bipolar transistor in a conductive state throughout said turn-on portion of said switching signal.

8. Apparatus according to any of claims 5 to 7 in which the base electrode current flowing in said bipolar transistor (Q1), during the flow of said current enabled by said supply of control current, is insufficient to maintain said transistor (Q1) in a saturated state during the later portion of conduction of said second switching means (Q2).

9. Apparatus according to any of claims 5 to 8 in which the base-collector junction of said bipolar transistor (Q1) is capable of conducting a portion of the controllable switch current to provide at least a part of said damper action.

10. Apparatus according to any of claims 5 to 9 in which said controllable switching arrangement includes a rectifier (D1) and in which a third switching means (Q3) couples a PN junction (collector-base) of said bipolar transistor (Q1) across said rectifier (D1) such that the voltage across said rectifier (D1) and said PN junction is substantially the same and wherein each of said PN junction (collector-base) and rectifier (D1) is conductive to provide said damper action.

11. Apparatus according to any of claims 1 to 9 in which said control current supplying means comprises a transformer (T1) which is coupled to said inductance (L_{H1}, L_{H2}) for supplying said control current from a terminal (42) of said transformer.

12. Apparatus according to claim 11 in which said control current supplying means further comprises a rectifier (D2) which couples said terminal (42) of said transformer (T1) to said control electrode (base of Q1), for conducting said control current during the occurrence of said damper action.

13. Apparatus according to any one of claims 1 to 9 in which said control current supplying means includes a third switching means (Q3) which is coupled to the control electrode of said first switching means (Q1) for supplying said control current to said control electrode.

14. Apparatus according to claim 13 in which the third switching means (Q3) conducts the control current from said inductance (L_{H1}, L_{H2}).

15. Apparatus according to any one of claims 1 to 9 and 11 to 14 in which said controllable switching arrangement further comprises a rectifier (D1) which conducts to provide at least a part of said damper action.

16. Apparatus according to any one of the preceding claims for generating a deflection current in a deflection winding in which:

said resonating capacitance is a retrace capacitance (Cr), and said inductance is a deflection winding (L_{H1}, L_{H2});

said controllable switching arrangement when conductive generates the trace deflection current;

said first interval is a retrace interval; and

said current which said first switching means (Q1) is enabled to conduct by said supply of a control current is said deflection current during the latter portion of trace.

17. Apparatus according to any one of the preceding claims in which said first switching means (Q1) is in a conductive state immediately prior to the initiation of the turn-on portion of said switching signal.

18. Apparatus according to any one of the preceding claims further comprising a resistor (R3) for coupling a second voltage (+15V) to said control electrode (base) of said first switching means (Q1) that supplies a voltage thereto to start-up the operation of said apparatus.

19. Apparatus according to any one of the preceding claims further comprising a zener diode (Z1) coupled to said control electrode of said first switching means (Q1).

Patentansprüche

1. Vorrichtung zur Erzeugung einer periodischen Resonanzimpulsspannung über einer Induktivität mit

einer mit der Induktivität gekoppelten Resonanzkapazität (Cr),

einer steuerbaren Schalteranordnung, die einen Strom in der Induktivität (L_{H1}, L_{H2}) fließen läßt, und

einer mit der steuerbaren Schalteranordnung gekoppelte Quelle (20) eines periodischen Schaltsignals, von dem jeder Zyklus einen Einschaltabschnitt und einen Ausschaltabschnitt enthält, wobei der Beginn des Ausschaltabschnittes die

steuerbare Schalteranordnung sperrt, so daß die Induktivität (L_{H1}, L_{H2}) und die Resonanzkapazität (Cr) einen Resonanzkreis bilden, der während eines ersten Intervalls an einem Anschluß (41) des Resonanzkreises eine Resonanzimpulsspannung erzeugt, und wobei die steuerbare Schalteranordnung für eine Dämpfungswirkung sorgt, welche die Erzeugung der Resonanzimpulsspannung am Schluß des ersten Intervalls vor Beginn des Einschaltabschnittes des Schaltsignals beendet,

dadurch gekennzeichnet,

daß die gesteuerte Schalteranordnung ein erstes (Q1) und ein zweites (Q2) Schalterelement enthält, die zu einer Reihenkaskodeschaltung zusammengeschaltet sind und das zweite Schalterelement (Q2) mit der Quelle (20) des periodischen Schaltsignals gekoppelt ist und zu Beginn von dessen Einschaltabschnitt gesperrt wird,

und daß einer Steuerelektrode (Basis) des ersten Schalterelementes (Q1) während des Vorhandenseins der Dämpfungswirkung ein Steuerstrom von einer Einrichtung (T1, D2; Q3, D4) zugeführt wird, um das erste Schalterelement (Q1) während des Leitens des zweiten Schalterelementes (Q2) Strom von der Induktivität (L_{H1}, L_{H2}) leiten zu lassen.

2. Anordnung nach Anspruch 1 mit einer Quelle (B+) einer ersten Spannung, bei welcher die Kaskodeschaltung die erste Spannung (B+) der Induktivität (L_{H1}, L_{H2}) zur Energiespeicherung zuführt, und mit mit der Steuerelektrode (Basis) des ersten Schalterelementes (Q1) gekoppelten Mitteln (die Ladungsspeicherung von Q1) zur Speicherung von Ladung während der Zeit, in welcher die steuerbare Schalteranordnung die Dämpfungswirkung ausübt.

3. Anordnung nach Anspruch 1 oder 2, bei welcher das erste Schalterelement (Q1) einen Transistor aufweist und bei welcher durch die Steuerstromzuführung während der Zeit, in welcher die steuerbare Schalteranordnung die Dämpfungswirkung ausübt, Ladung in den Transistor gespeichert wird.

4. Anordnung nach einem der vorstehenden Ansprüche, bei welcher das zweite Schalterelement (Q2) einen Feldeffekttransistor aufweist.

5. Anordnung nach einem der vorstehenden Ansprüche, bei welcher das erste Schalterelement (Q1) einen Bipolartransistor umfaßt und die Steuerelektrode dessen Basis ist.

6. Anordnung nach Anspruch 5, bei welcher der Strom, zu dessen Leitung das erste Schalterelement (Q1) durch Zuführung eines Steuerstroms in die Lage versetzt wird, den Vorwärtsleitungs-Kollektorstrom des Bipolartransistors umfaßt.

7. Anordnung nach Anspruch 5 oder 6, bei welcher durch die Steuerstromzuführung in der Basis des Bipolartransistors (Q1) genügend Ladung gespeichert wird, um den Bipolartransistor über den Einschaltabschnitt des Schaltsignales in einem Leitungszustand zu halten.

8. Anordnung nach einem der Ansprüche 5 bis 7, bei welcher der Basisstrom, der in den Bipolartransistor (Q1) während des durch die Zuführung des Steuerstroms ermöglichten Stromes fließt, ungenügend ist, um den Transistor (Q1) während des späteren Abschnittes des Leitens des zweiten Schalterelementes (Q2) im Sättigungszutstand zu halten.

9. Anordnung nach einem der Ansprüche 5 bis 8, bei welcher der Basis-Kollektor-Übergang des Bipolartransistors (Q1) in der Lage ist, einen Teil des Stroms des steuerbaren Schalters zu führen, um mindestens einen Teil der Dämpfungswirkung zu erbringen.

10. Anordnung nach einem der Ansprüche 5 bis 9, bei welcher die steuerbare Schalteranordnung einen Gleichrichter (D1) enthält und bei welcher ein drittes Schalterelement (Q3) einen PN-Übergang (Kollektor-Basis-Übergang) des Bipolartransistors (Q1) über den Gleichrichter (D1) schaltet derart, daß die Spannung über den Gleichrichter (D1) und dem PN-Übergang im wesentlichen die gleiche ist, und bei welcher sowohl der PN-Übergang (Kollektor-Basis-Übergang) als auch der Gleichrichter (D1) leiten, um die Dämpfungswirkung zu ergeben.

11. Anordnung nach einem der Ansprüche 1 bis 9, bei welcher die Steuerstromquelle einen Transformator (T1) aufweist, welcher mit der Induktivität (L_{H1}, L_{H2}) gekoppelt ist, um den Steuerstrom von einem Anschluß (42) des Transformators zu liefern.

12. Anordnung nach Anspruch 11, bei welcher die Steuerstromquelle weiterhin einen Gleichrichter (D2) aufweist, welcher den Anschluß (42) des Transformators (T1) mit der Steuerelektrode (Basis von Q1) koppelt, um den Steuerstrom während des Vorhandenseins der Dämpfungswirkung zu leiten.

13. Anordnung nach einem der Ansprüche 1 bis 9, bei welcher die Steuerstromquelle ein drittes Schalterelement (Q3) enthält, das mit der Steuerelektrode des ersten Schalterelementes (Q1) gekoppelt ist, um dieser den Steuerstrom zuzuführen.

14. Anordnung nach Anspruch 13, bei welcher das dritte Schalterelement (Q3) den Steuerstrom von der Induktivität (L_{H1}, L_{H2}) leitet.

15. Anordnung nach einem der Ansprüche 1 bis 9 und 11 bis 14, bei welcher die steuerbare Schalteranordnung ferner einen Gleichrichter (D1) aufweist, welcher zur Ausübung mindestens eines Teils der Dämpfungswirkung leitet.

16. Anordnung nach einem der vorstehenden Ansprüche zur Erzeugung eines Ablenkstroms in einer Ablenkwicklung, bei welcher

die Resonanzkapazität eine Rücklaufkapazität (Cr) und die Induktivität eine Ablenkwicklung (L_{H1}, L_{H2}) ist,

die steuerbare Schalteranordnung im Leitungszustand den Hinlaufablenkstrom erzeugt,

das erste Intervall das Rücklaufintervall ist,

und der Strom, der in dem ersten Schalterelement (Q1) durch die Zuführung eines Steuerstroms zum Leiten gebracht wird, der Ablenkstrom während des letzten Hinlaufabschnittes ist.

17. Anordnung nach einem der vorstehenden Ansprüche, bei welcher das erste Schalterele-

ment (Q1) unmittelbar vor Beginn des Einschaltabschnittes des Schaltsignals sich in einem Leitungszustand befindet.

18. Anordnung nach einem der vorstehenden Ansprüche mit weiterhin einem Widerstand (R3) zur Kopplung einer zweiten Spannung (+15V) an die Steuerelektrode (Basis) des ersten Schalterelementes (Q1), um dieser eine Anlaufspannung für den Betrieb der Anordnung zuzuführen.

19. Anordnung nach einem der vorstehenden Ansprüche, ferner mit einer an die Steuerelektrode des ersten Schalterelementes (Q1) angeschlossenen Zenerdiode (Z1).

Revendications

1. Un dispositif pour produire une tension impulsionnelle résonnante périodique à travers une inductance, comprenant:

un condensateur résonnant (Cr) couplé à ladite inductance;

un angencement de commutation contrôlable amenant du courant à circuler dans ladite inductance (L_{H1}, L_{H2}); et

une source (20) d'un signal de commutation périodique couplée audit agencement de commutation contrôlable, chaque cycle dudit signal de commutation comprenant une portion de mise en service et une portion de mise hors service, l'initialisation de ladite portion de mise hors service rendant l'agencement de commutation contrôlable non conducteur pour permettre à ladite inductance (L_{H1}, L_{H2}) et au condensateur résonnant (Cr) de former un circuit résonnant qui produit une tension impulsionnelle résonnante à une borne (41) dudit circuit résonnant pendant un premier intervalle, ledit agencement de commutation contrôlable produisant une action d'amortissement qui termine la production de la tension impulsionnelle résonnante à la fin dudit premier intervalle, avant l'initialisation de la portion de mise en service dudit signal de commutation;

caractérisé en ce que

ledit agencement de commutation contrôlé comprend des premier (Q1) et second (Q2) moyens de commutation couplés ensemble dans un agencement en cascade en série, ladite source (20) d'un signal de commutation périodique étant couplée audit second moyen de commutation (Q2) et l'initialisation de ladite portion de mise hors service du signal rendant le second moyen de commutation (Q2) non conducteur,

et caractérisé de plus par

un moyen (T1, D2; Q3, D4) pour appliquer un courant de commande à une électrode de commande (base) dudit premier moyen de commutation (Q1) pendant l'apparition de ladite action d'amortissement pour permettre au premier moyen de commutation (Q1) à conduire du courant de ladite inductance (L_{H1}, L_{H2}) pendant la conduction dudit second moyen de commutation (Q2).

2. Dispositif selon la revendication 1 ayant une source (B+) de première tension, l'agencement en cascade précité appliquant ladite première tension (B+) à l'inductance précitée (L_{H1}, L_{H2}) pour y stocker de l'énergie; et

un moyen (le stockage de charge de Q1) couplé à l'électrode de commande (base) du premier moyen de commutation précité (Q1) pour stocker de la charge pendant le temps dans lequel l'agencement de commutation contrôlable précité produit l'action d'amortissement précitée.

3. Dispositif selon la revendication 1 ou la revendication 2 dans lequel le premier moyen de commutation (Q1) comprend un transistor et dans lequel l'application précitée du courant de commande stocke de la charge dans le transistor pendant le temps dans lequel l'agencement de commutation contrôlable produit l'action d'amortissement précitée.

4. Dispositif selon l'une des revendications précédentes dans lequel le second moyen de commutation (Q2) comprend un transistor à effet de champ.

5. Dispositif selon l'une des revendications précédentes dans lequel le premier moyen de commutation (Q1) comprend un transistor bipolaire et l'électrode de commande précitée comprend la base du transistor bipolaire.

6. Dispositif selon la revendication 5 dans lequel le courant qui permet au premier moyen de commutation (Q1) de conduire par l'application précitée d'un courant de commande comprend un courant à collecteur en direct du transistor bipolaire précité.

7. Dispositif selon la revendication 5 ou la revendication 6 dans lequel l'application précitée du courant de commande stocke de la charge sur la base du transistor bipolaire précité (Q1) suffisante pour maintenir le transistor bipolaire à un état conducteur pendant la portion de mise en service du signal de commutation précité.

8. Dispositif selon l'une des revendications 5 à 7 dans lequel le courant d'électrode de base circulant dans le transistor bipolaire précité (Q1), pendant la circulation dudit courant permise par l'application précitée du courant de commande, est insuffisant pour maintenir ledit transistor (Q1) dans un état saturé pendant la dernière partie de conduction du second moyen de commutation précité (Q2).

9. Dispositif selon l'une des revendications 5 à 8 dans lequel la jonction base-collecteur du transistor bipolaire précité (Q1) est susceptible de conduire une portion du courant de commutation contrôlable pour produire au moins une partie de l'action d'amortissement précitée.

10. Dispositif selon l'une des revendications 5 à 9 dans lequel l'agencement de commutation contrôlable comprend un redresseur (D1) et dans lequel un troisième moyen de commutation (Q3) couple une jonction PN (collecteur-base) du transistor bipolaire précité (Q1) à travers le redresseur (D1) de façon que la tension à travers le redresseur (D1) et la jonction PN soit sensiblement la même et dans lequel chacun de la jonction PN (collecteur-base) et du redresseur (D1) est conducteur pour produire l'action d'amortissement précitée.

11. Dispositif selon l'une des revendications 1 à 9 dans lequel le moyen d'application du courant de commande précité comprend un transformateur (T1) qui est couplé à l'inductance précitée (L_{H1}, L_{H2}) pour appliquer le courant de commande précité d'une borne (42) dudit transformateur.

12. Dispositif selon la revendication 11 dans lequel le moyen d'application du courant de commande précité comprend de plus un redresseur (D2) qui couple la borne précitée (42) du transformateur précité (T1) à l'électrode de commande précitée (base de Q1), pour conduire le courant de commande pendant l'apparition de l'action d'amortissement précitée.

13. Dispositif selon l'une des revendications 1 à 9 dans lequel le moyen d'application du courant de commande précité comprend un troisième moyen de commutation (Q3) qui est couplé à l'électrode de commande du premier moyen de commutation précité (Q1) pour appliquer le courant de commande précité à l'électrode de commande.

14. Dispositif selon la revendication 13 dans lequel le troisième moyen de commutation (Q3) conduit le courant de commande de l'inductance précitée (L_{H1}, L_{H2}).

15. Dispositif selon l'une des revendications 1 à 9 et 11 à 14 dans lequel l'agencement de commutation contrôlable précité comprend de plus un redresseur (D1) qui conduit pour produire au moins une partie de l'action d'amortissement précitée.

16. Dispositif selon l'une des revendications précédentes pour produire un courant de déviation dans un enroulement de déviation dans lequel:

le condensateur résonnant précité est un condensateur de retour (Cr), et l'inductance précitée est un enroulement de déviation (L_{H1}, L_{H2});

l'agencement de commutation contrôlable précité lorsque ce conducteur produit le courant de déviation d'aller;

le premier intervalle précité est un intervalle de retour; et

le courant précité par lequel le premier de commutation précité (Q1) est permis de conduire par l'application précitée d'un courant de commande est le courant de déviation pendant la dernière portion d'aller.

17. Dispositif selon l'une des revendications précédentes dans lequel le premier moyen de commutation précité (Q1) est à un état conducteur immédiatement avant l'initialisation de la portion de mise en service du signal de commutation précité.

18. Dispositif selon l'une des revendications précédentes comprenant de plus une résistance (R3) pour coupler une seconde tension (+15V) à l'électrode de commande précitée (base) du premier de moyen de commutation précité (Q1) qui applique une tension à celui-ci pour démarrer le fonctionnement du dispositif.

19. Dispositif selon l'une des revendications précédentes comprenant de plus une diode Zener (Z1) couplée à l'électrode de commande précitée du premier moyen de commutation précité (Q1).

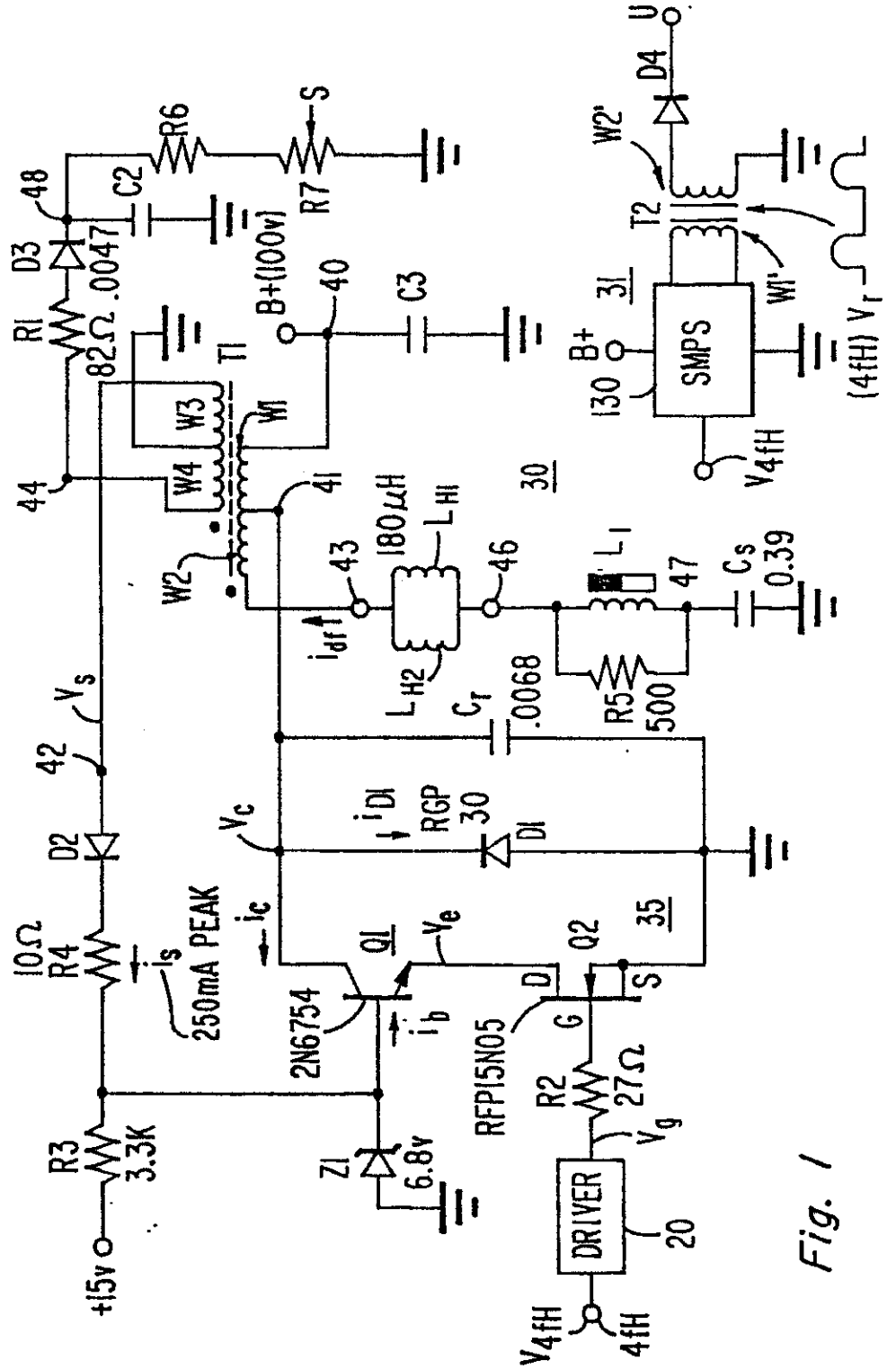
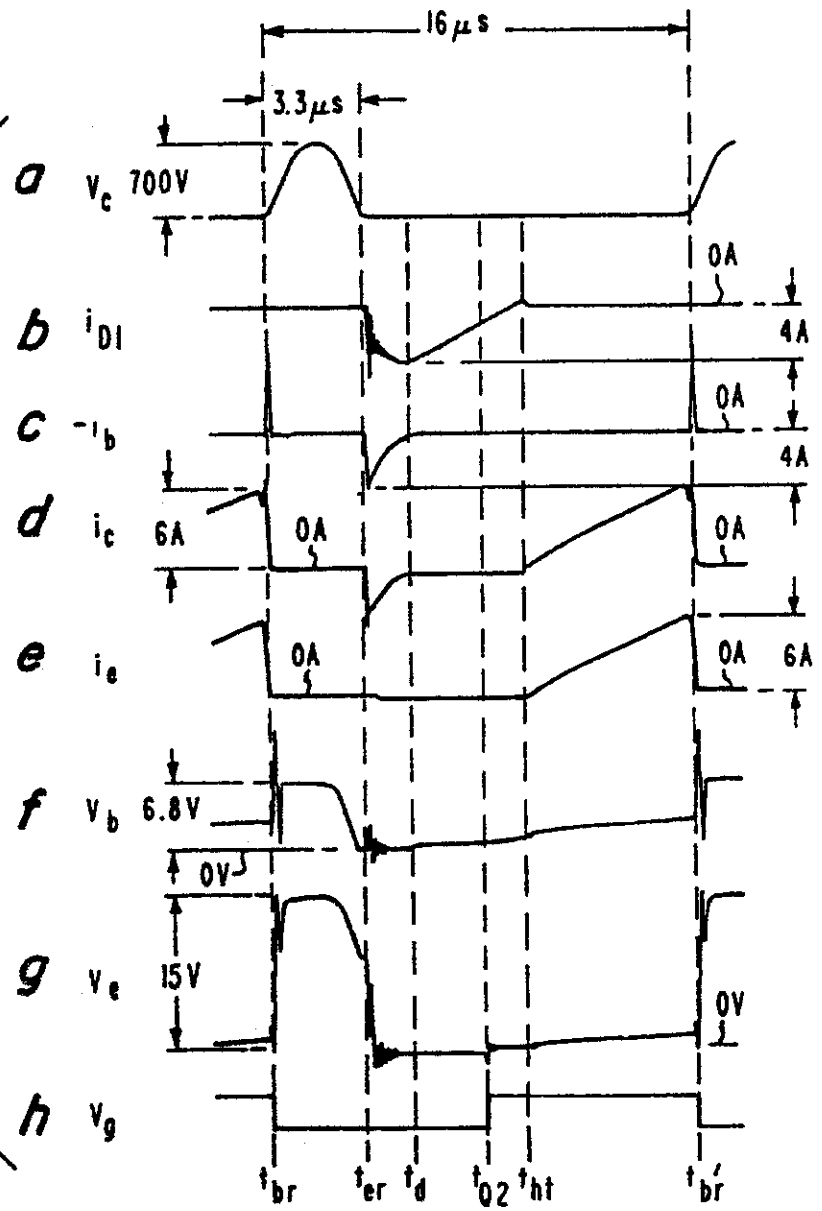

+15v
R3
3.3K
R4
10Ω
i_s
250mA PEAK
D2
42
V_s
44
R1
82Ω
D3
.0047
48
C2
R6
R7
S
B+(100v)
40
C3
T1
W1
W2
W3
W4
41
43
180μH
L_{H1}
L_{H2}
i_{df}
46
L_1
47
C_s
0.39
R5
500
C_r
.0068
30
V_c
i_{D1}
RGP
30
D1
i_c
Q1
V_e
2N6754
i_b
Q2
35
D
G
S
RFP15N05
R2
27Ω
V_g
Z1
6.8v
DRIVER
20
V_{4fH}
4fH
U
D4
W2'
T2
W1'
31
B+
130
SMPS
V_{4fH}
(4fH) V_r

Fig. 1

Fig. 2


16 μs
3.3μs
a
V_c
700V
b
i_{D1}
c
$-i_b$
d
i_c
6A
e
i_e
f
V_b
6.8V
0V
g
V_e
15V
h
V_g
0A
4A
0A
4A
0A
0A
0A
6A
0V
t_{br}
t_{er}
t_d
t_{02}
t_{ht}
t_{br}'

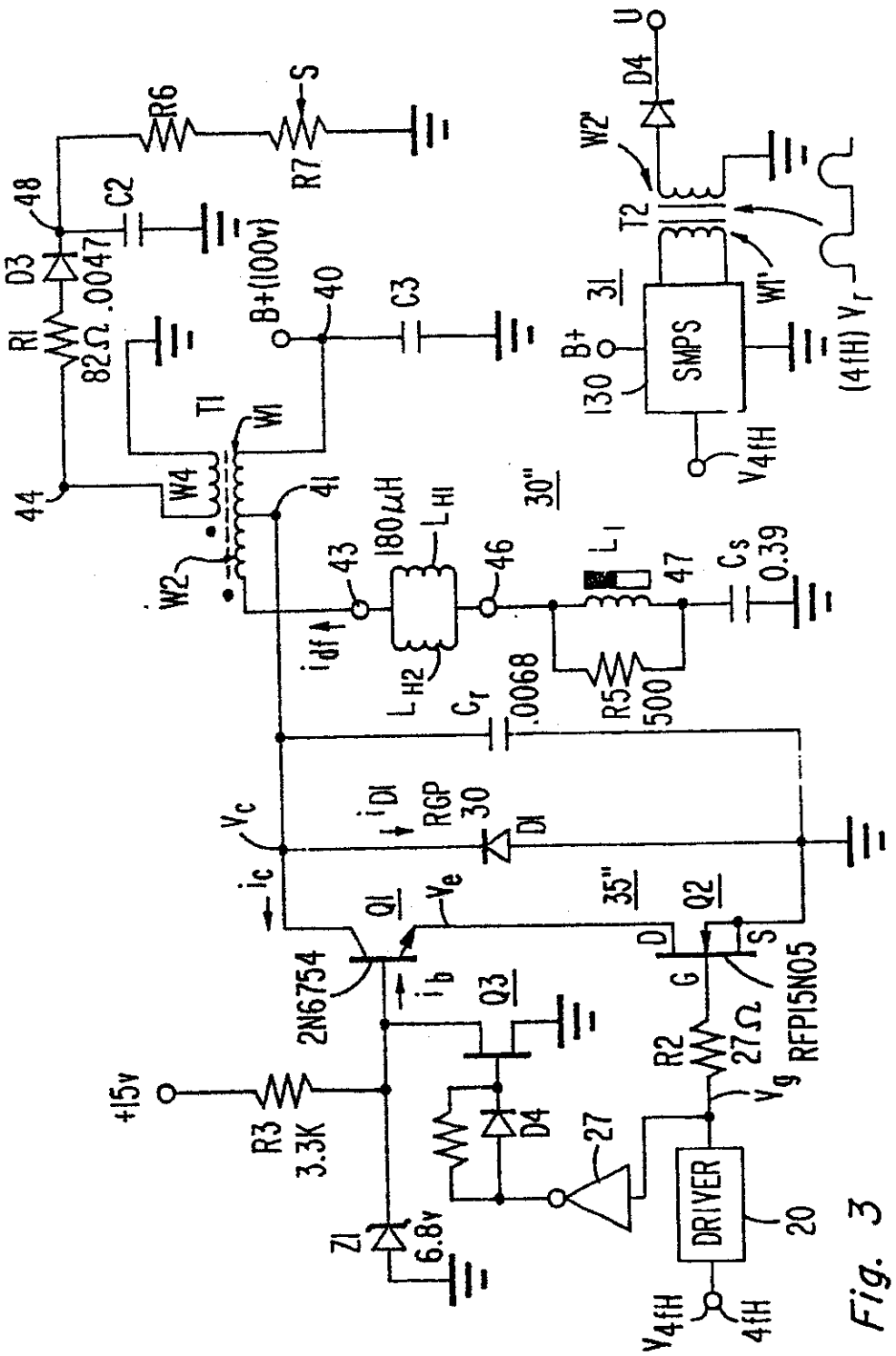
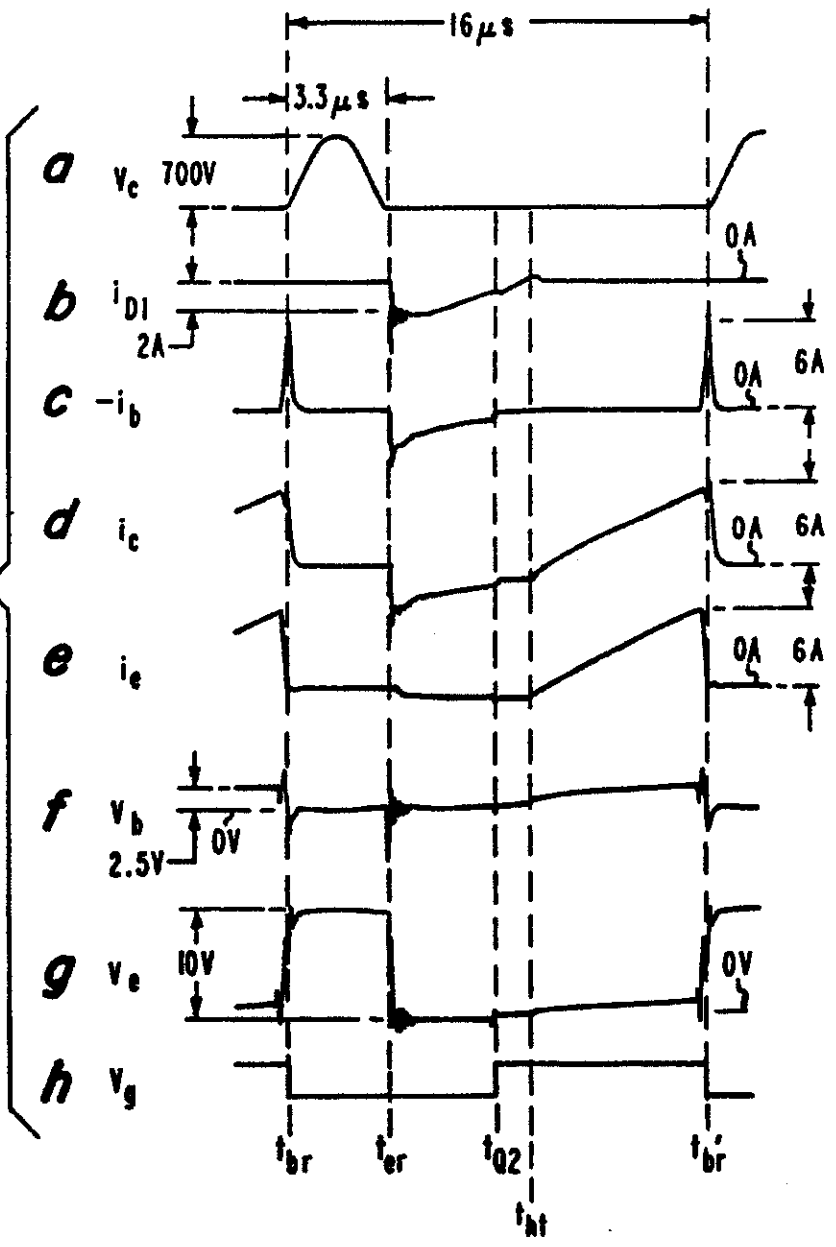

R6
S
R7
48
C2
D3
.0047
R1
82Ω
B+(100v)
40
C3
T1
W1
W4
44
41
W2
43
180μH
L_{H1}
46
L_1
47
C_s
0.39
30"
i_{df}
L_{H2}
C_r
.0068
R5
500
V_c
i_{D1}
RGP
30
D1
i_c
Q1
V_e
35"
Q2
D
S
G
2N6754
i_b
Q3
RFP15N05
R2
27Ω
V_g
+15v
R3
3.3K
D4
27
Z1
6.8v
DRIVER
20
V_{4fH}
4fH
U
D4
W2'
T2
W1'
31
B+
130
SMPS
V_{4fH}
(4fH) V_r

Fig. 3

Fig.4


16μs
3.3μs
a
V_c
700V
0A
b
i_{D1}
2A
0A
6A
c
$-i_b$
0A
6A
d
i_c
0A
6A
e
i_e
0A
6A
f
V_b
2.5V
0V
g
V_e
10V
0V
h
V_g
t_{br}
t_{er}
t_{Q2}
t_{ht}
t_{br}'

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Title A RESONANT SWITCHING APPARATUS USING A CASCODE ARRANGEMENT

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