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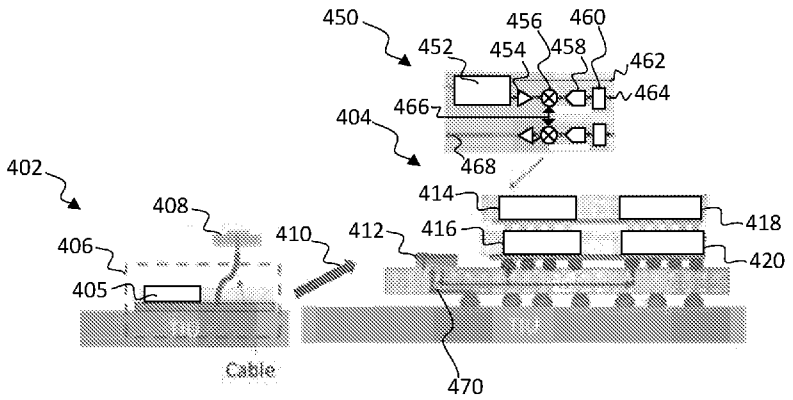


FIG. 4

(57) Abstract: A multichip package includes a first chip; a second chip; and a third chip. The third chip is electrically conductively coupled to the first chip and the second chip. The third chip includes an antenna; a multiplexer, configured to selectively couple the third chip to the first chip or the second chip; a first power combiner, configured to generate a first combined signal comprising a first antenna signal and a first baseband signal, and to output the first combined signal to the first chip; and a second power combiner, configured to generate a second combined signal comprising a second antenna signal and a second baseband signal, and to output the second combined signal to the second chip.

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# WIRELESS INTERCONNECT FOR TEST

## Technical Field

**[0001]** Various aspects of this disclosure generally relate to wireless chiplet testing in a multichip package.

## Background

**[0002]** The use of chiplet-based designs enables heterogeneous integration of dies having multiple process nodes into a single packaged system (the elements to be tested may be a final product or may be a subsystem of a final product). Such chiplet-based designs offer faster time-to-market and improved binning and yields for a given product; however, chiplet-based designs come with a high testing-interconnect cost. That is, chiplet-based designs often require a many pins to be reserved for testing purposes. For example, some existing chiplet-based designs currently require nearly fifty pins to be reserved for testing, and it is estimated that future chips may require sixty to one-hundred pins. Having so many test pins can greatly complicate the planning of the package bumps and package routing, particularly when the product is cost-sensitive or the package area is limited.

## Brief Description of the Drawings

**[0003]** In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the exemplary principles of the disclosure. In the following description, various exemplary embodiments of the disclosure are described with reference to the following drawings, in which:

FIG. 1 depicts a radio circuitry chiplet;

FIG. 2 depicts a wideband loop antenna with a balun;

FIG. 3 depicts a block diagram of the RFIC circuits;

FIG. 4 provides an overview of a downlink communication;

FIG. 5 depicts a configuration dedicated channels between the stacked dies and the radio circuitry chiplet;

FIG. 6 depicts an uplink communication;

FIG. 7 depicts an uplink communication between the dies and the radio circuitry chiplets;

FIG. 8 depicts a configuration for package-to-package communication;

FIG. 9 depicts a microbump used as an antenna;

FIG. 10 depicts an exemplary bump map and potential locations of transmitting and receiving antenna in the bump map;

FIG. 11 depicts a semiconductor die 1102 with an EDM-ring;

FIG. 12 depicts an EDM-ring within a plurality of chip layers;

FIGs. 13A-13D depict various configurations of EDM-ring antennas;

FIGs. 14A and 14B depicts two alternative configurations of debugging components; and

FIG. 15 depicts a multichip package.

## Description

**[0004]** The following detailed description refers to the accompanying drawings that show, by way of illustration, exemplary details and embodiments in which aspects of the present disclosure may be practiced.

**[0005]** The word "exemplary" is used herein to mean "serving as an example, instance, or illustration". Any embodiment or design described herein as "exemplary" is not

necessarily to be construed as preferred or advantageous over other embodiments or designs.

**[0006]** Throughout the drawings, it should be noted that like reference numbers are used to depict the same or similar elements, features, and structures, unless otherwise noted.

**[0007]** The phrase “at least one” and “one or more” may be understood to include a numerical quantity greater than or equal to one (e.g., one, two, three, four, [...], etc.). The phrase "at least one of" with regard to a group of elements may be used herein to mean at least one element from the group consisting of the elements. For example, the phrase "at least one of" with regard to a group of elements may be used herein to mean a selection of: one of the listed elements, a plurality of one of the listed elements, a plurality of individual listed elements, or a plurality of a multiple of individual listed elements.

**[0008]** The words “plural” and “multiple” in the description and in the claims expressly refer to a quantity greater than one. Accordingly, any phrases explicitly invoking the aforementioned words (e.g., “plural [elements]”, “multiple [elements]”) referring to a quantity of elements expressly refers to more than one of the said elements. For instance, the phrase “a plurality” may be understood to include a numerical quantity greater than or equal to two (e.g., two, three, four, five, [...], etc.).

**[0009]** The phrases “group (of)”, “set (of)”, “collection (of)”, “series (of)”, “sequence (of)”, “grouping (of)”, etc., in the description and in the claims, if any, refer to a quantity equal to or greater than one, i.e., one or more. The terms “proper subset”, “reduced subset”, and “lesser subset” refer to a subset of a set that is not equal to the set, illustratively, referring to a subset of a set that contains less elements than the set.

**[0010]** The term “data” as used herein may be understood to include information in any suitable analog or digital form, e.g., provided as a file, a portion of a file, a set of files, a signal or stream, a portion of a signal or stream, a set of signals or streams, and the like. Further, the term “data” may also be used to mean a reference to information, e.g., in

form of a pointer. The term "data", however, is not limited to the aforementioned examples and may take various forms and represent any information as understood in the art.

**[0011]** The terms "processor" or "controller" as, for example, used herein may be understood as any kind of technological entity that allows handling of data. The data may be handled according to one or more specific functions executed by the processor or controller. Further, a processor or controller as used herein may be understood as any kind of circuit, e.g., any kind of analog or digital circuit. A processor or a controller may thus be or include an analog circuit, digital circuit, mixed-signal circuit, logic circuit, processor, microprocessor, Central Processing Unit (CPU), Graphics Processing Unit (GPU), XPU (can include a tensor process, an artificial intelligence accelerator, etc.), Digital Signal Processor (DSP), Field Programmable Gate Array (FPGA), integrated circuit, Application Specific Integrated Circuit (ASIC), etc., or any combination thereof. Any other kind of implementation of the respective functions, which will be described below in further detail, may also be understood as a processor, controller, or logic circuit. It is understood that any two (or more) of the processors, controllers, or logic circuits detailed herein may be realized as a single entity with equivalent functionality or the like, and conversely that any single processor, controller, or logic circuit detailed herein may be realized as two (or more) separate entities with equivalent functionality or the like.

**[0012]** As used herein, "memory" is understood as a computer-readable medium (e.g., a non-transitory computer-readable medium) in which data or information can be stored for retrieval. References to "memory" included herein may thus be understood as referring to volatile or non-volatile memory, including random access memory (RAM), read-only memory (ROM), flash memory, solid-state storage, magnetic tape, hard disk drive, optical drive, 3D XPointTM, among others, or any combination thereof. Registers, shift registers, processor registers, data buffers, among others, are also embraced herein by the

term memory. The term "software" refers to any type of executable instruction, including firmware.

**[0013]** Unless explicitly specified, the term "transmit" encompasses both direct (point-to-point) and indirect transmission (via one or more intermediary points). Similarly, the term "receive" encompasses both direct and indirect reception. Furthermore, the terms "transmit," "receive," "communicate," and other similar terms encompass both physical transmission (e.g., the transmission of radio signals) and logical transmission (e.g., the transmission of digital data over a logical software-level connection). For example, a processor or controller may transmit or receive data over a software-level connection with another processor or controller in the form of radio signals, where the physical transmission and reception is handled by radio-layer components such as radiofrequency (RF) transceivers and antennas, and the logical transmission and reception over the software-level connection is performed by the processors or controllers. The term "communicate" encompasses one or both of transmitting and receiving, i.e., unidirectional or bidirectional communication in one or both of the incoming and outgoing directions. The term "calculate" encompasses both 'direct' calculations via a mathematical expression/formula/relationship and 'indirect' calculations via lookup or hash tables and other array indexing or searching operations.

**[0014]** Throughout this disclosure, the words "chip" and "chiplet" are used. Although a "chiplet" is often used to reference to a small integrated circuit with a particularized function, it is recognized that the definition of a chip and a chiplet may be understood differently in different contexts, in different branches, by different manufactures, and the like. Moreover, the line of demarcation between a chip and a chiplet may be unclear in some contexts. In light of this, it is expressly acknowledged that the structures, configurations and/or functions ascribed herein to a chiplet, with respect to the use of a removeable waveguide, may be performed or exhibited by a chip; similarly, any

structures, configurations and/or functions ascribed herein to a chip, with respect to the use of the removeable waveguide, may be performed or exhibited by a chiplet. Thus, any aspect of this disclosure that is described with respect to a chiplet may be applied to a chip, and vice versa.

**[0015]** A power combiner as used herein may refer to any device that is configured to combine a first power input with a second power input to generate a combined power output. Conventionally a power combiner is a passive device that generates a vector sum of two inputs as a combined output, although various active or powered combiners exist, and either configuration may be used for the principles and methods disclosed herein. The power combiner may optionally include a phase shifting mechanism to shift the phase of one or more inputs relative to each other to generate a combined output.

**[0016]** As described above, the testing requirements for chiplet-based packages create significant difficulties, as many pins must be reserved for testing, and this in turn creates extreme challenges in package routing and package bump planning. To mitigate the bump planning and placement constrains on both the package and die level, wireless-communication of test signals between dies and testers is disclosed, so as to avoid a package level bump-shortage while offering a mechanism to detect the assembly defects on the die bump and to authenticate the chiplet through an RF fingerprint. Moreover, the principles and methods disclosed herein further optionally exploit having the test signal share the die bump with some other low speed logic signals by using frequency division multiplexing to recognize and/or alleviate die bump defects.

**[0017]** In brief, test signals may be upconverted to passband signals and then combined with baseband digital signals to reduce the number of signal routings, package, and die level bumps reserved for testing. In addition, one or more bumps for testing can be used as antennas, thereby offering bump health detection and radiofrequency (RF) fingerprint functions (security/integrity). After the test is completed, the test signal may be reposed to

enable dual-band or multiband high data rates along with crosstalk reduction. Thus, the principles and methods disclosed herein may reduce the number of die bumps and package bumps reserved for testing only through pin sharing; reduce the routing complication both at bump level and package level; and offer faulty μ-bump joint detection and RF fingerprint function (security / integrity check) by reconfiguring test μ-bumps.

**[0018]** In a test environment, communication between the tester and the device under test DUT (e.g. the die or stacked dies) is unilateral, meaning it either goes from the tester to the DUT or goes from the DUT to the tester. For the purposes of this disclosure, communication from the tester to the DUT is designated as "Downlink", while communication from the DUT to the testers is referred as "Uplink."

**[0019]** FIG. 1 depicts an RF chiplet (also referred to herein as a radio circuitry chiplet). Such RF chiplets may be or include a radio frequency integrated circuit (RFIC)102 and may include an antenna interface or an antenna 104. RFIC 102 may itself include, for example, a radio receiver, a radio transceiver, a modem, and the like to enable the RFIC to amplify, modulate, transmit, receive, and demodulate signals. The RFIC 102 may play a critical role in enabling both the "Downlink" and "Uplink" wireless communication between the tester and any device under test (DUT) or devices under test (DUTs). The antenna 104 can take different forms, which may include a through silicon via (TSV) antenna, an omni-directional antenna (e.g., a zig-zag dipole antenna), or any other suitable antennas. FIG. 2 depicts, for example, a wideband loop antenna 202 with a lumped element balun 204, and which was designed and fabricated on a two-layer printed circuit board (PCB). In this exemplary design, the non-uniform loop is fed by a balun 204, which is a lumped element balun connected to the antenna through a coplanar strip. Since the antenna is a single layer structure, it can optionally be easily migrated to the die and be placed around the RFIC as indicated in FIG. 1. Of course, this is merely one option of a chip and antenna configuration, and many other varieties are conceivable.

**[0020]** FIG. 3 depicts a block diagram of the RFIC 102 circuits. These generally include multiple power combiners, multiple power amplifiers, a local oscillator circuit to generate an RF carrier signal, and a time division duplex (TDD) control circuit to allow the RF chiplet to be shared by multiple stacked chiplets. This exemplary circuit as depicted in FIG. 3 is configured for connection to two additional chips, although the number two is selected merely for demonstrative purposes, and a greater number of chips is conceivable. In greater detail, however, this RFIC 102 circuit includes a radiofrequency switch 302, such as for TDD (although other switching or multiplexing configurations are conceivable), two power combiners 304 and 308, and to power amplifiers 306 and 310, and a local oscillator 312. The radiofrequency switch 302 may be configured to receive a signal from the antenna and to route the signal to one of the power combiners 304 or 308, or to receive a signal from one of the power amplifiers 306 or 310, and to route this receive signal to the antenna. The power combiner 304 may be connected to a first chip, and may be configured to download a signal (e.g. a frequency division multiplexing signal) to the first chip. The power amplifier 306 may be connected to the first chip, and may be configured to upload a radiofrequency signal from the first chip to the radiofrequency switch 302. The power combiner 308 may be connected to a second chip, and may be configured to download a signal (e.g. a frequency division multiplexing signal) to the second chip. The power amplifier 310 may be connected to the second chip, and may be configured to upload a radiofrequency signal from the second chip to the radiofrequency switch 302. Of course, should additional numbers of chips be used, the radiofrequency integrated circuit may be configured with additional power combiners and power amplifiers to establish the necessary connections. In FIG. 3, solid arrows represent RF signals, while dashed arrows represent the frequency division multiplexing (FDM) enabled signals comprising an RF Passband signal and a digital baseband signal. The dotted arrow indicates the local oscillator signal.

**[0021]** FIG. 4 provides an overview of a downlink communication. In this figure, a testing device 402 establishes a wireless connection with a DUT 404 (e.g., a multi-chiplet package) for wireless transmission of a testing signal. The testing device includes an RFIC 405, a testing controller 406 (demarcated by the dashed box and including the RFIC 405), and an antenna 408 (e.g. a flexible antenna, an antenna on the package, or an antenna on the chip). The testing device 402 sends a wireless testing signal 410 to the DUT 404. The DUT 404 includes an RF chiplet 412 (e.g. the RF chiplet of FIG. 1), which itself includes an antenna (depicted within the RF chiplet 412), which then includes through-package connections to a plurality of chips. In this demonstrative example, the chip package includes a first chip 414, a second chip 416, the third chip 418, and if the forth chip 420. The first chip 414 and the second chip 416 may be connected to one another, such as through a plurality of microbumps and vias (e.g., through silicon vias). Similarly, the third chip 418 and the fourth chip 420 may be connected to one another, such as through a plurality of microbumps and vias (e.g., through silicon vias).

**[0022]** Each chip/chiplet (414, 416, 418, 420) of the multi-chiplet package, may include a frequency division multiplexing (FDM) module 450. Each FDM module 450 includes one or more filters 452 (e.g. frequency diplexer and filters), a low noise amplifier 454, a multiplexer 456, an analog-to-digital converter (ADC) 458, and a digital signal processing module 460. The filters 452 are configured to receive the test signal (as routed from the antenna through the DUT to the chiplet) and to output a baseband signal 462 and a modulated test signal. Said filtering may be achieved, for example, by employing a low-pass filter and a high-pass filter, or by using bandpass filters of differing ranger. The modulated test signal is amplified at the amplifier 454, and demodulated by use of the local oscillator signal 466I, the result of which is then converted to a digital signal in the ADC 458 and finally processed in the DSP 460 to generate a download test signal 464. The result of the local test undergoes an essentially opposite procedure to generate the uplink radiofrequency signal 468 with a test result. That is,

the uplink test result undergoes digital signal processing, a digital-to-analog conversion, modulation, amplification, and is then output as the uplink radiofrequency signal 468, which is sent to the RF Chiplet 412, and ultimately as a wireless signal to the testing device 402.

**[0023]** In this configuration, the test signal is upconverted to an RF signal and is sent to the RF chiplet on the package as the wireless test signal 410. This is received at the antenna of the RF Chiplet 412 and is then combined by the RF Chiplet 412 with a digital signal 470 coming from the bottom of the package and then output as a dual-band signal which is delivered to one of the stacked chiplets (414, 416, 418, 420) under testing. In one configuration, a simple diode may be placed on each die to serve as a bypass and to enable the routing sharing among multiple stacked dies. To provide a reliable wireless communication and flexible communication range, the antenna 408 on the tester side may optionally be fabricated on a flexible printed circuit board (PCB) (e.g. a flex PCB) and be connected the RFIC 405 on the tester through a connector (not labeled). The position of the tester antenna can be adjusted relative to the antenna integrated in the RF chiplet on the DUT package.

**[0024]** As stated above, this FDM module may be included in each die's test block (e.g. a test block in each of 414, 416, 418, and 420). After test, the test block in each die is generally treated as a "dead" area, meaning that the area has little or no function after testing is complete. This necessitates that the area of the FDM module remain small. For this reason, it is disclosed herein to generate local oscillator (LO) signals by the RF chiplet 412 and to interconnect these LO signals to each stacked chiplet for the purpose of demodulation at the die level.

**[0025]** For a downlink communication, the dual-band signal to the die test IP first undergoes "Frequency Diplexing" via the filters 452, during which the signal is bifurcated into two different paths. One path goes through a lowpass filter (e.g. part of 452) and is decoded to recover the baseband signal, while the other passes through an amplifier 454 and then is demodulated (e.g. at the demodulator 456) by mixing this signal with the LO signal 466, at

which time it is converted back to a digital signal via the ADC 458 and optionally submitted for further signal processing via the digital signal processor 460. On the other hand, for an uplink communication, the output test signal originated from each die passes a signal link including DSP, digital to analog converter (DAC), RF modulation, and amplification within the FDM module before it is interconnected to the RF chiplet for wireless transmission (see lower path of 450, showing the return process for an uplink signal).

**[0026]** FIG. 5 depicts an alternative configuration, in which each stacked die has its own dedicated channels connected to the RF chiplets. In this figure, the testing device 402 and the DUT 404 are essentially identical to the devices of FIG. 4, except that the digital baseband signal for each of the stacked die is recombined with its test signal by the RF chiplet, and the output dual-band signal is connected to the stacked die through its own dedicated interconnect. See, for example, a first connection 502 to a first stacked die, and a second connection 504 to a second stacked die. By doing so, testing several stacked dies can be feasible in parallel.

**[0027]** FIG. 6 depicts an uplink communication 602 from a die (or from multiple dies) to the tester. This can be realized once the test result signal generated by the die is upconverted to a modulated RF signal by the FDM module of the corresponding die (see FIG. 4 for the FDM module). In this configuration, a channel at the package level is employed to interconnect the stack dies to the RF chiplet, and this is shared among different stacked dies. As with the downlink case, the connection of a particular die to the shared channel can be enabled or disabled by a bypass circuitry in each die's test IP block. That is, the signal is modulated in the FDM module of the respective chip and sent from the chip to the package, where it travels to the RF Chiplet 412. From the RF Chiplet 412, the signal is sent via the antenna as an uplink communication 602 to the testing device.

**[0028]** In contrast to the topology of FIG. 6, FIG. 7 depicts an uplink communication between the dies and the RF chiplets, in which the topology is arranged such that each stacked die has

its own dedicated path (first path 702, second path 704) connecting to the RF Chiplet 412. However, the path may be shared between the dies in a stack, such as is depicted herein in which the first path 702 connects the dies in the left-stack to the RF Chiplet 412, and the second path 704 connects the dies in the right-stack to the RF Chiplet 412. This topology may be preferable in certain configurations, as it permits testing of multiple dies at the same time (e.g. simultaneous testing of multiple dies).

**[0029]** FIG. 8 depicts the configuration disclosed herein being used for package-to-package communication. That is, after testing, the RF Chiplet and FDM (located in each chip/chiplet as disclosed herein) can be repurposed to support the communication between two stacked dies on different packages. Specifically, FIG. 8 depicts a first package 802 and a second package 804, configured for wireless communication with one another via the FDM and RFIC as disclosed herein. For instance, a baseband signal 806 may be generated by a die in the stacked dies while another signal 808 may be originated by the same die as an RF modulated signal by the FDM in the die, using the FDM components that are described above. These two signals can be concurrently or simultaneously transmitted to other stacked dies in the neighboring package (e.g. a receiving package), such as through a wired interconnect (see path of signal 806) and through the wireless communication interface enabled by the RF chiplets (see the path of signal 808). Those two signals may be combined by the power combiner inside the RF chiplet (see FIG. 3, element 304 or 310) to form a dual-band signal. This dual band signal may then be routed to the intended die.

**[0030]** Using the chip-to-chip (e.g. package-to-package) RF communication techniques disclosed above, a testing device (e.g. as in FIG. 4, 402) can be used to make certain determinations about the health of the DUT. For example, the testing device can be used to determine bump health (e.g. health of the microbumps on the DUT or the DUT-package) and/or to provide certain RF fingerprint functions. This may be achieved, for example, by reconfiguring microbumps connecting to a wireless Joint Test Action Group (WJTAG)

software or device. First, diodes (or switches) on dies may be configured to select a group of microbumps on specific die (e.g. to select a subset of the microbumps on a die). In some configurations, these diodes may already be included in the JTAG device/software. Ultrawideband (UWB) testing signals can then be sent from the tester to a transmission microbump through the RF chiplet (see, e.g., FIG. 4, 405). The transmission microbump may act as a launcher and may excite the underfill as a dielectric antenna loaded with surrounding microbumps with various impedance conditions (see Fig. 9). The "sensed signal" may be captured at the receiving microbump and sent back to the tester for post-processing. If there are faulty microbumps, the "sensed signal" will differ from a signal with healthy microbumps. This signal corresponding to healthy microbumps may be understood as a root signal or other predetermined signal to serve as a basis of comparison. This capability can be used for each of bump health detection and RF fingerprint functions.

**[0031]** FIG. 9 depicts a microbump used as an antenna for assessment of microbump health, as described above. In this figure, the chip 902 (e.g., the die, the chiplet) is connected to a package layer 904 via a plurality of microbumps (a single microbump is depicted as 906). The microbumps themselves may be connected to the package layer 904 and or via a solder resist layer 908. The microbumps may be encased in an underfill layer 910. As stated above, a diode 912 , or alternatively a switch (not pictured), may be implemented between the chip 902 and the microbump 906 to select a microbump for excitement and testing.

**[0032]** In this manner, a first microbump may be selected for treatment as a transmitting antenna. In this manner, the diode and/or switch may be selected such that the first microbump will be excited with a signal (e.g. a wired connection to the microbump will transmit a signal for excitement of the microbump). The microbump, acting as an antenna, will radiate a portion of the signal, such as to neighboring microbumps. A second microbump may be selected as a receiving antenna. In this manner, a diode and/or switch may be engaged to select the second microbump functioning as a receiving antenna. A portion of the wireless

signal radiated from the first microbump may be received by the second microbump. This received signal can be analyzed to determine the health of the surrounding microbumps.

**[0033]** In greater detail, the surrounding microbumps each influence the radiating pattern emanating from the first microbump and traveling to the second microbump. In this manner, and when a known test signal (e.g. a test pattern, a test burst, etc.) is sent from the first microbump, and assuming that all surrounding microbumps are present and properly connected (e.g. properly soldered), a known or expected signal should result at the second microbump. That is, the microbump array functions as a system, wherein the input is the test pattern radiated from the first microbump, and the output is the signal received at the second microbump. This signal received at the second microbump may be compared to the known or expected signal (e.g. the signal that would occur if all microbumps are present and properly soldered). If the received signal is identical to, matches, or approximates the expected signal, it may be assumed that the surrounding microbumps are present and properly soldered. If however, the receive signal deviates significantly from the expected signal, it may be assumed that one or more microbumps is missing or improperly soldered, or otherwise defective. In this manner, a test for the health of the microbumps may be achieved.

**[0034]** The analysis/comparison between the received signal and the expected signal may be performed by a processor configured to compare these patterns. The processor may be configured to determine an amount of similarity between the received signal and the expected signal, and the processor may be configured to operate according to a first operational mode when the similarity between the receive signal and the expected signal is within a predetermined range, and to operate within a second operational mode when the similarity between the receive signal and the expected signal is outside of the predetermined range. In one aspect of the disclosure, the first operational mode may include the processor generating a signal representing a successful test, and the second operational mode may include the processor generating a signal representing a failure of the test. In some configurations, it may

be desirable to implement an artificial neural network to perform the comparison of the received signal and the expected signal.

**[0035]** FIG. 10 depicts an exemplary bump map. In this hypothetical configuration, the distance between microbumps in the diagonal direction is assumed to be 150 μm, although this distance is arbitrary and could be any other distance as desired for the implementation. A first microbump 1002 is selected as a transmitting antenna and a second microbump 1004 is selected as a receive antenna. A faulty cold solder joint bump 1006 is located between the first microbump 1002 and the second microbump 1004.

**[0036]** In a simulation of the time-domain response, a comparison was made between a healthy bump case (e.g. a case in which all microbumps are present and properly soldered) and a faulty bump case (e.g. a case in which one or more microbumps are missing or at least one microbump is not properly soldered). A sine-modulated Gaussian pulse was used as an input in the simulation, in which the pulse essentially covered the entire D band (110 – 170 GHz). The resulting RF fingerprints for the healthy bumps and faulty bump cases were quite different from each other, thereby allowing a determination of bump health to be made from a comparison of the system responses. Of note, although this comparison was made in the time domain, such a comparison could also be performed in the frequency or Laplace domain, which may be preferable to a comparison in the time domain for various purposes.

**[0037]** According to another aspect of the disclosure, an edge die monitor (EDM) ring may be repurposed as the antenna for the RFIC. FIG. 11 depicts a semiconductor die 1102 with an EDM-ring 1104. An EDM-ring may be a solid metal ring around the perimeter of the chip 1102. The EDM-ring may be in or on one or more layers of the chip 1104. The EDM-ring may include or be in proximity to one or more alignment markers 1106 and 1108. These alignment markers may be or include metal structures having a predetermined shape. The inclusion of these shapes in the die may assist in the positioning or alignment of the die, such as for die separation or other manufacturing and package assembly steps. Although alignment

marker 1106 is generally depicted herein as an 'H' and alignment marker 1108 is generally depicted herein as an upside-down 'U', these shapes are arbitrary, and other shapes may utilized as desired.

**[0038]** For context, most advanced semiconductor manufacturing processes utilize an EDM-ring for reliability, as its use assists in the detection of die cracking and defects related to chip dicing and pre-packaging. Such problems may not typically be detected by standard opens-testing or shorts-testing. It is possible to include the alignment markers within the EDM-ring, or, alternatively, the alignment markers may be external to the EDM-ring, so as not to encroach into design space. Regardless of how they are created, after fabrication and packaging, both the EDM-ring and the alignment markers become superfluous.

**[0039]** Although EDM-rings can be in a single plane (e.g. in or on a single layer of the chip), the EDM-ring can alternatively be designed along multiple layers of the chip. FIG. 12 depicts an EDM-ring within a plurality of chip layers. In this figure, the EDM-ring ranges from the ground plane at the bottom and continues upward to layers M1-M8 (e.g. from bottom to top). These EDM-ring layers may be connected to one another, such as by using vias. Such a configuration in which the EDM-ring is built across multiple layers may permit the antenna to have a length that is greater than the perimeter of the chip, i.e., a zig-zag antenna.

**[0040]** An antenna (e.g. a reconfigurable antenna) may be generated or built from the EDM-ring, and also optionally using the alignment markers. Such an antenna may be useful for debugging applications. The tuned antenna frequencies of typical chiplet sizes can range from sub-10 GHz to the mmWave range. This corresponds, for example with emerging Wireless I/O (WIO) transceiver (TRX) architectures. The EDM-ring can essentially be understood a square loop antenna with an omni-directional pattern. For a 2x2 $mm^2$ chiplet, EDM-ring antenna can operate at approximately 1 GHz, considering effective dielectric loading of silicon and underfill material. For a 4x4 $mm^2$ chiplet, it can operate around 250 MHz, and 62.5 MHz for an 8x8 $mm^2$ chiplet. Considering the zig-zag structure in Fig. 12, the operating

frequency of the EDM-ring antenna can be further lowered due to the increased electrical length. On the other hand, the EDM-ring antenna can operate at much higher frequency, e.g. mmWave frequency, than its natural resonant frequency. The EDM-ring antenna driven at mmWave frequency becomes electrically large, the corresponding radiation pattern is directional, and antenna communication range increases. The electrically-large EDM-ring antenna can support multi-band operation.

**[0041]** In an optional configuration, various impedance matching topology may be utilized to further tune the antenna. FIGs. 13A-13D depict various configurations of EDM-ring antennas. In FIG. 13A, the EDM-ring 1302 includes an opening (e.g. a break in the circumference or perimeter of the EDM-ring), which may optionally include a tuning capacitor 1304. The tuning capacitor 1304 may be implemented to alter or select a resonant frequency of the EDM-ring. A capacitance of the tuning capacitor may be selected according to known methods, and the skilled person will appreciate how a tuning capacitance is chosen. The EDM-ring 1302 may be further configured with a first terminal 1306 and a second terminal 1308, which may be connected to the RFIC chip for transmission and reception. In this manner, the EDM-ring may be utilized as an antenna for the RFIC chip, and therefore the RFIC chip may perform wireless communication without the need for an additional antenna, but rather merely by making use of an existing metal structure that otherwise possesses no utility following chip manufacture.

**[0042]** FIG. 13B depicts an alternative, in which the EDM-ring antenna 1302, tuning capacitor 1304, and terminals 1306 and 1308 further include additional impedance matching capacitors 1310 and 1312. These impedance matching capacitors may perform an impedance matching function on the EDM-ring antenna 1302 so as to improve overall load-balance and efficiency.

**[0043]** FIG. 13C depicts an EDM-ring 1302 comprising a tuning capacitor 1304, but in which the first terminal 1306 and the second terminal 1308 are located across the ring from the

tuning capacitor 1304. From this, it may be understood that the first terminal 1306 and the second terminal 1308 may be placed anywhere along the EDM-ring, as is preferred for a given implementation.

**[0044]** FIG. 13D depicts an optional configuration of the EDM-ring 1302 including a tuning capacitor 1304, in which the EDM-ring 1302 further includes an inductive coupler 1312, to which the terminals are attached. The inductive coupler 1312 may be utilized for any situations in which it may be desired, including, but not limited to, simplification of electrical connections to the EDM-ring 1302, or desire to electrically isolate the EDM-ring 1302 from the RFIC chip.

**[0045]** In an optional configuration, one or more of the alignment markers (see FIG. 11, 1106 and 1108) may be used as either a tuning capacitor or an impedance matching capacitor. That is, and alignment marker of the one or more alignment markers may include a shape that, itself, may generate a capacitance (e.g. by virtue of parallel metal portions, one of which being connected to a power source). Thus, this capacitance-generating shape may be both utilized as an alignment marker and as a tuning capacitor or impedance matching capacitor.

**[0046]** To support repurposing the EDM-ring as an antenna, the PRS markers may be designed to be part of the EDM-ring (while still providing necessary visual features) and to act as either feed points or as an inductive loads to fine-tune the antenna frequency, broaden operating frequency range, and/or to improve the radiation efficiency. Finally, a variable capacitor structure can be used to couple to the PRS markers to provide additional tuning and impedance matching for the Analog Front End (AFE) of the Transmitter (TX) and Receiver (RX) of the Debug WIO.

**[0047]** In addition to the illustrations above, in complex heterogeneous packages, the RFIC can be configured as a standalone chiplet or as part of an existing chiplet. In some configurations, the existing chiplet may be a base die. The antenna or coupler functionality described herein may be achieved by metallic structures fabricated inside the same chiplet

using vias. Test equipment can have sophisticated antenna and coupler structures that can be placed near the DUT from above and provide bi-directional or directional wireless links to complete test wirelessly.

**[0048]** FIG. 14A depicts a configuration in which the debugging components are built into each of a chiplet and a base die (see, e.g., the blocks "DFT hub" in each). In this manner, it may be necessary to transmit debugging information/results to the test equipment from multiple sites, such as from a chiplet and from the base die. FIG. 14B depicts an alternative configuration in which the debugging capabilities of the product chiplets are replaced with a debug chiplet. This debug chiplet may include a receiver and transceiver, and digital signal processing, such as equalizer ,ADC, DAC, modulator/demodulator, etc.). In addition being permanently part of the package assembly as shown in FIG. 14B, this debug chiplet may be temporarily attached to the package assembly and later removed once the testing is completed.

**[0049]** FIG. 15 depicts a multichip package that includes a first chip 1502; a second chip 1504; a third chip 1506, electrically conductively coupled to the first chip 1502 and the second chip 1504, the third chip 1506 comprising, an antenna 1508; a multiplexer 1510, configured to selectively couple the third chip to the first chip or the second chip; a first power combiner 1512, configured to generate a first combined signal comprising a first antenna signal and a first baseband signal, and to output the first combined signal to the first chip 1502; and a second power combiner 1514, configured to generate a second combined signal comprising a second antenna signal and a second baseband signal, and to output the second combined signal to the second chip 1504.

**[0050]** In some configurations, the third chip may further include an oscillator 1516. The oscillator may be configured to generate an oscillator output signal, and wherein the third chip is configured to output the oscillator output signal to the first chip or the second chip. The first chip 1502 may optionally include a first filter circuit 1518, which may be

configured to separate the first combined signal into the first antenna signal and the first baseband signal. Similarly, the second chip 1504 may include a second filter circuit 1520, which may be configured to separate the second combined signal into the second antenna signal and the second baseband signal.

**[0051]** In this manner, the first antenna signal may be a modulated first test signal, in that the first test signal has been modulated for wireless transmission according to a desired wireless transmission protocol. Similarly, the second antenna signal may be a modulated second test signal, in which the second test signal has been modulated for wireless transmission according to a desired wireless transmission protocol.

**[0052]** The first test signal and the second test signal, once received at the RFIC and sent to the first chip 1502 or the second chip 1504, respectively, will require demodulation. To that end, the first chip may further include a first demodulator 1522, which may be configured to recover the first test signal from the first antenna signal. Similarly, the second chip may further include a second demodulator 1524, which may be configured to recover the second test signal from the second antenna signal.

**[0053]** The first antenna signal may include comprises two different frequency bands of modulated signals. The first antenna signal may include a wide-band signal, which itself includes a modulated signal from at least two frequency bands. The multiple frequency bands may be separated upon receipt in the respective chip. This may allow for two signals to be carried on a single transmission line between the third chip and either the first chip or the second chip. In this manner, an additional transmission line (e.g. an electrically conductive connection) between the third chip and the first chip and between the third chip and the second chip can be uses for another purpose (e.g. such connections do not have to be reserved for testing).

**[0054]** The multichip package may include a first electrically conductive path 1526 between the multiplexer 1510 of the third chip and the first chip 1502, and a second

electrically conductive path 1528 between the multiplexer 1510 of the third chip and the second chip 1504. In this manner, the multichip package may include an electrically conductive path 1526 between the third chip 1506 and both of the first chip 1502 and the second chip 1504.

**[0055]** In one configuration, the antenna may be formed on rigid, flexible, hybrid printed circuit board. This may permit simplification of manufacture by simply incorporating the antenna within a PCB design. In an alternative configuration, the antenna may be formed on the multichip package itself, or formed on the third chip. The antenna may be an EDM-ring antenna, in which the antenna is formed of an EDM-ring that is otherwise used for chip manufacture. In some configurations, the third chip may include two antennas, in which case the two antennas and third chip may be configured to support multi-band modulated signals or multiple number of wireless links simultaneously.

**[0056]** The first chip may include a first underfill layer, which itself may include a plurality of first microbumps. The first chip may be configured, in response to a first test signal, to excite a first microbump of the first plurality of microbumps. That is, the first microbump may be electrically conductively coupled to the EDM module, such that a wirelessly-received test signal is demodulated and processed, and this test signal is then electrically conducted to the first microbump. In this manner, the first microbump acts as an antenna, and radiates the test signal at least to a second microbump. The second microbump may be configured to receive a first microbump excitation signal (e.g. the test signal radiated from the first microbump). This received signal may then be processed as described herein to evaluate a health of one or more microbumps. This evaluation may optionally be performed by the respective chip (e.g. the first chip or the second chip) performing a transform of the first microbump excitation signal from a time domain into a frequency domain. In this manner, the chip may determine whether the microbump of the first plurality of microbumps is faulty by comparing the transform of the first

microbump excitation signal into the frequency domain with a predetermined pattern. That is, if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined pattern is within a range (e.g. a predetermined range), the first chip may be configured to generate a signal representing a determination that the microbumps of the first underfill layer are acceptable, and if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined pattern is outside the range, the first chip may be configured to generate a signal representing a determination that the microbumps of the first underfill layer are unacceptable.

**[0057]** Similarly, the multichip package may further include a second underfill layer beneath the second die. The second underfill layer may include a plurality of second microbumps. As with the first plurality of microbumps, and in response to the second test signal, the second chip may be configured to excite a first microbump of the second plurality of microbumps and to receive a second microbump excitation signal received at a second microbump of the second plurality of microbumps. This second microbump excitation signal may be generated by a radiofrequency emission resulting from the excitation of the first microbump of the second plurality of microbumps. Accordingly, the second chip is further configured to determine from the second microbump excitation signal whether a microbump of the second plurality of microbumps is faulty.

**[0058]** Alternatively or additionally, the third chip may include an edge die ring, and the edge die ring may comprise a metal conductor around a perimeter of the third chip. The edge die ring may be configured as the antenna. The edge die ring may have a first end and a second end, positioned such that they form a gap with respect to one another; wherein the first end is coupled to a first terminal of the third chip and the second end is coupled to a second terminal of the second third chip.

**[0059]** Additional aspects of the disclosure will be shown by way of Example:

**[0060]** In Example 1, a multichip package, comprising a first chip; a second chip; a third chip, electrically conductively coupled to the first chip and the second chip, the third chip comprising, an antenna; a multiplexer, configured to selectively couple the third chip to the first chip or the second chip; a first power combiner, configured to generate a first combined signal comprising a first antenna signal and a first baseband signal, and to output the first combined signal to the first chip; and a second power combiner, configured to generate a second combined signal comprising a second antenna signal and a second baseband signal, and to output the second combined signal to the second chip.

**[0061]** In Example 2, the multichip package of claim 1, wherein the third chip further comprises an oscillator, configured to generate an oscillator output signal, and wherein the third chip is configured to output the oscillator output signal to the first chip or the second chip.

**[0062]** In Example 3, the multichip package of claim 1 or 2, wherein the first chip comprises a first filter circuit, configured to separate the first combined signal into the first antenna signal and the first baseband signal.

**[0063]** In Example 4, the multichip package of any one of claims 1 to 3, wherein the second chip comprises a second filter circuit, configured to separate the second combined signal into the second antenna signal and the second baseband signal.

**[0064]** In Example 5, the multichip package of any one of claims 1 to 4: wherein the first antenna signal is a modulated first test signal; wherein the second antenna signal is a modulated second test signal; wherein the first chip further comprises a first demodulator, configured to recover the first test signal from the first antenna signal; and wherein the second chip further comprises a second demodulator, configured to recover the second test signal from the second antenna signal.

**[0065]** In Example 6, the multichip package of any one of claims 1 to 5, wherein the first antenna signal comprises two or more different frequency bands of modulated signals

**[0066]** In Example 7, the multichip package of any one of claims 1 to 6, wherein the first antenna signal comprises a wide-band signal which comprises modulated signal from at least two frequency bands.

**[0067]** In Example 8, the multichip package of any one of claims 1 to 7, wherein the multichip package comprises a first electrically conductive path between the multiplexer of the third chip and the first chip, and a second electrically conductive path between the multiplexer of the third chip and the second chip.

**[0068]** In Example 9, the multichip package of any one of claims 1 to 7, wherein the multichip package comprises an electrically conductive path between the third chip and both of the first chip and the second chip.

**[0069]** In Example 10, the multichip package of any one of claims 1 to 9, wherein the antenna is formed on rigid, flexible, hybrid printed circuit board.

**[0070]** In Example 11, the multichip package of any one of claims 1 to 9, wherein the antenna is formed on the multichip package.

**[0071]** In Example 12, the multichip package of any one of claims 1 to 11, wherein the antenna is formed on the third chip.

**[0072]** In Example 13, the multichip package of any one of claims 1 to 12, further comprising two antennas, configured to support multi-band modulated signals or multiple number of wireless links simultaneously.

**[0073]** In Example 14, the multichip package of any one of claims 1 to 13, further comprising a first underfill layer beneath the first die; wherein the first underfill layer comprises a plurality of first microbumps; and wherein, in response to the first test signal, the first chip is configured to excite a first microbump of the first plurality of microbumps and to receive a first microbump excitation signal received at a second microbump of the first plurality of microbumps.

**[0074]** In Example 15, the multichip package of claim 14, wherein the first microbump excitation signal is generated by a radiofrequency emission resulting from the excitation of the first microbump of the first plurality of microbumps; wherein the first chip is further configured to determine from the first microbump excitation signal whether a microbump of the first plurality of microbumps is faulty.

**[0075]** In Example 16, the multichip package of claim 15, wherein the first chip determining whether the microbump of the first plurality of microbumps is faulty comprises the first chip performing a transform of the first microbump excitation signal from a time domain into a frequency domain.

**[0076]** In Example 17, the multichip package of claim 16, wherein the first chip determining whether the microbump of the first plurality of microbumps is faulty further comprises comparing the transform of the first microbump excitation signal into the frequency domain with a predetermined pattern; wherein if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined pattern is within a range, the first chip is configured to generate a signal representing a determination that the microbumps of the first underfill layer are acceptable, and if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined pattern is outside the range, the first chip is configured to generate a signal representing a determination that the microbumps of the first underfill layer are unacceptable.

**[0077]** In Example 18, the multichip package of any one of claims 14 to 17, further comprising a second underfill layer beneath the second die; wherein the second underfill layer comprises a plurality of second microbumps; and wherein, in response to the second test signal, the second chip is configured to excite a first microbump of the second plurality of microbumps and to receive a second microbump excitation signal received at a second microbump of the second plurality of microbumps.

**[0078]** In Example 19, the multichip package of claim 18, wherein the second microbump excitation signal is generated by a radiofrequency emission resulting from the excitation of the first microbump of the second plurality of microbumps; wherein the second chip is further configured to determine from the second microbump excitation signal whether a microbump of the second plurality of microbumps is faulty.

**[0079]** In Example 20, the multichip package of claim 19, wherein the first chip determining whether the microbump of the second plurality of microbumps is faulty comprises the first chip performing a transform of the first microbump excitation signal from a time domain into a frequency domain.

**[0080]** In Example 21, the multichip package of claim 20, wherein the first chip determining whether the microbump of the second plurality of microbumps is faulty further comprises comparing the transform of the second microbump excitation signal into the frequency domain with a predetermined pattern; wherein if a similarly between the transform of the second microbump excitation signal into the frequency domain and the predetermined pattern is within a range, the second chip is configured to generate a signal representing a determination that the microbumps of the second underfill layer are acceptable, and if a similarly between the transform of the second microbump excitation signal into the frequency domain and the predetermined pattern is outside the range, the second chip is configured to generate a signal representing a determination that the microbumps of the second underfill layer are unacceptable.

**[0081]** In Example 22, the multichip package of any one of claims 1 to 21, wherein the third chip comprises an edge die ring, and wherein the edge die ring comprises a metal conductor around a perimeter of the third chip; wherein the edge die ring is configured as the antenna.

**[0082]** In Example 23, the multichip package of claim 22, wherein the edge die ring has a first end and a second end, positioned such that they form a gap with respect to one

another; wherein the first end is coupled to a first terminal of the third chip and the second end is coupled to a second terminal of the second third chip.

**[0083]** In Example 24, the multichip package of claim 23, further comprising a capacitor between the first end and the second end, wherein the capacitor is configured to tune an impedance of the antenna.

**[0084]** In Example 25, the multichip package of claim 23 or 24, wherein the capacitor is a first capacitor; further comprising a second capacitor along a connection between the first end and the first terminal of the third chip, and a third capacitor along a connection between the second end and the second terminal of the second chip.

**[0085]** In Example 26, the multichip package of any one of claims 1 to 25, wherein the first die further comprises a modulator, configured to modulate a test signal, and to send the modulated test signal to the third chip for transmission via the antenna.

**[0086]** In Example 27, the multichip package of claim 26, wherein the first chip is configured to receive the oscillator signal from the third chip, and wherein the first chip modulating the test signal comprises the first chip modulating the test signal using the received oscillator signal.

**[0087]** In Example 28, the multichip package of claim 26 or 27, wherein the second die further comprises a modulator, configured to modulate a test signal, and to send the modulated test signal to the third chip for transmission via the antenna.

**[0088]** In Example 29, the multichip package of claim 28, wherein the second chip is configured to receive the oscillator signal from the third chip, and wherein the second chip modulating the test signal comprises the second chip modulating the test signal using the received oscillator signal.

**[0089]** In Example 30, a multichip package, comprising: a first processing means; a second processing means; a third processing means, electrically conductively connected to the first processing means and the second processing means, the third processing

means comprising: an antenna; a multiplexing means, configured to selectively couple the third processing means to the first processing means or the second processing means; a first power combiner, configured to generate a first combined signal comprising a first antenna signal and a first baseband signal, and to output the first combined signal to the first processing means; and a second power combiner, configured to generate a second combined signal comprising a second antenna signal and a second baseband signal, and to output the second combined signal to the second processing means.

**[0090]** In Example 31, the multichip package of claim 30, wherein the third processing means further comprises an oscillator, configured to generate an oscillator output signal, and wherein the third processing means is configured to output the oscillator output signal to the first processing means or the second processing means.

**[0091]** In Example 32, the multichip package of claim 30 or 31, wherein the first processing means comprises a first filter circuit, configured to separate the first combined signal into the first antenna signal and the first baseband signal.

**[0092]** In Example 33, the multichip package of any one of claims 30 to 32, wherein the second processing means comprises a second filter circuit, configured to separate the second combined signal into the second antenna signal and the second baseband signal.

**[0093]** In Example 34, the multichip package of any one of claims 30 to 33: wherein the first antenna signal is a modulated first test signal; wherein the second antenna signal is a modulated second test signal; wherein the first processing means further comprises a first demodulator, configured to recover the first test signal from the first antenna signal; and wherein the second processing means further comprises a second demodulator, configured to recover the second test signal from the second antenna signal.

**[0094]** In Example 35, the multichip package of any one of claims 30 to 34, wherein the first antenna signal comprises two or more different frequency bands of modulated signals

**[0095]** In Example 36, the multichip package of any one of claims 30 to 35, wherein the first antenna signal comprises a wide-band signal which comprises modulated signal from at least two frequency bands.

**[0096]** In Example 37, the multichip package of any one of claims 30 to 36, wherein the multichip package comprises a first electrically conductive path between the multiplexing means of the third processing means and the first processing means, and a second electrically conductive path between the multiplexing means of the third processing means and the second processing means.

**[0097]** In Example 38, the multichip package of any one of claims 30 to 36, wherein the multichip package comprises an electrically conductive path between the third processing means and both of the first processing means and the second processing means.

**[0098]** In Example 39, the multichip package of any one of claims 30 to 38, wherein the antenna is formed on rigid, flexible, hybrid printed circuit board.

**[0099]** In Example 40, the multichip package of any one of claims 30 to 38, wherein the antenna is formed on the multichip package.

**[0100]** In Example 41, the multichip package of any one of claims 30 to 40, wherein the antenna is formed on the third processing means.

**[0101]** In Example 42, the multichip package of any one of claims 30 to 41, further comprising two antennas, configured to support multi-band modulated signals or multiple number of wireless links simultaneously.

**[0102]** In Example 43, the multichip package of any one of claims 30 to 42, further comprising a first underfill layer beneath the first die; wherein the first underfill layer comprises a plurality of first microbumps; and wherein, in response to the first test signal, the first processing means is configured to excite a first microbump of the first plurality of microbumps and to receive a first microbump excitation signal received at a second microbump of the first plurality of microbumps.

**[0103]** In Example 44, the multichip package of claim 43, wherein the first microbump excitation signal is generated by a radiofrequency emission resulting from the excitation of the first microbump of the first plurality of microbumps; wherein the first processing means is further configured to determine from the first microbump excitation signal whether a microbump of the first plurality of microbumps is faulty.

**[0104]** In Example 45, the multichip package of claim 44, wherein the first processing means determining whether the microbump of the first plurality of microbumps is faulty comprises the first processing means performing a transform of the first microbump excitation signal from a time domain into a frequency domain.

**[0105]** In Example 46, the multichip package of claim 45, wherein the first processing means determining whether the microbump of the first plurality of microbumps is faulty further comprises comparing the transform of the first microbump excitation signal into the frequency domain with a predetermined pattern; wherein if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined pattern is within a range, the first processing means is configured to generate a signal representing a determination that the microbumps of the first underfill layer are acceptable, and if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined pattern is outside the range, the first processing means is configured to generate a signal representing a determination that the microbumps of the first underfill layer are unacceptable.

**[0106]** In Example 47, the multichip package of any one of claims 43 to 46, further comprising a second underfill layer beneath the second die; wherein the second underfill layer comprises a plurality of second microbumps; and wherein, in response to the second test signal, the second processing means is configured to excite a first microbump of the second plurality of microbumps and to receive a second microbump excitation signal received at a second microbump of the second plurality of microbumps.

**[0107]** In Example 48, the multichip package of claim 47, wherein the second microbump excitation signal is generated by a radiofrequency emission resulting from the excitation of the first microbump of the second plurality of microbumps; wherein the second processing means is further configured to determine from the second microbump excitation signal whether a microbump of the second plurality of microbumps is faulty.

**[0108]** In Example 49, the multichip package of claim 48, wherein the first processing means determining whether the microbump of the second plurality of microbumps is faulty comprises the first processing means performing a transform of the first microbump excitation signal from a time domain into a frequency domain.

**[0109]** In Example 50, the multichip package of claim 49, wherein the first processing means determining whether the microbump of the second plurality of microbumps is faulty further comprises comparing the transform of the second microbump excitation signal into the frequency domain with a predetermined pattern; wherein if a similarly between the transform of the second microbump excitation signal into the frequency domain and the predetermined pattern is within a range, the second processing means is configured to generate a signal representing a determination that the microbumps of the second underfill layer are acceptable, and if a similarly between the transform of the second microbump excitation signal into the frequency domain and the predetermined pattern is outside the range, the second processing means is configured to generate a signal representing a determination that the microbumps of the second underfill layer are unacceptable.

**[0110]** In Example 51, the multichip package of any one of claims 30 to 50, wherein the third processing means comprises an edge die ring, and wherein the edge die ring comprises a metal conductor around a perimeter of the third processing means; wherein the edge die ring is configured as the antenna.

**[0111]** In Example 52, the multichip package of claim 51, wherein the edge die ring has a first end and a second end, positioned such that they form a gap with respect to one another; wherein the first end is coupled to a first terminal of the third processing means and the second end is coupled to a second terminal of the second third processing means.

**[0112]** In Example 53, the multichip package of claim 52, further comprising a capacitor between the first end and the second end, wherein the capacitor is configured to tune an impedance of the antenna.

**[0113]** In Example 54, the multichip package of claim 52 or 53, wherein the capacitor is a first capacitor; further comprising a second capacitor along a connection between the first end and the first terminal of the third processing means, and a third capacitor along a connection between the second end and the second terminal of the second processing means.

**[0114]** In Example 55, the multichip package of any one of claims 30 to 54, wherein the first die further comprises a modulator, configured to modulate a test signal, and to send the modulated test signal to the third processing means for transmission via the antenna.

**[0115]** In Example 56, the multichip package of claim 55, wherein the first processing means is configured to receive the oscillator signal from the third processing means, and wherein the first processing means modulating the test signal comprises the first processing means modulating the test signal using the received oscillator signal.

**[0116]** In Example 57, the multichip package of claim 55 or 56, wherein the second die further comprises a modulator, configured to modulate a test signal, and to send the modulated test signal to the third processing means for transmission via the antenna.

**[0117]** In Example 58, the multichip package of claim 57, wherein the second processing means is configured to receive the oscillator signal from the third processing means, and wherein the second processing means modulating the test signal comprises the second processing means modulating the test signal using the received oscillator signal.

**[0118]** In Example 59, a method of manufacturing a multichip package, comprising: providing a first chip; providing a second chip; providing a third chip, electrically conductively connected to the first chip and the second chip; selectively coupling the third chip to the first chip or the second chip; generating a first combined signal comprising a first antenna signal and a first baseband signal, and outputting the first combined signal to the first chip; and generating a second combined signal comprising a second antenna signal and a second baseband signal, and outputting the second combined signal to the second chip.

**[0119]** In Example 60, the method of manufacturing a multichip package of claim 59, further comprising generating an oscillator output signal, and outputting via the third chip the oscillator output signal to the first chip or the second chip.

**[0120]** In Example 61, the method of manufacturing a multichip package of claim 59 or 60, further comprising separating the first combined signal into the first antenna signal and the first baseband signal.

**[0121]** In Example 62, the method of manufacturing a multichip package of any one of claims 59 to 61, further comprising separating the second combined signal into the second antenna signal and the second baseband signal.

**[0122]** In Example 63, the method of manufacturing a multichip package of any one of claims 59 to 62: wherein the first antenna signal is a modulated first test signal; wherein the second antenna signal is a modulated second test signal; further comprising recovering the first test signal from the first antenna signal; and recovering the second test signal from the second antenna signal.

**[0123]** In Example 64, the method of manufacturing a multichip package of any one of claims 59 to 63, wherein the first antenna signal comprises two different frequency bands of modulated signals

**[0124]** In Example 65, the method of manufacturing a multichip package of any one of claims 59 to 64, wherein the first antenna signal comprises a wide-band signal which comprises modulated signal from at least two frequency bands.

**[0125]** In Example 66, the method of manufacturing a multichip package of any one of claims 59 to 65, further comprising providing a first electrically conductive path between the multiplexer of the third chip and the first chip, and a second electrically conductive path between the multiplexer of the third chip and the second chip.

**[0126]** In Example 67, the method of manufacturing a multichip package of any one of claims 59 to 65, further comprising providing an electrically conductive path between the third chip and both of the first chip and the second chip.

**[0127]** In Example 68, the method of manufacturing a multichip package of any one of claims 59 to 67, further comprising forming the antenna on a rigid, flexible, hybrid printed circuit board.

**[0128]** In Example 69, the method of manufacturing a multichip package of any one of claims 59 to 67, further comprising forming the antenna on the multichip package.

**[0129]** In Example 70, the method of manufacturing a multichip package of any one of claims 59 to 69, further comprising forming the antenna on the third chip.

**[0130]** In Example 71, the method of manufacturing a multichip package of any one of claims 59 to 70, further comprising providing two antennas, configured to support multi-band modulated signals or multiple number of wireless links simultaneously.

**[0131]** In Example 72, the method of manufacturing a multichip package of any one of claims 59 to 71, further comprising providing a first underfill layer beneath the first die; in response to the first test signal, exciting a first microbump of the first plurality of microbumps and receiving a first microbump excitation signal at a second microbump of the first plurality of microbumps.

**[0132]** In Example 73, the method of manufacturing a multichip package of claim 72, further comprising generating the first microbump excitation signal by a radiofrequency emission resulting from the excitation of the first microbump of the first plurality of microbumps; and determining from the first microbump excitation signal whether a microbump of the first plurality of microbumps is faulty.

**[0133]** In Example 74, the method of manufacturing a multichip package of claim 73, wherein determining whether the microbump of the first plurality of microbumps is faulty comprises performing a transform of the first microbump excitation signal from a time domain into a frequency domain.

**[0134]** In Example 75, the method of manufacturing a multichip package of claim 74, wherein determining whether the microbump of the first plurality of microbumps is faulty further comprises comparing the transform of the first microbump excitation signal into the frequency domain with a predetermined pattern; wherein if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined pattern is within a range, further comprising generating a signal representing a determination that the microbumps of the first underfill layer are acceptable, and if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined pattern is outside the range, further comprising generating a signal representing a determination that the microbumps of the first underfill layer are unacceptable.

**[0135]** In Example 76, the method of manufacturing a multichip package of any one of claims 72 to 75, further comprising, in response to the second test signal, exciting a first microbump of the second plurality of microbumps and receiving a second microbump excitation signal received at a second microbump of the second plurality of microbumps.

**[0136]** In Example 77, the method of manufacturing a multichip package of claim 76, further comprising generating the second microbump excitation signal by a

radiofrequency emission resulting from the excitation of the first microbump of the second plurality of microbumps; and determining from the second microbump excitation signal whether a microbump of the second plurality of microbumps is faulty.

**[0137]** In Example 78, the method of manufacturing a multichip package of claim 77, wherein the determining whether the microbump of the second plurality of microbumps is faulty comprises performing a transform of the first microbump excitation signal from a time domain into a frequency domain.

**[0138]** In Example 79, the method of manufacturing a multichip package of claim 78, wherein the determining whether the microbump of the second plurality of microbumps is faulty further comprises comparing the transform of the second microbump excitation signal into the frequency domain with a predetermined pattern; wherein if a similarly between the transform of the second microbump excitation signal into the frequency domain and the predetermined pattern is within a range, further comprising generating a signal representing a determination that the microbumps of the second underfill layer are acceptable, and if a similarly between the transform of the second microbump excitation signal into the frequency domain and the predetermined pattern is outside the range, further comprising generating a signal representing a determination that the microbumps of the second underfill layer are unacceptable.

**[0139]** In Example 80, the method of manufacturing a multichip package of any one of claims 59 to 79, further comprising providing an edge die ring having a metal conductor around a perimeter of the third chip and configuring the edge die ring as the antenna.

**[0140]** In Example 81, the method of manufacturing a multichip package of claim 80, wherein the edge die ring has a first end and a second end, positioned such that they form a gap with respect to one another; further comprising coupling the first end to a first terminal of the third chip and coupling the second end to a second terminal of the second third chip.

**[0141]** In Example 82, the method of manufacturing a multichip package of claim 81, further comprising providing a capacitor between the first end and the second end and configuring the capacitor to tune an impedance of the antenna.

**[0142]** In Example 83, the method of manufacturing a multichip package of claim 81 or 82, wherein the capacitor is a first capacitor; further comprising providing a second capacitor along a connection between the first end and the first terminal of the third chip, and providing a third capacitor along a connection between the second end and the second terminal of the second chip.

**[0143]** In Example 84, the method of manufacturing a multichip package of any one of claims 59 to 83, further comprising modulating a test signal and sending the modulated test signal to the third chip for transmission via the antenna.

**[0144]** In Example 85, the method of manufacturing a multichip package of claim 84, further comprising receiving the oscillator signal from the third chip, and modulating the test signal using the received oscillator signal.

**[0145]** In Example 86, the method of manufacturing a multichip package of claim 84 or 85, further comprising modulating a test signal and sending the modulated test signal to the third chip for transmission via the antenna.

**[0146]** In Example 87, the method of manufacturing a multichip package of claim 86, further comprising modulating the test signal using the received oscillator signal.

**[0147]** While the above descriptions and connected figures may depict components as separate elements, skilled persons will appreciate the various possibilities to combine or integrate discrete elements into a single element. Such may include combining two or more circuits for form a single circuit, mounting two or more circuits onto a common chip or chassis to form an integrated element, executing discrete software components on a common processor core, etc. Conversely, skilled persons will recognize the possibility to separate a single element into two or more discrete elements, such as splitting a single circuit into two or

more separate circuits, separating a chip or chassis into discrete elements originally provided thereon, separating a software component into two or more sections and executing each on a separate processor core, etc.

**[0148]** It is appreciated that implementations of methods detailed herein are demonstrative in nature, and are thus understood as capable of being implemented in a corresponding device. Likewise, it is appreciated that implementations of devices detailed herein are understood as capable of being implemented as a corresponding method. It is thus understood that a device corresponding to a method detailed herein may include one or more components configured to perform each aspect of the related method.

**[0149]** All acronyms defined in the above description additionally hold in all claims included herein.

# CLAIMS

What is claimed is:

1. A multichip package, comprising:
a first chip;
a second chip;
a third chip, electrically conductively coupled to the first chip and the second chip, the third chip comprising:
an antenna;
a multiplexer, configured to selectively couple the third chip to the first chip or the second chip;
a first power combiner, configured to generate a first combined signal comprising a first antenna signal and a first baseband signal, and to output the first combined signal to the first chip; and
a second power combiner, configured to generate a second combined signal comprising a second antenna signal and a second baseband signal, and to output the second combined signal to the second chip.

2. The multichip package of claim 1, wherein the third chip further comprises an oscillator, configured to generate an oscillator output signal, and wherein the third chip is configured to output the oscillator output signal to the first chip or the second chip.

3. The multichip package of claim 1 or 2, wherein the first chip comprises a first filter circuit, configured to separate the first combined signal into the first antenna signal and the first baseband signal; and wherein the second chip comprises a second filter circuit, configured to separate the second combined signal into the second antenna signal and the second baseband signal.

4. The multichip package of any one of claims 1 to 3:
wherein the first antenna signal is a modulated first test signal;
wherein the second antenna signal is a modulated second test signal;
wherein the first chip further comprises a first demodulator, configured to recover the first test signal from the first antenna signal; and

wherein the second chip further comprises a second demodulator, configured to recover the second test signal from the second antenna signal.

5. The multichip package of any one of claims 1 to 4, wherein the first antenna signal comprises two different frequency bands of modulated signals

6. The multichip package of any one of claims 1 to 4, wherein the multichip package comprises an electrically conductive path between the third chip and both of the first chip and the second chip.

7. The multichip package of any one of claims 1 to 6, further comprising two antennas, configured to support multi-band modulated signals or multiple number of wireless links simultaneously.

8. The multichip package of any one of claims 1 to 7, further comprising a first underfill layer beneath the first die;
wherein the first underfill layer comprises a plurality of first microbumps; and
wherein, in response to the first test signal, the first chip is configured to excite a first microbump of the first plurality of microbumps and to receive a first microbump excitation signal received at a second microbump of the first plurality of microbumps.

9. The multichip package of claim 8, wherein the first microbump excitation signal is generated by a radiofrequency emission resulting from the excitation of the first microbump of the first plurality of microbumps;
wherein the first chip is further configured to determine from the first microbump excitation signal whether a microbump of the first plurality of microbumps is faulty.

10. The multichip package of claim 9, wherein the first chip determining whether the microbump of the first plurality of microbumps is faulty comprises the first chip performing a transform of the first microbump excitation signal from a time domain into a frequency domain;
comparing the transform of the first microbump excitation signal into the frequency domain with a predetermined pattern; wherein if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined

pattern is within a range, the first chip is configured to generate a signal representing a determination that the microbumps of the first underfill layer are acceptable, and if a similarly between the transform of the first microbump excitation signal into the frequency domain and the predetermined pattern is outside the range, the first chip is configured to generate a signal representing a determination that the microbumps of the first underfill layer are unacceptable.

11. The multichip package of any one of claims 7 to 10, further comprising a second underfill layer beneath the second die;
wherein the second underfill layer comprises a plurality of second microbumps; and
wherein, in response to the second test signal, the second chip is configured to excite a first microbump of the second plurality of microbumps and to receive a second microbump excitation signal received at a second microbump of the second plurality of microbumps;
wherein the second microbump excitation signal is generated by a radiofrequency emission resulting from the excitation of the first microbump of the second plurality of microbumps;
wherein the second chip is further configured to determine from the second microbump excitation signal whether a microbump of the second plurality of microbumps is faulty; and
wherein the first chip determining whether the microbump of the second plurality of microbumps is faulty comprises the first chip performing a transform of the first microbump excitation signal from a time domain into a frequency domain.

12. The multichip package of claim 11, wherein the first chip determining whether the microbump of the second plurality of microbumps is faulty further comprises comparing the transform of the second microbump excitation signal into the frequency domain with a predetermined pattern;
wherein if a similarly between the transform of the second microbump excitation signal into the frequency domain and the predetermined pattern is within a range, the second chip is configured to generate a signal representing a determination that the microbumps of the second underfill layer are acceptable, and if a similarly between the transform of the second microbump excitation signal into the frequency domain and the predetermined pattern is outside the range, the second chip is configured to generate a signal

representing a determination that the microbumps of the second underfill layer are unacceptable.

13. The multichip package of any one of claims 1 to 12, wherein the third chip comprises an edge die ring, and wherein the edge die ring comprises a metal conductor around a perimeter of the third chip;
wherein the edge die ring is configured as the antenna.

14. The multichip package of claim 13, wherein the edge die ring has a first end and a second end, positioned such that they form a gap with respect to one another; wherein the first end is coupled to a first terminal of the third chip and the second end is coupled to a second terminal of the second third chip.

15. The multichip package of claim 14, further comprising a capacitor between the first end and the second end, wherein the capacitor is configured to tune an impedance of the antenna.

16. The multichip package of claim 14 or 15, wherein the capacitor is a first capacitor; further comprising a second capacitor along a connection between the first end and the first terminal of the third chip, and a third capacitor along a connection between the second end and the second terminal of the second chip.

17. The multichip package of any one of claims 1 to 16, wherein the first die further comprises a modulator, configured to modulate a test signal, and to send the modulated test signal to the third chip for transmission via the antenna;
wherein the first chip is configured to receive the oscillator signal from the third chip, and wherein the first chip modulating the test signal comprises the first chip modulating the test signal using the received oscillator signal.

18. The multichip package of claim 16 or 17, wherein the second die further comprises a modulator, configured to modulate a test signal, and to send the modulated test signal to the third chip for transmission via the antenna;

wherein the second chip is configured to receive the oscillator signal from the third chip, and wherein the second chip modulating the test signal comprises the second chip modulating the test signal using the received oscillator signal.

19. A multichip package, comprising:
a first processing means;
a second processing means;
a third processing means, electrically conductively coupled to the first processing means and the second processing means, the third processing means comprising:

an antenna; a multiplexing means, configured to selectively couple the third processing means to the first processing means or the second processing means; a first power combiner, configured to generate a first combined signal comprising a first antenna signal and a first baseband signal, and to output the first combined signal to the first processing means; and a second power combiner, configured to generate a second combined signal comprising a second antenna signal and a second baseband signal, and to output the second combined signal to the second processing means.

20. The multichip package of claim 19, wherein the third processing means further comprises an oscillator, configured to generate an oscillator output signal, and wherein the third processing means is configured to output the oscillator output signal to the first processing means or the second processing means.

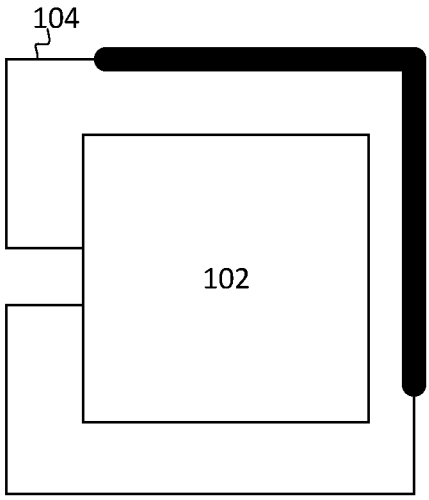



FIG. 1

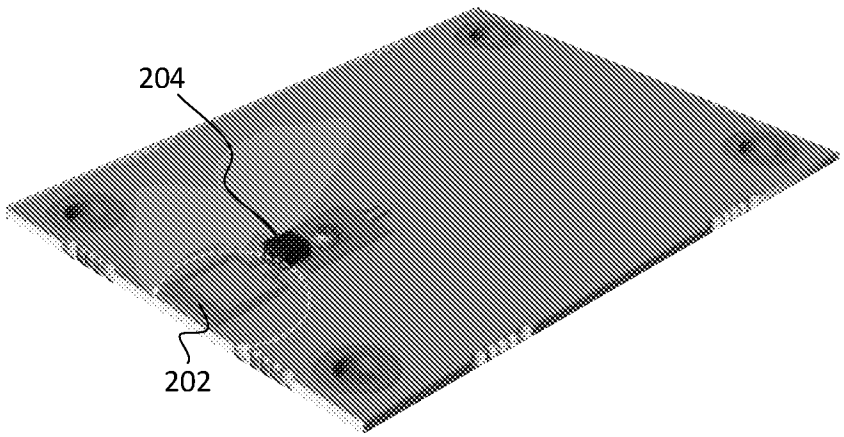



FIG. 2

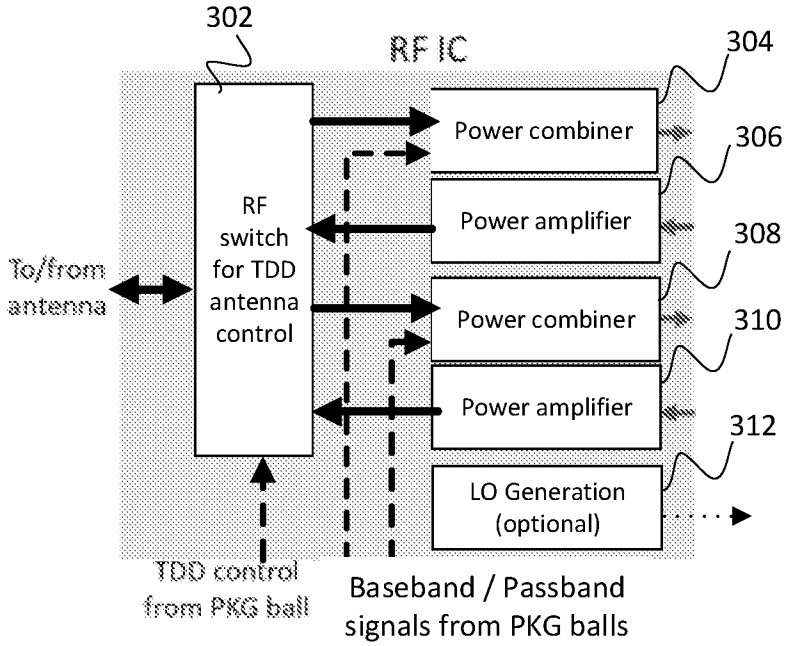
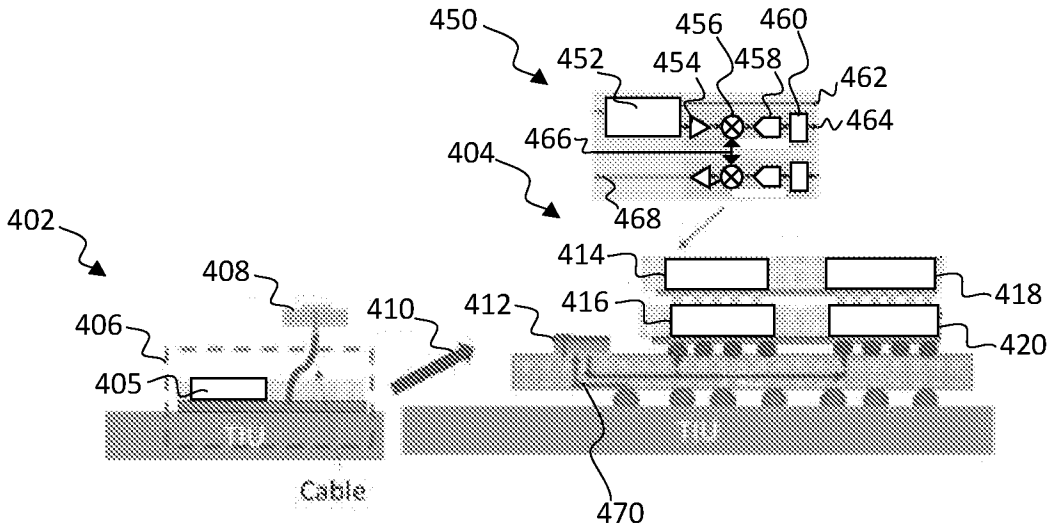

302
RF IC
304
Power combiner
306
RF switch for TDD antenna control
Power amplifier
308
To/from antenna
Power combiner
310
Power amplifier
312
LO Generation (optional)
TDD control from PKG ball
Baseband / Passband signals from PKG balls

FIG. 3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420
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Cable
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FIG. 4

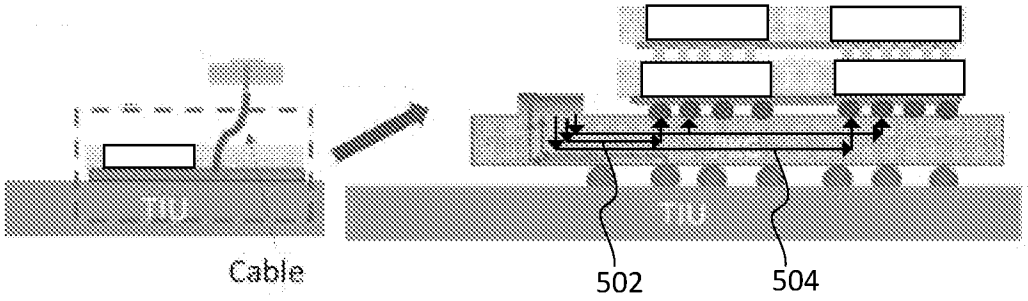


FIG. 5

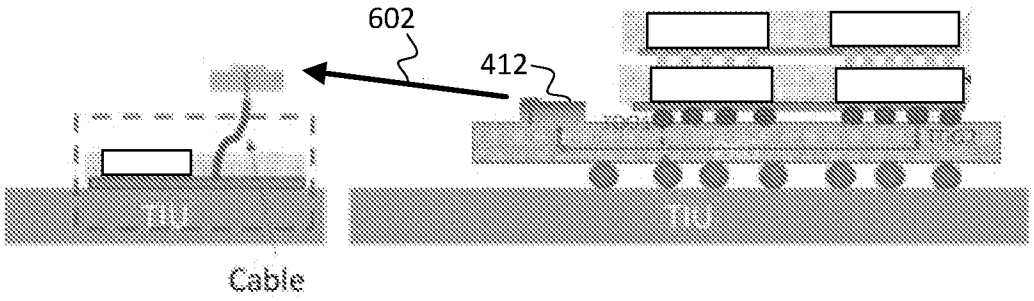


FIG. 6

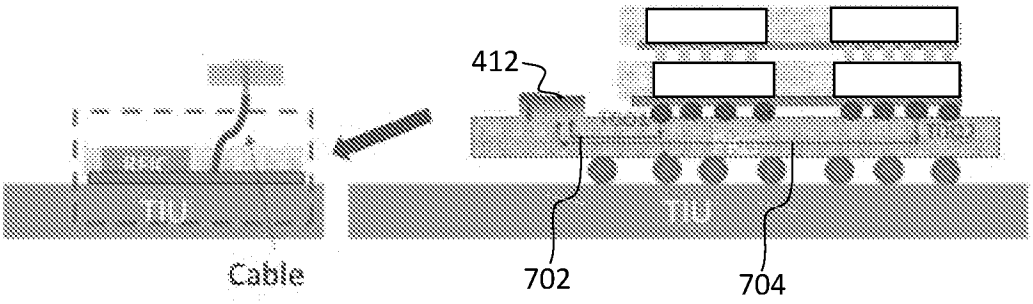


FIG. 7

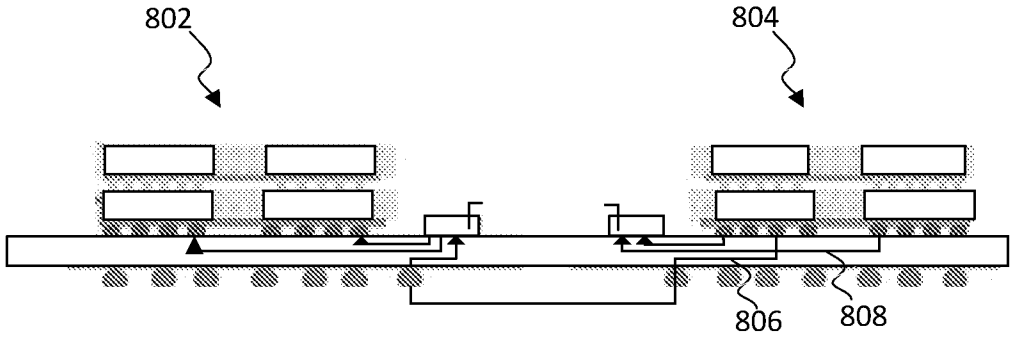


FIG. 8

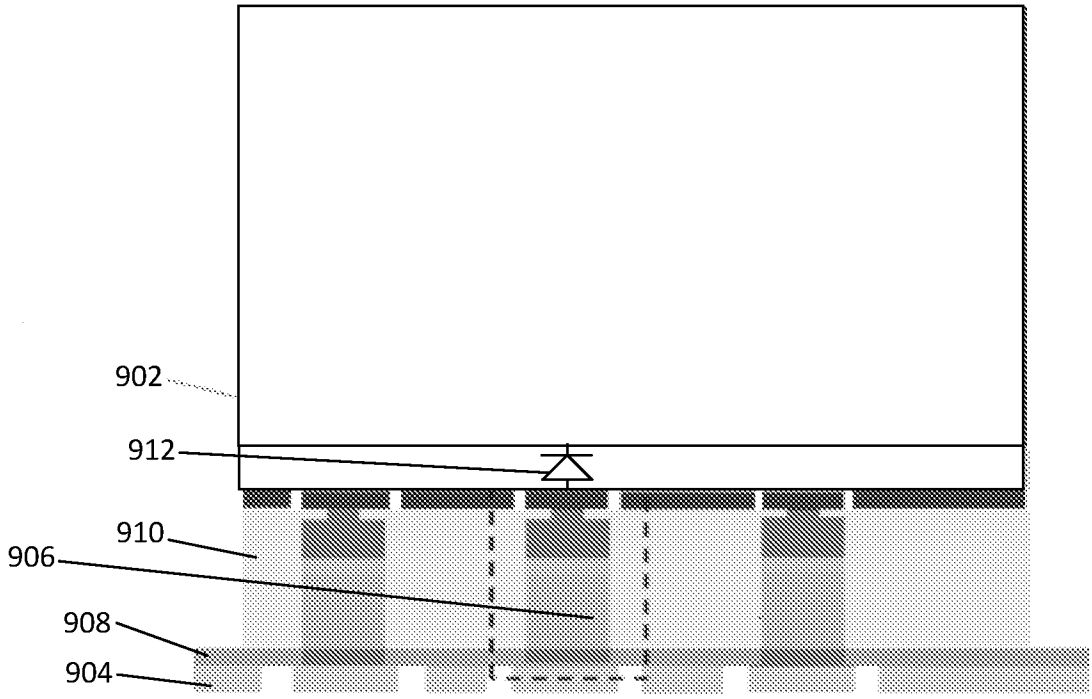


FIG. 9

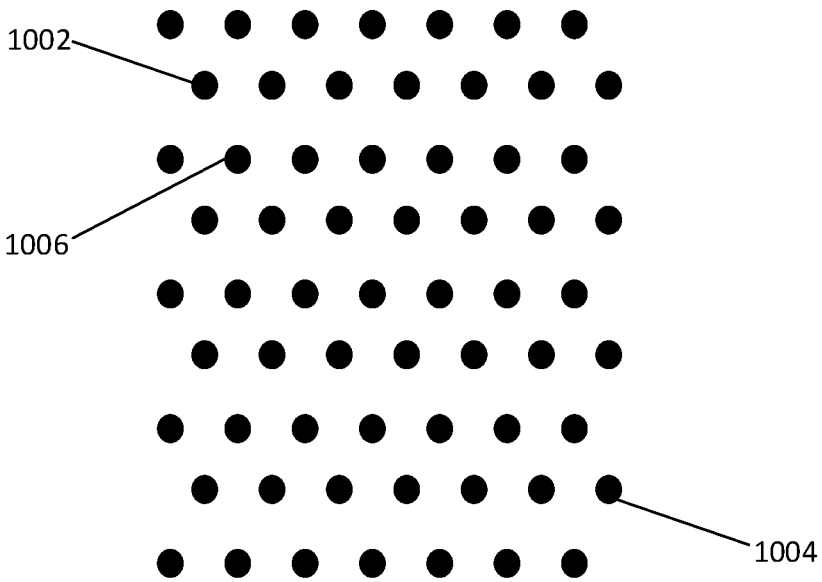


FIG. 10

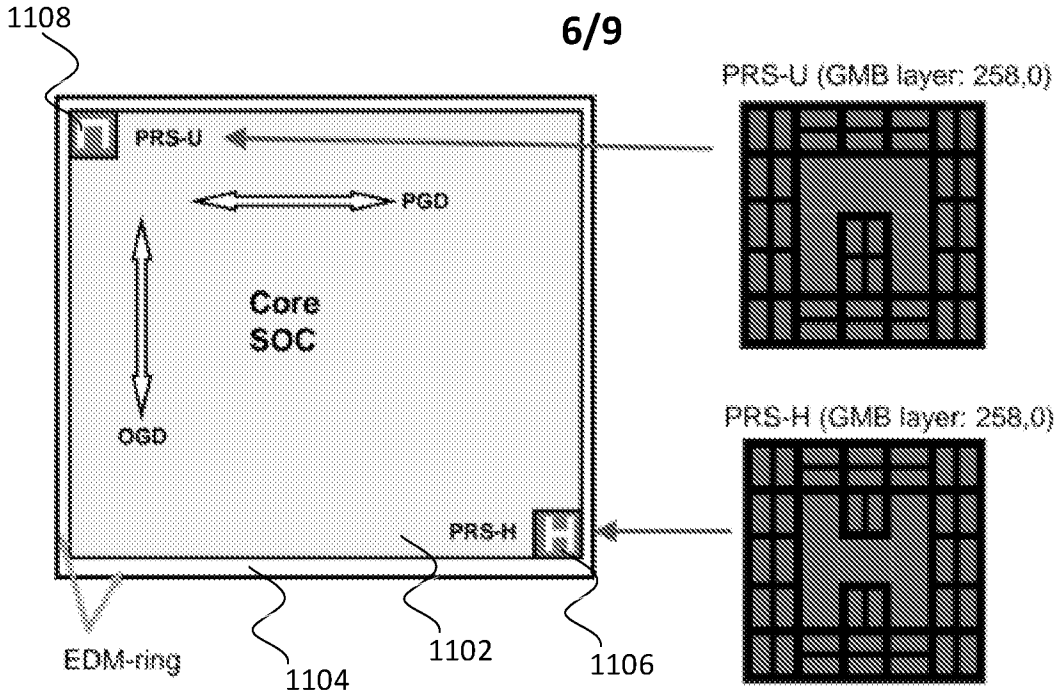
1108
PRS-U (GMB layer: 258,0)
PRS-U
PGD
Core
SOC
OGD
PRS-H (GMB layer: 258,0)
PRS-H
EDM-ring
1104
1102
1106

FIG. 11

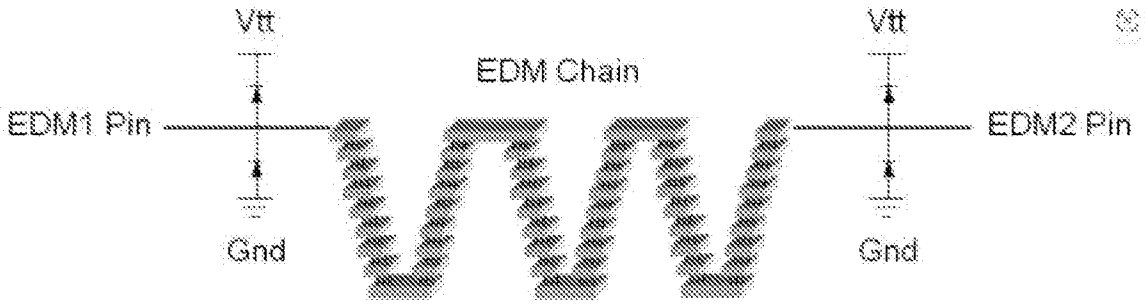
Vtt
EDM Chain
Vtt
EDM1 Pin
EDM2 Pin
Gnd
Gnd

FIG. 12

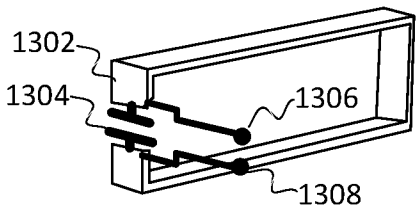


FIG. 13A

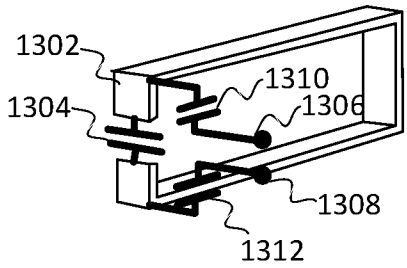


FIG. 13B

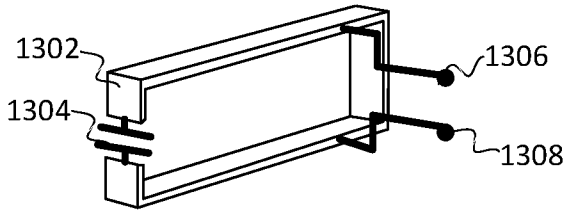


FIG. 13C

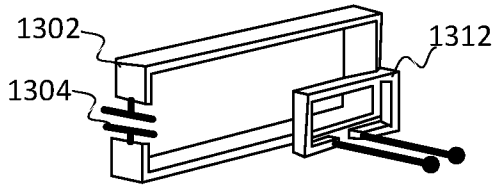


FIG. 13D

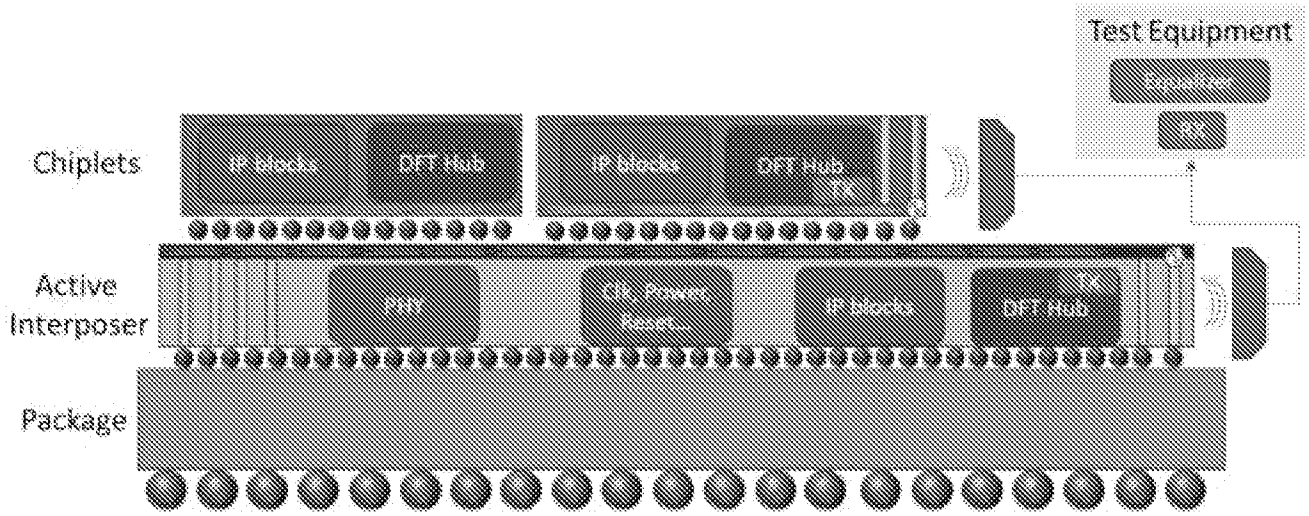


FIG. 14A

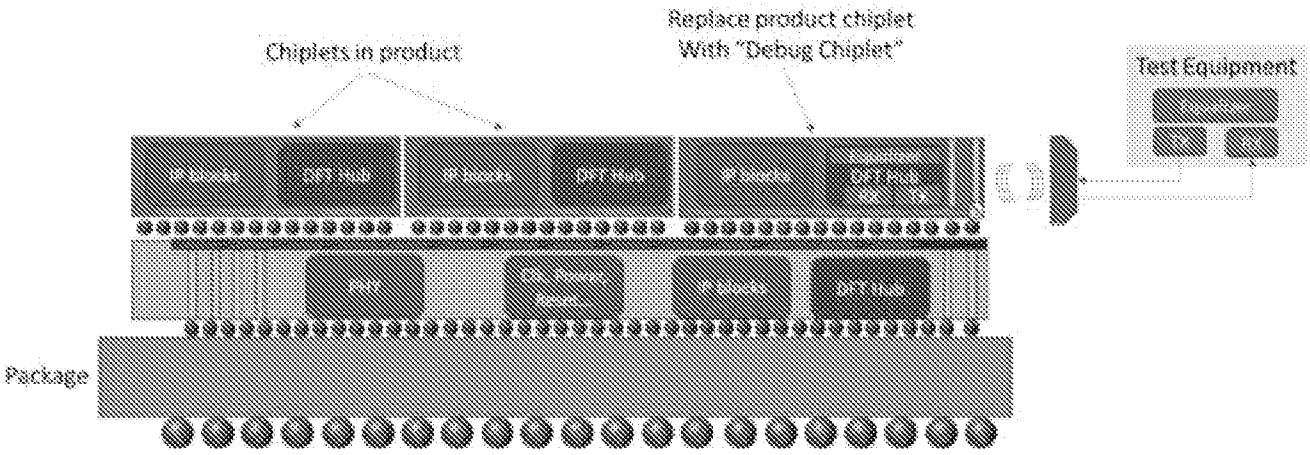


FIG. 14B

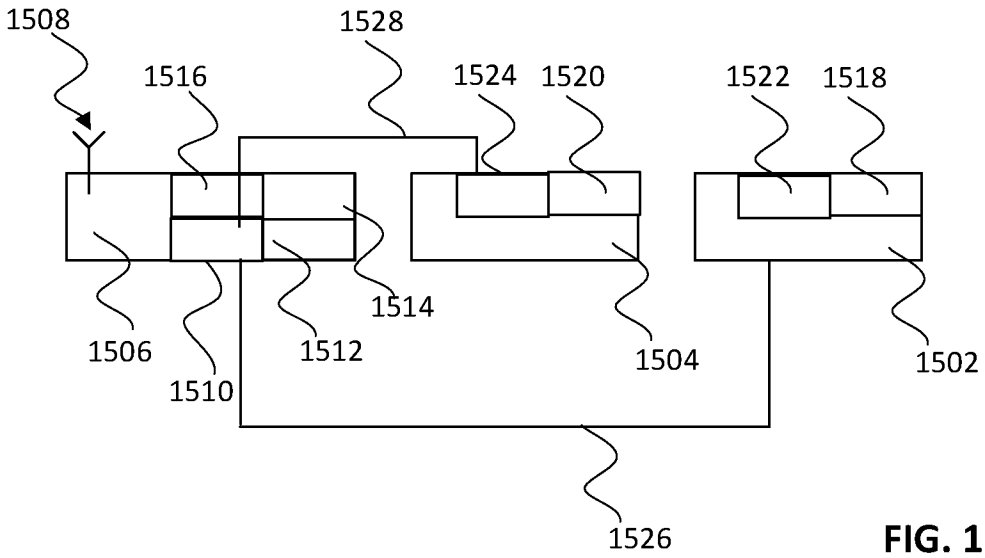
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FIG. 15

# INTERNATIONAL SEARCH REPORT

International application No.
**PCT/US2023/085599**

## A. CLASSIFICATION OF SUBJECT MATTER

**H01L 25/16**(2006.01)i; **H01L 25/065**(2006.01)i; **H01L 23/66**(2006.01)i; **H01L 23/538**(2006.01)i; **H01Q 1/22**(2006.01)i; **G01R 31/28**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/16(2006.01); G01R 31/28(2006.01); H01L 21/822(2006.01); H01Q 21/22(2006.01); H03F 3/24(2006.01); H04B 1/16(2006.01); H04B 1/401(2015.01); H04B 1/44(2006.01); H04L 5/14(2006.01); H04W 72/04(2009.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: antenna, multiplexer, power combiner, oscillator, filter, test signal, demodulator

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 2022-0021510 A1 (MURATA MANUFACTURING CO., LTD.) 20 January 2022 (2022-01-20)<br>See paragraph [0048] and figures 1-2B. | 1-20 |
| A | US 2023-0129253 A1 (INNOPHASE, INC.) 27 April 2023 (2023-04-27)<br>See paragraph [0051] and figure 3. | 1-20 |
| A | JP 2015-197365 A (DENSO CORP.) 09 November 2015 (2015-11-09)<br>See paragraphs [0009]-[0012] and figure 1. | 1-20 |
| A | US 2019-0028073 A1 (SAMSUNG ELECTRONICS CO., LTD.) 24 January 2019 (2019-01-24)<br>See paragraphs [0096]-[0098] and figure 6A. | 1-20 |
| A | US 2006-0035601 A1 (CHEOL-SOO SEO) 16 February 2006 (2006-02-16)<br>See paragraphs [0086]-[0088] and figure 5. | 1-20 |

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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