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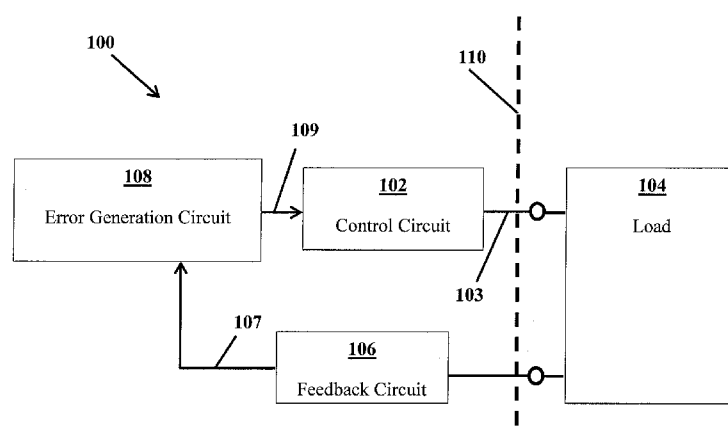


FIG. 1

(57) Abstract: Source measure units may operate as a voltage/current (V/I) source for a load, such as a device under test (DUT). Source measure units having a voltage controlled mode and a current controlled mode are described. The source measure units may have a suitable configuration to transition between the voltage controlled mode and current controlled mode in a smooth manner, and may be operated accordingly.

SMOOTH VI MODE CROSSOVER METHOD AT COMPLIANCE LIMIT THRESHOLD

RELATED APPLICATIONS

[0001] This Application claims priority to U.S. Application Serial No. 13/804,579, filed in the United States on March 14, 2013 under Attorney Docket No. T0529.70149US00 and entitled “SMOOTH VI MODE CROSSOVER METHOD AT COMPLIANCE LIMIT THRESHOLD,” which is hereby incorporated herein by reference in its entirety.

FIELD

[0002] The technology described herein relates to source measure units and methods of operation of the same.

RELATED ART

[0003] Source measure units (SMUs) are used in some automated test equipment (ATE) to provide a source voltage or current signal to a device under test (DUT).

SUMMARY

[0004] According to an aspect of the present application, a method of operating a source measure unit (SMU) configured to couple to a load is provided. The SMU may operate in a plurality of modes including a voltage-controlled mode and a current-controlled mode. The method may comprise generating a control signal to apply to a control circuit of the SMU when switching between the plurality of modes, wherein generating the control signal comprises generating the control signal based on both a voltage and a current.

[0005] According to an aspect of the present application, a source measure unit (SMU) configured to operate in a plurality of modes including a voltage-controlled mode and a current-controlled mode is provided. The SMU may comprise combination circuitry configured to generate, when the SMU transitions between the voltage-controlled mode and the current controlled mode, a control signal to provide to a control circuit of the SMU, the control signal being based on both a voltage and a current.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Various aspects and embodiments of the application will be described with reference to the following figures. It should be appreciated that the figures are not necessarily drawn to scale. Items appearing in multiple figures are indicated by the same reference number in all the figures in which they appear.

[0007] FIG. 1 illustrates a SMU according to a non-limiting embodiment coupled to a load.

[0008] FIG. 2 illustrates a method of operating a source measure unit (SMU) according to a non-limiting embodiment of the present application.

[0009] FIG. 3 illustrates a more detailed method expanding on the method of FIG. 2, according to a non-limiting embodiment.

[0010] FIG. 4 illustrates a non-limiting detailed implementation of the SMU of FIG. 1, according to a non-limiting embodiment of the present application.

[0011] FIG. 5 illustrates weighting factor behavior for weighting error signals, according to a non-limiting embodiment.

[0012] FIG. 6 provides an expanded view of a transition region from FIG. 5.

DETAILED DESCRIPTION

[0013] Some source measure units (SMUs) are operable as either a voltage source or a current source, and thus are sometimes referred to as V/I sources. The SMU may provide an output signal (sometimes referred to as a drive signal), for example to a load such as a DUT, having a voltage and a current. When operating as a voltage source, the voltage of the output signal applied across the load may be considered the main, and may be intended to assume a target value. The current through the load may be considered the limit, and may be intended to stay within a desired current range (e.g., upper and lower current thresholds or compliance limits which may be symmetrical or asymmetrical about zero). When operating as a current

source, the current of the output signal passing through the load may be considered the main, and may be intended to assume a target value. The voltage across the load may be considered the limit, and may be intended to stay within a desired voltage range (e.g., upper and lower voltage thresholds or compliance limits).

[0014] In a voltage controlled mode, the voltage across the load may be compared to the target voltage, and any difference between the two may be used to generate a control signal (e.g., within the SMU) to adjust the voltage of the output signal provided by the SMU. The current through the load may be monitored, but so long as it remains within the compliance limits may not impact the control signal.

[0015] In a current controlled mode, the current through the load may be compared to the target current, and any difference between the two may be used to generate a control signal (e.g., within the SMU) to adjust the current of the output signal provided by the SMU. The voltage across the load may be monitored, but so long as it remains within the compliance limits may not impact the control signal.

[0016] The SMUs may be switched between a voltage controlled mode and a current controlled mode, when the limit signal (the current in the voltage controlled mode scenario and the voltage in the current controlled mode scenario) falls outside the compliance limits. The limit signal then becomes the main signal and the main signal becomes the limit signal. Such behavior may be described as a switch between main control (when the value of the main signal dictates operation of the SMU) and limit control (when the value of the limit signal dictates operation of the SMU).

[0017] Applicants have appreciated that abrupt or discontinuous switching between the voltage controlled mode and the current controlled mode of the SMU can give rise to undesirable behavior. For example, discontinuous switching between a voltage controlled mode and a current controlled mode can cause noise in the output signal, chatter, oscillation, or other undesirable behaviors. Such behaviors may, for example, cause erroneous test results when the SMU is being used in combination with ATE to test a DUT, or may cause other undesirable behaviors.

[0018] Accordingly, aspects of the present application provide SMUs and methods of operating SMUs that achieve smooth or continuous switching between main control and limit

control (e.g., between voltage controlled modes and current controlled modes) of the SMU. The smooth transition (which may also be referred to as crossover) may be achieved, for example, by creating a drive signal for the SMU which is based on both the voltage across the load and the current through the load, rather than only one or the other. As a non-limiting example, when a determination is made that the limit signal falls outside the compliance limits (or compliance range or threshold range), transition between the main mode and the limit mode may be initiated. During the transition the error of the limit signal may be combined suitably with the error of the main signal to generate the drive signal used to adjust the output signal of the SMU. By combining the errors of the main signal and limit signal a smooth transition may be provided, which may avoid the drawbacks associated with an abrupt or discontinuous switch between voltage controlled and current controlled modes.

[0019] The aspects and embodiments described above, as well as additional aspects and embodiments, are described further below. These aspects and/or embodiments may be used individually, all together, or in any combination of two or more, as the application is not limited in this respect.

[0020] FIG. 1 illustrates a non-limiting example of a SMU 100 according to an aspect of the present application coupled to a load. The SMU may be configured to exhibit smooth transitions between a main control mode and a limit control mode.

[0021] As shown, the SMU 100, which includes the components to the left of dashed line 110, comprises a control circuit 102 for controlling generation of an output signal 103 to be provided to the load 104. The output signal 103 may also be considered a drive signal for driving the load. A feedback circuit 106 may provide one or more feedback signals 107 to an error generation circuit 108. The one or more feedback signals 107 may be representative of a voltage across the load 104 and/or a current through the load 104. The error generation circuit 108 may determine errors in the main signal (e.g., voltage in a voltage controlled mode and current in a current controlled mode) and the limit signal (e.g., current in a voltage controlled mode and voltage in a current controlled mode) and generate a control signal 109 to provide to the control circuit 102 for controlling the output signal 103. When transitioning between main control and limit control modes, the error generation circuit may produce a control signal 109 based on both an error of the main signal and an error of the limit signal. Such operation is described in further detail below with respect to FIG. 2.

[0022] The circuitry of SMU 100 may take any suitable form for performing in the described manner. A non-limiting detailed example is described below in connection with FIG. 4. The load 104 may be any suitable load. In some embodiments, the load may be a DUT, such as a semiconductor device (e.g., a memory device) or other device to be tested with ATE or otherwise. However, the various aspects described herein are not limited to use with any particular type(s) of load.

[0023] FIG. 2 illustrates a method of operating a source measure unit (SMU), such as SMU 100 of FIG. 1, according to a non-limiting embodiment of the present application. The method may provide for smooth (or continuous) transitions (or crossover) between main control and limit control modes.

[0024] The method 200 begins at stage 202 with setting a target value of the main signal (e.g., the voltage of the SMU output signal in a voltage controlled mode and the current of the SMU output signal in a current controlled mode). At stage 204, a compliance range for the limit signal may be set, including upper and lower limit values, which may also be referred to as threshold values or compliance limits. It should be appreciated that stages 202 and 204 may be performed in any suitable order, including being performed at substantially the same time, as the method 200 is not limited in this respect.

[0025] At stage 206, errors may be determined, including an error of the main signal and one or more errors of the limit signal. For example, in scenarios in which a compliance range with upper and lower compliance limits is established at stage 204, errors of the limit signal with respect to both the upper and lower compliance limits may be determined.

[0026] At stage 208, a combined or mixed error (which may also be referred to herein as a total error) may be determined from the errors determined in stage 206. The combined error may then be used to generate a control signal (e.g., control signal 109 of FIG. 1) at stage 210. In some embodiments, the combined error may itself serve as the control signal, i.e., the combined error may be sent without modification to a control circuit which then generates a drive signal (e.g., output signal 103). However, the method 200 also contemplates scenarios in which the combined error may be modified in some manner (e.g., scaled, amplified, etc.) to become the control signal that then gets sent to a control circuit.

[0027] At stage 212, the control signal generated at stage 210 may be used to generate the drive signal (or output signal) of the SMU to drive the load. For example, the control signal generated at stage 210 may be sent to a control circuit which, in response to receiving the control signal, generates a drive signal. Thus, it should be appreciated that method 200 provides a manner of operating an SMU in which the drive signal or output signal of the SMU is based on errors in both the main and limit signals. This is to be contrasted with approaches in which only the errors in the main signal are used to generate the drive signal, and in which abrupt switches between the main control and limit control modes are exhibited.

[0028] The method 200 may be iterative, as indicated by the arrow connecting stages 212 and 206. Any number of desired iterations may be performed during operation of the SMU. In some embodiments, the loop represented by stages 206, 208, 210, and 212 may be performed continuously or substantially continuously during operation of the SMU. In some embodiments, stages 202 and 204 may be performed only once when initializing the SMU, or may be performed at various times when it is desired to adjust the target value for the main signal and the compliance range for the limit signal.

[0029] Stages 206 and 208 may be performed in various manners, and the method 200 is not limited to the particular manner of implementing those stages. FIG. 3, however, illustrates a non-limiting manner of implementing stages 206 and 208.

[0030] As shown, stage 206 may comprise performance of three stages (or sub-stages) 302, 304, and 306. At stage 302, the main error (i.e., the error of the main signal) may be determined by comparing the value of the main signal to the target value of the main signal. At stage 304, an upper limit error may be determined by comparing the value of the limit signal to the upper limit threshold or value. At stage 306, the lower limit error may be determined by comparing the value of the limit signal to the lower limit threshold or value.

[0031] Thus, stage 206 may produce three error components in some embodiments: a main error component; an upper limit error component; and a lower limit error component. Stage 208 may then generate a combined error by suitable combination of these error components.

[0032] As shown in FIG. 3, stage 208 may, in some embodiments, comprise two stages (or sub-stages) 308 and 310. At stage 308, the main error, upper limit error, and lower

limit error determined from stage 206 may be weighted. The weighting may be static (i.e., the weighting of the main error and upper and lower limit errors may not change during operation of the SMU) or variable (i.e., the weighting of the main error and/or the upper limit error and/or the lower limit error may change during operation of the SMU). The weighting may be performed according to a function or in any other suitable manner. Non-limiting examples of weighting are described further below.

[0033] At stage 310, the weighted main error, weighted upper limit error, and weighted lower limit error may be combined in any suitable manner to generate the combined error signal. For example, the weighted errors may be added in some embodiments. A non-limiting example is described further below in connection with FIG. 4.

[0034] FIG. 4 illustrates a non-limiting detailed implementation of SMU 100 of FIG. 1 which is suitable for operating in accordance with the methods illustrated in FIGs. 2 and 3.

[0035] As described previously, the control circuit 102 may take any suitable form. In the non-limiting embodiment of FIG. 4, the control circuit 102 may be configured to receive a digital signal (i.e., the control signal 109 may be a digital signal in this non-limiting embodiment) and output an analog signal (i.e., the output signal 103 may be an analog signal in this non-limiting embodiment). The control circuit 102 may include a controller 402, a digital-to-analog converter (DAC) 404 and an amplifier 406. The controller 402 may be an integrator. In some embodiments, the controller 402 may be a proportional-integral-derivative (PID) controller, though other controllers may alternatively be used. The controller 402 may receive the control signal 109, which in some embodiments represents a combined or total error signal, and may generate a code for application to the DAC 404. The amplifier 406 may be a buffer amplifier, and in some embodiments may amplify current while providing unity gain of voltage.

[0036] The feedback circuit 106 may, in the non-limiting embodiment shown, include circuitry for generating distinct signals representing the voltage across the load 104 and the current through the load 104. In particular, the feedback circuit 106 may include a first amplifier 408 which may be a differential amplifier coupled across the load 104 (e.g., coupled to input and output terminals of the load 104) to provide a signal representative of the voltage across the load to an analog-to-digital converter (ADC) 410. The ADC 410 may output a signal **V_{mon}** representative of the voltage across the load 104.

[0037] The feedback circuit 106 may also include an amplifier 412 coupled across a resistor 413 (which may be a variable resistor in some embodiments) to provide a signal to ADC 414 representative of the current through the load 104. The ADC 414 may then output a digital representation of the current through the load 104, labeled as **Vimon**. It should be appreciated that in the embodiment illustrated **Vimon** is a voltage representing the current through the load. However, not all embodiments are limited to generating a voltage representative of the current through the load.

[0038] While the example of FIG. 4 illustrates a configuration in which multiple (e.g., two in the example) distinct signals are taken to determine the voltage across the load and the current through the load, it should be appreciated that not all embodiments are limited in this respect. Rather, the feedback circuit 106 may utilize any one or more signals to determine the voltage across the load and the current through the load. For example, if the resistance of the load is known, then the signal from the amplifier 408 may provide both the voltage across the load and may be used to determine the current through the load. Thus, the voltage across the load and the current through the load may be determined from a single feedback signal in some embodiments.

[0039] The error generation circuit 108 may include suitable circuitry for generating the main error and upper and lower limit errors as described, for example, in connection with stages 302, 304, and 306 in FIG. 3. In particular, in the non-limiting embodiment illustrated, the error generation circuit 108 includes a first combination circuit 416a, which in some embodiments may be an adder or summation circuit, or a comparator. The first combination circuit 416a may receive the target value for the main signal, labeled as **set_m** in FIG. 4, as well as the previously described voltage signal **Vvmon** and may generate an error signal **Verr_m** representative of the error of the main signal relative to the target value for the main signal.

[0040] Similarly, the error generation circuit 108 may include a second combination circuit 416b which may be any of the types previously described in connection with 416a. The second combination circuit 416b may receive the positive (or upper in some embodiments) limit value (also referred to herein as the upper threshold value) of the limit signal, labeled as **set_lim_p**, as well as the previously described signal **Vimon** and may

generate an error signal **Verr_p** representative of the error of the limit signal relative to the upper threshold value.

[0041] Similarly, the error generation circuit 108 may include a third combination circuit 416c which may be any of the types previously described in connection with 416a. The third combination circuit 416c may receive the negative (or lower in some embodiments) limit value (also referred to herein as the lower threshold value) of the limit signal, labeled as **set_lim_n**, as well as the previously described signal **Vimon** and may generate an error signal **Verr_n** representative of the error of the limit signal relative to the lower threshold value.

[0042] In some embodiments, **Verr_m**, **Verr_p**, **Verr_n** may be considered as different components (or sub-components) of the error of the drive signal produced by the SMU. The error generation circuit 108 may further comprise a combination circuit 418 (e.g., an adder or summation circuit) configured to combine (e.g., sum in some embodiments) the error components **Verr_m**, **Verr_p**, **Verr_n** to generate a combined error signal (or total error signal) which may be used as control signal 109. Thus, it should be appreciated that the control signal 109 used to control generation of a drive signal of a SMU may be based on errors in both the voltage and current of the drive signal, rather than being based on an error in only the voltage or the current.

[0043] As previously described in connection with stage 308 of FIG. 3, in some embodiments the error components representing errors in the main and limit signals may be weighted before being combined to generate a total error signal. The error generation circuit 108 shown in FIG. 4 may perform such weighting. Namely, as shown, the signals **Verr_m**, **Verr_p**, **Verr_n** may be weighted by weighting factors **W_m**, **W_p**, and **W_n**, respectively and then multiplied by respective multipliers 420a, 420b, and 420c to produce weighted error signals 422a-422c. In some embodiments, the control signal 109 produced by combination circuit 418 may represent a combination of the weighted error signals.

[0044] As described previously, when weighting (or, more generally, adjusting) of error signals is performed, any suitable weighting may be applied. For example, the weighting factors **W_m**, **W_p**, and **W_n** may be fixed values in some embodiments, or may be variable. In some embodiments, the weighting may be piece-wise linear, sine-based, Gaussian, or any other suitable weighting function. In some embodiments, the weighting may

be a function of the error in the limit signal (rather than a function of the error in the main). For example, the weighting may be given in some embodiments by:

$$\mathbf{Verr_p} = \mathbf{set_lim_p} - \mathbf{Vimon}. \quad \text{Eq. 1}$$

[0045] Other weighting functions may alternatively be applied.

[0046] FIG. 5 illustrates a non-limiting example of how the weighting factors **Wm**, **Wp**, and **Wn** may change during operation of the SMU shown in FIG. 4. In this non-limiting example, each of **Wm**, **Wp**, and **Wn** may be capable of having a value within the range from 0 to 1 and each may be defined by a piece-wise linear function. Moreover, the total of **Wm+Wp+Wn** may remain 1 during operation. FIG. 5 is illustrated based on the assumption that the SMU is operating in a voltage controlled mode in which the limit signal is current (labeled as “output current” on the x-axis) having positive and negative thresholds labeled as **set_lim_p** and **set_lim_n**.

[0047] As shown, when the output current is less than **set_lim_n**, **Wn** may be 1 and **Wm** and **Wp** may be zero. When the output current is within the compliance range (i.e., between **set_lim_p** and **set_lim_n**), **Wm** may be 1 and **Wp** and **Wn** may be 0, except for in the transition regions 502a and 502b described below. When the output current is greater than **set_lim_p**, **Wp** may be 1 and **Wm** and **Wn** may be 0. Thus, it should be appreciated that during normal operation when the limit signal is within the compliance range, there is no contribution from the limit errors to generation of the control signal.

[0048] Moreover, it should be appreciated that **Wm**, **Wp**, and **Wn** are defined by piece-wise linear functions in the non-limiting example of FIG. 5. Namely, each of **Wm**, **Wp**, and **Wn** assumes a constant value within certain segments of the operating space but assumes a linearly changing value in one or both of the transition regions 502a and 502b.

[0049] As shown in FIG. 5, transition regions 502a and 502b represent transitions between main mode control and limit mode control (e.g., between voltage controlled mode and current controlled mode). The transition regions are continuous as represented by the sloping lines for **Wm**, **Wp**, and **Wn**, rather than being abrupt. Thus, the transition regions represent gradual, or smooth, transfers of control from one mode to another. In the transition

regions 502a and 502b, the drive signal of the SMU is based on both the voltage error(s) and current error(s). In this sense, the transition regions 502a and 502b may be considered to represent a mixed or shared mode of operation mixed/shared between voltage controlled and current controlled modes. Thus, voltage control and current control may operate simultaneously in varying or variable proportions.

[0050] FIG. 6 illustrates an expanded view of the transition region 502b of FIG. 5, focusing on the values for **W_m** and **W_p** (i.e., ignoring **W_n**). As shown, when the limit signal is (well) within the compliance range, **W_m** is 1 and **W_p** is 0. However, as the limit signal approaches **set_lim_p**, transition of control from the main control to the limit control begins. Namely, **W_m** and **W_p** both adjust smoothly or continuously until the output current reaches **set_lim_p** and control is transferred fully from the main control to the limit control.

[0051] The rate (in terms of the change of the weighting factor for a given change in the error signal) at which **W_m**, **W_p**, and **W_n** change in the transition regions 502a and 502b may be any suitable rate to provide a smooth transition avoiding undesirable behavior (e.g., chatter) in the output signal of the SMU, or any other desired rate. As a non-limiting example, the transition regions may span approximately 0.2 Volts when the error signal is expressed as a voltage (e.g., **V_{imon}** or **V_{vmon}**). In some embodiments, the transition regions may span voltage changes in the error signal of between 0.1 Volt and 1 Volt, between 0.2 Volts and 0.5 Volts, any values within those ranges, or any other suitable voltage gap. It should also be appreciated that the piece-wise linear functions illustrated in FIG. 5 may be more complex in some embodiments. For example, additional inflection points of the function may be implemented. The illustrated linear transition regions may instead have multiple portions of different slopes, or other suitable behavior.

[0052] It should be noted that in some embodiments the values of **W_m**, **W_p**, and **W_n** sum to 1 which may provide operational stability, though not all embodiments are limited in this respect.

[0053] A specific non-limiting example of the manner of determining weighting factors **W_m**, **W_p**, and **W_n** and thus a combined error signal is now provided. A positive weighting function may be implemented in which the weighting factors are a function of the positive limit error (e.g., **W_p(V_{err_p})** with **V_{err_p}** given by Eq. 1). The value of **W_m** may

then be given by $W_m = 1 - W_p$. The total error (e.g., out of combination circuit 418 in FIG. 4) may then be given by:

$$Verr_sum = ((1 - W_p) \times (1 - W_n) \times Verr_m) + (W_p \times Verr_p) + (W_n \times Verr_n).$$

[0054] In some embodiments, W_m , W_p , and W_n may be calculated on-the-fly (e.g., during operation) of the SMU. However, in some embodiments a look-up table may be used to lookup values of W_m , W_p , and W_n . Alternatives are possible.

[0055] FIGs. 5 and 6 illustrate scenarios in which mode switching is completed, i.e., control is transferred fully from main control to limit control or vice versa. It should be appreciated that not all embodiments require such a transition. Rather, for example, at some time during transition from main control to limit control (or vice versa), the voltage and current values of the output signal of the SMU may be such that control begins to shift back in the other direction. The ability of the circuits and methods described herein to accommodate such shifting back and forth in a smooth manner may be a further benefit to providing desirable or acceptable behavior in the output signal of the SMU.

[0056] The aspects of the present application may provide one or more benefits. Described now are some non-limiting examples of such benefits. It should be appreciated that not all aspects and embodiments necessarily provide all of the benefits now described. Further, it should be appreciated that aspects of the present application may provide additional benefits to those now described.

[0057] Some aspects of the present application provide a manner of switching between voltage controlled and current controlled modes of a SMU (or V/I source) that reduces or eliminates noise, chatter, or other undesirable signal behavior at the output of the SMU. Some aspects provide sliding scale control capability to slide between discrete modes of operation of the SMU (e.g., between voltage and current controlled modes). Some aspects of the present application provide a SMU with adjustable control between voltage controlled and current controlled modes, thus increasing flexibility in the use of the SMU.

[0058] Some aspects of the present application provide simple SMUs. For example, it should be appreciated that the SMU of FIG. 4 lacks any state machine and also lacks hysteresis circuitry. State machines and hysteresis circuits are generally complex and therefore the SMUs according to aspects of the present application may be relatively simple in

design and operation. Other benefits may also be provided according to the various aspects of the present application.

[0059] The SMUs and methods described herein may be used in various contexts. As previously described, in some embodiments SMUs may be used as part of ATE when testing a DUT. However, the aspects described herein are not limited to use in the ATE context. Rather, aspects of the present application may apply more generally to provision of a V/I source for driving a load of various types. Moreover, various aspects of the present application may be used with either analog or digital control loops.

[0060] Having thus described several aspects and embodiments of the technology of this application, it is to be appreciated that various alterations, modifications, and improvements will readily occur to those of ordinary skill in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the technology described in the application. For example, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the embodiments described herein. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described. In addition, any combination of two or more features, systems, articles, materials, kits, and/or methods described herein, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the scope of the present disclosure.

[0061] The above-described embodiments can be implemented in any of numerous ways. One or more aspects and embodiments of the present application involving the performance of processes or methods may utilize program instructions executable by a device (e.g., a computer, a processor, or other device) to perform, or control performance of, the processes or methods. In this respect, various inventive concepts may be embodied as a computer readable storage medium (or multiple computer readable storage media) (e.g., a computer memory, one or more floppy discs, compact discs, optical discs, magnetic tapes,

flash memories, circuit configurations in Field Programmable Gate Arrays or other semiconductor devices, or other tangible computer storage medium) encoded with one or more programs that, when executed on one or more computers or other processors, perform methods that implement one or more of the various embodiments described above. The computer readable medium or media can be transportable, such that the program or programs stored thereon can be loaded onto one or more different computers or other processors to implement various ones of the aspects described above. In some embodiments, computer readable media may be non-transitory media.

[0062] The terms “program” or “software” are used herein in a generic sense to refer to any type of computer code or set of computer-executable instructions that can be employed to program a computer or other processor to implement various aspects as described above. Additionally, it should be appreciated that according to one aspect, one or more computer programs that when executed perform methods of the present application need not reside on a single computer or processor, but may be distributed in a modular fashion among a number of different computers or processors to implement various aspects of the present application.

[0063] Computer-executable instructions may be in many forms, such as program modules, executed by one or more computers or other devices. Generally, program modules include routines, programs, objects, components, data structures, etc. that perform particular tasks or implement particular abstract data types. Typically the functionality of the program modules may be combined or distributed as desired in various embodiments.

[0064] Also, data structures may be stored in computer-readable media in any suitable form. For simplicity of illustration, data structures may be shown to have fields that are related through location in the data structure. Such relationships may likewise be achieved by assigning storage for the fields with locations in a computer-readable medium that convey relationship between the fields. However, any suitable mechanism may be used to establish a relationship between information in fields of a data structure, including through the use of pointers, tags or other mechanisms that establish relationship between data elements.

[0065] When implemented in software, the software code can be executed on any suitable processor or collection of processors, whether provided in a single computer or distributed among multiple computers.

[0066] Further, it should be appreciated that a computer may be embodied in any of a number of forms, such as a rack-mounted computer, a desktop computer, a laptop computer, or a tablet computer, as non-limiting examples. Additionally, a computer may be embedded in a device not generally regarded as a computer but with suitable processing capabilities, including a Personal Digital Assistant (PDA), a smart phone or any other suitable portable or fixed electronic device.

[0067] Also, a computer may have one or more input and output devices. These devices can be used, among other things, to present a user interface. Examples of output devices that can be used to provide a user interface include printers or display screens for visual presentation of output and speakers or other sound generating devices for audible presentation of output. Examples of input devices that can be used for a user interface include keyboards, and pointing devices, such as mice, touch pads, and digitizing tablets. As another example, a computer may receive input information through speech recognition or in other audible formats.

[0068] Such computers may be interconnected by one or more networks in any suitable form, including a local area network or a wide area network, such as an enterprise network, and intelligent network (IN) or the Internet. Such networks may be based on any suitable technology and may operate according to any suitable protocol and may include wireless networks or wired networks.

[0069] Also, as described, some aspects may be embodied as one or more methods. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[0070] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[0071] The indefinite articles “a” and “an,” as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean “at least one.”

[0072] The phrase “and/or,” as used herein in the specification and in the claims, should be understood to mean “either or both” of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with “and/or” should be construed in the same fashion, i.e., “one or more” of the elements so conjoined. Elements other than those specifically identified by the “and/or” clause may optionally be present, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to “A and/or B”, when used in conjunction with open-ended language such as “comprising” can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

[0073] As used herein in the specification and in the claims, the phrase “at least one,” in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase “at least one” refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, “at least one of A and B” (or, equivalently, “at least one of A or B,” or, equivalently “at least one of A and/or B”) can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

[0074] Also, the phraseology and terminology used herein is for the purpose of description and should not be regarded as limiting. The use of “including,” “comprising,” or “having,” “containing,” “involving,” and variations thereof herein, is meant to encompass the items listed thereafter and equivalents thereof as well as additional items.

[0075] In the claims, as well as in the specification above, all transitional phrases such as “comprising,” “including,” “carrying,” “having,” “containing,” “involving,” “holding,” “composed of,” and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases “consisting of” and “consisting essentially of” shall be closed or semi-closed transitional phrases, respectively.

CLAIMS

What is claimed is:

1. A method of operating a source measure unit (SMU) configured to couple to a load, the SMU operating in a plurality of modes including a voltage-controlled mode and a current-controlled mode, the method comprising:
generating a control signal to apply to a control circuit of the SMU when switching between the plurality of modes, wherein generating the control signal comprises generating the control signal based on both a voltage and a current.
2. The method of claim 1, wherein the voltage is a voltage across the load and wherein the current is a current through the load.
3. The method of claim 2, wherein generating the control signal comprises generating a mixed signal representing a mixture of a first signal and a second signal, the first signal representing a voltage error based on the voltage across the load and the second signal representing a current error based on the current through the load.
4. The method of claim 3, wherein the first signal is indicative of a voltage error of the voltage detected across the load relative to a target voltage of a drive signal of the SMU, and wherein the second signal is indicative of a current error of the current through the load relative to an upper current threshold.
5. The method of claim 3, wherein generating the mixed signal comprises generating a weighted combination of the first signal and the second signal.
6. The method of claim 3, wherein the first signal is indicative of a voltage error of the voltage detected across the load relative to an upper voltage threshold, and wherein the second signal is indicative of a current error of the current through the load relative to a target current.
7. The method of claim 3, wherein generating the control signal comprises combining the first signal, the second signal and a third signal, the third signal being based at least in part on the voltage detected across the load or the current through the load.

8. The method of claim 7, wherein the first signal is indicative of a voltage error of the voltage detected across the load relative to a target voltage, and wherein the second signal is indicative of a first current error of the current through the load relative to an upper current threshold, and wherein the third signal is indicative of a second current error of the current through the load relative to a lower current threshold.
9. The method of claim 7, wherein the first signal is indicative of a first voltage error of the voltage detected across the load relative to an upper voltage threshold, and wherein the second signal is indicative of a current error of the current through the load relative to a target current, and wherein the third signal is indicative of a second voltage error of the voltage detected across the load relative to a lower voltage threshold.
10. The method of claim 7, wherein generating the mixed signal comprises generating a weighted combination of the first signal, the second signal, and the third signal.
11. The method of claim 10, wherein a first weighting factor is associated with the first signal, a second weighting factor is associated with the second signal, and a third weighting factor is associated with the third signal, and wherein a sum of the first weighting factor, the second weighting factor, and the third weighting factor is one.
12. The method of claim 10, wherein the first weighting factor and/or the second weighting factor and/or the third weighting factor is variable.
13. The method of claim 12, wherein the first weighting factor and/or second weighting factor and/or third weighting factor is generated by a function.
14. The method of claim 13, wherein the function is dependent on voltage.
15. The method of claim 14, wherein the function is dependent on voltage error.
16. The method of claim 13, wherein the function is dependent on current.

17. The method of claim 16, wherein the function is dependent on current error.
18. The method of claim 1, wherein the load is a device under test (DUT).
19. A source measure unit (SMU) configured to operate in a plurality of modes including a voltage-controlled mode and a current-controlled mode, the SMU comprising:
combination circuitry configured to generate, when the SMU transitions between the voltage-controlled mode and the current controlled mode, a control signal to provide to a control circuit of the SMU, the control signal being based on both a voltage and a current.
20. The SMU of claim 19, wherein the voltage is representative of a voltage error and the current is representative of a current error.
21. The SMU of claim 20, wherein the combination circuitry is configured to combine the voltage error and the current error with a third error to produce the control signal, the third error being representative of an additional voltage error or an additional current error.
22. The SMU of claim 20, wherein the combination circuitry comprises weighting circuitry configured to formed a weighted combination of the voltage error and the current error.
23. The SMU of claim 19, further comprising setting circuitry configured to set a target voltage or target current.
24. The SMU of claim 23, wherein the setting circuitry is further configured to set a limit value of the voltage or current.

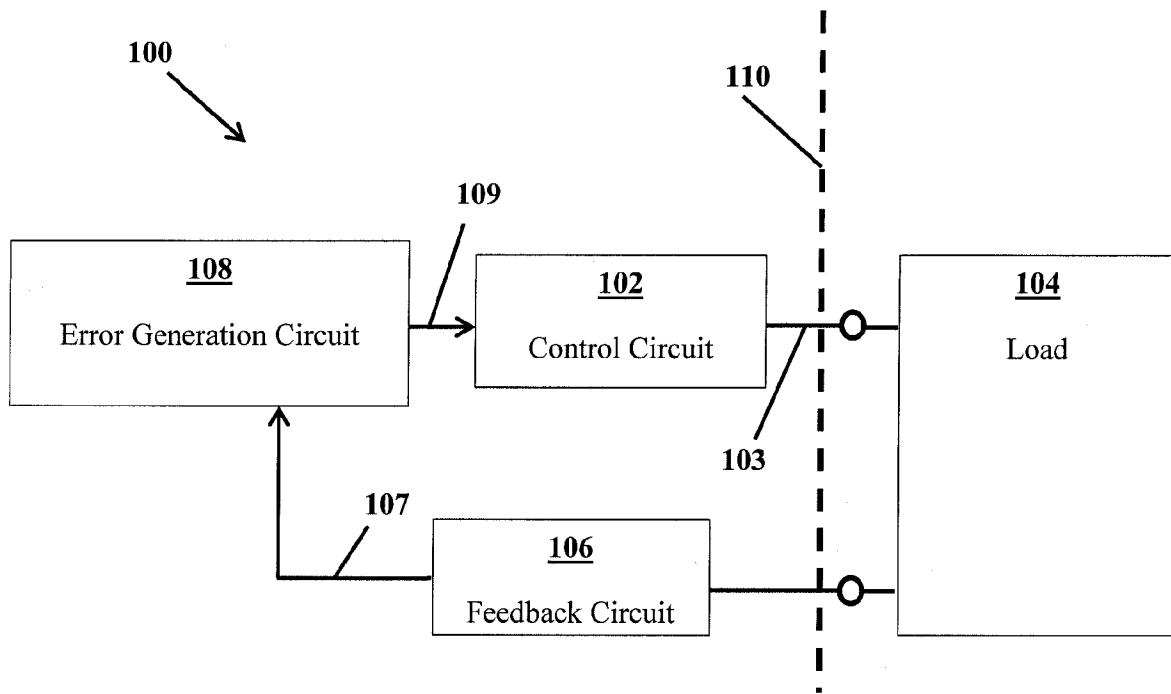
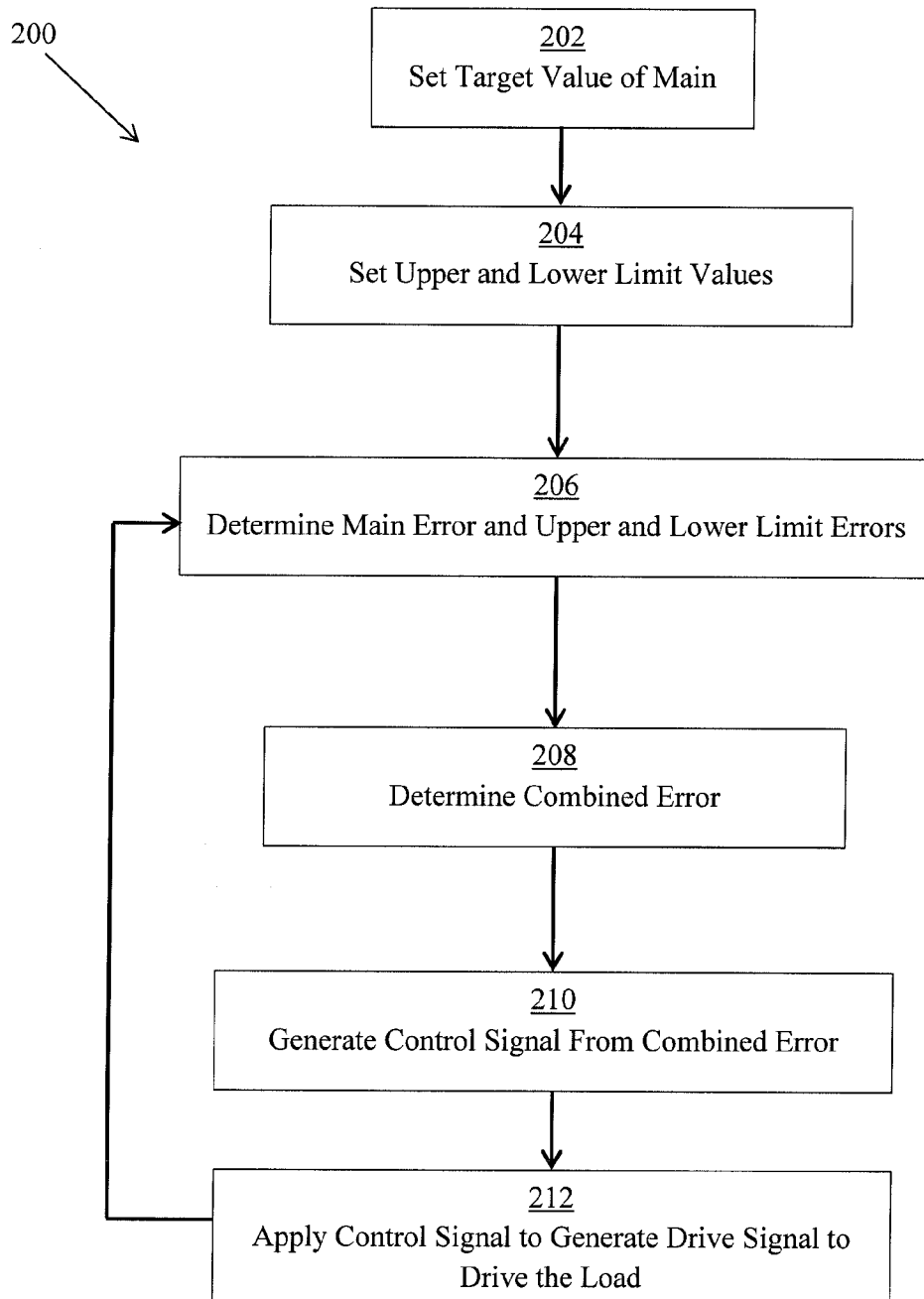
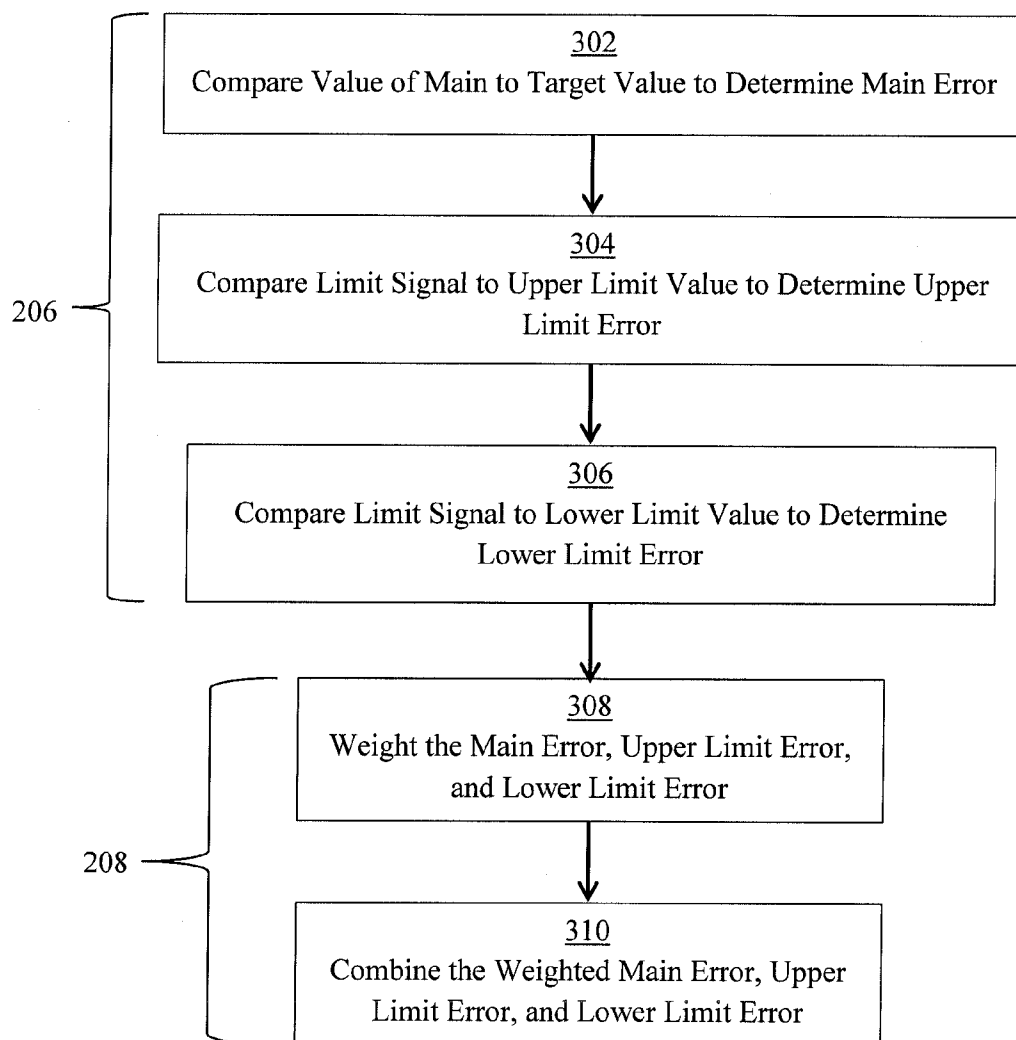


FIG. 1

**FIG. 2**

**FIG. 3**

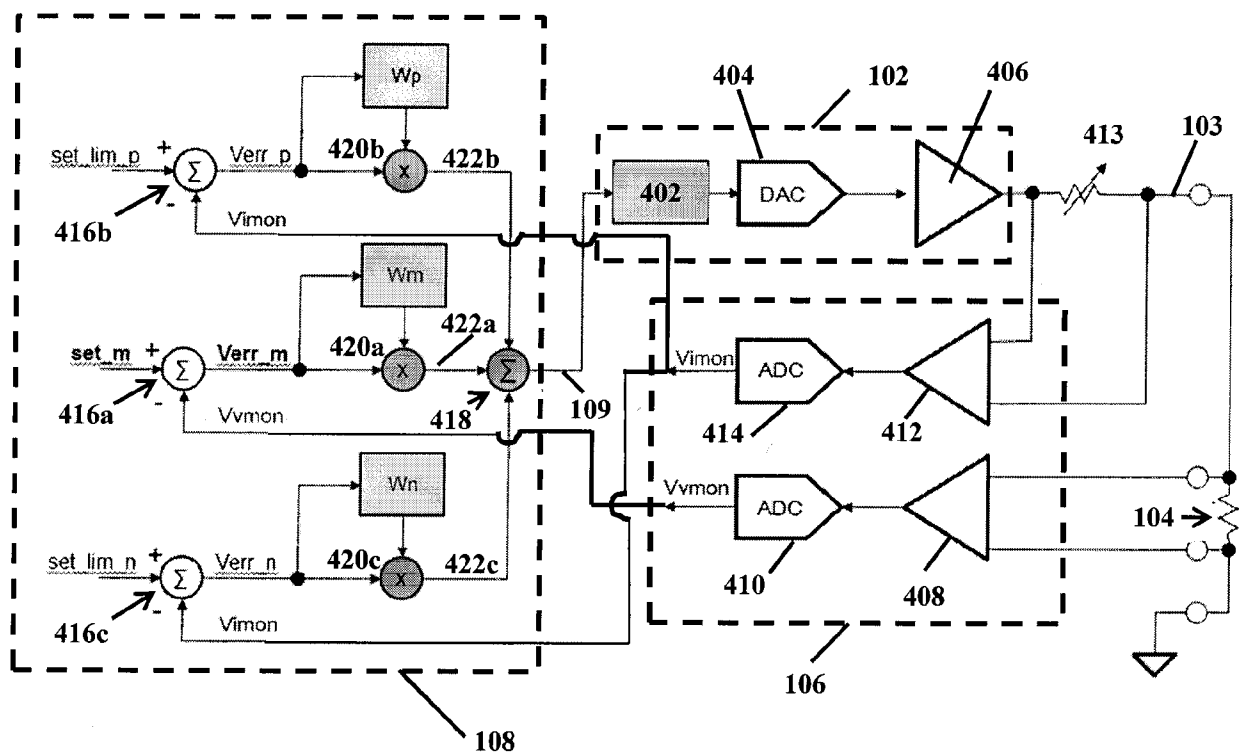


FIG. 4

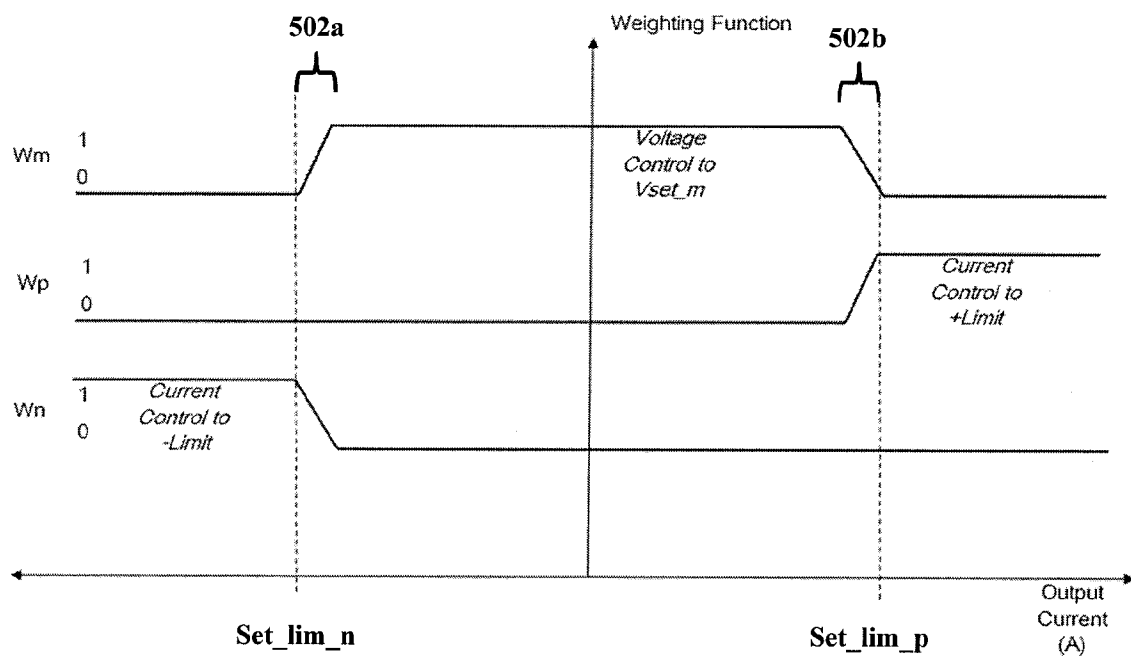


FIG. 5

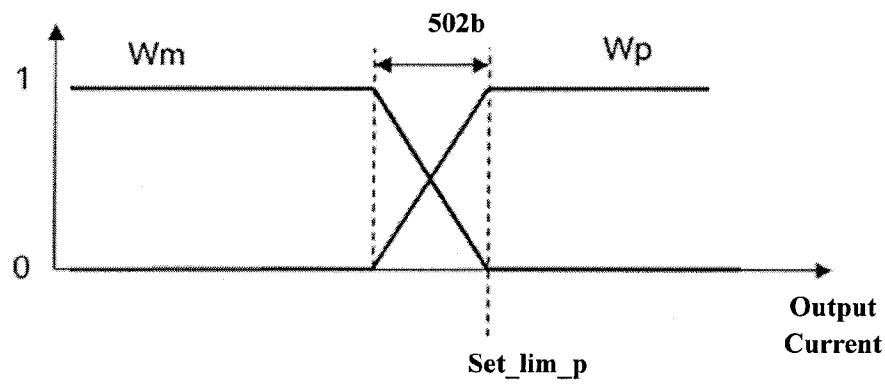


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2014/021915

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G05B 13/02 (2014.01)

USPC - 324/140R

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - G05B 13/02, 11/36; G01R 17/00, 17/02, 1/28, 19/00, 31/00 (2014.01)

USPC - 324/140R, 73.1, 114, 115, 76.11; 700/28, 32, 33, 40, 67, 75

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

CPC - G05B 13/02, 11/36; G01R 17/00, 17/02, 1/28, 19/00, 31/00 (2014.02)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Orbit, Google Patents, Google Scholar, Google

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009/0121908 A1 (REGIER) 14 May 2009 (14.05.2009) entire document	1-24
A	US 2004/0135591 A1 (TSUTSUI) 15 July 2004 (15.07.2004) entire document	1-24
A	WO 2011/066554 A2 (GOSTEIN et al) 03 June 2011 (03.06.2011) entire document	1-24
A	US 2012/0306559 A1 (REGIER et al) 06 December 2012 (06.12.2012) entire document	1-24

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

08 June 2014

Date of mailing of the international search report

07 JUL 2014

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