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(54) **SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME**

(71) Applicant: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi (JP)

(72) Inventor: **Shunpei YAMAZAKI**, Setagaya (JP)

(21) Appl. No.: **15/357,045**

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H01L 29/08	(2006.01)
H01L 29/66	(2006.01)
H01L 21/02	(2006.01)
H01L 21/426	(2006.01)
H01L 27/12	(2006.01)
H01L 29/49	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/7869*** (2013.01); ***H01L 27/1229*** (2013.01); ***H01L 27/1225*** (2013.01); ***H01L 29/04*** (2013.01); ***H01L 29/42384*** (2013.01); ***H01L 29/4908*** (2013.01); ***H01L 29/66969*** (2013.01); ***H01L 29/78696*** (2013.01); ***H01L 21/02554*** (2013.01); ***H01L 21/02565*** (2013.01); ***H01L 21/02631*** (2013.01); ***H01L 21/426*** (2013.01); ***H01L 29/0847*** (2013.01); ***H01L 29/78621*** (2013.01)

(57) **ABSTRACT**

A semiconductor device in which fluctuation in electric characteristics due to miniaturization is less likely to be caused is provided. The semiconductor device includes an oxide semiconductor film including a first region, a pair of second regions in contact with side surfaces of the first region, and a pair of third regions in contact with side surfaces of the pair of second regions; a gate insulating film provided over the oxide semiconductor film; and a first electrode that is over the gate insulating film and overlaps with the first region. The first region is a CAAC oxide semiconductor region. The pair of second regions and the pair of third regions are each an amorphous oxide semiconductor region containing a dopant. The dopant concentration of the pair of third regions is higher than the dopant concentration of the pair of second regions.

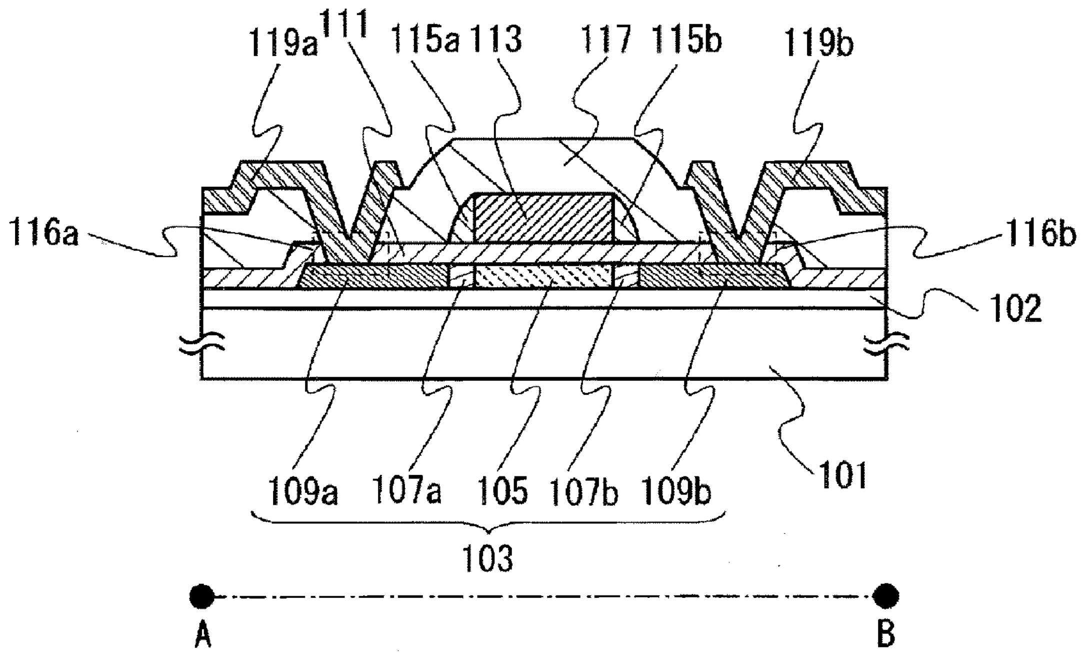
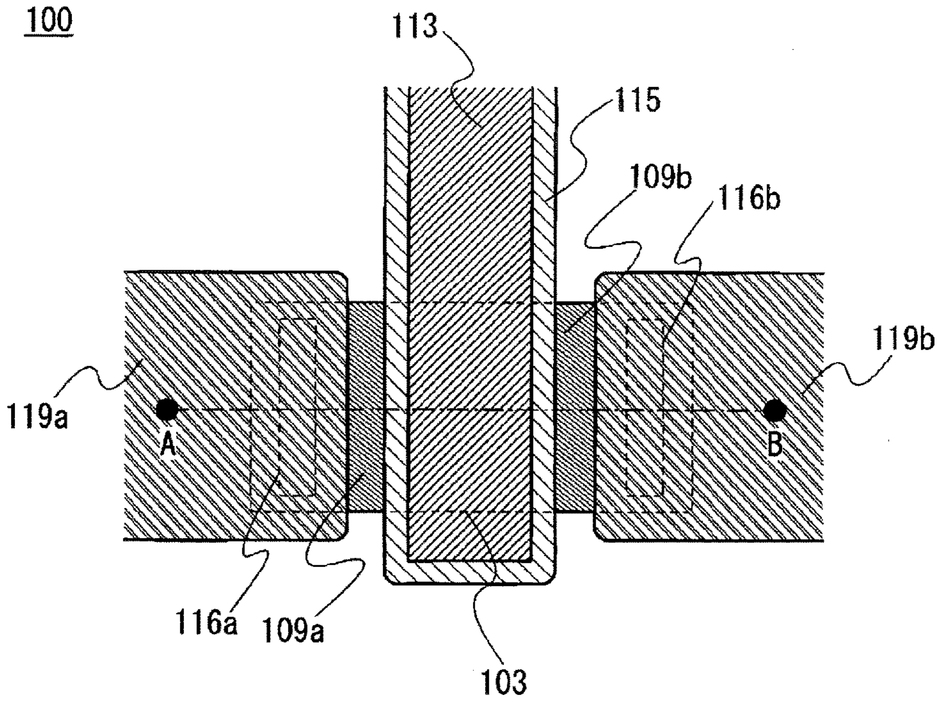


FIG. 1A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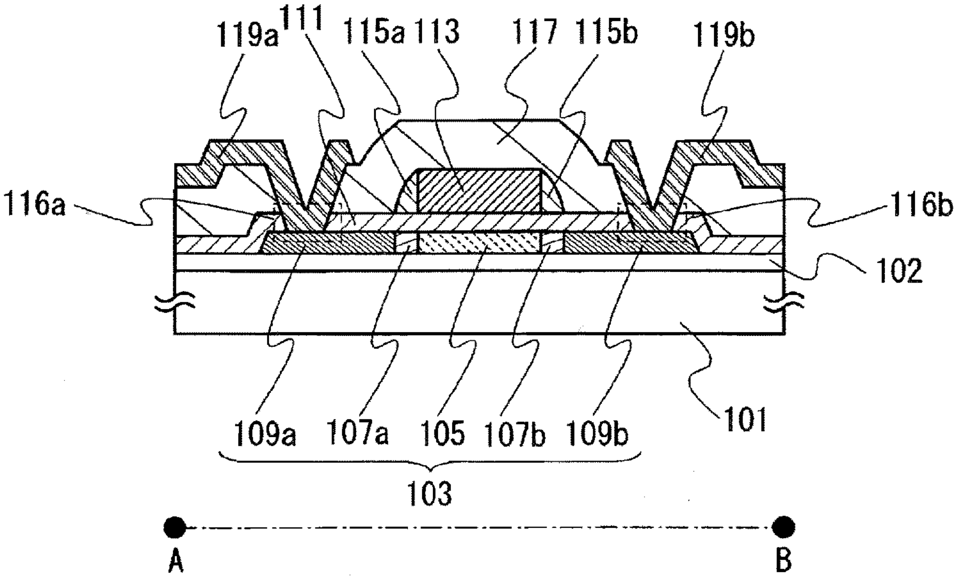
113
115
109b
116b
119b
119a
A
B
116a
109a
103

FIG. 1B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103
A
B

FIG. 2A

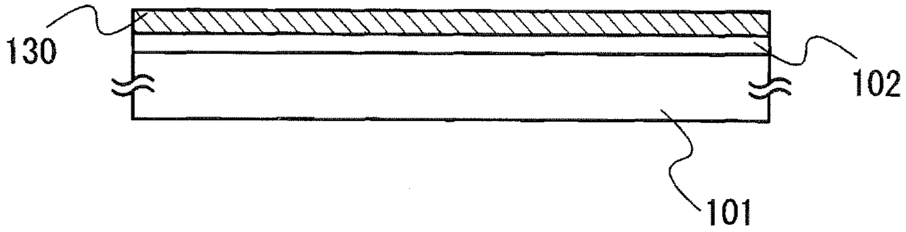


FIG. 2B

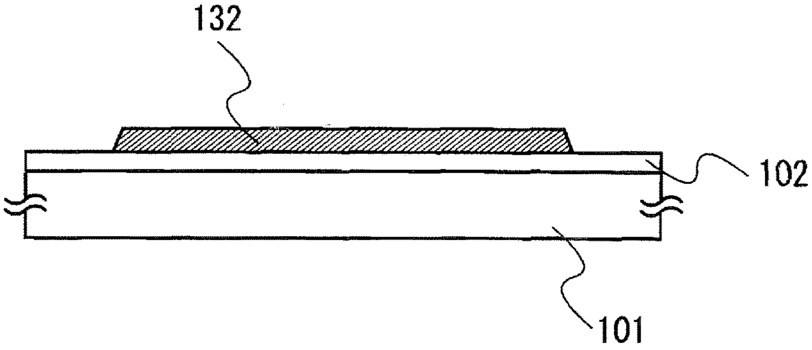


FIG. 2C

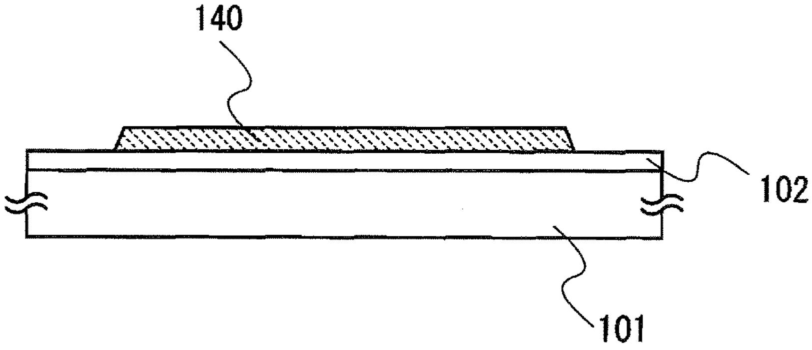


FIG. 3A

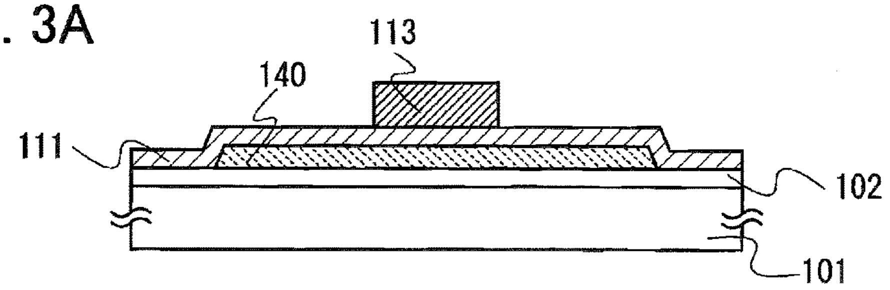


FIG. 3B

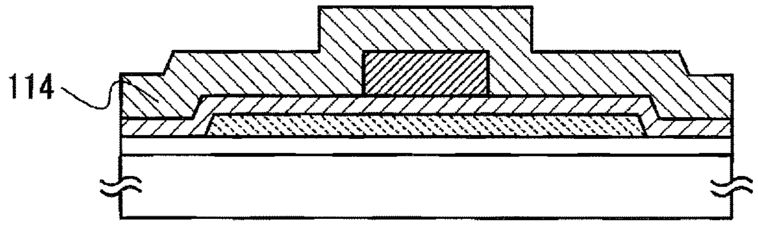


FIG. 3C

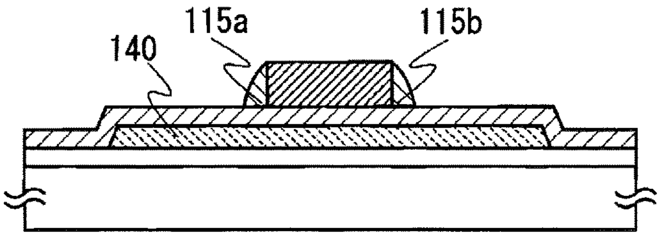


FIG. 3D

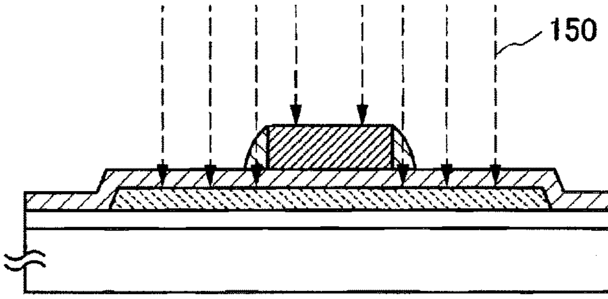


FIG. 3E

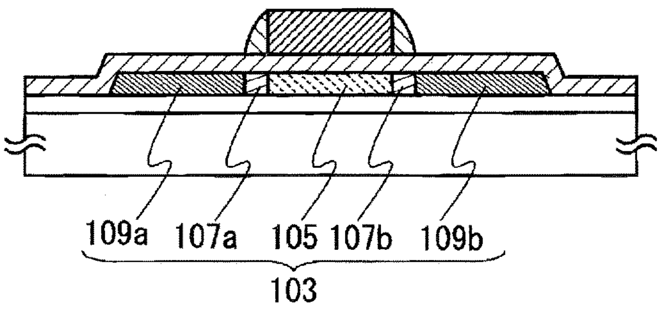


FIG. 4A

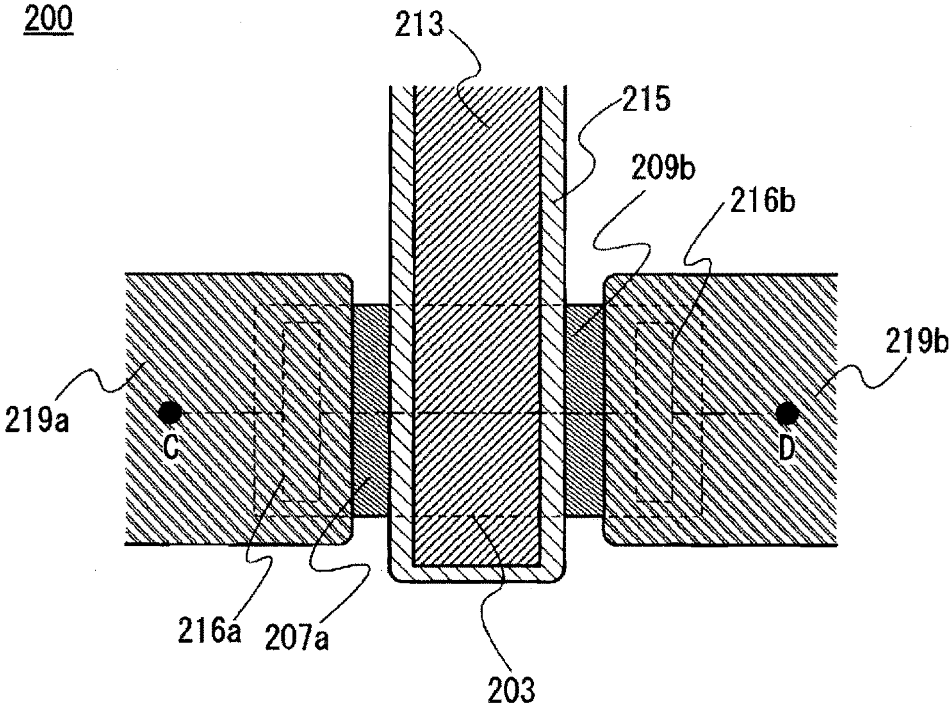
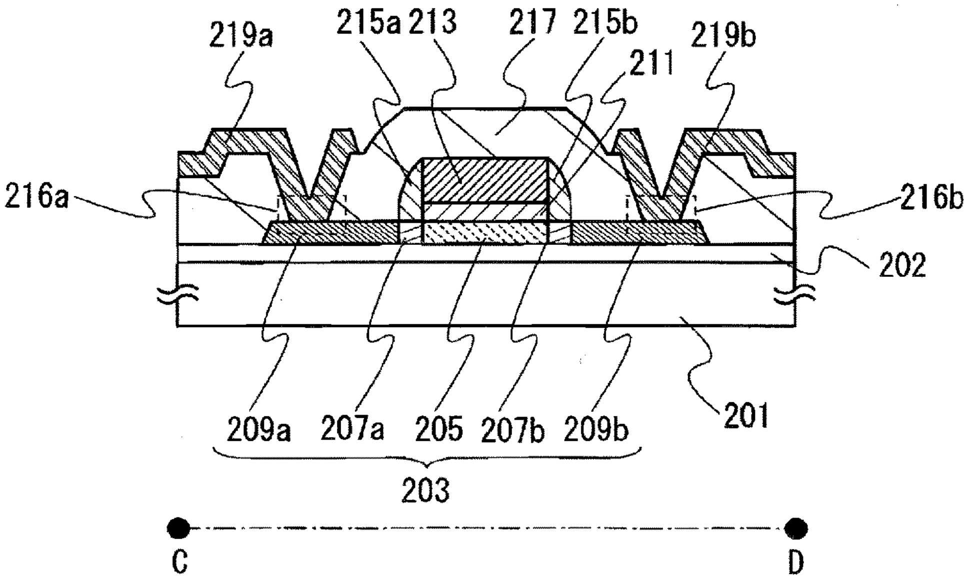

200
213
215
209b
216b
219b
219a
C
D
216a
207a
203

FIG. 4B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215a
213
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215b
211
219b
216a
216b
202
201
209a
207a
205
207b
209b
203
C
D

FIG. 5A

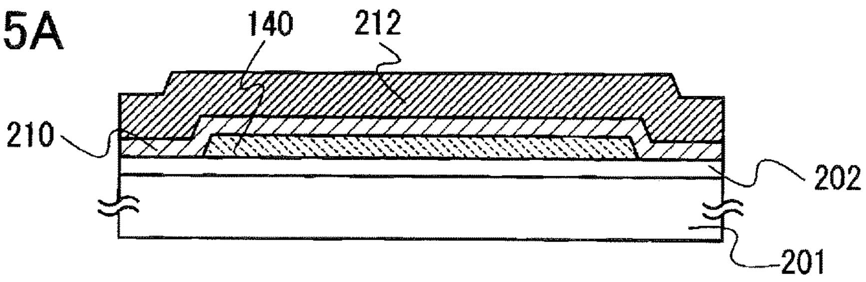


FIG. 5B

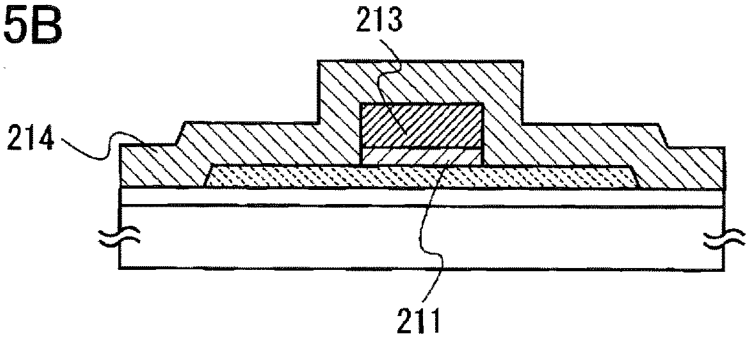


FIG. 5C

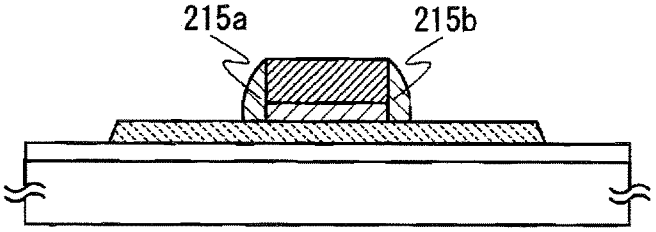


FIG. 5D

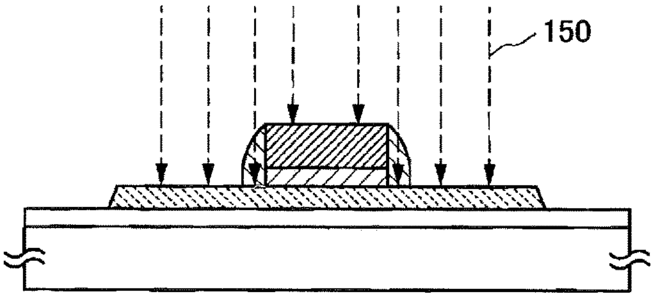


FIG. 5E

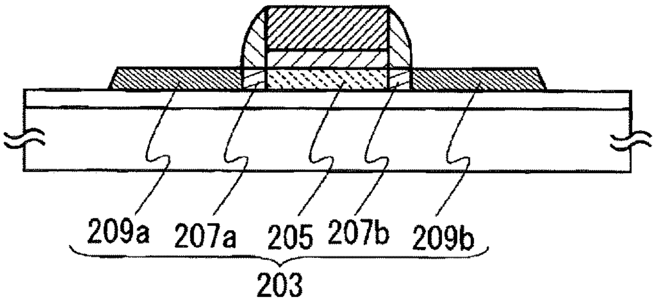
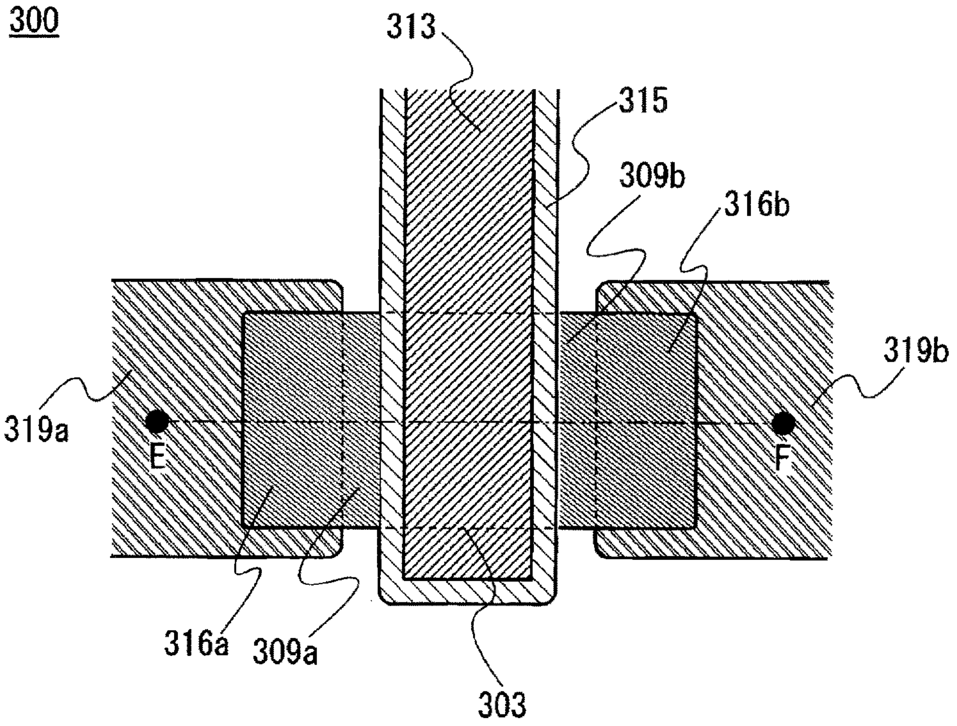


FIG. 6A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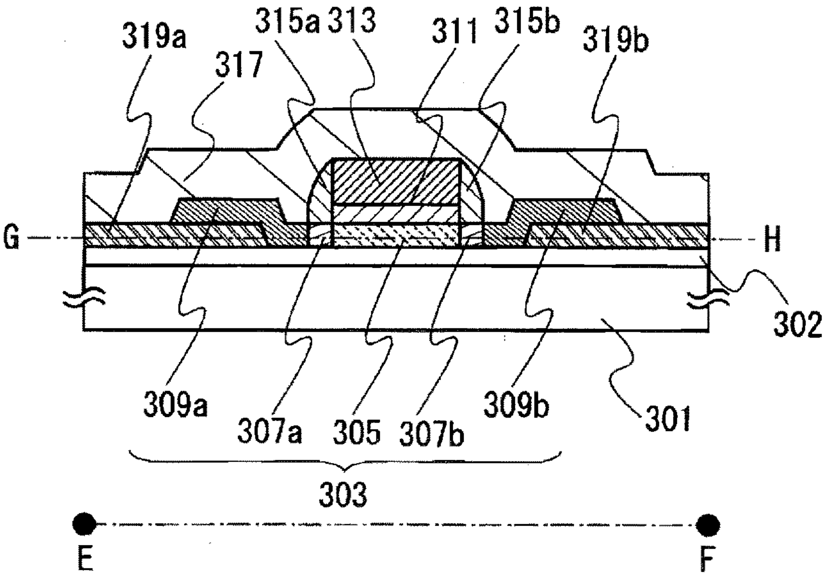
316b
319b
319a
E
F
316a
309a
303

FIG. 6B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307b
309b
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E
F

FIG. 7A

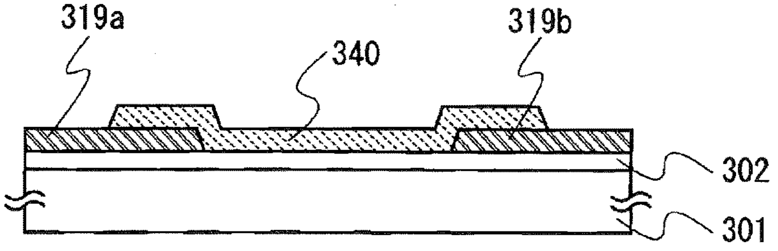


FIG. 7B

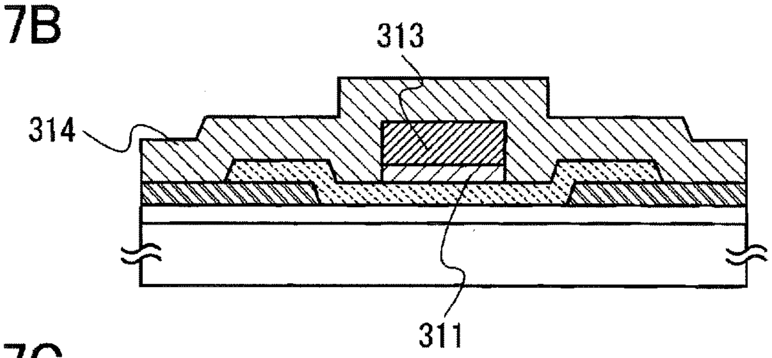


FIG. 7C

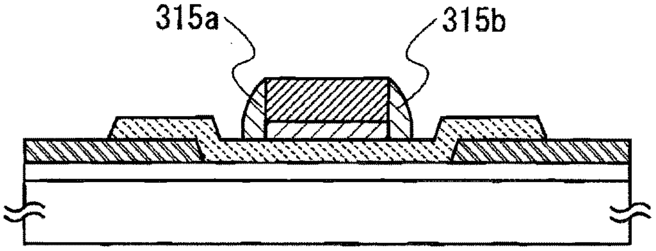


FIG. 7D

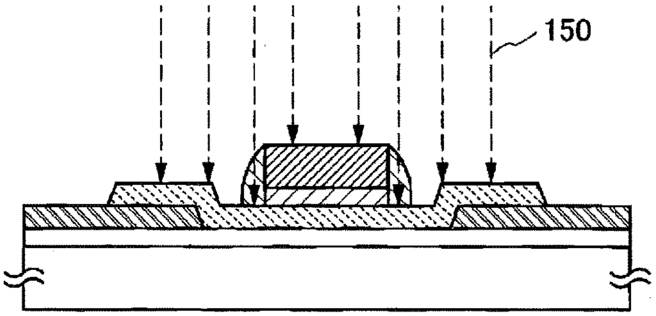


FIG. 7E

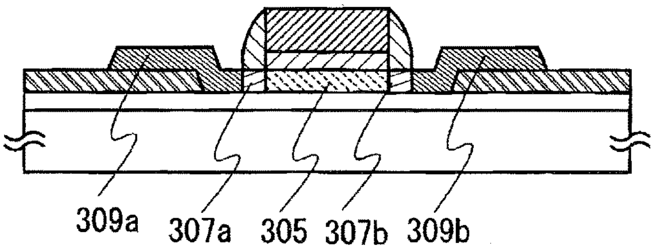
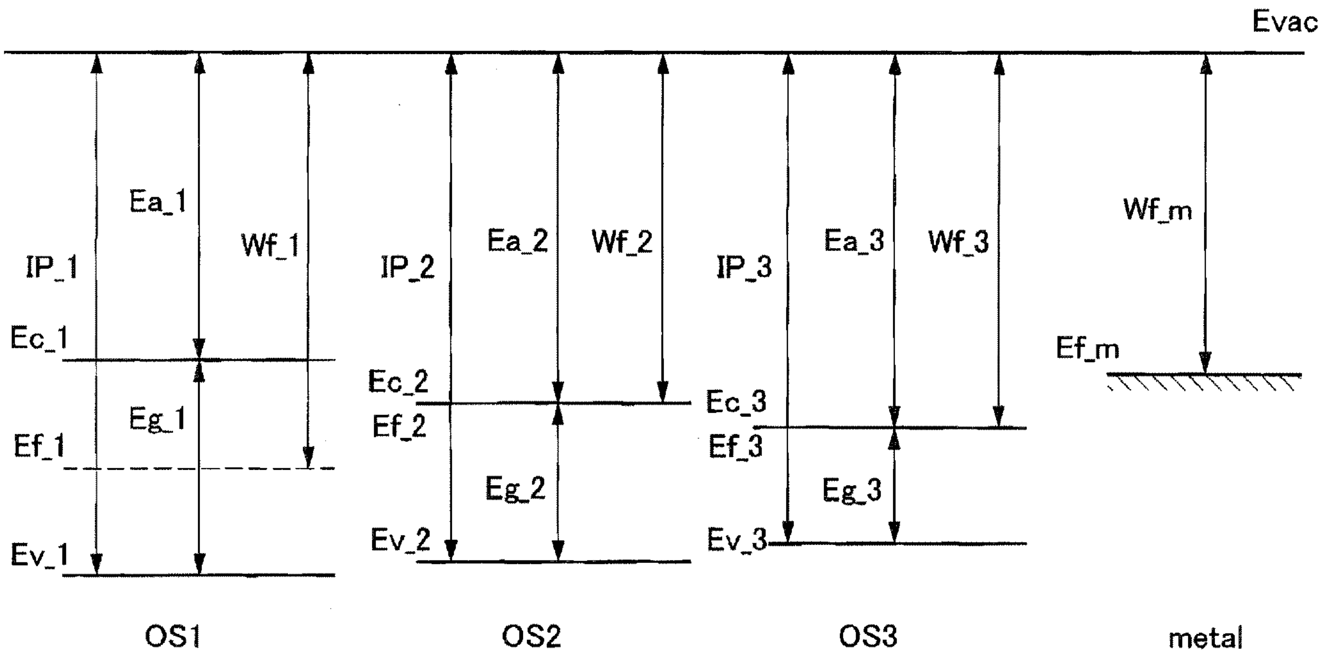


FIG. 8A


Evac
IP_1
Ea_1
Wf_1
Ec_1
Eg_1
Ef_1
Ev_1
OS1
IP_2
Ea_2
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Ec_2
Ef_2
Eg_2
Ev_2
OS2
IP_3
Ea_3
Wf_3
Ec_3
Ef_3
Eg_3
Ev_3
OS3
Wf_m
Ef_m
metal

FIG. 8B

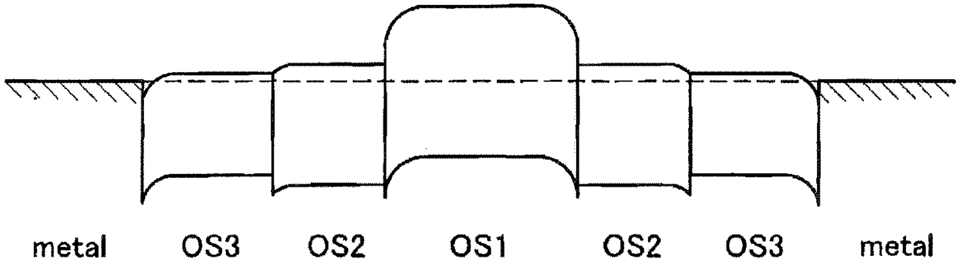

metal
OS3
OS2
OS1
OS2
OS3
metal

FIG. 9A

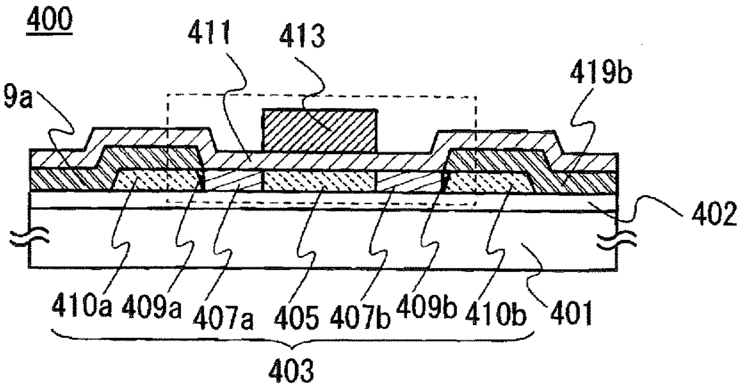


FIG. 9B

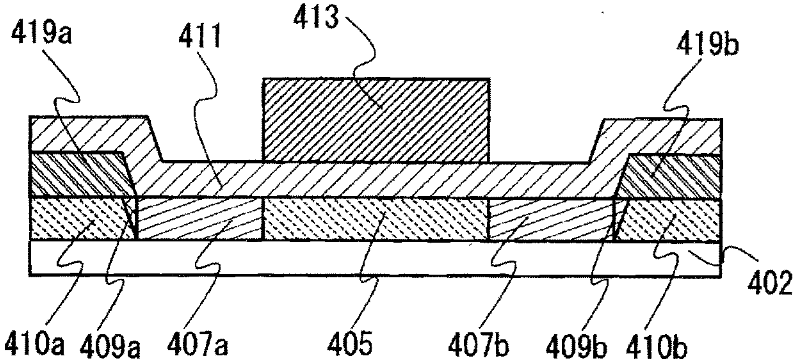


FIG. 9C

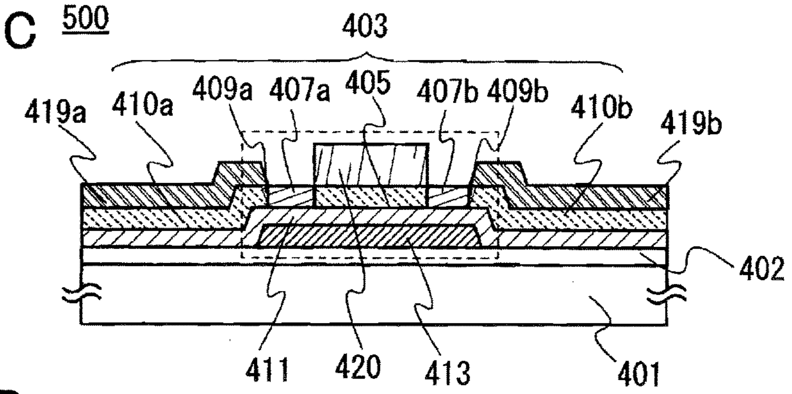


FIG. 9D

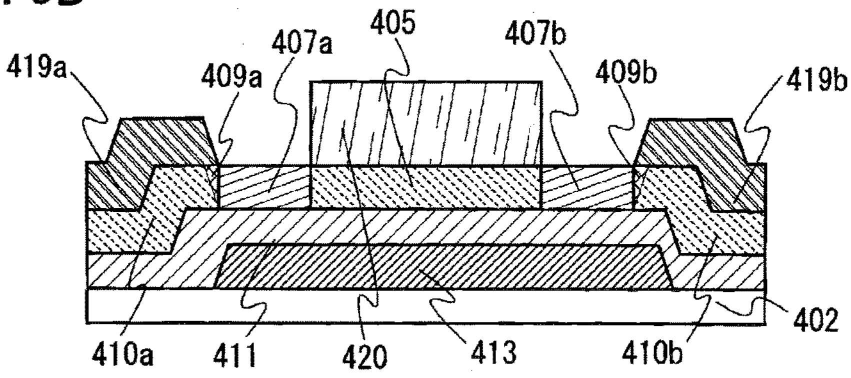


FIG. 10A

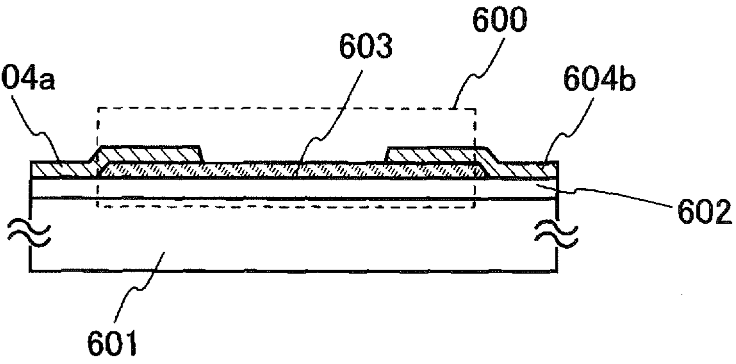


FIG. 10B

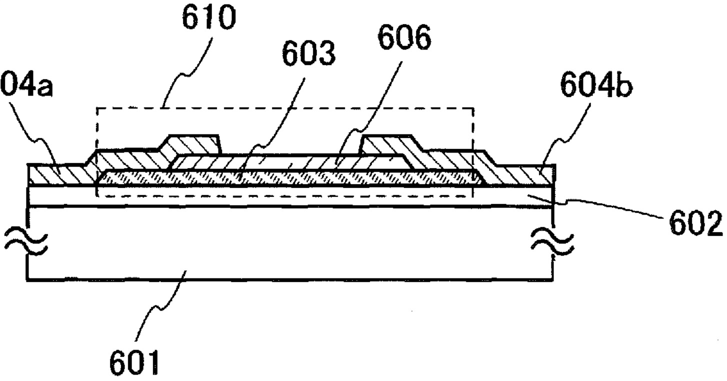


FIG. 11A

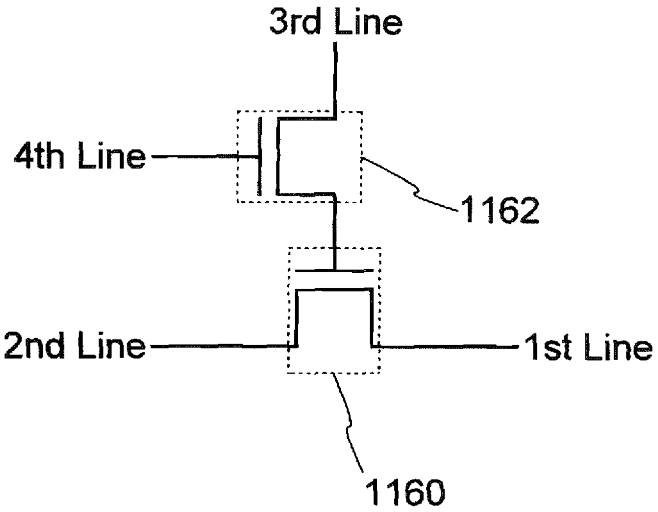


FIG. 11B

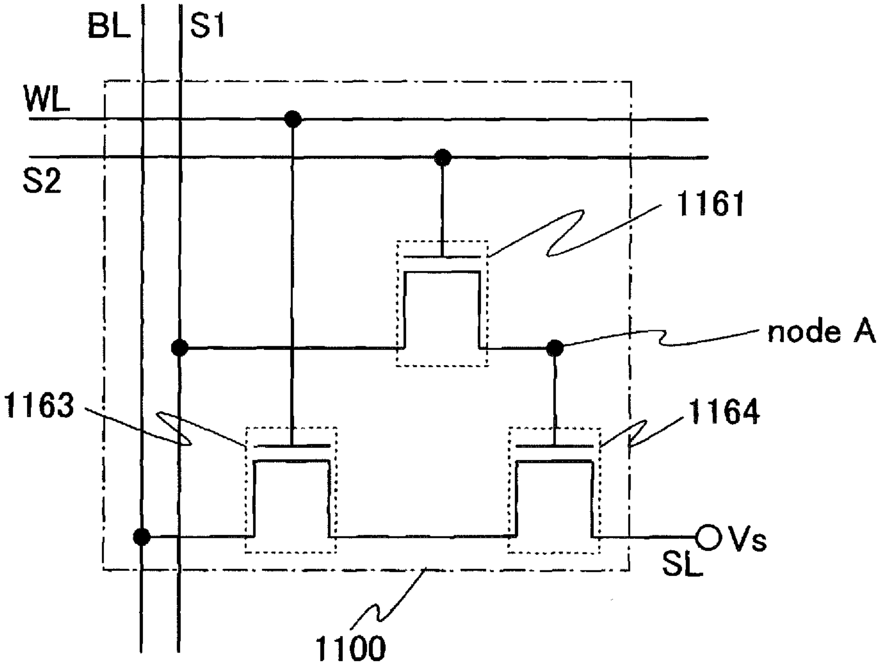


FIG. 12

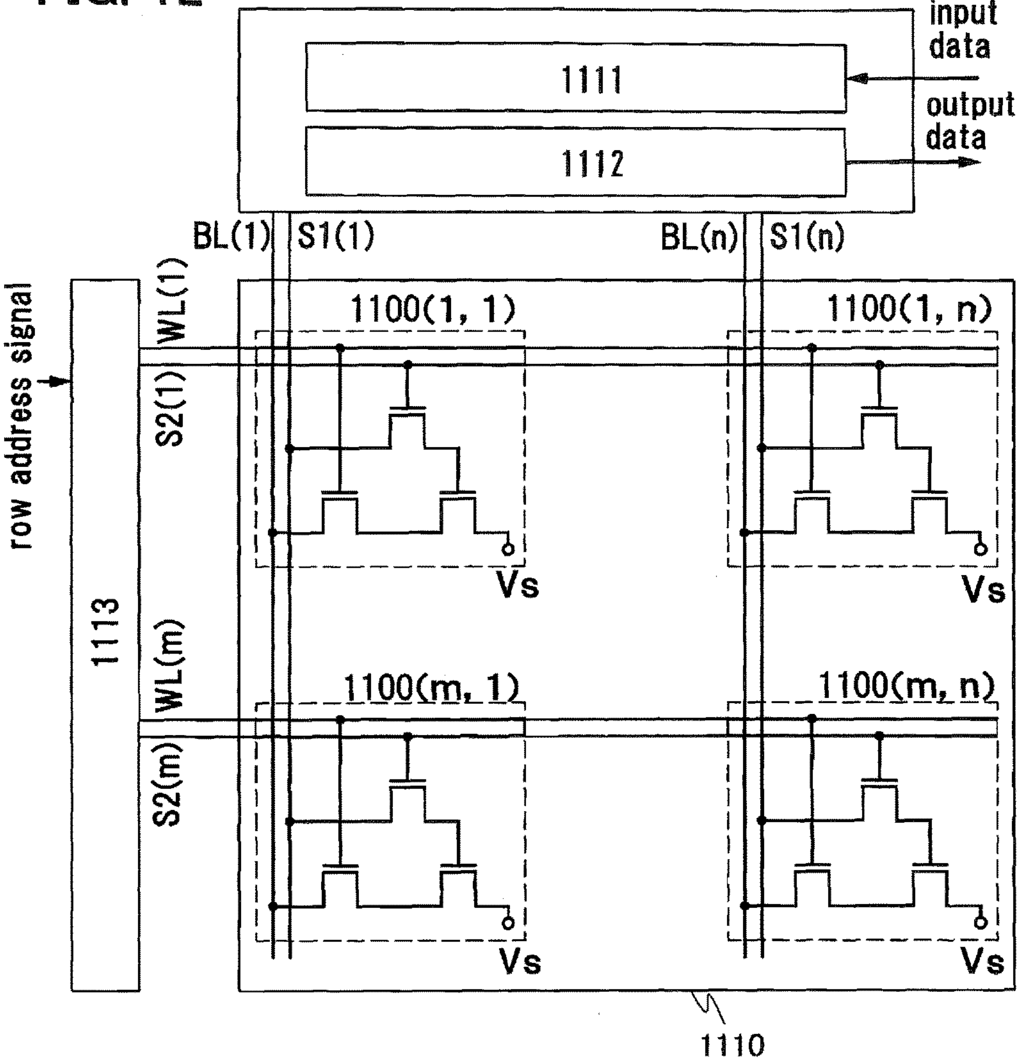

input data
1111
output data
1112
BL(1)
S1(1)
BL(n)
S1(n)
row address signal
1113
WL(1)
S2(1)
1100(1, 1)
1100(1, n)
Vs
Vs
WL(m)
S2(m)
1100(m, 1)
1100(m, n)
Vs
Vs
1110

FIG. 13A

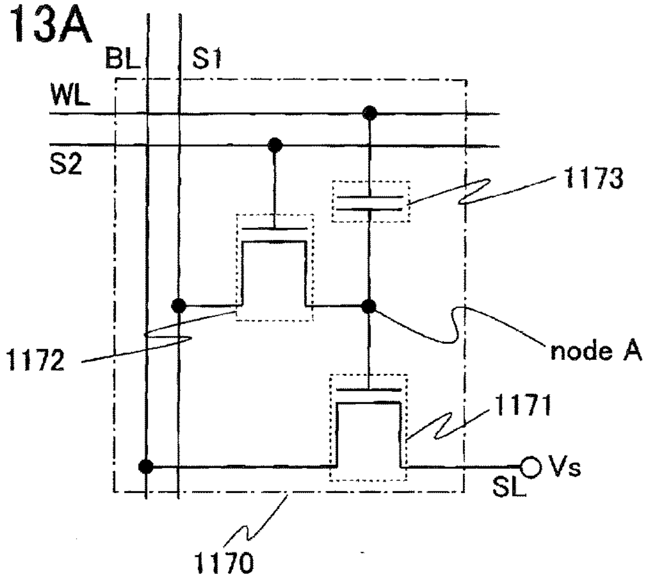


FIG. 13B

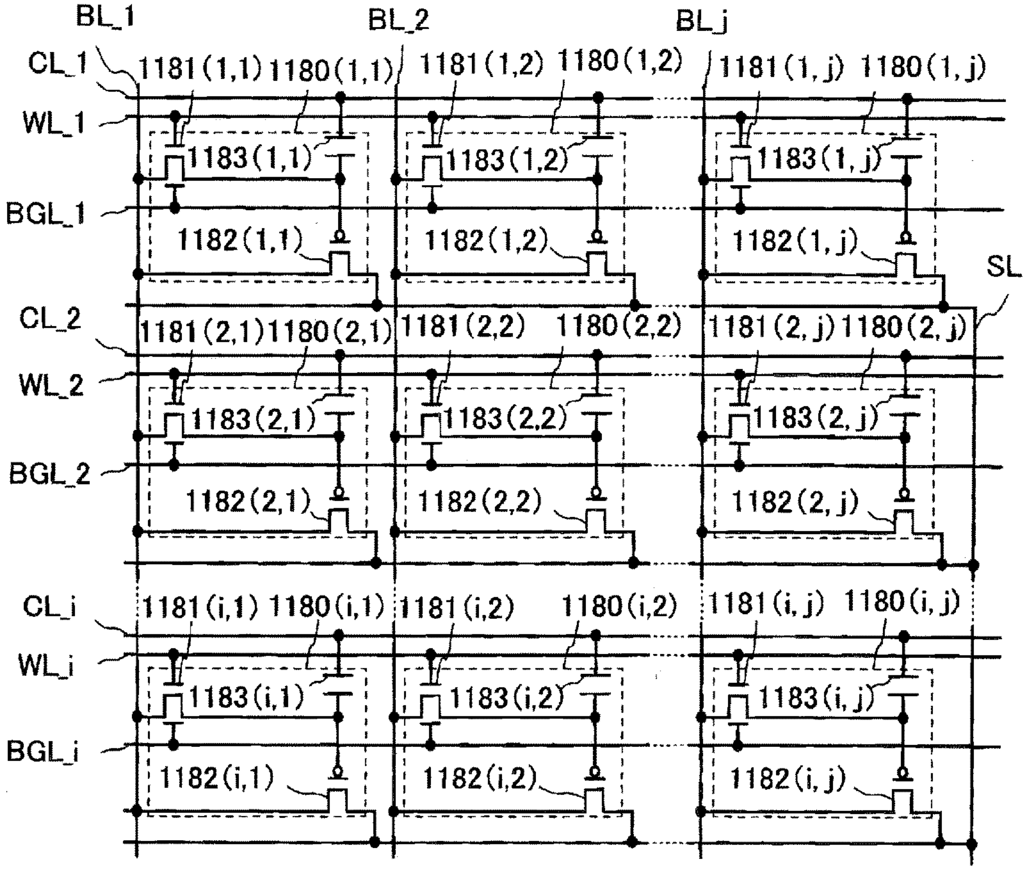


FIG. 14A

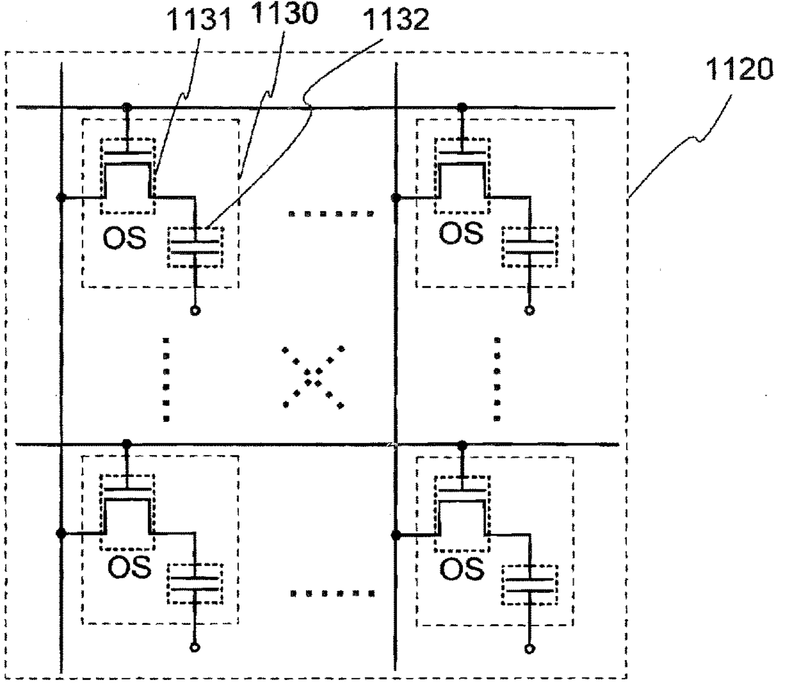


FIG. 14B

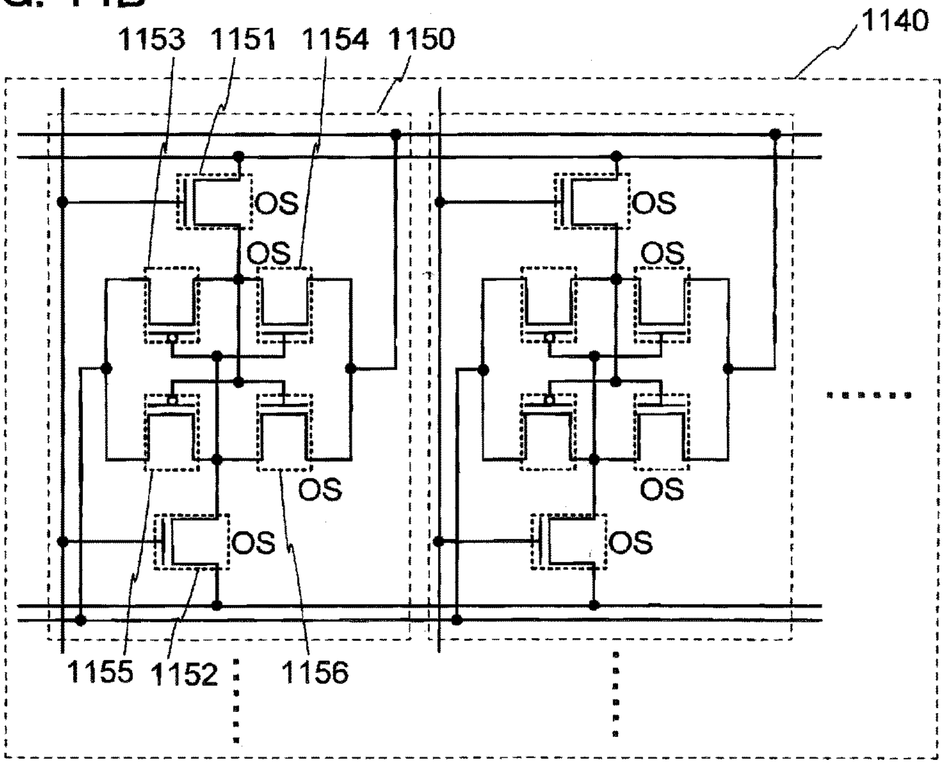


FIG. 15A

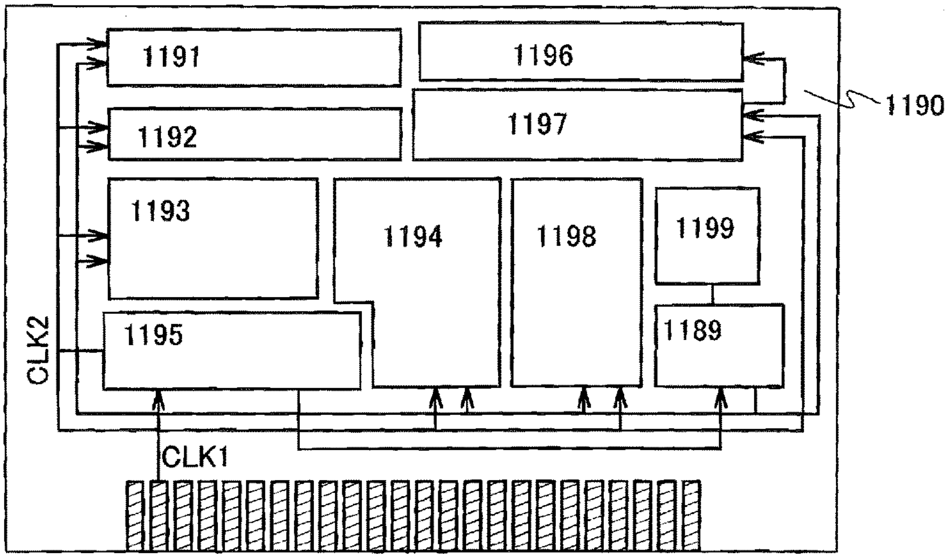


FIG. 15B

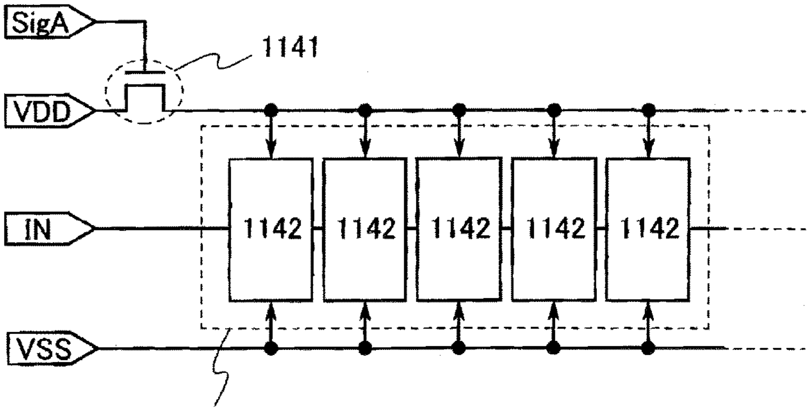
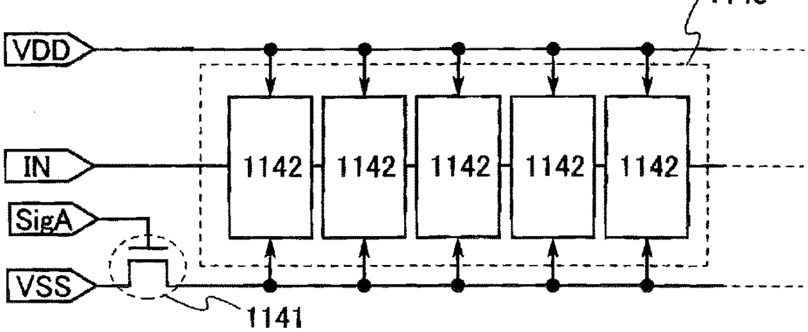


FIG. 15C



SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device including an oxide semiconductor and method for manufacturing a semiconductor device.

[0002] In this specification, the semiconductor device refers to all devices that can function by utilizing semiconductor characteristics. A transistor in this specification is a semiconductor device, and an electrooptic device, a semiconductor circuit, and an electronic device including the transistor are all semiconductor devices.

BACKGROUND ART

[0003] Transistors used for most flat panel displays typified by a liquid crystal display device and a light-emitting display device are formed using silicon semiconductors such as amorphous silicon, single crystal silicon, and polycrystalline silicon provided over glass substrates. Further, transistors formed using such silicon semiconductors are used in integrated circuits (ICs) and the like.

[0004] Attention has been directed to a technique in which, instead of the above silicon semiconductors, metal oxides exhibiting semiconductor characteristics are used for transistors. Note that in this specification, a metal oxide exhibiting semiconductor characteristics is referred to as an oxide semiconductor.

[0005] For example, a technique is disclosed in which a transistor is manufactured using zinc oxide or an In—Ga—Zn—O-based oxide as an oxide semiconductor and the transistor is used as a switching element or the like of a pixel of a display device (see Patent Documents 1 and 2).

[0006] Further, a technique is disclosed in which in a transistor including an oxide semiconductor, a highly conductive oxide semiconductor containing nitrogen is provided as buffer layers between a source region and a source electrode and between a drain region and a drain electrode, and thereby the contact resistance between the oxide semiconductor and the source electrode and between the oxide semiconductor and the drain electrode is reduced (see Patent Document 3).

[0007] Further, a technique is disclosed by which in a top-gate transistor including an oxide semiconductor, a channel region, a source region, and a drain region are formed in a self-aligned manner (see Non-Patent Document 1).

REFERENCE

Patent Document

[0008] [Patent Document 1] Japanese Published Patent Application No. 2007-123861

[0009] [Patent Document 2] Japanese Published Patent Application No. 2007-096055

[0010] [Patent Document 3] Japanese Published Patent Application No. 2010-135774

Non-Patent Document

[0011] [Non-Patent Document 1] Jae Chul Park et al., "High performance amorphous oxide thin film transistors with self-aligned top-gate structure" IEDM2009, pp. 191-194

DISCLOSURE OF INVENTION

[0012] In an integrated circuit including a transistor, the transistor needs to be miniaturized to achieve higher integration.

[0013] A transistor whose channel length is extremely shortened for miniaturization may have fluctuation in electric characteristics, such as decrease in the threshold voltage. This phenomenon is called a short-channel effect, and suppression of the short-channel effect is a challenge for miniaturization of a transistor.

[0014] It is known that a transistor including an oxide semiconductor particularly has small off-state current at room temperature, as compared with a transistor including silicon. It is considered that this is because the number of carriers generated by thermal excitation is small, that is, the carrier density is low.

[0015] An object of one embodiment of the present invention is to provide a semiconductor device in which fluctuation in electric characteristics due to miniaturization is less likely to be caused.

[0016] As a means for achieving the above object, in a transistor including an oxide semiconductor, a region containing a dopant is provided in an oxide semiconductor film including a channel formation region. Specifically, two pairs of amorphous regions each containing a dopant are provided in the oxide semiconductor film including the channel formation region, and the dopant concentration is varied between the pairs of regions. In this manner, an electric field generated in a drain region of the oxide semiconductor film can relieve an electric field applied to the channel formation region, and thus a short-channel effect can be suppressed. Note that in this specification, a dopant collectively refers to elements added to an oxide semiconductor film including a channel formation region.

[0017] In addition, the oxide semiconductor of the channel formation region is non-single-crystal; specifically, the channel formation region includes crystal portion having a region in which atoms are arranged in a triangle, a hexagon, a regular triangle, or a regular hexagon when seen from the direction perpendicular to the a-b plane of the non-single-crystal and in which metal atoms or metal atoms and oxygen atoms are arranged in layers when seen from the direction perpendicular to the c-axis. Note that in this specification, such crystal portion is referred to as c-axis aligned crystal (CAAC) and such oxide semiconductor including the c-axis aligned crystal is referred to as CAAC oxide semiconductor (CAAC-OS: c-axis aligned crystalline oxide semiconductor). With the channel formation region is formed as a CAAC oxide semiconductor region, fluctuation in electric characteristics of the transistor due to irradiation with visible light or ultraviolet light can be suppressed and the reliability of the semiconductor device can be improved.

[0018] One embodiment of the present invention is a semiconductor device which includes an oxide semiconductor film including a first region, a pair of second regions in contact with side surfaces of the first region, and a pair of third regions in contact with side surfaces of the pair of second regions; a gate insulating film provided over the oxide semiconductor film; and a first electrode that is over the gate insulating film and overlaps with the first region. The first region is a CAAC oxide semiconductor region that is non-single-crystal and has a c-axis aligned crystal region. The pair of second regions and the pair of third regions are each an amorphous oxide semiconductor region containing a dopant. The dopant concentration of the pair of third regions is higher than the dopant concentration of the pair of second regions.

[0019] The oxide semiconductor film preferably contains two or more elements selected from In, Ga, Sn, and Zn.

[0020] The above semiconductor device further includes a second electrode and a third electrode that are electrically connected to the pair of third regions.

[0021] The pair of second regions and the pair of third regions can be formed in a self-aligned manner by adding the dopant through the gate insulating film and a sidewall insulating film provided on side surfaces of the first electrode. In other words, with the sidewall insulating film, the pair of second regions can be regions to which a smaller amount of dopant is added (referred to as low-concentration regions in this specification). The pair of third regions can be regions to which a larger amount of dopant is added (referred to as high-concentration regions in this specification). Further, with the sidewall insulating film, the pair of second regions can be provided between the first region functioning as a channel formation region and the pair of third regions functioning as a source region and a drain region.

[0022] The dopant added to the pair of second regions and the pair of third regions is a Group 15 element. For example, the dopant is one or more elements selected from nitrogen, phosphorus, and arsenic, and the concentration of the dopant contained in each of the pair of second regions and the pair of third regions is preferably higher than or equal to 1×10^{19} atoms/cm^3 and lower than or equal to 1×10^{22} atoms/cm^3. It is further preferable that the dopant concentration of the pair of second regions be higher than or equal to 5×10^{18} atoms/cm^3 and lower than 5×10^{19} atoms/cm^3 and that the dopant concentration of the pair of third regions be higher than or equal to 5×10^{19} atoms/cm^3 and lower than or equal to 1×10^{22} atoms/cm^3.

[0023] In the semiconductor device according to one embodiment of the present invention, the second electrode and the third electrode may be in contact with either top surfaces of the pair of third regions or bottom surfaces of the pair of third regions.

[0024] An area where the gate insulating film is formed depends on how to form the sidewall insulating film. Specifically, the gate insulating film can be formed over the first region, the second regions, and the third regions or only over the first region.

[0025] In the case where a nitride insulating film is used as the sidewall insulating film and an oxide insulating film is used as the gate insulating film, the gate insulating film functions as an etching stopper in formation of the sidewall insulating film owing to the etching selectivity between the nitride insulator and the oxide insulator, so that excessive etching of the oxide semiconductor film in contact with a bottom surface of the gate insulating film can be suppressed. As a result, in the semiconductor device having the structure, the gate insulating film is left over the first region, the pair of second regions, and the pair of third regions.

[0026] In the case where an oxide insulating film is used as each of the sidewall insulating film and the gate insulating film, the gate insulating film provided over the pair of second regions and the pair of third regions can be etched by utilizing the etching selectivity between the oxide insulating film and the first electrode. As a result, in the semiconductor device having the structure, the gate insulating film is left over the first region.

[0027] According to one embodiment of the present invention, a semiconductor device which includes an oxide semiconductor, has favorable electric characteristics and reliability, and is easily miniaturized can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0028] In the accompanying drawings:

[0029] FIGS. **1**A and **1**B are a top view and a cross-sectional view, respectively, illustrating an example of a semiconductor device which is one embodiment of the present invention;

[0030] FIGS. **2**A to **2**C illustrate a method for manufacturing a semiconductor device which is one embodiment of the present invention;

[0031] FIGS. **3**A to **3**E illustrate a method for manufacturing a semiconductor device which is one embodiment of the present invention;

[0032] FIGS. **4**A and **4**B are a top view and a cross-sectional view, respectively, illustrating an example of a semiconductor device which is one embodiment of the present invention;

[0033] FIGS. **5**A to **5**E illustrate a method for manufacturing a semiconductor device which is one embodiment of the present invention;

[0034] FIGS. **6**A and **6**B are a top view and a cross-sectional view, respectively, illustrating an example of a semiconductor device which is one embodiment of the present invention;

[0035] FIGS. **7**A to **7**E illustrate a method for manufacturing a semiconductor device which is one embodiment of the present invention;

[0036] FIGS. **8**A and **8**B illustrate band structures of oxide semiconductors and a metal material;

[0037] FIGS. **9**A to **9**D are cross-sectional views illustrating examples of a semiconductor device which is one embodiment of the present invention;

[0038] FIGS. **10**A and **10**B are cross-sectional views illustrating examples of a resistor element which is one embodiment of the present invention;

[0039] FIGS. **11**A and **11**B are examples of circuit diagrams each illustrating one embodiment of the present invention;

[0040] FIG. **12** is an example of a circuit diagram illustrating one embodiment of the present invention;

[0041] FIGS. **13**A and **13**B are examples of circuit diagrams each illustrating one embodiment of the present invention;

[0042] FIGS. **14**A and **14**B are examples of circuit diagrams each illustrating one embodiment of the present invention; and

[0043] FIG. **15**A is a block diagram illustrating a specific example of a CPU, and FIGS. **15**B and **15**C are circuit diagrams of part thereof.

BEST MODE FOR CARRYING OUT THE INVENTION

[0044] Embodiments of the present invention will be described in detail with reference to the accompanying drawings. Note that the present invention is not limited to the description below, and it is easily understood by those skilled in the art that various changes and modifications can be made without departing from the spirit and scope of the present invention. Therefore, the present invention should not be construed as being limited to the description in the following embodiments. Note that in structures of the present invention described below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and description thereof is not repeated.

[0045] Note that in each drawing described in this specification, the size, the film thickness, or the region of each component is exaggerated for clarity in some cases. Therefore, embodiments of the present invention are not limited to such scales.

[0046] Note that terms such as "first", "second", and "third" in this specification are used in order to avoid confusion among components, and the terms do not limit the components numerically. Therefore, for example, the term "first" can be replaced with the term "second", "third", or the like as appropriate.

[0047] Functions of a "source" and a "drain" may be replaced with each other when the direction of current flow is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be used to denote the drain and the source, respectively, in this specification.

Embodiment 1

[0048] In this embodiment, a structure of a transistor which is one embodiment of the present invention and a method for manufacturing the transistor will be described with reference to FIGS. **1**A and **1**B, FIGS. **2**A to **2**C, and FIGS. **3**A to **3**E.

(Structure and Characteristic of Transistor **100**)

[0049] FIG. **1**A is a plan view of a transistor **100**. Note that a base insulating film **102**, a gate insulating film **111**, and an interlayer insulating film **117** are not illustrated in FIG. **1**A for convenience.

[0050] In FIG. **1**A, a first electrode **113** and a sidewall insulating film **115** on side surfaces of the first electrode **113** are provided over an oxide semiconductor film **103**. Further, a second electrode **119***a* and a third electrode **119***b* are provided over a pair of third regions **109***a* and **109***b* in the oxide semiconductor film **103** through openings **116***a* and **116***b*. The second electrode **119***a* and the third electrode **119***b* are in contact with top surfaces of the pair of third regions **109***a* and **109***b*. The transistor **100** is a top-gate top-contact transistor.

[0051] FIG. **1**B is a cross-sectional view of the transistor **100** along A-B. In FIG. **1**B, the base insulating film **102** is provided over a substrate **101**, and the oxide semiconductor film **103** including a first region **105**, a pair of second regions **107***a* and **107***b*, and the pair of third regions **109***a* and **109***b* is provided over the base insulating film **102**. The pair of second regions **107***a* and **107***b* is provided in contact with side surfaces of the first region **105**. The pair of third regions **109***a* and **109***b* is provided in contact with side surfaces of the pair of second regions **107***a* and **107***b*.

[0052] The gate insulating film **111** is provided over the oxide semiconductor film **103**. The first electrode **113** which overlaps with the first region **105** is provided over the gate insulating film **111**. Sidewall insulating films **115***a* and **115***b* (the sidewall insulating film **115**) are provided in contact with the side surfaces of the first electrode **113**.

[0053] The interlayer insulating film **117** is provided over the gate insulating film **111**, the first electrode **113**, and the sidewall insulating films **115***a* and **115***b*.

[0054] The second electrode **119***a* and the third electrode **119***b* are provided in contact with the pair of third regions **109***a* and **109***b* through the opening **116***a* and **116***b* provided in the gate insulating film **111** and the interlayer insulating film **117**. Note that the gate insulating film **111** is in contact with the first region **105**, the pair of second regions **107***a* and **107***b*, and the pair of third regions **109***a* and **109***b*.

[0055] Although end portions of the second electrode **119***a* and the third electrode **119***b* may be tapered, the first electrode **113** preferably has a vertical end. The first electrode **113** is formed to have a vertical end, an insulating film to be the sidewall insulating film **115** (the sidewall insulating films **115***a* and **115***b*) is formed over the first electrode **113**, and highly anisotropic etching is performed; thus, the sidewall insulating film **115** (the sidewall insulating films **115***a* and **115***b*) can be formed.

[0056] In FIGS. **1**A and **1**B, the pair of second regions **107***a* and **107***b* corresponds to regions where the oxide semiconductor film **103** overlaps with the sidewall insulating film **115**, which will be described in detail later. Further, at least part of the sidewall insulating film **115** (the sidewall insulating films **115***a* and **115***b*) may be curved except for regions in contact with the side surfaces of the first electrode **113** and the gate insulating film **111**.

[0057] The oxide semiconductor film **103** including the first region **105**, the pair of second regions **107***a* and **107***b*, and the pair of third regions **109***a* and **109***b* is a metal oxide containing two or more elements selected from In, Ga, Sn, and Zn. Note that the metal oxide has a bandgap greater than or equal to 2 eV, preferably greater than or equal to 2.5 eV, further preferably greater than or equal to 3 eV. The off-state current of the transistor **100** can be reduced by using such a metal oxide having a wide bandgap.

[0058] In the transistor **100**, the first region **105** functions as a channel formation region.

[0059] The first region **105** is the CAAC oxide semiconductor region described above. The CAAC oxide semiconductor is not single crystal, but this does not mean that the CAAC is composed of only an amorphous component. Although the CAAC oxide semiconductor includes a crystallized portion (a crystalline portion), a boundary between one crystalline portion and another crystalline portion is not clear in some cases. Nitrogen may be substituted for part of oxygen included in the CAAC oxide semiconductor. The c-axes of individual crystalline portions included in the CAAC oxide semiconductor may be aligned in one direction (e.g., a direction perpendicular to a surface of a substrate over which the CAAC oxide semiconductor is formed or a surface, a film surface, an interface, or the like of the CAAC oxide semiconductor). Alternatively, the normals of the a-b planes of the individual crystalline portions included in the CAAC oxide semiconductor may be aligned in one direction (e.g., a direction perpendicular to the substrate surface or the surface over which the CAAC oxide semiconductor is formed, the film surface, the interface, or the like of the CAAC oxide semiconductor film). Note that the CAAC oxide semiconductor can be a conductor, a semiconductor, or an insulator, depending on the composition or the like. Further, the CAAC oxide semiconductor transmits or does not transmit visible light, depending on the composition or the like. As an example of the CAAC oxide semiconductor, a material is given in which triangular or hexagonal atomic arrangement can be observed from the direction perpendicular to a surface of the deposited material, a surface of a substrate over which the material is deposited, or an interface of the deposited material and in which layered arrangement of metal atoms or layered arrangement of metal atoms and oxygen atoms (or nitrogen atoms) can be observed in a cross section of the deposited material.

[0060] The hydrogen concentration of the first region **105** is lower than or equal to 1×10^{20} atoms/cm^3, preferably lower than or equal to 1×10^{19} atoms/cm^3, further preferably lower than or equal to 1×10^{18} atoms/cm^3. The transistor **100** in which the first region **105** serving as the channel formation region is the CAAC oxide semiconductor region and the hydrogen concentration is reduced is a highly reliable transistor having stable electric characteristics, because change in the threshold voltage between before and after light irradiation and a gate bias-temperature (BT) stress test is small.

[0061] The pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* each have a conductivity higher than or equal to 10 S/cm and lower than or equal to 1000 S/cm, preferably higher than or equal to 100 S/cm and lower than or equal to 1000 S/cm. Further, the conductivity of the pair of third regions **109***a* and **109***b* is higher than the conductivity of the pair of second regions **107***a* and **107***b*. Note that when the conductivity is too low, the on-state current of the transistor **100** is decreased.

[0062] In addition, the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* are each an amorphous region containing a dopant. One or more elements selected from Group 15 elements such as nitrogen, phosphorus, and arsenic are added to the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* as the dopant.

[0063] The carrier density can be increased when the dopant concentrations of the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* are increased; however, an excessively high dopant concentration causes the dopant to inhibit transfer of carriers, resulting in decrease in the conductance of the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b*.

[0064] Therefore, it is preferable that the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* each have a dopant concentration higher than or equal to 5×10^{18} atoms/cm^3 and lower than or equal to 1×10^{22} atoms/cm^3. Further, the dopant concentration of the pair of third regions **109***a* and **109***b* is higher than the dopant concentration of the pair of second regions **107***a* and **107***b*. Specifically, it is preferable that the dopant concentration of the pair of second regions **107***a* and **107***b* be higher than or equal to 5×10^{18} atoms/cm^3 and lower than 5×10^{19} atoms/cm^3 and that the dopant concentration of the pair of third regions **109***a* and **109***b* be higher than or equal to 5×10^{19} atoms/cm^3 and lower than or equal to 1×10^{22} atoms/cm^3. In addition, such a difference in the dopant concentration is made in a self-aligned manner in a step of adding the dopant, because the sidewall insulating film **115** (the sidewall insulating films **115***a* and **115***b*) is provided in the transistor **100**.

[0065] The pair of third regions **109***a* and **109***b* functions as a source region and a drain region of the transistor **100**. In the transistor **100**, amorphous regions having different dopant concentrations (low-concentration regions and high-concentration regions) are provided at both ends of the first region **105** serving as the channel formation region, whereby an electric field applied to the first region **105** serving as the channel formation region can be relieved. Specifically, the pair of second regions **107***a* and **107***b* serving as the low-concentration regions and the pair of third regions **109***a* and **109***b* serving as the high-concentration regions are provided at both the ends of the first region **105** serving as the channel formation region, whereby an effect in which a band edge of a channel formed in the first region **105** is hardly curved is exhibited in the transistor **100**. Accordingly, provision of the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* can suppress a short-channel effect.

(Method for Manufacturing Transistor **100**)

[0066] Next, a method for manufacturing the transistor **100** will be described with reference to FIGS. **2**A to **2**C and FIGS. **3**A to **3**E.

[0067] The base insulating film **102** is formed over the substrate **101**. The base insulating film **102** can be formed by a sputtering method, a CVD method, a coating method, or the like. Note that the thickness of the base insulating film **102** is preferably, but not limited to, 50 nm or more.

[0068] There is no particular limitation on a material and the like of the substrate **101** as long as the material has heat resistance high enough to withstand at least heat treatment performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, or a sapphire substrate may be used as the substrate **101**. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, an SOI substrate, or the like may be used as the substrate **101**. Further alternatively, any of these substrates provided with a semiconductor element may be used as the substrate **101**.

[0069] A flexible substrate may also be used as the substrate **101**. In the case where a transistor is provided over the flexible substrate, the transistor may be formed directly on the flexible substrate, or the transistor may be formed over a different substrate and then separated from the substrate to be transferred to the flexible substrate. In order to separate the transistor from the substrate and transfer it to the flexible substrate, a region which is easily separated is preferably provided between the different substrate and the transistor.

[0070] The base insulating film **102** prevents diffusion of an impurity (e.g., an alkali metal such as Li or Na) from the substrate **101** and etching of the substrate **101** in an etching step in a manufacturing process of the transistor **100**.

[0071] The base insulating film **102** is formed to have a single-layer structure or a staked-layer structure using any of insulating films selected from oxide insulating films such as a silicon oxide film, a gallium oxide film, and an aluminum oxide film; nitride insulating films such as a silicon nitride film and an aluminum nitride film; a silicon oxynitride film; an aluminum oxynitride film; and a silicon nitride oxide film. Note that the base insulating film **102** preferably contains oxygen in a portion in contact with the oxide semiconductor film **103**. An aluminum nitride film, an aluminum nitride oxide film, and a silicon nitride film which have high thermal conductivity are particularly effective in improving thermal dissipation when used for the base insulating film **102**.

[0072] In the case of being formed by a sputtering method, the base insulating film **102** may be formed using a silicon target, a quartz target, an aluminum target, an aluminum oxide target, or the like in an atmosphere gas containing oxygen. The proportion of oxygen in the atmosphere gas is 6 vol. % or higher, preferably 50 vol. % or higher, to the whole atmosphere gas. By increasing the proportion of the oxygen gas in the atmosphere gas, an insulating film from which oxygen is released by heating can be formed.

[0073] Hydrogen in the target is preferably removed as much as possible. Specifically, an oxide target including an OH group at 100 ppm or lower, preferably 10 ppm or lower, further preferably 1 ppm or lower is used, whereby the hydrogen concentration in the base insulating film **102** can be reduced and thus the electric characteristics and reliability of the transistor **100** can be improved. For example, fused quartz is preferable because it is easily formed so as to include an OH group at 10 ppm or lower and is inexpensive. Needless to say, a target of synthetic quartz having a low OH group concentration may be used.

[0074] Furthermore, in the manufacture of the transistor **100**, the content of an alkali metal such as Li or Na, which is an impurity, is preferably low. In the case where a glass substrate containing an impurity such as an alkali metal is used as the substrate **101**, the above nitride insulating film is preferably formed as the base insulating film **102** in order to prevent entry of an alkali metal. It is further preferable to stack the above oxide insulating film over the nitride insulating film.

[0075] In this specification, silicon oxynitride refers to a substance that contains more oxygen than nitrogen and for example, silicon oxynitride includes oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from greater than or equal to 50 at. % and less than or equal to 70 at. %, greater than or equal to 0.5 at. % and less than or equal to 15 at. %, greater than or equal to 25 at. % and less than or equal to 35 at. %, and greater than or equal to 0 at. % and less than or equal to 10 at. %, respectively. Further, silicon nitride oxide refers to a substance that contains more nitrogen than oxygen and for example, silicon nitride oxide includes oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from greater than or equal to 5 at. % and less than or equal to 30 at. %, greater than or equal to 20 at. % and less than or equal to 55 at. %, greater than or equal to 25 at. % and less than or equal to 35 at. %, and greater than or equal to 10 at. % and less than or equal to 25 at. %, respectively. Note that the above ranges are obtained by measurement using Rutherford backscattering spectrometry (RBS) or hydrogen forward scattering spectrometry (HFS). In addition, the total of the percentages of the constituent elements does not exceed 100 at. %.

[0076] In addition, since the base insulating film **102** preferably contains oxygen in a portion in contact with the oxide semiconductor film **103**, an insulating film from which oxygen is released by heating may be used as the base insulating film **102**. Note that the expression "oxygen is released by heating" means that the amount of released oxygen which is converted into oxygen atoms is greater than or equal to 1.0×10^{18} atoms/cm^3, preferably greater than or equal to 3.0×10^{20} atoms/cm^3, in thermal desorption spectroscopy (TDS) analysis.

[0077] A method for quantifying the amount of released oxygen which is converted into oxygen atoms, with the use of TDS analysis will be described below.

[0078] The amount of released gas in TDS analysis is proportional to the integral value of a spectrum. Therefore, the amount of released gas can be calculated from the ratio of the integral value of a spectrum of an insulating film to the reference value of a standard sample. The reference value of a standard sample refers to the ratio of the density of a predetermined atom contained in a sample to the integral value of a spectrum.

[0079] For example, the number of released oxygen molecules (N_{O2}) from an insulating film can be found according to Numerical Expression 1 with the TDS analysis results of a silicon wafer containing hydrogen at a predetermined density which is the standard sample and the TDS analysis results of the insulating film. Here, all spectra having a mass number of 32 which are obtained by the TDS analysis are assumed to originate from an oxygen molecule. CH_3OH, which is given as a gas having a mass number of 32, is not taken into consideration on the assumption that it is unlikely to be present. Further, an oxygen molecule including an oxygen atom having a mass number of 17 or 18 which is an isotope of an oxygen atom is not taken into consideration either because the proportion of such a molecule in the natural world is minimal.

[FORMULA 1]

$$N_{O2}=N_{H2}/S_{H2}\times S_{O2}\times\alpha \qquad \text{(Numerical Expression 1)}$$

[0080] N_{H2} is the value obtained by conversion of the number of hydrogen molecules desorbed from the standard sample into density. S_{H2} is the integral value of a spectrum of the standard sample which is analyzed by TDS. Here, the reference value of the standard sample is set to N_{H2}/S_{H2}. Sm is the integral value of a spectrum of the insulating film which is analyzed by TDS. α is a coefficient which influences spectrum intensity in TDS analysis. Japanese Published Patent Application No. H6-275697 can be referred to for details of Numerical Expression 1. Note that the above value of the amount of released oxygen is obtained by measurement with a thermal desorption spectroscopy apparatus produced by ESCO Ltd., EMD-WA1000S/W using a silicon wafer containing hydrogen atoms at 1×10^{16} atoms/cm^3 as the standard sample.

[0081] Further, in the TDS analysis, part of oxygen is detected as an oxygen atom. The ratio between oxygen molecules and oxygen atoms can be calculated from the ionization rate of the oxygen molecules. Note that, since the above a includes the ionization rate of the oxygen molecules, the number of the released oxygen atoms can also be estimated through the evaluation of the number of the released oxygen molecules.

[0082] Note that N_{O2} is the number of the released oxygen molecules. For the insulating film, the amount of released oxygen in the case of being converted into oxygen atoms is twice the number of the released oxygen molecules.

[0083] As an example of the insulating film from which oxygen is released by heating, oxygen-excess silicon oxide (SiO_X (X>2)) is given. In the oxygen-excess silicon oxide (SiO_X (X>2)), the number of oxygen atoms per unit volume is more than twice the number of silicon atoms per unit volume. The number of silicon atoms and the number of oxygen atoms per unit volume are measured by Rutherford backscattering spectrometry.

[0084] By using the insulating film from which oxygen is released by heating as the base insulating film **102**, oxygen can be supplied to the oxide semiconductor film **103** and interface states between the base insulating film **102** and the oxide semiconductor film **103** can be reduced. Accordingly, electric charge or the like that can be generated owing to operation of the transistor **100** can be prevented from being trapped at the interface between the base insulating film **102** and the oxide semiconductor film **103**, and thus the transistor **100** can be a transistor with little deterioration of electric characteristics.

[0085] Further, electric charge is generated owing to an oxygen vacancy in the oxide semiconductor film **103** in some cases. In general, when oxygen vacancies are caused in an oxide semiconductor, part of the oxygen vacancies becomes a donor to generate an electron as a carrier. That is, also in the transistor **100**, part of oxygen vacancies in the oxide semiconductor film **103** becomes a donor to generate an electron as a carrier and thus the threshold voltage of the transistor **100** is negatively shifted. In addition, the generation of an electron in the oxide semiconductor film **103** often occurs in oxygen vacancies caused in the vicinity of the interface between the oxide semiconductor film **103** and the base insulating film **102**. When oxygen is sufficiently released from the base insulating film **102** to the oxide semiconductor film **103**, oxygen vacancies in the oxide semiconductor film **103**, which might cause the negative shift of the threshold voltage, can be compensated.

[0086] That is, by using the insulating film from which oxygen is released by heating as the base insulating film **102**, interface states between the oxide semiconductor film **103** and the base insulating film **102** and oxygen vacancies in the oxide semiconductor film **103** can be reduced; thus, an influence of charge trap at the interface between the oxide semiconductor film **103** and the base insulating film **102** can be reduced.

[0087] Next, the oxide semiconductor film **103** is formed over the base insulating film **102**.

[0088] Specifically, an oxide semiconductor film **140** which is an entirely CAAC oxide semiconductor film is formed, and then a dopant is added to the oxide semiconductor film **140**, so that the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* are formed. In this manner, the oxide semiconductor film **103** is formed. Here, a method for forming the oxide semiconductor film **140** which is a CAAC oxide semiconductor film in the state before the dopant is added to form the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* will be described.

[0089] There are two methods for forming the oxide semiconductor film **140** which is a CAAC oxide semiconductor film.

[0090] One of the methods is a method in which an oxide semiconductor is deposited while a substrate is heated (referred to as a 1-step method for convenience), and the other method is a method in which an oxide semiconductor is deposited twice and heat treatment is performed twice (referred to as a 2-step method for convenience).

[0091] Firstly, a method for forming the oxide semiconductor film **140** on the basis of the 1-step method will be described.

[0092] First, the oxide semiconductor material given in the description of the oxide semiconductor film **103** is deposited by a sputtering method while the substrate **101** provided with the base insulating film **102** is heated. Note that an oxide semiconductor film formed in this step is referred to as an oxide semiconductor film **130** for convenience. The temperature at which the substrate **101** is heated may be higher than or equal to 200° C. and lower than or equal to 400° C., preferably higher than or equal to 250° C. and lower than or equal to 350° C. The oxide semiconductor film **130** may be formed to a thickness greater than or equal to 1 nm and less than or equal to 50 nm.

[0093] Here, a sputtering apparatus used for formation of the oxide semiconductor film **130** will be described in detail below.

[0094] The leakage rate of a treatment chamber in which the oxide semiconductor film **130** is formed is preferably lower than or equal to 1×10^{-10} Pa·m^3/s; thus, entry of an impurity into the film can be suppressed in the formation by a sputtering method.

[0095] In order to lower the leakage rate, internal leakage as well as external leakage needs to be reduced. The external leakage refers to inflow of gas from the outside of a vacuum system through a minute hole, a sealing defect, or the like. The internal leakage is due to leakage through a partition, such as a valve, in a vacuum system or due to released gas from an internal member. Measures need to be taken from both aspects of external leakage and internal leakage in order that the leakage rate be lower than or equal to 1×10^{-10} Pa·m^3/s.

[0096] In order to reduce external leakage, an open/close portion of the treatment chamber is preferably sealed with a metal gasket. For the metal gasket, a metal material covered with iron fluoride, aluminum oxide, or chromium oxide is preferably used. The metal gasket realizes higher adhesion than an O-ring, and can reduce the external leakage. Further, by use of a metal material covered with iron fluoride, aluminum oxide, chromium oxide, or the like which is in the passive state, released gas containing hydrogen generated from the metal gasket is suppressed, so that the internal leakage can also be reduced.

[0097] As a member for an inner wall of the treatment chamber, aluminum, chromium, titanium, zirconium, nickel, or vanadium, from which a gas containing hydrogen is less likely to be released, or an alloy material which contains at least one of iron, chromium, nickel, and the like and is covered with any of these elements may be used. The alloy material containing at least one of iron, chromium, nickel, and the like is rigid, resistant to heat, and suitable for processing. Here, when surface unevenness of the member is reduced by polishing or the like to reduce the surface area of the inner wall of the treatment chamber, the released gas can be reduced. Alternatively, the member may be covered with iron fluoride, aluminum oxide, chromium oxide, or the like which is in the passive state.

[0098] Furthermore, it is preferable to provide a refiner for an atmosphere gas just in front of the treatment chamber. At this time, the length of a pipe between the refiner and the treatment chamber is less than or equal to 5 m, preferably less than or equal to 1 m. When the length of the pipe is less than or equal to 5 m or less than or equal to 1 m, an influence of the released gas from the pipe can be reduced accordingly.

[0099] Evacuation of the treatment chamber is preferably performed with a rough vacuum pump, such as a dry pump, and a high vacuum pump, such as a sputter ion pump, a turbo molecular pump, or a cryopump, in appropriate combination. The turbo molecular pump has an outstanding capability in evacuating a large-sized molecule, whereas it has a low capability in evacuating hydrogen or water. Hence, combination of a cryopump having a high capability in evacuating water and a sputter ion pump having a high capability in evacuating hydrogen is effective.

[0100] An adsorbate present in the treatment chamber does not affect the pressure in the treatment chamber because it is adsorbed on the inner wall, but the adsorbate leads to release of gas at the time of the evacuation of the treatment chamber. Therefore, although the leakage rate and the evacuation rate do not have a correlation, it is important that the adsorbate present in the treatment chamber be desorbed as much as possible and evacuation be performed in advance with the use of a pump having high evacuation capability. Note that the treatment chamber may be subjected to baking for promotion of desorption of the adsorbate. By the baking, the rate of desorption of the adsorbate can be increased about tenfold. The baking may be performed at a temperature higher than or equal to 100° C. and lower than or equal to 450° C. At this time, when the adsorbate is removed while an inert gas is introduced, the rate of desorption of water or the like, which is difficult to desorb only by evacuation, can be further increased.

[0101] In a sputtering method, an RF power supply device, an AC power supply device, a DC power supply device, or the like can be used as appropriate as a power supply device for generating plasma.

[0102] As a target used for forming the oxide semiconductor film **130** by a sputtering method, a metal oxide target containing zinc can be used. Alternatively, a metal oxide target containing two or more elements selected from indium, gallium, tin, and zinc can be used. As the target, for example, any of the following targets can be used: a four-component metal oxide such as an In—Sn—Ga—Zn-based metal oxide; three-component metal oxides such as an In—Ga—Zn-based metal oxide, an In—Sn—Zn-based metal oxide, an In—Al—Zn-based metal oxide, a Sn—Ga—Zn-based metal oxide, an Al—Ga—Zn-based metal oxide, a Sn—Al—Zn-based metal oxide, an In—Hf—Zn-based metal oxide, an In—La—Zn-based metal oxide, an In—Ce—Zn-based metal oxide, an In—Pr—Zn-based metal oxide, an In—Nd—Zn-based metal oxide, an In—Sm—Zn-based metal oxide, an In—Eu—Zn-based metal oxide, an In—Gd—Zn-based metal oxide, an In—Tb—Zn-based metal oxide, an In—Dy—Zn-based metal oxide, an In—Ho—Zn-based metal oxide, an In—Er—Zn-based metal oxide, an In—Tm—Zn-based metal oxide, an In—Yb—Zn-based metal oxide, and an In—Lu—Zn-based metal oxide; two-component metal oxides such as an In—Zn-based metal oxide, a Sn—Zn-based metal oxide, and an In—Ga-based metal oxide; and a single-component metal oxide containing indium, tin, zinc, or the like.

[0103] As an example of the target, a metal oxide target containing In, Ga, and Zn (an In—Ga—Zn-based metal oxide) has a composition ratio where $In_2O_3:Ga_2O_3:ZnO=1:1:1$ [molar ratio]. Alternatively, a target having a composition ratio where $In_2O_3:Ga_2O_3:ZnO=1:1:2$ [molar ratio], a target having a composition ratio where $In_2O_3:Ga_2O_3:ZnO=1:1:4$ [molar ratio], or a target having a composition ratio where $In_2O_3:Ga_2O_3:ZnO=2:1:8$ [molar ratio] can be used.

[0104] As the atmosphere gas, a rare gas (typically argon) atmosphere, an oxygen atmosphere, or a mixed gas of a rare gas and oxygen is used as appropriate. It is preferable that a high-purity gas from which impurities such as hydrogen, water, hydroxyl, and hydride are removed be used as the atmosphere gas.

[0105] With the use of the above sputtering apparatus, the oxide semiconductor film **130** into which entry of hydrogen is suppressed can be formed.

[0106] The base insulating film **102** and the oxide semiconductor film **130** may be successively formed in vacuum. For example, after impurities including hydrogen over the surface of the substrate **101** are removed by heat treatment or plasma treatment, the base insulating film **102** may be formed without exposure to the air, and the oxide semiconductor film **130** may be successively formed without exposure to the air. In this manner, impurities including hydrogen over the surface of the substrate **101** can be reduced, and an atmospheric component can be prevented from attaching to the interface between the substrate **101** and the base insulating film **102** and the interface between the base insulating film **102** and the oxide semiconductor film **130**. As a result, it is possible to manufacture the transistor **100** having favorable electric characteristics and high reliability.

[0107] Then, a resist mask is formed over the oxide semiconductor film **130** in a first photolithography step. Processing is performed using the resist mask in a first etching step, so that an island-shaped oxide semiconductor film **132** is formed. Note that the resist mask can be formed by an ink-jet method, a printing method, or the like as appropriate, as well as through the photolithography step.

[0108] In the first etching step, etching is preferably performed so that an end portion of the island-shaped oxide semiconductor film **132** is tapered. The island-shaped oxide semiconductor film **132** is formed to have a tapered end portion, whereby the coverage with the gate insulating film **111** formed later can be improved. In the case of using a photolithography step, the tapered shape can be obtained by etching while removing the resist mask.

[0109] The first etching step may be dry etching, wet etching, or combination thereof. As an etchant used for wet etching, a mixed solution of phosphoric acid, acetic acid, and nitric acid, an ammonia hydrogen peroxide mixture (31 wt % hydrogen peroxide water: 28 wt % ammonia water: water=5:2:2 (volume ratio)), or the like can be used. Alternatively, ITO07N (produced by KANTO CHEMICAL CO., INC.) may be used.

[0110] As an etching gas for dry etching, a gas containing chlorine (a chlorine-based gas such as chlorine (Cl_2), boron trichloride (BCl_3), silicon tetrachloride ($SiCl_4$), or carbon tetrachloride (CCl_4)) is preferably used.

[0111] Alternatively, a gas containing fluorine (a fluorine-based gas such as carbon tetrafluoride (CF_4), sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), or trifluoromethane (CHF_3)); hydrogen bromide (HBr); oxygen (O_2); any of these gases to which a rare gas such as helium (He) or argon (Ar) is added; or the like can be used.

[0112] For dry etching, a parallel plate reactive ion etching (RIE) method or an inductively coupled plasma (ICP) etching method can be used. In order to process the film into a desired shape, the etching condition (the amount of electric power applied to a coil-shaped electrode, the amount of electric power applied to an electrode on a substrate side, the temperature of the electrode on the substrate side, or the like) is adjusted as appropriate.

[0113] Heat treatment is performed after the oxide semiconductor film **132** is formed, so that the oxide semiconductor film **140** is formed. The heat treatment is performed at a temperature higher than or equal to 150° C. and lower than or equal to 650° C., preferably higher than or equal to

250° C. and lower than or equal to 450° C., in an oxidation atmosphere or an inert atmosphere. Here, the oxidation atmosphere refers to an atmosphere including an oxidation gas such as oxygen, ozone, or nitrogen oxide at 10 ppm or higher. The inert atmosphere refers to an atmosphere which includes the oxidation gas at lower than 10 ppm and is filled with nitrogen or a rare gas. The treatment time is 3 minutes to 24 hours. The ratio of a crystalline region to an amorphous region in the oxide semiconductor film can be increased as the treatment time is increased. Note that heat treatment for longer than 24 hours is not preferable because the productivity is decreased. Note that the heat treatment may be performed after formation of the oxide semiconductor film **132** and the gate insulating film **111**.

[0114] By the heat treatment, hydrogen is released from the oxide semiconductor film **132**, and in addition, part of oxygen contained in the base insulating film **102** is diffused to the oxide semiconductor film **132** and a portion of the base insulating film **102**, which is in the vicinity of the interface with the oxide semiconductor film **132**.

[0115] There is no particular limitation on a heat treatment apparatus used for the heat treatment, and the apparatus may be provided with a device for heating an object to be processed by heat radiation or heat conduction from a heating element such as a resistance heating element. For example, an electric furnace, or a rapid thermal annealing (RTA) apparatus such as a gas rapid thermal annealing (GRTA) apparatus or a lamp rapid thermal annealing (LRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas.

[0116] Here, a method for forming the oxide semiconductor film **140** on the basis of the 2-step method will be described.

[0117] A first oxide semiconductor film is formed, and first heat treatment is performed at a temperature higher than or equal to 400° C. and lower than or equal to 750° C. in an atmosphere of nitrogen, oxygen, a rare gas, or dry air. By the first heat treatment, a first crystalline oxide semiconductor film having a crystalline region is formed in a region including a surface of the first oxide semiconductor film. Then, a second oxide semiconductor film which is thicker than the first oxide semiconductor film is formed, and second heat treatment is performed at a temperature higher than or equal to 400° C. and lower than or equal to 750° C., so that crystal growth proceeds upward with the use of the first crystalline oxide semiconductor film as a seed for the crystal growth and the whole second oxide semiconductor film is crystallized (a second crystalline oxide semiconductor film is formed). The first crystalline oxide semiconductor film and the second crystalline oxide semiconductor film, which are formed in the above-described manner, are used as the oxide semiconductor film **130**, the first photolithography step and the first etching step are performed so that the oxide semiconductor film **132** is formed, and the heat treatment performed after the formation of the oxide semiconductor film **132** in the 1-step method is performed; thus, the oxide semiconductor film **140** can be formed. Note that a heat treatment apparatus used for the first heat treatment and the second heat treatment may be any of the heat treatment apparatuses which can be used for the heat treatment performed after the formation of the oxide semiconductor film **132** in the 1-step method.

[0118] Next, the gate insulating film **111** and the first electrode **113** are formed over the oxide semiconductor film **140** (see FIG. 3A). The gate insulating film **111** can be formed in a manner similar to that of the base insulating film **102**. The thickness of the gate insulating film **111** is preferably greater than or equal to 1 nm and less than or equal to 300 nm, further preferably greater than or equal to 5 nm and less than or equal to 50 nm.

[0119] The gate insulating film **111** is formed to have a single-layer structure or a stacked-layer structure using any of insulating films selected from a silicon oxide film, a gallium oxide film, an aluminum oxide film, a silicon nitride film, a silicon oxynitride film, an aluminum oxynitride film, and a silicon nitride oxide film. It is preferable that the gate insulating film **111** also contain oxygen in a portion in contact with the oxide semiconductor film **103**. Alternatively, an insulating film from which oxygen is released by heating may be used. The insulating film from which oxygen is released by heating is used as the gate insulating film **111**, whereby a defect caused in the oxide semiconductor film **103** can be repaired and deterioration of electric characteristics of the transistor **100** can be suppressed.

[0120] A high-k material such as hafnium oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x>0$, $y>0$)), hafnium silicate to which nitrogen is added ($HfSi_xO_yN_z$ ($x>0$, $y>0$, $z>0$)), or hafnium aluminate ($HfAl_xO_y$ ($x>0$, $y>0$)) may be used. Because of high dielectric constant, a high-k material enables increase in the physical thickness of the gate insulating film while maintaining the capacitance of the gate insulating film as the same as the case that, for example, a silicon film is used for the gate insulating film, thereby reducing the gate leakage current. Note that the gate insulating film **111** may have a single-layer structure using the high-k material or a stacked-layer structure using a film of the high-k material and the above insulating film.

[0121] For the first electrode **113**, a conductive film is formed using any of the above conductive materials by a sputtering method. A second photolithography step is performed to form a resist mask over the conductive film, and then the conductive film is processed using the resist mask in a second etching step; thus, the first electrode **113** is formed. The thickness of the first electrode **113** is not particularly limited and can be determined as appropriate in consideration of the electric resistance of the conductive material used and time for the formation step.

[0122] Further, it is preferable that the gate insulating film **111** and the conductive film to be the first electrode **113** be successively formed without exposure to the air.

[0123] The first electrode **113** is formed to have a single-layer structure or a stacked-layer structure including, as a conductive material, any of metals such as aluminum, titanium, chromium, nickel, copper, yttrium, zirconium, molybdenum, silver, tantalum, and tungsten and an alloy containing any of these metals as a main component. For example, a single-layer structure of an aluminum film containing silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a two-layer structure in which a titanium film is stacked over a tungsten film, a two-layer structure in which a copper film is formed over a copper-magnesium-aluminum alloy film, and a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order can be given. Note that a transparent conductive material containing indium oxide, tin oxide, or zinc oxide may be used. Note that the first electrode **113** also functions as a wiring.

[0124] Further, an In—Ga—Zn—O film containing nitrogen, an In—Sn—O film containing nitrogen, an In—Ga—O film containing nitrogen, an In—Zn—O film containing nitrogen, a Sn—O film containing nitrogen, an In—O film containing nitrogen, or a film of a metal nitride (such as InN or ZnN) is preferably provided between the first electrode **113** and the gate insulating film **111**. These films each have a work function of 5 eV or higher, preferably 5.5 eV or higher, and thus the threshold voltage in electric characteristics of the transistor **100** can be positively shifted; consequently, the transistor **100** can be a so-called normally-off transistor. For example, in the case of using an In—Ga—Zn—O film containing nitrogen, an In—Ga—Zn—O film having a higher nitrogen concentration than at least the oxide semiconductor film **140**, specifically, an In—Ga—Zn—O film having a nitrogen concentration of 7 at. % or higher is used.

[0125] Next, the sidewall insulating films **115***a* and **115***b* are formed. The sidewall insulating film **115** (including the sidewall insulating films **115***a* and **115***b*) is formed using any of the insulating films given in the description of the base insulating film **102** and the gate insulating film **111**.

[0126] In the transistor **100**, the gate insulating film **111** is provided over all of the first region **105**, the pair of second regions **107***a* and **107***b*, and the pair of third regions **109***a* and **109***b*. In order to obtain such a structure, the gate insulating film **111** and the sidewall insulating film **115** (including the sidewall insulating films **115***a* and **115***b*) may be formed using insulating films having different etching rates. With such a structure, the gate insulating film **111** can function as an etching stopper in formation of the sidewall insulating film **115**. By using the gate insulating film **111** as an etching stopper, excessive etching of the oxide semiconductor film **140** can be suppressed. Moreover, an end point of the etching for forming the sidewall insulating film **115** can be easily detected. In addition, when the gate insulating film **111** functions as an etching stopper, the width of the sidewall insulating film **115** (the widths of portions where the sidewall insulating films **115***a* and **115***b* are in contact with the gate insulating film **111** in FIG. 1B) can be easily controlled. The area of the pair of second regions **107***a* and **107***b* serving as the low-concentration regions is determined in accordance with the width of the sidewall insulating film **115** (the widths of the portions where the sidewall insulating films **115***a* and **115***b* are in contact with the gate insulating film **111** in FIG. 1B). As the area of the low-concentration regions is increased, an electric field applied to the first region **105** functioning as the channel formation region can be further relieved.

[0127] First, an insulating film **114** to be the sidewall insulating films **115***a* and **115***b* is formed over the gate insulating film **111** and the first electrode **113** (see FIG. 3B). The insulating film **114** can be formed in a manner similar to that of the base insulating film **102** and is formed using any of the insulating films listed above. There is no particular limitation on the thickness of the insulating film **114**. The insulating film **114** is subjected to a third etching step, so that the sidewall insulating films **115***a* and **115***b* are formed (see FIG. 3C). The third etching step is highly anisotropic etching, and the sidewall insulating films **115***a* and **115***b* can be formed in a self-aligned manner by performing the highly anisotropic etching step on the insulating film **114**. Here, dry etching is preferably employed as the highly anisotropic etching, and a gas containing fluorine such as trifluoromethane (CHF_3), octafluorocyclobutane (C_4F_8), or tetrafluoromethane (CF_4) can be used as an etching gas, for example. A rare gas such as helium (He) or argon (Ar) or hydrogen (H_2) may be added to the etching gas. In addition, as the dry etching, a reactive ion etching method (an RIE method) in which high-frequency voltage is applied to a substrate is preferably used.

[0128] Further, the dopant concentration of the pair of second regions **107***a* and **107***b* formed later depends on the thicknesses of the sidewall insulating films **115***a* and **115***b*; therefore, the thicknesses of the sidewall insulating films **115***a* and **115***b* and the thickness of the first electrode **113** may be determined so that the dopant concentration of the pair of second regions **107***a* and **107***b* is within the above range. Note that the thickness of the sidewall insulating film **115***a* or **115***b* here means the length from a plane thereof which is in contact with the gate insulating film **111** to the highest point of a plane thereof which is in contact with the first electrode **113**.

[0129] In addition, the area of the pair of second regions **107***a* and **107***b* serving as the low-concentration regions is determined in accordance with the width of the sidewall insulating film **115** (here, the widths of the portions where the sidewall insulating films **115***a* and **115***b* are in contact with the gate insulating film **111** in FIG. 1B). Furthermore, the width of the sidewall insulating film **115** depends on the thickness of the first electrode **113**; therefore, the thickness of the first electrode **113** may be determined so that the pair of second regions **107***a* and **107***b* has a desired area.

[0130] Next, treatment for adding a dopant **150** to the oxide semiconductor film **140** is performed, so that the oxide semiconductor film **103** is formed (see FIG. 3D).

[0131] The dopant **150** added is one or more elements selected from Group 15 elements such as nitrogen, phosphorus, and arsenic. As a method for adding the dopant **150** to the oxide semiconductor film **140**, an ion doping method or an ion implantation method can be used. When an ion doping method or an ion implantation method is used, the depth to which the dopant **150** is added (an addition region) can be easily controlled and thus the dopant **150** can be added to the oxide semiconductor film **140** with high accuracy. The dopant **150** may be added by an ion doping method or an ion implantation method while the substrate **101** is heated.

[0132] In the addition of the dopant **150** to the oxide semiconductor film **140**, the dopant **150** is added to the oxide semiconductor film **140** through the gate insulating film **111** and the sidewall insulating films **115***a* and **115***b*. Further, in the oxide semiconductor film **140**, the amount of the added dopant **150** is smaller in a region to which the dopant **150** is added through the gate insulating film **111** and the sidewall insulating film **115***a* or **115***b* than in a region to which the dopant **150** is added through only the gate insulating film **111**. Thus, the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* are formed in a self-aligned manner (see FIG. 3E). Note that the dopant **150** is not added to a region of the oxide semiconductor film **140**, which overlaps with the first electrode **113**.

[0133] Further, the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* get lower crystallinity because of damage due to the addition of the dopant **150** and become amorphous regions. Note that by adjusting the additive amount of the dopant **150** or the like, the degree of damage can be reduced so that the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* are prevented from becoming completely amorphous. In that case, the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* each have at least a higher proportion of an amorphous region than the first region **105**.

[0134] Further, heat treatment may be performed after the dopant **150** is added. The heat treatment may be performed in a manner similar to that of the heat treatment performed in the formation of the oxide semiconductor film **140**, and is preferably performed at a temperature at which the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b* are not crystallized.

[0135] Note that the treatment for adding the dopant **150** to the oxide semiconductor film **140** may be performed plural times. In the case where the treatment for adding the dopant **150** to the oxide semiconductor film **140** is performed plural times, the kind of the dopant **150** may be the same in the plural treatments or different in every treatment. For example, treatment may be performed in the following order: the first electrode **113** is formed as in FIG. **3**A, treatment for adding the dopant **150** (first addition treatment) is performed, the sidewall insulating films **115***a* and **115***b* are formed, and treatment for adding the dopant **150** (second addition treatment) is performed. The dopant **150** may be the same element or different elements in the first addition treatment and the second addition treatment.

[0136] Next, an insulating film to be the interlayer insulating film **117** is formed over the gate insulating film **111**, the sidewall insulating films **115***a* and **115***b*, and the first electrode **113**, and a third photolithography step and a fourth etching step are performed on the insulating film and the gate insulating film **111**, so that the openings **116***a* and **116***b* are formed. The third photolithography step and the fourth etching step may be similar to the first photolithography step and the first etching step.

[0137] The interlayer insulating film **117** may be formed using a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, or a silicon nitride film by a sputtering method, a CVD method, or the like. At this time, a film from which oxygen is less likely to be released by heating is preferably used as the interlayer insulating film **117** in order to prevent decrease in the conductivity of the pair of second regions **107***a* and **107***b* and the pair of third regions **109***a* and **109***b*. Specifically, the interlayer insulating film **117** may be formed by a CVD method with the use of a mixture which includes a silane gas as a main material and a proper source gas selected from a nitrogen oxide gas, a nitrogen gas, a hydrogen gas, and a rare gas. In addition, the substrate temperature may be higher than or equal to 300° C. and lower than or equal to 550° C. By using a CVD method, the film from which oxygen is less likely to be released by heating can be formed.

[0138] Next, the second electrode **119***a* and the third electrode **119***b* are formed to be connected to the pair of third regions **109***a* and **109***b* through the openings **116***a* and **116***b* (see FIG. **1**B).

[0139] Each of the second electrode **119***a* and the third electrode **119***b* also functions as a wiring and is formed using any of the materials given in the description of the first electrode **113**.

[0140] In the transistor **100**, the pair of third regions **109***a* and **109***b* in contact with the second electrode **119***a* and the third electrode **119***b* is regions having high conductivity, to which the dopant is added; therefore, the contact resistance between the second electrode **119***a* and the third region **109***a* and between the third electrode **119***b* and the third region **109***b* can be reduced. Accordingly, the on-state current of the transistor **100** can be increased.

[0141] The second electrode **119***a* and the third electrode **119***b* are formed in such a manner that a conductive film is formed using any of the above conductive materials as in the case of the first electrode **113** and is then subjected to a fourth photolithography step and a fifth etching step. Note that the fourth photolithography step and the fifth etching step may be similar to the first photolithography step and the first etching step.

[0142] Through the above steps, the transistor **100** can be manufactured.

[0143] As described above, according to one embodiment of the disclosed invention, a problem due to miniaturization can be solved. As a result, the size of the transistor can be sufficiently reduced. When the size of the transistor is sufficiently reduced, the area occupied by a semiconductor device is also reduced and thus the number of semiconductor devices manufactured from one substrate is increased. Accordingly, manufacturing cost of the semiconductor device is reduced. Further, the size of the semiconductor device can be reduced with its function maintained; therefore, the semiconductor device can have improved functions as compared with a conventional one of the same size. Further, effects such as high-speed operation, low power consumption, and the like can be obtained because of reduction in channel length. Thus, miniaturization of a transistor including an oxide semiconductor can be achieved according to one embodiment of the disclosed invention, and various effects accompanied with the miniaturization can be obtained. Note that this embodiment can be combined with any of the other embodiments as appropriate.

Embodiment 2

[0144] In this embodiment, a transistor **200** having a structure which is partly different from the structure of the transistor **100** described in Embodiment 1 will be described.

(Structure and Characteristic of Transistor **200**)

[0145] The transistor **200** is a transistor which includes a gate insulating film having a shape different from that of the gate insulating film **111** of the transistor **100**.

[0146] FIG. **4**A is a plan view of the transistor **200**. Note that a base insulating film **202**, a gate insulating film **211**, and an interlayer insulating film **217** are not illustrated in FIG. **4**A for convenience.

[0147] In FIG. **4**A, a first electrode **213** and a sidewall insulating film **215** on side surfaces of the first electrode **213** are provided over an oxide semiconductor film **203**. Further, a second electrode **219***a* and a third electrode **219***b* are provided over third regions **209***a* and **209***b* in the oxide semiconductor film **203** through openings **216***a* and **216***b*. The second electrode **219***a* and the third electrode **219***b* are in contact with top surfaces of the third regions **209***a* and **209***b*. The transistor **200** is a top-gate top-contact transistor.

[0148] FIG. **4**B is a cross-sectional view of the transistor **200** along C-D. In FIG. **4**B, the base insulating film **202** is provided over a substrate **201**, and the oxide semiconductor film **203** including a first region **205**, a pair of second regions **207***a* and **207***b*, and the pair of third regions **209***a* and **209***b* is provided over the base insulating film **202**. The pair of second regions **207***a* and **207***b* is provided in contact with side surfaces of the first region **205**. The pair of third regions **209***a* and **209***b* is provided in contact with side surfaces of the pair of second regions **207***a* and **207***b*.

[0149] The gate insulating film **211** is provided over the oxide semiconductor film **203**. The gate insulating film **211** is in contact with the first region **205**. The first electrode **213** which overlaps with the first region **205** is provided over the gate insulating film **211**. Sidewall insulating films **215***a* and **215***b* are provided in contact with the side surfaces of the first electrode **213**.

[0150] The second electrode **219***a* and the third electrode **219***b* are in contact with the top surfaces of the pair of third regions **209***a* and **209***b* through the openings **216***a* and **216***b* in the interlayer insulating film **217** which is provided over the first electrode **213** and the sidewall insulating films **215***a* and **215***b*.

[0151] Although end portions of the second electrode **219***a* and the third electrode **219***b* may be tapered, the first electrode **213** preferably has a vertical end. The first electrode **213** is formed to have a vertical end, an insulating film to be the sidewall insulating film **215** (the sidewall insulating films **215***a* and **215***b*) is formed over the first electrode **213**, and highly anisotropic etching is performed; thus, the sidewall insulating film **215** (the sidewall insulating films **215***a* and **215***b*) can be formed.

[0152] In FIG. **4**A, the second regions **207***a* and **207***b* correspond to regions where the oxide semiconductor film **203** overlaps with the sidewall insulating film **215**. Further, at least part of the sidewall insulating film **215** is curved except for regions in contact with the side surfaces of the first electrode **213** and the gate insulating film **211**.

[0153] In the transistor **100**, since the gate insulating film **111** is in contact with the first region **105**, the pair of second regions **107***a* and **107***b*, and the pair of third regions **109***a* and **109***b*, the openings **116***a* and **116***b* are provided in the gate insulating film **111** and the interlayer insulating film **117**. In contrast, in the transistor **200**, since the gate insulating film **211** is only in contact with the first region **205**, the openings **216***a* and **216***b* are provided only in the interlayer insulating film **217**.

[0154] In the transistor **200**, the gate insulating film **211** is in contact with the first region **205**, and the gate insulating film **211** does not follow the shape of (does not cover a step formed by) the oxide semiconductor film **203**. In other words, the gate insulating film **211** does not have a portion which extends beyond a step formed by the oxide semiconductor film **203**. The gate insulating film **211** does not have a portion which extends beyond a step formed by the oxide semiconductor film **203**, which contributes to reduction in the leakage current of the transistor **200** due to the gate insulating film **211** and increase in the withstand voltage of the gate insulating film **211**. Therefore, even when the gate insulating film **211** whose thickness is reduced to around 5 nm is used, the transistor can operate. Note that reduction in the thickness of the gate insulating film **211** leads to suppression of a short-channel effect and increase in the operation speed of the transistor.

[0155] Moreover, in the transistor **200**, since the gate insulating film **211** does not have a portion which extends beyond a step, parasitic capacitance is hardly caused between the first electrode **213** and the pair of second regions **207***a* and **207***b* and between the first electrode **213** and the pair of third regions **209***a* and **209***b*. Consequently, even when the channel length of the transistor **200** is shortened, fluctuation in the threshold voltage can be reduced.

(Method for Manufacturing Transistor **200**)

[0156] Next, a method for manufacturing the transistor **200** will be described with reference to FIGS. **2**A to **2**C and FIGS. **5**A to **5**E.

[0157] In the method for manufacturing the transistor **200**, steps preceding a step of forming the insulating film **210** which becomes the gate insulating film **211** (steps up to and including a step of forming the oxide semiconductor film **140** in FIGS. **2**A to **2**C) are the same as those of the transistor **100**; thus, Embodiment 1 can be referred to (see FIGS. **2**A to **2**C). Note that the substrate **201** and the base insulating film **202** may have the same structures as the substrate **101** and the base insulating film **102** described in Embodiment 1.

[0158] Next, an insulating film **210** is formed over the oxide semiconductor film **140**. The insulating film **210** is formed using a material which can be used for the gate insulating film **111** in Embodiment 1. Then, a conductive film **212** to be the first electrode **213** is formed over the insulating film **210** (see FIG. **5**A). The conductive film **212** is formed using a conductive material which can be used for the first electrode **113** described in Embodiment 1. Note that as a method for forming the conductive film **212**, a sputtering method may be used as in Embodiment 1.

[0159] Further, it is preferable that the insulating film **210** and the conductive film **212** be successively formed without exposure to the air.

[0160] The insulating film **210** and the conductive film **212** are processed, so that the gate insulating film **211** and the first electrode **213** are formed. By this processing, the gate insulating film **211** which has a shape different from that of the gate insulating film **111** of the transistor **100** can be formed. Note that the insulating film **210** and the conductive film **212** may be processed using the photolithography step and the etching step described in Embodiment 1 as appropriate. The thickness of the gate insulating film **211** may be determined as appropriate on the basis of the description in Embodiment 1.

[0161] Next, an insulating film **214** to be the sidewall insulating films **215***a* and **215***b* is formed over the oxide semiconductor film **140**, the gate insulating film **211**, and the first electrode **213** (see FIG. **5**B). The insulating film **214** is formed using a material which can be used for the base insulating film **102** in Embodiment 1. After that, the insulating film **214** is processed, so that the sidewall insulating films **215***a* and **215***b* are formed (see FIG. **5**C). A method for processing the insulating film **214** into the sidewall insulating films **215***a* and **215***b* may be the same as the method for processing the insulating film **114** into the sidewall insulating films **115***a* and **115***b*, which is described in Embodiment 1.

[0162] The thickness of the sidewall insulating film **215***a* or **215***b* means the length from a plane thereof which is in contact with the oxide semiconductor film **140** to be the oxide semiconductor film **203** later to the highest point of a plane thereof which is in contact with the first electrode **213**. Further, the dopant concentration of the pair of second regions **207***a* and **207***b* formed later depends on the thicknesses of the sidewall insulating films **215***a* and **215***b*; therefore, the thicknesses of the sidewall insulating films **215***a* and **215***b* and the thickness of the first electrode **213** may be determined so that the dopant concentration of the pair of second regions **207***a* and **207***b* is within the range described in Embodiment 1.

[0163] In addition, the area of the pair of second regions **207***a* and **207***b* serving as low-concentration regions is determined in accordance with the width of the sidewall insulating film **215** (here, the widths of portions where the sidewall insulating films **215***a* and **215***b* are in contact with the oxide semiconductor film **203** in FIG. 4B). As the area of the low-concentration regions is increased, an electric field applied to the first region **205** functioning as a channel formation region can be further relieved. The width of the sidewall insulating film **215** depends on the thickness of the first electrode **213**; therefore, the thickness of the first electrode **213** may be determined so that the pair of second regions **207***a* and **207***b* has a desired area.

[0164] Next, treatment for adding the dopant **150** to the oxide semiconductor film **140** is performed (see FIG. **5**D). The treatment for adding the dopant **150** to the oxide semiconductor film **140** may be performed as in Embodiment 1. By this treatment, the first region **205**, the pair of second regions **207***a* and **207***b*, and the pair of third regions **209***a* and **209***b* are formed (see FIG. **5**E). Note that the first region **205**, the pair of second regions **207***a* and **207***b*, and the pair of third regions **209***a* and **209***b* which are formed by this treatment have structures similar to those of the first region **105**, the pair of second regions **107***a* and **107***b*, and the pair of third regions **109***a* and **109***b* described in Embodiment 1.

[0165] Further, the transistor **200** has such a structure that the dopant **150** is added with part of the oxide semiconductor film **140** exposed, and therefore the dopant **150** can be added by a method other than an ion doping method or an ion implantation method. For example, plasma treatment can be given in which plasma is generated in an atmosphere of a gas containing an element added and an object to which the element is added (here, the oxide semiconductor film **140**) is irradiated with the plasma. As an apparatus for generating the plasma, a dry etching apparatus, a plasma CVD apparatus, a high-density plasma CVD apparatus, or the like can be used. Note that the plasma treatment may be performed while the substrate **201** is heated.

[0166] Note that the treatment for adding the dopant **150** to the oxide semiconductor film **140** can be performed plural times as in Embodiment 1.

[0167] Further, heat treatment may be performed after the dopant **150** is added. The heat treatment may be performed in a manner similar to that of the heat treatment performed in the formation of the oxide semiconductor film **140**, and is preferably performed at a temperature at which the pair of second regions **207***a* and **207***b* and the pair of third regions **209***a* and **209***b* are not crystallized.

[0168] The interlayer insulating film **217**, the openings **216***a* and **216***b*, the second electrode **219***a*, and the third electrode **219***b* may be formed in manners similar to those of the interlayer insulating film **117**, the openings **116***a* and **116***b*, the second electrode **119***a*, and the third electrode **119***b* described in Embodiment 1. Through the above steps, the transistor **200** can be manufactured (see FIG. **4**B).

[0169] The transistor **200** described in this embodiment can achieve an effect similar to that in Embodiment 1. Note that this embodiment can be combined with any of the other embodiments as appropriate.

Embodiment 3

[0170] In this embodiment, a transistor **300** having a structure which is partly different from the structure of the transistor described in the above embodiment will be described.

(Structure and Characteristic of Transistor **300**)

[0171] Which surfaces of a second electrode and a third electrode are in contact with a pair of third regions differs between the transistor **300** and the transistor **200**.

[0172] FIG. **6**A is a plan view of the transistor **300**. Note that a base insulating film **302**, a gate insulating film **311**, and an interlayer insulating film **317** are not illustrated in FIG. **6**A for convenience.

[0173] In FIG. **6**A, a first electrode **313** and a sidewall insulating film **315** on side surfaces of the first electrode **313** are provided over an oxide semiconductor film **303**. Further, a second electrode **319***a* and a third electrode **319***b* are in contact with bottom surfaces of third regions **309***a* and **309***b* in the oxide semiconductor film **303**. The transistor **300** is a top-gate bottom-contact transistor.

[0174] FIG. **6**B is a cross-sectional view of the transistor **300** along E-F. In FIG. **6**B, the base insulating film **302** is provided over a substrate **301**, and the oxide semiconductor film **303** including a first region **305**, a pair of second regions **307***a* and **307***b*, and the pair of third regions **309***a* and **309***b*, the second electrode **319***a*, and the third electrode **319***b* are provided over the base insulating film **302**. The pair of second regions **307***a* and **307***b* is provided in contact with side surfaces of the first region **305**. The pair of third regions **309***a* and **309***b* is provided in contact with side surfaces of the pair of second regions **307***a* and **307***b*.

[0175] The gate insulating film **311** is provided over the oxide semiconductor film **303**. The gate insulating film **311** is in contact with the first region **305**. The first electrode **313** which overlaps with the first region **305** is provided over the gate insulating film **311**. Sidewall insulating films **315***a* and **315***b* are provided in contact with the side surfaces of the first electrode **313**.

[0176] The interlayer insulating film **317** is provided over the gate insulating film **311**, the first electrode **313**, and the sidewall insulating films **315***a* and **315***b*.

[0177] Although end portions of the second electrode **319***a* and the third electrode **319***b* may be tapered, the first electrode **313** preferably has a vertical end. The first electrode **313** is formed to have a vertical end, an insulating film to be the sidewall insulating film **315** (the sidewall insulating films **315***a* and **315***b*) is formed over the first electrode **313**, and highly anisotropic etching is performed; thus, the sidewall insulating film **315** (the sidewall insulating films **315***a* and **315***b*) can be formed.

[0178] In FIG. **6**A, the second regions **307***a* and **307***b* correspond to regions where the oxide semiconductor film

303 overlaps with the sidewall insulating film **315**. Further, at least part of the sidewall insulating film **315** is curved except for regions in contact with the side surfaces of the first electrode **313** and the gate insulating film **311**.

[0179] In the transistor **300**, the gate insulating film **311** is in contact with the first region **305**, and the gate insulating film **311** does not follow the shape of (does not cover a step formed by) the oxide semiconductor film **303**. In other words, the gate insulating film **311** does not have a portion which extends beyond a step formed by the oxide semiconductor film **303**. The gate insulating film **311** does not have a portion which extends beyond a step formed by the oxide semiconductor film **303**, which contributes to reduction in the leakage current of the transistor **300** due to the gate insulating film **311** and increase in the withstand voltage of the gate insulating film **311**. Therefore, even when the gate insulating film **311** whose thickness is reduced to around 5 nm is used, the transistor can operate. Note that reduction in the thickness of the gate insulating film **311** leads to suppression of a short-channel effect and increase in the operation speed of the transistor.

[0180] Moreover, in the transistor **300**, since the gate insulating film **311** does not have a portion which extends beyond a step, parasitic capacitance is hardly caused between the first electrode **313** and the pair of second regions **307***a* and **307***b* and between the first electrode **313** and the pair of third regions **309***a* and **309***b*. Consequently, even when the channel length of the transistor **300** is shortened, fluctuation in the threshold voltage can be reduced.

[0181] The transistor **300** illustrated in FIGS. **6**A and **6**B has a structure in which the gate insulating film **311** is provided only in a region in contact with the first electrode **313**; however, the gate insulating film **311** may also be provided over the third regions **309***a* and **309***b* (and further over the second electrode **319***a* and the third electrode **319***b*) as in Embodiment 1.

(Method for Manufacturing Transistor **300**)

[0182] Next, a method for manufacturing the transistor **300** will be described with reference to FIGS. **7**A to **7**E.

[0183] The base insulating film **302** is formed over the substrate **301**; then, a conductive film to be the second electrode **319***a* and the third electrode **319***b* is formed over the base insulating film **302** and the conductive film is processed, so that the second electrode **319***a* and the third electrode **319***b* are formed. The substrate **301** and the base insulating film **302** may have the same structures as the substrate **101** and the base insulating film **102** described in Embodiment 1. The conductive film is formed using a conductive material which can be used for the second electrode **119***a* and the third electrode **119***b* described in Embodiment 1. Note that as a method for forming the conductive film, a sputtering method may be used as in Embodiment 1. In addition, the conductive film may be processed using the photolithography step and the etching step described in Embodiment 1 as appropriate.

[0184] An oxide semiconductor film **340** is formed over the base insulating film **302**, the second electrode **319***a*, and the third electrode **319***b* (see FIG. **7**A). The oxide semiconductor film **340** can be formed in a manner similar to that of the oxide semiconductor film **140** described in Embodiment 1 (see FIGS. **2**A to **2**C).

[0185] Next, the gate insulating film **311** and the first electrode **313** are formed over the second electrode **319***a*, the third electrode **319***b*, and the oxide semiconductor film **340**. First, an insulating film to be the gate insulating film **311** is formed over the oxide semiconductor film **340**. The gate insulating film **311** and the first electrode **313** may be formed in manners similar to those of the gate insulating film **211** and the first electrode **213** in Embodiment 2.

[0186] Next, an insulating film **314** to be the sidewall insulating films **315***a* and **315***b* is formed over the oxide semiconductor film **340**, the gate insulating film **311**, and the first electrode **313** (see FIG. **7**B). The insulating film **314** is formed using a material which can be used for the base insulating film **102** in Embodiment 1. After that, the insulating film **314** is processed, so that the sidewall insulating films **315***a* and **315***b* are formed (see FIG. **7**C). A method for processing the insulating film **314** into the sidewall insulating films **315***a* and **315***b* may be the same as the method for processing the insulating film **114** into the sidewall insulating films **115***a* and **115***b*, which is described in Embodiment 1.

[0187] The thickness of the sidewall insulating film **315***a* or **315***b* means the length from a plane thereof which is in contact with the oxide semiconductor film **340** to be the oxide semiconductor film **303** later to the highest point of a plane thereof which is in contact with the first electrode **313**. Further, the dopant concentration of the pair of second regions **307***a* and **307***b* formed later depends on the thicknesses of the sidewall insulating films **315***a* and **315***b*; therefore, the thicknesses of the sidewall insulating films **315***a* and **315***b* and the thickness of the first electrode **313** may be determined so that the dopant concentration of the pair of second regions **307***a* and **307***b* is within the range described in Embodiment 1.

[0188] In addition, the area of the pair of second regions **307***a* and **307***b* serving as low-concentration regions is determined in accordance with the width of the sidewall insulating film **315** (here, the widths of portions where the sidewall insulating films **315***a* and **315***b* are in contact with the oxide semiconductor film **340** in FIG. **6**B). As the area of the low-concentration regions is increased, an electric field applied to the first region **305** functioning as a channel formation region can be further relieved. The width of the sidewall insulating film **315** depends on the thickness of the first electrode **313**; therefore, the thickness of the first electrode **313** may be determined so that the pair of second regions **307***a* and **307***b* has a desired area.

[0189] Next, treatment for adding the dopant **150** to the oxide semiconductor film **340** is performed (see FIG. **7**D). The treatment for adding the dopant **150** to the oxide semiconductor film **340** may be performed as in Embodiment 1. By this treatment, the first region **305**, the pair of second regions **307***a* and **307***b*, and the pair of third regions **309***a* and **309***b* are formed (see FIG. **7**E). Note that the first region **305**, the pair of second regions **307***a* and **307***b*, and the pair of third regions **309***a* and **309***b* which are formed by this treatment have structures similar to those of the first region **105**, the pair of second regions **107***a* and **107***b*, and the pair of third regions **109***a* and **109***b* described in Embodiment 1.

[0190] Further, as in the case of the transistor **200**, the transistor **300** has a structure in which the dopant **150** is added with part of the oxide semiconductor film **340** exposed. Therefore, as a method for adding the dopant **150**, plasma treatment can be used as in Embodiment 2. Note that the plasma treatment is similar to the plasma treatment described in Embodiment 2.

[0191] Note that the treatment for adding the dopant **150** to the oxide semiconductor film **340** can be performed plural times as in Embodiment 1.

[0192] Even in the case where the gate insulating film **311** is also provided over the third regions **309***a* and **309***b* (and further over the second electrode **319***a* and the third electrode **319***b*) as in Embodiment 1, the treatment for adding the dopant **150** to the oxide semiconductor film **340** can be performed. In that case, the dopant **150** is added to the oxide semiconductor film **340** through the gate insulating film **311** and the sidewall insulating films **315***a* and **315***b*.

[0193] Further, heat treatment may be performed after the dopant **150** is added. The heat treatment may be performed in a manner similar to that of heat treatment performed in the formation of the oxide semiconductor film **340**, and is preferably performed at a temperature at which the pair of second regions **307***a* and **307***b* and the pair of third regions **309***a* and **309***b* are not crystallized.

[0194] Next, the interlayer insulating film **317** is formed over the first electrode **313**, the second electrode **319***a*, the third electrode **319***b*, and the sidewall insulating films **315***a* and **315***b* in a manner similar to that of the interlayer insulating film **117** described in Embodiment 1. Through the above steps, the transistor **300** can be manufactured (see FIG. 6B).

[0195] The transistor **300** described in this embodiment can achieve an effect similar to that in Embodiment 1. Note that this embodiment can be combined with any of the other embodiments as appropriate.

Embodiment 4

[0196] In this embodiment, as for the transistors described in Embodiments 1 to 3, influences of electric characteristics of the first region, the pair of second regions, and the pair of third regions which are included in the oxide semiconductor film on the transistor will be described using band diagrams. Note that the transistor **300** illustrated in FIGS. **6**A and **6**B will be used as an example.

[0197] FIGS. **8**A and **8**B are each an energy band diagram (a schematic diagram) of the transistor **300** (see FIG. **6**B) in a cross section along G-H. Note that FIG. **8**B shows the case where the potential of a source region is equal to that of a drain region (VD=0 V). The transistor **300** includes the oxide semiconductor film **303** including the first region **305** (denoted by OS**1**), the pair of second regions **307***a* and **307***b* (denoted by OS**2**), and the pair of third regions **309***a* and **309***b* (denoted by OS**3**); and the second and third electrodes **319***a* and **319***b* (denoted by metal).

[0198] The channel formation region of the transistor **300** is formed using OS**1**, and OS**1** is formed using an intrinsic (i-type) oxide semiconductor or a substantially intrinsic oxide semiconductor which is obtained by removing or eliminating impurities such as moisture (including hydrogen) from the film as much as possible so that the purity is increased. Thus, the Fermi level (Ef) can be at the same level as the intrinsic Fermi level (Ei).

[0199] The low-concentration regions of the transistor **300** are formed using OS**2**, and the source region and the drain region are formed using OS**3**. As in the case of OS**1**, each of OS**2** and OS**3** is formed using an intrinsic (i-type) or substantially intrinsic oxide semiconductor which is obtained by removing or eliminating impurities such as moisture (including hydrogen) from the film as much as possible so that the purity is increased. Then, one or more kinds of dopants selected from Group 15 elements such as nitrogen, phosphorus, and arsenic are added to OS**2** and OS**3**. Accordingly, OS**2** and OS**3** each have high carrier density and a Fermi level close to the conduction band, as compared with O**81**.

[0200] FIG. **8**A shows the relation between the vacuum level (denoted by Evac) and band structures of the first region **305** (denoted by O**81**), the pair of second regions **307***a* and **307***b* (denoted by OS**2**), the pair of third regions **309***a* and **309***b* (denoted by OS**3**), and the second and third electrodes **319***a* and **319***b* (denoted by metal). Here, IP represents the ionization potential; Ea, the electron affinity; Eg, the band gap; and Wf, the work function. In addition, Ec represents the conduction band minimum; Ev, the valence band maximum; and Ef, the Fermi level. As for a sign at the end of each symbol, 1 denotes OS**1**, 2 denotes OS**2**, 3 denotes OS**3**, and m denotes metal. Here, a metal having a work function of 4.1 eV (such as titanium) is assumed as metal.

[0201] OS**1** is a highly purified oxide semiconductor and thus has extremely low carrier density; therefore, Ef_**1** is around the middle point between Ec and Ev. Further, OS**2** and OS**3** are each an oxide semiconductor having high carrier density, to which a dopant is added, and Ec_**2** and Ec_**3** generally correspond to Ef_**2** and Ef_**3**, respectively.

[0202] The oxide semiconductor denoted by OS**1** is said to have a band gap of 3.15 eV and an electron affinity (Ea) of 4.3 eV. The band gap of each of the oxide semiconductors denoted by OS**2** and OS**3** can be made smaller than 3.15 by adjusting the additive amount of the dopant. In that case, there is little change in the ionization potentials of the oxide semiconductors denoted by OS**2** and OS**3**, and thus the electron affinities and work functions thereof are increased. FIGS. **8**A and **8**B show the case where OS**2** and OS**3** both have smaller Eg than OS**1**. In addition, since the additive amount of the dopant for 0S**3** is larger than that for OS**2**, Eg of OS**3** is smaller than Eg of OS**2**. That is, Eg of OS**1**, OS**2**, and OS**3** descends in this order (i.e., Eg_**1**>Eg_**2**>Eg_**3**).

[0203] As illustrated in FIG. **8**B, when OS**1** serving as the channel formation region is in contact with OS**2** serving as the low-concentration regions, carriers transfer so that the Fermi levels of OS**1** and OS**2** become equal and band edges of OS**1** are curved. Similarly, when OS**2** serving as the low-concentration regions is in contact with OS**3** serving as the source region and the drain region, carriers transfer so that the Fermi levels of OS**2** and OS**3** become equal and band edges of OS**2** are curved. Further, similarly, when OS**3** serving as the source region and the drain region is in contact with metal, carriers transfer so that the Fermi levels of OS**3** and metal become equal and band edges of OS**3** are curved.

[0204] As described above, OS**2** and OS**3** which are oxide semiconductors having different high carrier densities are formed between OS**1** serving as the channel and metal serving as the second electrode **319***a* and the third electrode **319***b*, whereby an ohmic contact can be formed between the oxide semiconductor film **303** and metal, and the contact resistance can be reduced. As a result, the on-state current of the transistor **300** can be increased. Moreover, the curve at the band edges of OS**1** can be suppressed, and thus a short-channel effect in the transistor **300** can be reduced.

Embodiment 5

[0205] In this embodiment, examples of transistors which are different from the transistors described in the above embodiments will be described with reference to FIGS. **9**A to **9**D.

[0206] FIG. **9**A is a cross-sectional view of a transistor **400**, and FIG. **9**B is an enlarged view of a portion surrounded by a dotted line in FIG. **9**A.

[0207] The transistor **400** has the following structure. A base insulating film **402** is provided over a substrate **401**. An oxide semiconductor film **403** including a first region **405**, a pair of second regions **407***a* and **407***b*, a pair of third regions **409***a* and **409***b*, and a pair of fourth regions **410***a* and **410***b* is provided over the base insulating film **402**. A second electrode **419***a* and a third electrode **419***b* are provided over the pair of fourth regions **410***a* and **410***b*. A gate insulating film **411** is provided over the first region **405**, the pair of second regions **407***a* and **407***b*, the pair of third regions **409***a* and **409***b*, the pair of fourth regions **410***a* and **410***b*, the second electrode **419***a*, and the third electrode **419***b*. A first electrode **413** is provided over the gate insulating film **411** to overlap with the first region **405**.

[0208] The transistor **400** is a top-gate top-contact transistor and is different from the transistor **100**, the transistor **200**, and the transistor **300** in that the pair of fourth regions **410***a* and **410***b* is provided.

[0209] The substrate **401**, the base insulating film **402**, the first region **405**, the gate insulating film **411**, the first electrode **413**, the second electrode **419***a*, and the third electrode **419***b* can be formed in manners similar to those of the substrate **101**, the base insulating film **102**, the first region **105**, the gate insulating film **111**, the first electrode **113**, the second electrode **119***a*, and the third electrode **119***b* described in Embodiment 1.

[0210] The first region **405** serving as a channel formation region is the CAAC oxide semiconductor region described in Embodiment 1, and the pair of fourth regions **410***a* and **410***b* also is the CAAC oxide semiconductor region described in Embodiment 1. The pair of second regions **407***a* and **407***b* and the pair of third regions **409***a* and **409***b* are each an amorphous region containing a dopant, and the dopant is similar to that described in Embodiment 1. Further, the dopant concentration of the pair of second regions **407***a* and **407***b* is different from the dopant concentration of the pair of third regions **409***a* and **409***b*. The dopant concentrations of the pair of second regions **407***a* and **407***b* and the pair of third regions **409***a* and **409***b* are within the respective ranges of dopant concentrations described in Embodiment 1.

[0211] In the transistor **400**, after formation of the oxide semiconductor film **140** described in Embodiment 1, regions having different dopant concentrations (the first region **405**, the pair of second regions **407***a* and **407***b*, the pair of third regions **409***a* and **409***b*, and the pair of fourth regions **410***a* and **410***b*) can be formed by utilizing the first electrode **413**, the second electrode **419***a*, and the third electrode **419***b*.

[0212] The pair of third regions **409***a* and **409***b* is formed owing to tapered shapes of the second electrode **419***a* and the third electrode **419***b*. In addition, by reducing the thicknesses of the second electrode **419***a* and the third electrode **419***b*, the area of the pair of third regions **409***a* and **409***b* can be increased.

[0213] Note that each of the transistor **100**, the transistor **200**, and the transistor **300** is a transistor in which the regions having different dopant concentrations (the first region, the pair of second regions, and the pair of third regions) are formed by utilizing the first electrode and the sidewall insulating film.

[0214] As described above, in the transistor **400**, the pair of second regions **407***a* and **407***b* and the pair of third regions **409***a* and **409***b*, which have different dopant concentrations, are provided with the first region **405** serving as the channel formation region positioned in the middle; therefore, an electric field applied to the first region **405** serving as the channel formation region can be relieved and thus a short-channel effect can be suppressed.

[0215] Besides the transistor **400**, a transistor **500** will be described as an example of a transistor which is different from the transistors described in the above embodiments.

[0216] FIG. **9**C is a cross-sectional view of the transistor **500**, and FIG. **9**D is an enlarged view of a portion surrounded by a dotted line in FIG. **9**C.

[0217] The transistor **500** has the following structure. The base insulating film **402** is provided over the substrate **401**. The first electrode **413** and the gate insulating film **411** which covers the first electrode **413** are provided over the base insulating film **402**. The oxide semiconductor film **403** including the first region **405**, the pair of second regions **407***a* and **407***b*, the pair of third regions **409***a* and **409***b*, and the pair of fourth regions **410***a* and **410***b* is provided over the gate insulating film **411**. The second electrode **419***a* and the third electrode **419***b* are provided over the pair of fourth regions **410***a* and **410***b*. An insulating film **420** is provided over the first region **405**.

[0218] The transistor **500** is a bottom-gate top-contact transistor and is different from the transistor **100**, the transistor **200**, and the transistor **300** in that the pair of fourth regions **410***a* and **410***b* is provided.

[0219] The substrate **401**, the base insulating film **402**, the first region **405**, the gate insulating film **411**, the first electrode **413**, the second electrode **419***a*, and the third electrode **419***b* can be formed in manners similar to those of the substrate **101**, the base insulating film **102**, the first region **105**, the gate insulating film **111**, the first electrode **113**, the second electrode **119***a*, and the third electrode **119***b* described in Embodiment 1. Since the transistor **500** has a bottom-gate structure, the first electrode **413** preferably has a tapered shape as in the case of the second electrode **419***a* and the third electrode **419***b*. The first electrode **413** is formed to have a tapered shape, whereby the coverage with the gate insulating film **411** can be improved.

[0220] The first region **405** serving as a channel formation region is the CAAC oxide semiconductor region described in Embodiment 1, and the pair of fourth regions **410***a* and **410***b* also is the CAAC oxide semiconductor region described in Embodiment 1. The pair of second regions **407***a* and **407***b* and the pair of third regions **409***a* and **409***b* are each an amorphous region containing a dopant, and the dopant is similar to that described in Embodiment 1. Further, the dopant concentration of the pair of second regions **407***a* and **407***b* is different from the dopant concentration of the pair of third regions **409***a* and **409***b*. The dopant concentrations of the pair of second regions **407***a* and **407***b* and the pair of third regions **409***a* and **409***b* are within the respective ranges of dopant concentrations described in Embodiment 1.

[0221] In the transistor **500**, after the oxide semiconductor film **140** described in Embodiment 1 is formed over the gate insulating film **411**, regions having different dopant concentrations (the first region **405**, the pair of second regions **407***a* and **407***b*, the pair of third regions **409***a* and **409***b*, and the pair of fourth regions **410***a* and **410***b*) can be formed by utilizing the second electrode **419***a*, the third electrode **419***b*, and the insulating film **420**. It is necessary that the insulating film **420** be formed to have a thickness large enough to prevent the dopant from being added to the first region **405**.

[0222] Further, the pair of third regions **409***a* and **409***b* is formed owing to tapered shapes of the second electrode **419***a* and the third electrode **419***b*. In addition, by reducing the thicknesses of the second electrode **419***a* and the third electrode **419***b*, the area of the pair of third regions **409***a* and **409***b* can be increased.

[0223] Note that each of the transistor **100**, the transistor **200**, and the transistor **300** is a transistor in which the regions having different dopant concentrations (the first region, the pair of second regions, and the pair of third regions) are formed by utilizing the first electrode and the sidewall insulating film.

[0224] As described above, in the transistor **500**, the pair of second regions **407***a* and **407***b* and the pair of third regions **409***a* and **409***b*, which have different dopant concentrations, are provided with the first region **405** serving as the channel formation region positioned in the middle; therefore, an electric field applied to the first region **405** serving as the channel formation region can be relieved and thus a short-channel effect can be suppressed.

Embodiment 6

[0225] In this embodiment, resistor elements each including an oxide semiconductor to which a dopant is added will be described with reference to FIGS. **10**A and **10**B.

[0226] FIG. **10**A illustrates a resistor element **600**. The structure of the resistor element **600** will be described below. A base insulating film **602** is provided over a substrate **601**. An oxide semiconductor film **603** to which a dopant is added is provided over the base insulating film **602**. Conductive films **604***a* and **604***b* are provided over the oxide semiconductor film **603**. That is, the oxide semiconductor film **603** serves as a resistor in the resistor element **600**. The oxide semiconductor film **603** to which the dopant is added can be formed, for example, in such a manner that a portion where the gate insulating film **211** and the first electrode **213** are not formed over the oxide semiconductor film **140** described in Embodiment 2 (see FIGS. **5**A and **5**B) is prepared and then the dopant is added to the portion. The conductive films **604***a* and **604***b* can be formed using a conductive material which can be used for the first electrodes described in the above embodiments.

[0227] FIG. **10**B illustrates a resistor element **610**. The structure of the resistor element **610** will be described below. The base insulating film **602** is provided over the substrate **601**. The oxide semiconductor film **603** to which a dopant is added is provided over the base insulating film **602**. An insulating film **606** is provided over the oxide semiconductor film **603**. The conductive films **604***a* and **604***b* are provided in contact with the insulating film **606** and part of the oxide semiconductor film **603**. The oxide semiconductor film **603** serves as a resistor also in the resistor element **610**. The oxide semiconductor film **603** to which the dopant is added can be formed, for example, in such a manner that a portion where the gate insulating film **211** and the first electrode **213** are not formed over the oxide semiconductor film **140** described in Embodiment 2 (see FIGS. **5**A and **5**B) is prepared and then the dopant is added to the portion. As the insulating film **606**, any of the base insulating films, the gate insulating films, and the interlayer insulating films described in the above embodiments may be used as appropriate. The conductive films **604***a* and **604***b* can be formed using a conductive material which can be used for the first electrodes described in the above embodiments. In this manner, in the resistor element **610**, a current path in the oxide semiconductor film **603** which serves as a resistor and is in contact with the conductive films **604***a* and **604***b* can be uniform and more accurate resistance can be obtained.

Embodiment 7

[0228] An example of a circuit diagram of a memory element (hereinafter also referred to as a memory cell) included in a semiconductor device is illustrated in FIG. **11**A. The memory cell includes a transistor **1160** in which a channel formation region is formed using a material other than an oxide semiconductor and a transistor **1162** in which a channel formation region is formed using an oxide semiconductor.

[0229] The transistor **1162** in which the channel formation region is formed using an oxide semiconductor can be manufactured in accordance with any of the above embodiments.

[0230] As illustrated in FIG. **11**A, a gate electrode of the transistor **1160** is electrically connected to one of a source electrode and a drain electrode of the transistor **1162**. A first wiring (a 1st Line, also referred to as a source line) is electrically connected to a source electrode of the transistor **1160**. A second wiring (a 2nd Line, also referred to as a bit line) is electrically connected to a drain electrode of the transistor **1160**. A third wiring (a 3rd Line, also referred to as a first signal line) is electrically connected to the other of the source electrode and the drain electrode of the transistor **1162**. A fourth wiring (a 4th Line, also referred to as a second signal line) is electrically connected to a gate electrode of the transistor **1162**.

[0231] The transistor **1160** in which the channel formation region is formed using a material other than an oxide semiconductor, e.g., single crystal silicon can operate at sufficiently high speed. Therefore, with the use of the transistor **1160**, high-speed reading of stored contents and the like are possible. The transistor **1162** in which the channel formation region is formed using an oxide semiconductor is characterized by its off-state current which is smaller than the off-state current of the transistor **1160**. Therefore, when the transistor **1162** is turned off, a potential of the gate electrode of the transistor **1160** can be held for a very long time.

[0232] By utilizing a characteristic in which the potential of the gate electrode of the transistor **1160** can be held, writing, holding, and reading of data are possible as described below.

[0233] First, writing and holding of data will be described. First, a potential of the fourth wiring is set to a potential at which the transistor **1162** is turned on, so that the transistor **1162** is turned on. Thus, a potential of the third wiring is supplied to the gate electrode of the transistor **1160** (writing). After that, the potential of the fourth wiring is set to a potential at which the transistor **1162** is turned off, so that the transistor **1162** is turned off, and thus, the potential of the gate electrode of the transistor **1160** is held (holding).

[0234] Since the off-state current of the transistor **1162** is smaller than the off-state current of the transistor **1160**, the potential of the gate electrode of the transistor **1160** is held for a long time. For example, when the potential of the gate electrode of the transistor **1160** is a potential at which the transistor **1160** is in an on state, the on state of the transistor **1160** is held for a long time. In addition, when the potential of the gate electrode of the transistor **1160** is a potential at which the transistor **1160** is an off state, the off state of the transistor **1160** is held for a long time.

[0235] Then, reading of data will be described. When a predetermined potential (a low potential) is supplied to the first wiring in a state where the on state or the off state of the transistor **1160** is held as described above, a potential of the second wiring varies depending on the on state or the off state of the transistor **1160**. For example, when the transistor **1160** is in the on state, the potential of the second wiring becomes lower than the potential of the first wiring. On the other hand, when the transistor **1160** is in the off state, the potential of the second wiring is not changed.

[0236] In such a manner, the potential of the second wiring and the predetermined potential are compared with each other in a state where data is held, whereby the data can be read out.

[0237] Then, rewriting of data will be described. Rewriting of data is performed in a manner similar to that of the writing and holding of data. That is, a potential of the fourth wiring is set to a potential at which the transistor **1162** is turned on, so that the transistor **1162** is turned on. Thus, a potential of the third wiring (a potential for new data) is supplied to the gate electrode of the transistor **1160**. After that, the potential of the fourth wiring is set to a potential at which the transistor **1162** is turned off, so that the transistor **1162** is turned off, and thus, the new data is held.

[0238] In the memory cell according to the disclosed invention, data can be directly rewritten by another writing of data as described above. For that reason, erasing operation which is necessary for a flash memory or the like is not needed, so that decrease in operation speed because of erasing operation can be suppressed. In other words, high-speed operation of the semiconductor device including the memory cell can be realized.

[0239] FIG. **11**B is a circuit diagram illustrating an application example of the memory cell illustrated in FIG. **11**A.

[0240] A memory cell **1100** illustrated in FIG. **11**B includes a first wiring SL (a source line), a second wiring BL (a bit line), a third wiring S**1** (a first signal line), a fourth wiring S**2** (a second signal line), a fifth wiring WL (a word line), a transistor **1164** (a first transistor), a transistor **1161** (a second transistor), and a transistor **1163** (a third transistor). In each of the transistors **1164** and **1163**, a channel formation region is formed using a material other than an oxide semiconductor, and in the transistor **1161**, a channel formation region is formed using an oxide semiconductor.

[0241] Here, a gate electrode of the transistor **1164** is electrically connected to one of a source electrode and a drain electrode of the transistor **1161**. In addition, the first wiring SL is electrically connected to a source electrode of the transistor **1164**, and a drain electrode of the transistor **1164** is electrically connected to a source electrode of the transistor **1163**. The second wiring BL is electrically connected to a drain electrode of the transistor **1163**, and the third wiring S**1** is electrically connected to the other of the source electrode and the drain electrode of the transistor **1161**. The fourth wiring S**2** is electrically connected to a gate electrode of the transistor **1161**, and the fifth wiring WL is electrically connected to a gate electrode of the transistor **1163**.

[0242] Next, operation of the circuit will be specifically described.

[0243] When data is written into the memory cell **1100**, the first wiring SL is set to 0 V, the fifth wiring WL is set to 0 V, the second wiring BL is set to 0 V, and the fourth wiring S**2** is set to 2 V. The third wiring S**1** is set to 2 V in order to write data “1” and set to 0 V in order to write data “0”. At this time, the transistor **1163** is in an off state and the transistor **1161** is in an on state. Note that, to finish writing, before the potential of the third wiring S**1** is changed, the fourth wiring S**2** is set to 0 V so that the transistor **1161** is turned off.

[0244] As a result, a potential of a node (referred to as a node A) connected to the gate electrode of the transistor **1164** is set to approximately 2 V after the writing of data “1” and set to approximately 0 V after the writing of data “0”. Electric charge corresponding to a potential of the third wiring S**1** is accumulated at the node A; since the off-state current of the transistor **1161** is smaller than that of a transistor in which a channel formation region is formed using single crystal silicon, the potential of the gate electrode of the transistor **1164** is held for a long time.

[0245] When data is read from the memory cell, the first wiring SL is set to 0 V, the fifth wiring WL is set to 2 V, the fourth wiring S**2** is set to 0 V, the third wiring S**1** is set to 0 V, and a reading circuit connected to the second wiring BL is set in an operation state. At this time, the transistor **1163** is in an on state and the transistor **1161** is in an off state.

[0246] The transistor **1164** is in an off state when data “0” has been written, that is, the node A is set to approximately 0 V, so that the resistance between the second wiring BL and the first wiring SL is high. On the other hand, the transistor **1164** is in an on state when data “1” has been written, that is, the node A is set to approximately 2 V, so that the resistance between the second wiring BL and the first wiring SL is low. The reading circuit can read data “0” or data “1” in accordance with the difference in resistance state of the memory cell. The second wiring BL at the time of the writing is set to 0 V; however, it may be in a floating state or may be charged to have a potential higher than 0 V. The third wiring S**1** at the time of the reading is set to 0 V; however, it may be in a floating state or may be charged to have a potential higher than 0 V.

[0247] Note that data “1” and data “0” are defined for convenience and can be reversed. In addition, the above operation voltages are examples. The operation voltages are set so that the transistor **1164** is turned off in the case of data “0” and turned on in the case of data “1”, the transistor **1161** is turned on at the time of writing and turned off in periods except the time of writing, and the transistor **1163** is turned on at the time of reading. A power supply potential VDD of a peripheral logic circuit may also be used instead of 2 V.

[0248] In this embodiment, the memory cell with a minimum storage unit (one bit) is described for easy understanding; however, the structure of the memory cell is not limited thereto. It is also possible to make a more developed semiconductor device with a plurality of memory cells connected to each other as appropriate. For example, it is possible to make a NAND-type or NOR-type semiconductor device by using more than one of the above memory cells.

The wiring structure is not limited to that in FIG. **11**A or **11**B and can be changed as appropriate.

[0249] FIG. **12** is a block circuit diagram of a semiconductor device according to one embodiment of the present invention. The semiconductor device has m×n bits of memory capacity.

[0250] The semiconductor device illustrated in FIG. **12** includes m fourth wirings S**2**(**1**) to S**2**(*m*), m fifth wirings WL(**1**) to WL(m), n second wirings BL(**1**) to BL(n), n third wirings S**1**(**1**) to S**1**(*n*), a memory cell array **1110** in which a plurality of memory cells **1100**(**1**,**1**) to **1100**(*m,n*) is arranged in a matrix of m rows by n columns (m and n are each a natural number), and peripheral circuits such as a driver circuit **1111** for the second wirings and the third wirings, a driver circuit **1113** for the fourth wirings and the fifth wirings, and a reading circuit **1112**. A refresh circuit or the like may be provided as another peripheral circuit.

[0251] A memory cell **1100**(*i,j*) is considered as a typical example of the memory cell. Here, the memory cell **1100**(*i,j*) (i is an integer greater than or equal to 1 and less than or equal to m and j is an integer greater than or equal to 1 and less than or equal to n) is connected to a second wiring BL(j), a third wiring S**1**(*j*), a fourth wiring S**2**(*i*), a fifth wiring WL(i), and a first wiring. A first wiring potential Vs is supplied to the first wiring. The second wirings BL(**1**) to BL(n) and the third wirings S**1**(**1**) to S**1**(*n*) are connected to the driver circuit **1111** for the second wirings and the third wirings and the reading circuit **1112**. The fifth wirings WL(**1**) to WL(m) and the fourth wirings S**2**(**1**) to S**2**(*m*) are connected to the driver circuit **1113** for the fourth wirings and the fifth wirings.

[0252] The operation of the semiconductor device illustrated in FIG. **12** will be described. In this structure, data is written and read per row.

[0253] When data is written into memory cells **1100**(*i*, **1**) to **1100**(*i,n*) of an i-th row, the first wiring potential Vs is set to 0 V, the fifth wiring WL(i) is set to 0 V, the second wirings BL(**1**) to BL(n) are set to 0 V, and the fourth wiring S**2**(*i*) is set to 2 V. At this time, the transistors **1161** are turned on. Among the third wirings S**1**(**1**) to S**1**(*n*), the third wiring in a column in which data "1" is to be written is set to 2 V and the third wiring in a column in which data "0" is to be written is set to 0 V. Note that, to finish writing, the fourth wiring S**2**(*i*) is set to 0 V before the potentials of the third wirings S**1**(**1**) to S**1**(*n*) are changed, so that the transistors **1161** are turned off. Moreover, a non-selected fifth wiring WL and a non-selected fourth wiring S**2** are set to 0 V.

[0254] As a result, the potential of the node (referred to as the node A) connected to the gate electrode of the transistor **1164** in the memory cell into which data "1" has been written is set to approximately 2 V, and the potential of the node A in the memory cell into which data "0" has been written is set to approximately 0 V (see FIG. **11**B and FIG. **12**). The potential of the node A of the non-selected memory cell is not changed.

[0255] When data is read from the memory cells **1100**(*i*,**1**) to **1100**(*i,n*) of the i-th row, the first wiring potential Vs is set to 0 V, the fifth wiring WL(i) is set to 2 V, the fourth wiring S**2**(*i*) is set to 0 V, the third wirings S**1**(**1**) to S**1**(*n*) are set to 0 V, and the reading circuit connected to the second wirings BL(**1**) to BL(n) is set in an operation state. The reading circuit can read data "0" or data "1" in accordance with the difference in resistance state of the memory cell, for example. Note that the non-selected fifth wiring WL and the non-selected fourth wiring S**2** are set to 0 V. The second wiring BL at the time of the writing is set to 0 V; however, it may be in a floating state or may be charged to have a potential higher than 0 V. The third wiring S**1** at the time of the reading is set to 0 V; however, it may be in a floating state or may be charged to have a potential higher than 0 V.

[0256] Note that data "1" and data "0" are defined for convenience and can be reversed. In addition, the above operation voltages are examples. The operation voltages are set so that the transistor **1164** is turned off in the case of data "0" and turned on in the case of data "1", the transistor **1161** is turned on at the time of writing and turned off in periods except the time of writing, and the transistor **1163** is turned on at the time of reading. A power supply potential VDD of a peripheral logic circuit may also be used instead of 2 V.

Embodiment 8

[0257] In this embodiment, an example of a circuit diagram of a memory cell including a capacitor will be shown. A memory cell **1170** illustrated in FIG. **13**A includes a first wiring SL, a second wiring BL, a third wiring S**1**, a fourth wiring S**2**, a fifth wiring WL, a transistor **1171** (a first transistor), a transistor **1172** (a second transistor), and a capacitor **1173**. In the transistor **1171**, a channel formation region is formed using a material other than an oxide semiconductor, and in the transistor **1172**, a channel formation region is formed using an oxide semiconductor.

[0258] Here, a gate electrode of the transistor **1171**, one of a source electrode and a drain electrode of the transistor **1172**, and one electrode of the capacitor **1173** are electrically connected to each other. In addition, the first wiring SL and a source electrode of the transistor **1171** are electrically connected to each other. The second wiring BL and a drain electrode of the transistor **1171** are electrically connected to each other. The third wiring S**1** and the other of the source electrode and the drain electrode of the transistor **1172** are electrically connected to each other. The fourth wiring S**2** and a gate electrode of the transistor **1172** are electrically connected to each other. The fifth wiring WL and the other electrode of the capacitor **1173** are electrically connected to each other.

[0259] Next, operation of the circuit will be specifically described.

[0260] When data is written into the memory cell **1170**, the first wiring SL is set to 0 V, the fifth wiring WL is set to 0 V, the second wiring BL is set to 0 V, and the fourth wiring S**2** is set to 2 V. The third wiring S**1** is set to 2 V in order to write data "1" and set to 0 V in order to write data "0". At this time, the transistor **1172** is turned on. Note that, to finish writing, the fourth wiring S**2** is set to 0 V before the potential of the third wiring S**1** is changed, so that the transistor **1172** is turned off.

[0261] As a result, the potential of a node (referred to as a node A) connected to the gate electrode of the transistor **1171** is set to approximately 2 V after the writing of data "1" and set to approximately 0 V after the writing of data "0".

[0262] When data is read from the memory cell **1170**, the first wiring SL is set to 0 V, the fifth wiring WL is set to 2 V, the fourth wiring S**2** is set to 0 V, the third wiring S**1** is set to 0 V, and a reading circuit connected to the second wiring BL is set in an operation state. At this time, the transistor **1172** is turned off.

[0263] The state of the transistor **1171** in the case where the fifth wiring WL is set to 2 V will be described. The potential of the node A which determines the state of the transistor **1171** depends on capacitance C**1** between the fifth wiring WL and the node A, and capacitance C**2** between the gate electrode of the transistor **1171** and the source and drain electrodes of the transistor **1171**.

[0264] Note that the third wiring S**1** at the time of the reading is set to 0 V; however, it may be in a floating state or may be charged to have a potential higher than 0 V. Data "1" and data "0" are defined for convenience and can be reversed.

[0265] The potential of the third wiring S**1** at the time of writing may be selected from the potentials of data "0" and data "1" so that the transistor **1172** is turned off after the writing and the transistor **1171** is in an off state in the case where the potential of the fifth wiring WL is set to 0 V. The potential of the fifth wiring WL at the time of reading is set so that the transistor **1171** is turned off in the case of data "0" and turned on in the case of data "1". Furthermore, the threshold voltage of the transistor **1171** is an example. The transistor **1171** can have any threshold voltage so that the transistor **1171** operates in the above-described manner.

[0266] An example of a NOR-type semiconductor memory device in which a memory cell including a capacitor and a selection transistor having a first gate electrode and a second gate electrode is used will be described with reference to FIG. **13**B.

[0267] A semiconductor device illustrated in FIG. **13**B according to one embodiment of the present invention includes a memory cell array including a plurality of memory cells arranged in a matrix of I rows (I is a natural number of 2 or more) by J columns (J is a natural number).

[0268] The memory cell array illustrated in FIG. **13**B includes a plurality of memory cells **1180** arranged in a matrix of i rows (i is a natural number of 3 or more) by j columns (j is a natural number of 3 or more), i word lines WL (word lines WL_**1** to WL_i), i capacitor lines CL (capacitor lines CL_**1** to CL_i), i gate lines BGL (gate lines BGL_**1** to BGL_i), j bit lines BL (bit lines BL_**1** to BL_j), and a source line SL.

[0269] Further, each of the plurality of memory cells **1180** (also referred to as a memory cell **1180**(M,N) (note that N is a natural number greater than or equal to 1 and less than or equal to j and that M is a natural number greater than or equal to 1 and less than or equal to i)) includes a transistor **1181**(M,N), a capacitor **1183**(M,N), and a transistor **1182** (M,N).

[0270] Note that in the semiconductor memory device, the capacitor includes a first capacitor electrode, a second capacitor electrode, and a dielectric layer overlapping with the first capacitor electrode and the second capacitor electrode. Electric charge is accumulated in the capacitor in accordance with voltage applied between the first capacitor electrode and the second capacitor electrode.

[0271] The transistor **1181**(M,N) is an n-channel transistor which has a source electrode, a drain electrode, a first gate electrode, and a second gate electrode. Note that in the semiconductor memory device in this embodiment, the transistor **1181** does not necessarily need to be an n-channel transistor.

[0272] One of the source electrode and the drain electrode of the transistor **1181**(M,N) is connected to a bit line BL_N. The first gate electrode of the transistor **1181**(M,N) is connected to a word line WL_M. The second gate electrode of the transistor **1181**(M,N) is connected to a gate line BGL_M. With the structure in which the one of the source electrode and the drain electrode of the transistor **1181**(M,N) is connected to the bit line BL_N, data can be selectively read from memory cells.

[0273] The transistor **1181**(M,N) serves as a selection transistor in the memory cell **1180**(M,N).

[0274] As the transistor **1181**(M,N), a transistor in which a channel formation region is formed using an oxide semiconductor can be used.

[0275] The transistor **1182**(M,N) is a p-channel transistor. Note that in the semiconductor memory device in this embodiment, the transistor **1182** does not necessarily need to be a p-channel transistor.

[0276] One of a source electrode and a drain electrode of the transistor **1182**(M,N) is connected to the source line SL. The other of the source electrode and the drain electrode of the transistor **1182**(M,N) is connected to the bit line BL_N. A gate electrode of the transistor **1182**(M,N) is connected to the other of the source electrode and the drain electrode of the transistor **1181**(M,N).

[0277] The transistor **1182**(M,N) serves as an output transistor in the memory cell **1180**(M,N). As the transistor **1182**(M,N), for example, a transistor in which a channel formation region is formed using single crystal silicon can be used.

[0278] A first capacitor electrode of the capacitor **1183**(M,N) is connected to a capacitor line CL_M. A second capacitor electrode of the capacitor **1183**(M,N) is connected to the other of the source electrode and the drain electrode of the transistor **1181**(M,N). Note that the capacitor **1183**(M,N) serves as a storage capacitor.

[0279] The voltages of the word lines WL_**1** to WL_i are controlled by, for example, a driver circuit including a decoder.

[0280] The voltages of the bit lines BL_**1** to BL_j are controlled by, for example, a driver circuit including a decoder.

[0281] The voltages of the capacitor lines CL_**1** to CL_i are controlled by, for example, a driver circuit including a decoder.

[0282] The voltages of the gate lines BGL_**1** to BGL_i are controlled by, for example, a gate line driver circuit.

[0283] The gate line driver circuit is formed using a circuit which includes a diode and a capacitor whose first capacitor electrode is electrically connected to an anode of the diode and the gate line BGL, for example.

[0284] By adjustment of the voltage of the second gate electrode of the transistor **1181**, the threshold voltage of the transistor **1181** can be adjusted. Accordingly, by adjustment of the threshold voltage of the transistor **1181** functioning as a selection transistor, current flowing between the source electrode and the drain electrode of the transistor **1181** in an off state can be made extremely small. Thus, a data retention period in the memory circuit can be made longer. In addition, voltage necessary for writing and reading data can be made lower than that of a conventional semiconductor device; thus, power consumption can be reduced.

Embodiment 9

[0285] In this embodiment, examples of a semiconductor device using the transistor described in any of the above embodiments will be described with reference to FIGS. **14**A and **14**B.

[0286] FIG. **14**A illustrates an example of a semiconductor device whose structure corresponds to that of a so-called dynamic random access memory (DRAM). A memory cell array **1120** illustrated in FIG. **14**A has a structure in which a plurality of memory cells **1130** is arranged in a matrix. Further, the memory cell array **1120** includes m first wirings and n second wirings. Note that in this embodiment, the first wiring and the second wiring are referred to as a bit line BL and a word line WL, respectively.

[0287] The memory cell **1130** includes a transistor **1131** and a capacitor **1132**. A gate electrode of the transistor **1131** is connected to the first wiring (the word line WL). Further, one of a source electrode and a drain electrode of the transistor **1131** is connected to the second wiring (the bit line BL). The other of the source electrode and the drain electrode of the transistor **1131** is connected to one electrode of the capacitor. The other electrode of the capacitor is connected to a capacitor line CL and is supplied with a predetermined potential. The transistor described in any of the above embodiments is applied to the transistor **1131**.

[0288] The transistor in which a channel formation region is formed using an oxide semiconductor, which is described in any of the above embodiments, is characterized by having smaller off-state current than a transistor in which a channel formation region is formed using single crystal silicon. Accordingly, when the transistor is applied to the semiconductor device illustrated in FIG. **14**A, which is regarded as a so-called DRAM, a substantially nonvolatile memory can be obtained.

[0289] FIG. **14**B illustrates an example of a semiconductor device whose structure corresponds to that of a so-called static random access memory (SRAM). A memory cell array **1140** illustrated in FIG. **14**B can have a structure in which a plurality of memory cells **1150** is arranged in a matrix. Further, the memory cell array **1140** includes a plurality of first wirings (word lines WL), a plurality of second wirings (bit lines BL), and a plurality of third wirings (inverted bit lines/BL).

[0290] The memory cell **1150** includes a first transistor **1151**, a second transistor **1152**, a third transistor **1153**, a fourth transistor **1154**, a fifth transistor **1155**, and a sixth transistor **1156**. The first transistor **1151** and the second transistor **1152** function as selection transistors. One of the third transistor **1153** and the fourth transistor **1154** is an n-channel transistor (here, the fourth transistor **1154** is an n-channel transistor), and the other of the third transistor **1153** and the fourth transistor **1154** is a p-channel transistor (here, the third transistor **1153** is a p-channel transistor). In other words, the third transistor **1153** and the fourth transistor **1154** form a CMOS circuit. Similarly, the fifth transistor **1155** and the sixth transistor **1156** form a CMOS circuit.

[0291] The first transistor **1151**, the second transistor **1152**, the fourth transistor **1154**, and the sixth transistor **1156** are n-channel transistors and the transistor described in any of the above embodiments can be applied to these transistors. Each of the third transistor **1153** and the fifth transistor **1155** is a p-channel transistor in which a channel formation region is formed using a material (e.g., single crystal silicon) other than an oxide semiconductor.

[0292] The methods, structures, and the like described in this embodiment can be combined with any of the methods, structures, and the like described in the other embodiments, as appropriate.

Embodiment 10

[0293] A central processing unit (CPU) can be formed using a transistor in which a channel formation region is formed using an oxide semiconductor for at least part of the CPU.

[0294] FIG. **15**A is a block diagram illustrating a specific structure of a CPU. The CPU illustrated in FIG. **15**A includes an arithmetic logic unit (ALU) **1191**, an ALU controller **1192**, an instruction decoder **1193**, an interrupt controller **1194**, a timing controller **1195**, a register **1196**, a register controller **1197**, a bus interface (Bus I/F) **1198**, a rewritable ROM **1199**, and an ROM interface (ROM I/F) **1189** over a substrate **1190**. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate **1190**. The ROM **1199** and the ROM I/F **1189** may be provided over a separate chip. Obviously, the CPU illustrated in FIG. **15**A is only an example in which the structure is simplified, and an actual CPU may have various structures depending on the application.

[0295] An instruction that is input to the CPU through the Bus I/F **1198** is input to the instruction decoder **1193** and decoded therein, and then, input to the ALU controller **1192**, the interrupt controller **1194**, the register controller **1197**, and the timing controller **1195**.

[0296] The ALU controller **1192**, the interrupt controller **1194**, the register controller **1197**, and the timing controller **1195** conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller **1192** generates signals for controlling the operation of the ALU **1191**. While the CPU is executing a program, the interrupt controller **1194** judges an interrupt request from an external input/output device or a peripheral circuit on the basis of its priority or a mask state, and processes the request. The register controller **1197** generates an address of the register **1196**, and reads/writes data from/into the register **1196** in accordance with the state of the CPU.

[0297] The timing controller **1195** generates signals for controlling operation timings of the ALU **1191**, the ALU controller **1192**, the instruction decoder **1193**, the interrupt controller **1194**, and the register controller **1197**. For example, the timing controller **1195** includes an internal clock generator for generating an internal clock signal CLK**2** based on a reference clock signal CLK**1**, and supplies the clock signal CLK**2** to the above circuits.

[0298] In the CPU illustrated in FIG. **15**A, a memory element is provided in the register **1196**. The memory element described in Embodiment 8 can be used as the memory element provided in the register **1196**.

[0299] In the CPU illustrated in FIG. **15**A, the register controller **1197** selects operation of holding data in the register **1196** in accordance with an instruction from the ALU **1191**. That is, the register controller **1197** selects whether data is held by a phase-inversion element or a capacitor in the memory element included in the register **1196**. When data holding by the phase-inversion element is selected, power supply voltage is supplied to the memory element in the register **1196**. When data holding by the capacitor is selected, the data is rewritten in the capacitor, and supply of power supply voltage to the memory element in the register **1196** can be stopped.

[0300] The power supply can be stopped by providing a switching element between a memory element group and a node to which a power supply potential VDD or a power supply potential VSS is supplied, as illustrated in FIG. **15**B or FIG. **15**C. Circuits illustrated in FIGS. **15**B and **15**C will be described below.

[0301] FIGS. **15**B and **15**C each illustrate an example of a structure of a memory circuit including a transistor in which a channel formation region is formed using an oxide semiconductor as a switching element for controlling supply of a power supply potential to a memory element.

[0302] The memory device illustrated in FIG. **15**B includes a switching element **1141** and a memory element group **1143** including a plurality of memory elements **1142**. Specifically, as each of the memory elements **1142**, the memory element described in Embodiment 8 can be used. Each of the memory elements **1142** included in the memory element group **1143** is supplied with the high-level power supply potential VDD via the switching element **1141**. Further, each of the memory elements **1142** included in the memory element group **1143** is supplied with a potential of a signal IN and the low-level power supply potential VSS.

[0303] In FIG. **15**B, a transistor in which a channel formation region is formed using an oxide semiconductor is used as the switching element **1141**, and the switching of the transistor is controlled by a signal Sig A supplied to a gate electrode thereof.

[0304] Note that FIG. **15**B illustrates the structure in which the switching element **1141** includes only one transistor; however, without limitation thereto, the switching element **1141** may include a plurality of transistors. In the case where the switching element **1141** includes a plurality of transistors which serves as switching elements, the plurality of transistors may be connected to each other in parallel, in series, or in combination of parallel connection and series connection.

[0305] Although the switching element **1141** controls the supply of the high-level power supply potential VDD to each of the memory elements **1142** included in the memory element group **1143** in FIG. **15**B, the switching element **1141** may control the supply of the low-level power supply potential VSS.

[0306] In FIG. **15**C, an example of a memory device in which each of the memory elements **1142** included in the memory element group **1143** is supplied with the low-level power supply potential VSS via the switching element **1141** is illustrated. The supply of the low-level power supply potential VSS to each of the memory elements **1142** included in the memory element group **1143** can be controlled by the switching element **1141**.

[0307] When a switching element is provided between a memory element group and a node to which the power supply potential VDD or the power supply potential VSS is supplied, data can be held even in the case where operation of a CPU is temporarily stopped and the supply of the power supply voltage is stopped; accordingly, power consumption can be reduced. Specifically, for example, while a user of a personal computer does not input data to an input device such as a keyboard, the operation of the CPU can be stopped, so that the power consumption can be reduced.

[0308] Although the CPU is given as an example, the transistor can also be applied to an LSI such as a digital signal processor (DSP), a custom LSI, or a field programmable gate array (FPGA).

[0309] This embodiment can be combined with any of the above embodiments as appropriate.

EXPLANATION OF REFERENCE

[0310] **100**: transistor, **101**: substrate, **102**: base insulating film, **103**: oxide semiconductor film, **105**: first region, **107***a*: second region, **107***b*: second region, **109***a*: third region, **109***b*: third region, **111**: gate insulating film, **113**: first electrode, **115**: sidewall insulating film, **115***a*: sidewall insulating film, **115***b*: sidewall insulating film, **117**: interlayer insulating film, **119***a*: second electrode, **119***b*: third electrode, **116***a*: opening, **116***b*: opening, **130**: oxide semiconductor film, **132**: island-shaped oxide semiconductor film, **140**: oxide semiconductor film, **114**: insulating film, **150**: dopant, **200**: transistor, **201**: substrate, **202**: base insulating film, **203**: oxide semiconductor film, **205**: first region, **207***a*: second region, **207***b*: second region, **209***a*: third region, **209***b*: third region, **211**: gate insulating film, **212**: conductive film, **213**: first electrode, **215**: sidewall insulating film, **215***a*: sidewall insulating film, **215***b*: sidewall insulating film, **217**: interlayer insulating film, **219***a*: second electrode, **219***b*: third electrode, **216***a*: opening, **216***b*: opening, **210**: insulating film, **214**: insulating film, **300**: transistor, **301**: substrate, **302**: base insulating film, **303**: oxide semiconductor film, **305**: first region, **307***a*: second region, **307***b*: second region, **309***a*: third region, **309***b*: third region, **311**: gate insulating film, **313**: first electrode, **314**: insulating film, **315**: sidewall insulating film, **315***a*: sidewall insulating film, **315***b*: sidewall insulating film, **317**: interlayer insulating film, **319***a*: second electrode, **319***b*: third electrode, **340**: oxide semiconductor film, **400**: transistor, **401**: substrate, **402**: base insulating film, **403**: oxide semiconductor film, **405**: first region, **407***a*: second region, **407***b*: second region, **409***a*: third region, **409***b*: third region, **410***a*: fourth region, **410***b*: fourth region, **411**: gate insulating film, **413**: first electrode, **415***a*: sidewall insulating film, **415***b*: sidewall insulating film, **419***a*: second electrode, **419***b*: third electrode, **420**: insulating film, **500**: transistor, **600**: resistor element, **601**: substrate, **602**: base insulating film, **603**: oxide semiconductor film, **604***a*: conductive film, **604***b*: conductive film, **606**: insulating film, **610**: resistor element, **1100**: memory cell, **1110**: memory cell array, **1111**: driver circuit, **1112**: reading circuit, **1113**: driver circuit, **1120**: memory cell array, **1130**: memory cell, **1131**: transistor, **1132**: capacitor, **1140**: memory cell array, **1141**: switching element, **1142**: memory element, **1143**: memory element group, **1150**: memory cell, **1151**: transistor, **1152**: transistor, **1153**: transistor, **1154**: transistor, **1155**: transistor, **1156**: transistor, **1160**: transistor, **1161**: transistor, **1162**: transistor, **1163**: transistor, **1164**: transistor, **1170**: memory cell, **1171**: transistor, **1172**: transistor, **1173**: capacitor, **1180**: memory cell, **1181**: transistor, **1182**: transistor, **1183**: capacitor, **1189**: ROM interface, **1190**: substrate, **1191**: ALU, **1192**: ALU controller, **1193**: instruction decoder, **1194**: interrupt controller, **1195**: timing controller, **1196**: register, **1197**: register controller, **1198**: bus interface, and **1199**: ROM.

[0311] This application is based on Japanese Patent Application serial no. 2010-293051 filed with the Japan Patent Office on Dec. 28, 2010, the entire contents of which are hereby incorporated by reference.

1. (canceled)

2. A semiconductor device comprising:

an insulating film;

an oxide semiconductor film on the insulating film, the oxide semiconductor film comprising:

a first region;

a pair of second regions, the first region located between the pair of second regions; and

a pair of third regions, the first region and the pair of second regions located between the pair of third regions;

a gate insulating film over the oxide semiconductor film; and

a first electrode over the gate insulating film and overlapping with the first region,

wherein each of a crystallinity of the pair of second regions and a crystallinity of the pair of third regions is lower than a crystallinity of the first region.

3. The semiconductor device according to claim **2**, further comprising:

a first sidewall insulating film and a second sidewall insulating film located on side surfaces of the first electrode,

wherein the first sidewall insulating film overlaps with one of the pair of second regions, and the second sidewall insulating film overlaps with the other of the pair of second regions.

4. The semiconductor device according to claim **2**,

wherein the first region is a c-axis aligned crystal oxide semiconductor region.

5. The semiconductor device according to claim **2**, further comprising:

a second electrode electrically connected to one of the pair of third regions; and

a third electrode electrically connected to the other of the pair of third regions.

6. The semiconductor device according to claim **5**,

wherein the second electrode is in contact with a top surface of the one of the pair of third regions, and

wherein the third electrode is in contact with a top surface of the other of the pair of third regions.

7. The semiconductor device according to claim **5**,

wherein the second electrode is in contact with a bottom surface of the one of the pair of third regions, and

wherein the third electrode is in contact with a bottom surface of the other of the pair of third regions.

8. The semiconductor device according to claim **2**,

wherein the gate insulating film overlaps with the first region, the pair of second regions, and the pair of third regions.

9. The semiconductor device according to claim **2**,

wherein the gate insulating film is an oxide insulating film.

10. The semiconductor device according to claim **2**,

wherein the pair of second regions and the pair of third regions comprise one or more elements selected from nitrogen, phosphorus, and arsenic as the dopant, and

wherein the dopant concentration of the pair of second regions and the dopant concentration of the pair of third regions are higher than or equal to 5×10^{18} atoms/cm^3 and lower than or equal to 1×10^{22} atoms/cm^3.

11. The semiconductor device according to claim **2**,

wherein the pair of second regions and the pair of third regions comprise one or more elements selected from nitrogen, phosphorus, and arsenic as the dopant,

wherein the dopant concentration of the pair of second regions is higher than or equal to 5×10^{18} atoms/cm^3 and lower than 5×10^{19} atoms/cm^3, and

wherein the dopant concentration of the pair of third regions is higher than or equal to 5×10^{19} atoms/cm^3 and lower than or equal to 1×10^{22} atoms/cm^3.

12. The semiconductor device according to claim **2**,

wherein the oxide semiconductor film comprises two or more elements selected from In, Ga, Sn, and Zn.

13. A semiconductor device comprising:

a base insulating film;

an oxide semiconductor film on an insulating surface of the base insulating film, the oxide semiconductor film including a channel formation region and a pair of impurity regions with the channel formation region therebetween, wherein the oxide semiconductor film comprises indium and zinc;

a gate insulating film over the oxide semiconductor film;

a gate electrode over the channel formation region of the oxide semiconductor film with the gate insulating film interposed therebetween; and

first insulating films on side surfaces of the gate electrode, the first insulating films comprising silicon nitride,

wherein each of the pair of impurity regions comprises a first region and a second region, the first region being located between the channel formation region and the second region,

wherein the first regions of the pair of impurity regions are overlapped with the first insulating films while the second regions of the pair of impurity regions are not overlapped with the first insulating films, and

wherein the pair of impurity regions of the oxide semiconductor film contains nitrogen at a higher concentration than the channel formation region.

14. The semiconductor device according to claim **13**,

wherein the channel formation region is a c-axis aligned crystal oxide semiconductor region.

15. The semiconductor device according to claim **13**,

wherein the second region contains nitrogen at a higher concentration than the first region.

16. The semiconductor device according to claim **13**, further comprising a second insulating film over the gate electrode,

wherein the second insulating film is in contact with the first insulating films and the second regions of the pair of impurity regions, and

wherein the second insulating film comprises a material selected from the group consisting of silicon oxide, silicon oxynitride, silicon nitride oxide, and silicon nitride.

17. The semiconductor device according to claim **13**, further comprising a transistor having a channel formation region comprising single crystalline silicon, wherein the transistor is operationally connected to the oxide semiconductor film.

18. The semiconductor device according to claim **13**,

wherein the oxide semiconductor film comprises In, Ga, and Zn.

19. The semiconductor device according to claim **13**,

wherein a crystallinity of the pair of impurity regions is lower than a crystallinity of the channel formation region.

wherein a crystallinity of the pair of impurity regions is lower than a crystallinity of the channel formation region.

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