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MEARS et al.

(54) **METHOD FOR MAKING SEMICONDUCTOR DEVICE INCLUDING A SUPERLATTICE PROVIDING METAL WORK FUNCTION TUNING**

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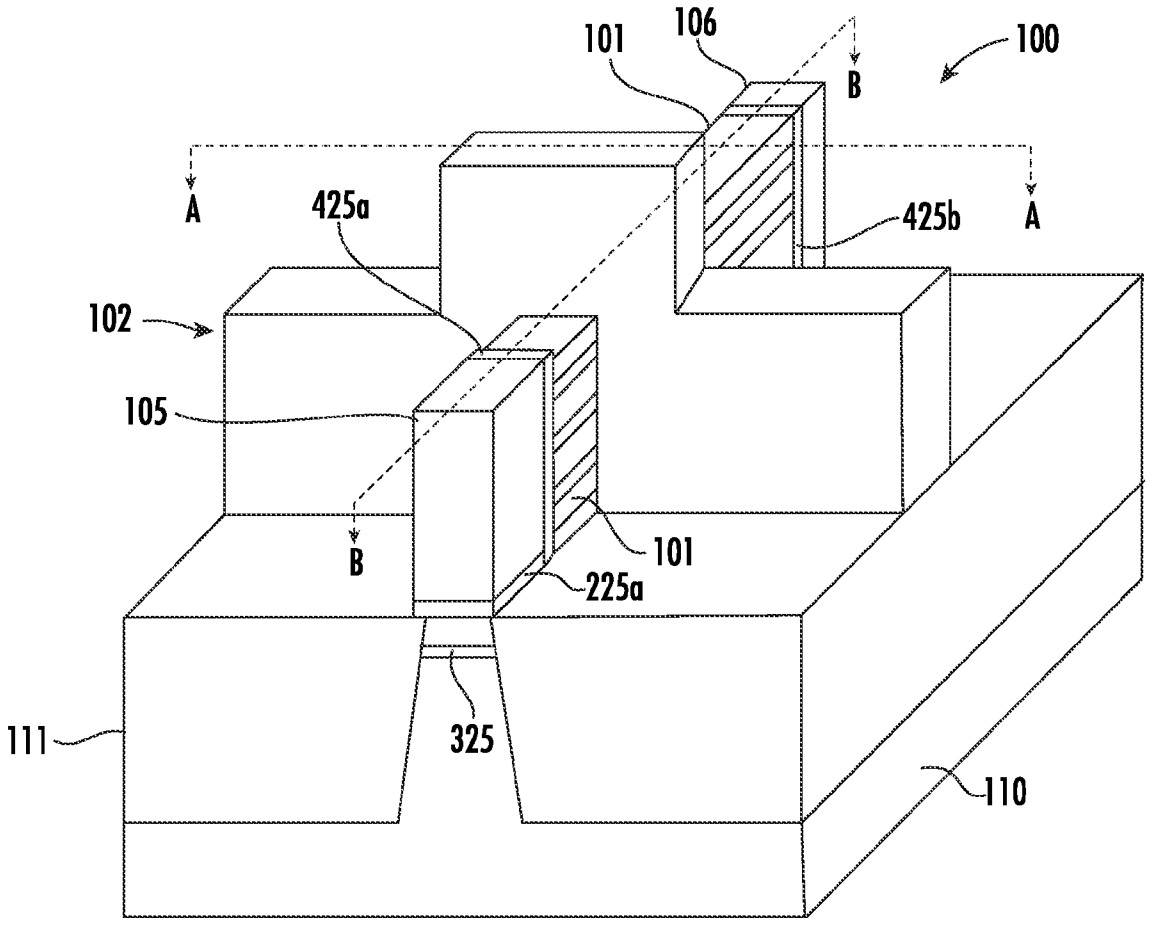
(57) **ABSTRACT**

A method for making a semiconductor gate-all-around (GAA) device may include forming source and drain regions on a semiconductor substrate, forming a plurality of semiconductor nanostructures extending between the source and drain regions, forming a gate surrounding the plurality of semiconductor nanostructures in a gate-all-around arrangement, and forming a dopant diffusion liner adjacent at least one of the source and drain regions and comprising a first superlattice. The first superlattice may include a plurality of stacked groups of layers, with each group of layers including a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.



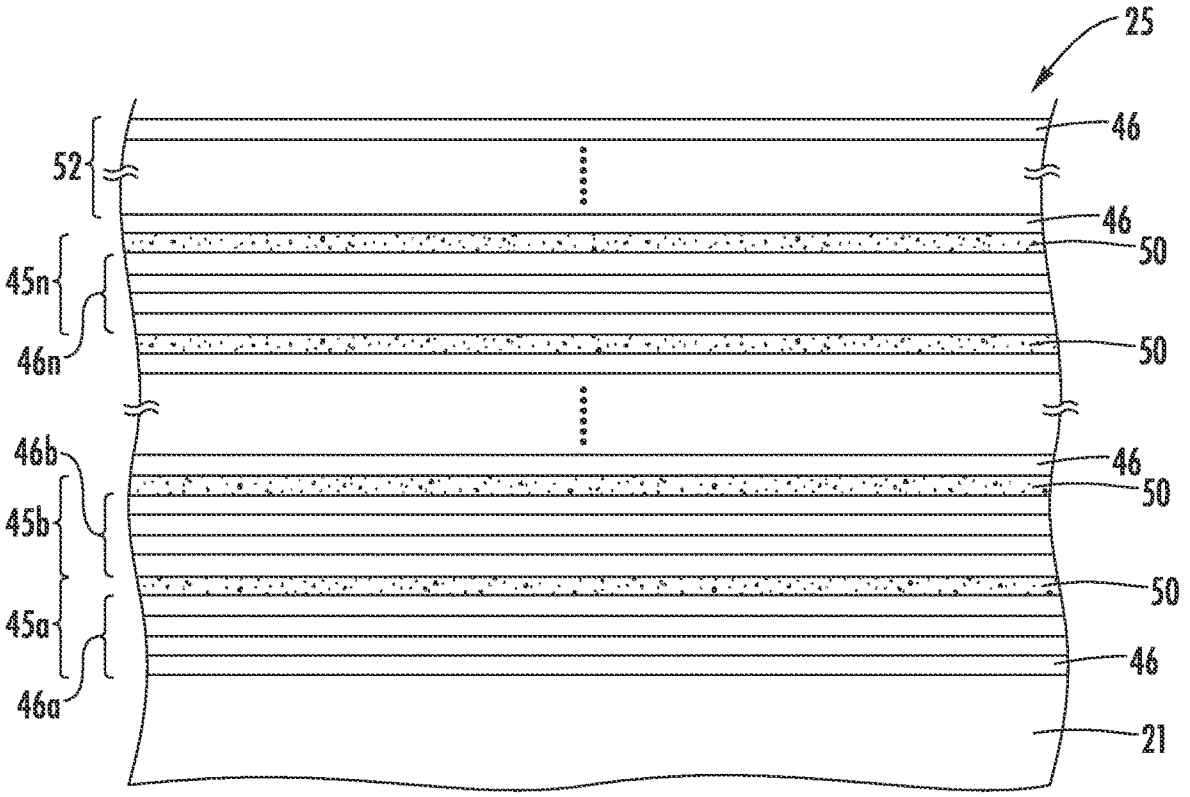


FIG. 1

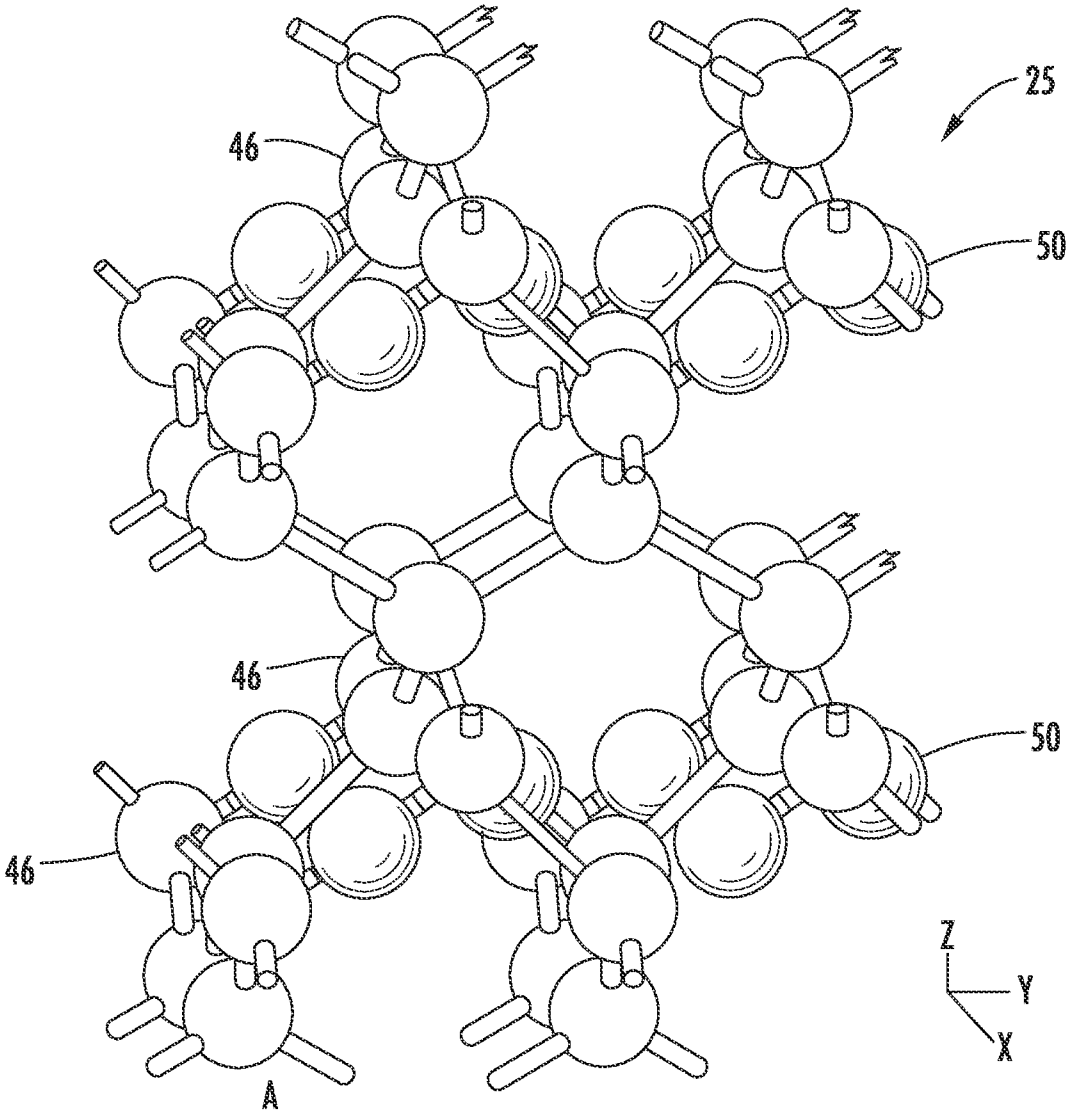


FIG. 2

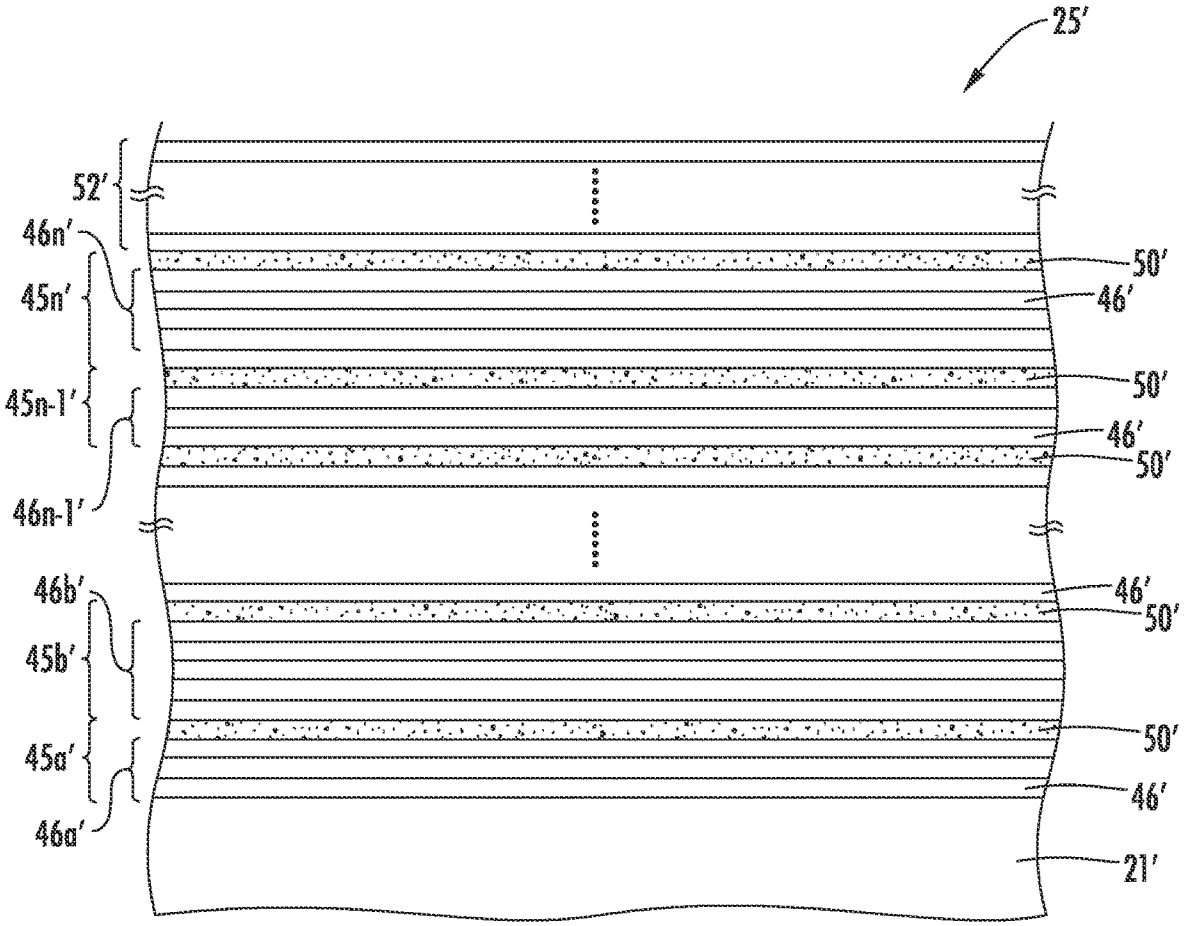

25'
52'
46n'
45n'
45n-1'
46n-1'
46b'
45b'
45a'
46a'
50'
46'
50'
46'
50'
46'
50'
50'
46'
21'

FIG. 3

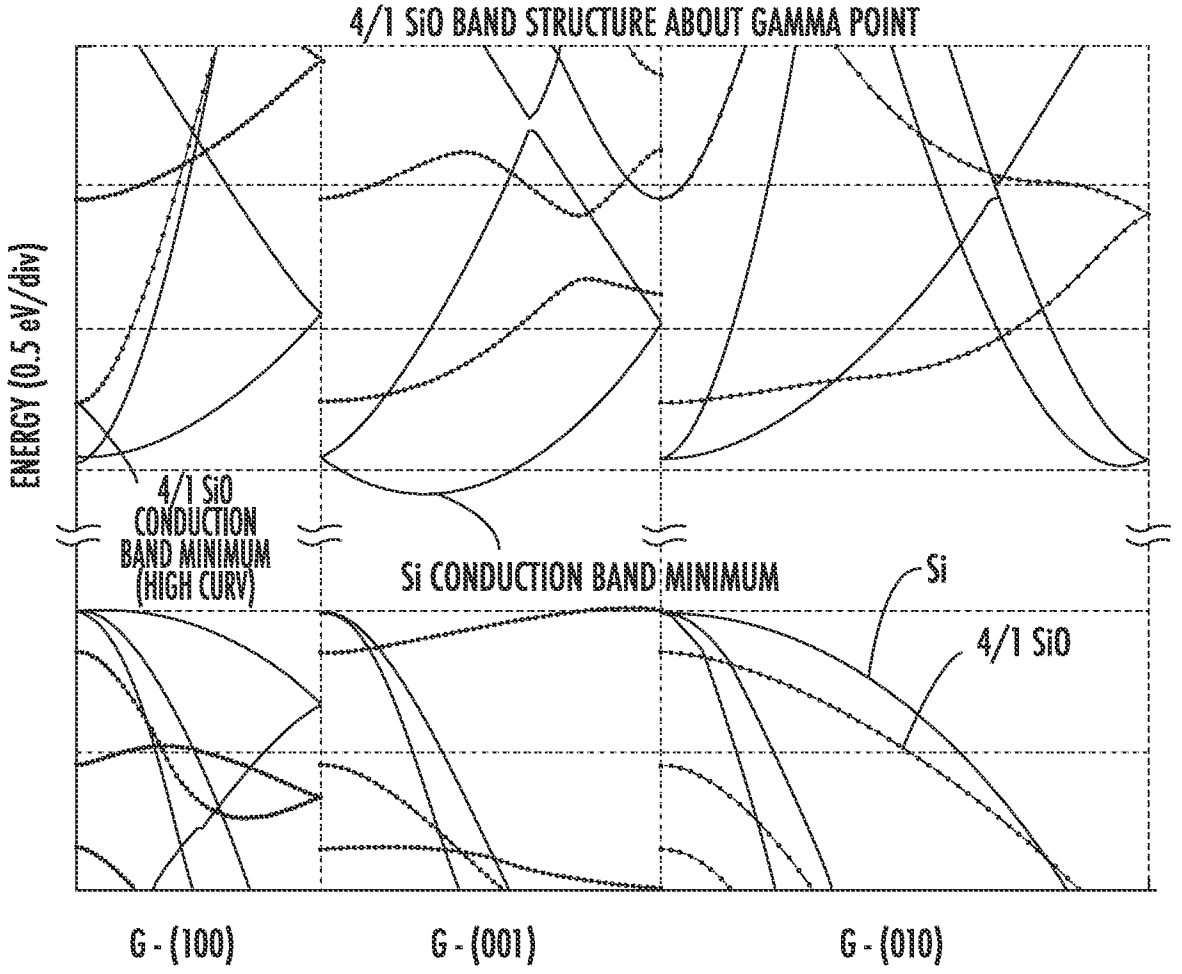

4/1 SiO BAND STRUCTURE ABOUT GAMMA POINT
ENERGY (0.5 eV/div)
4/1 SiO CONDUCTION BAND MINIMUM (HIGH CURV)
Si CONDUCTION BAND MINIMUM
Si
4/1 SiO
G - (100)
G - (001)
G - (010)

FIG. 4A

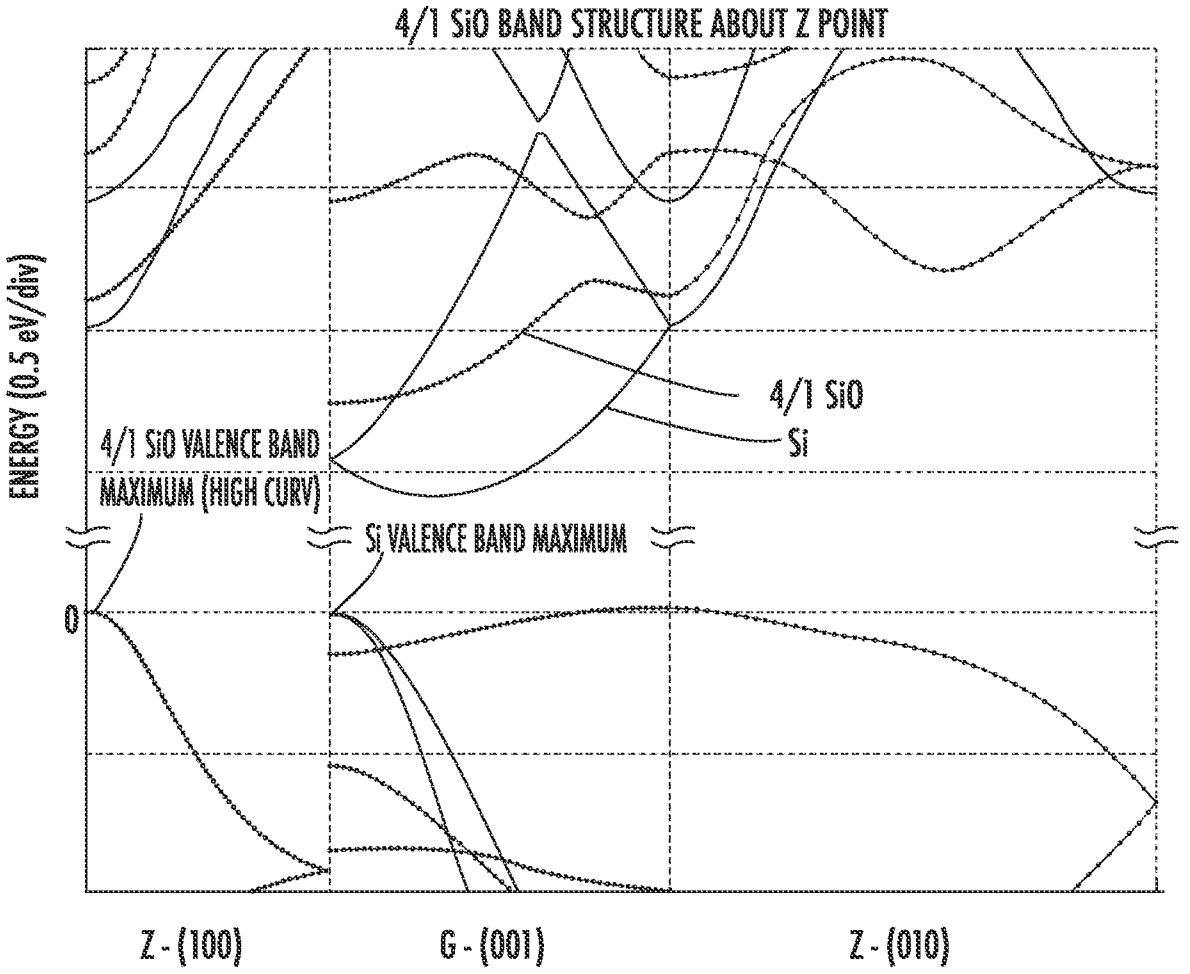

4/1 SiO BAND STRUCTURE ABOUT Z POINT
ENERGY (0.5 eV/div)
4/1 SiO
Si
4/1 SiO VALENCE BAND MAXIMUM (HIGH CURV)
Si VALENCE BAND MAXIMUM
0
Z - (100)
G - (001)
Z - (010)

FIG. 4B

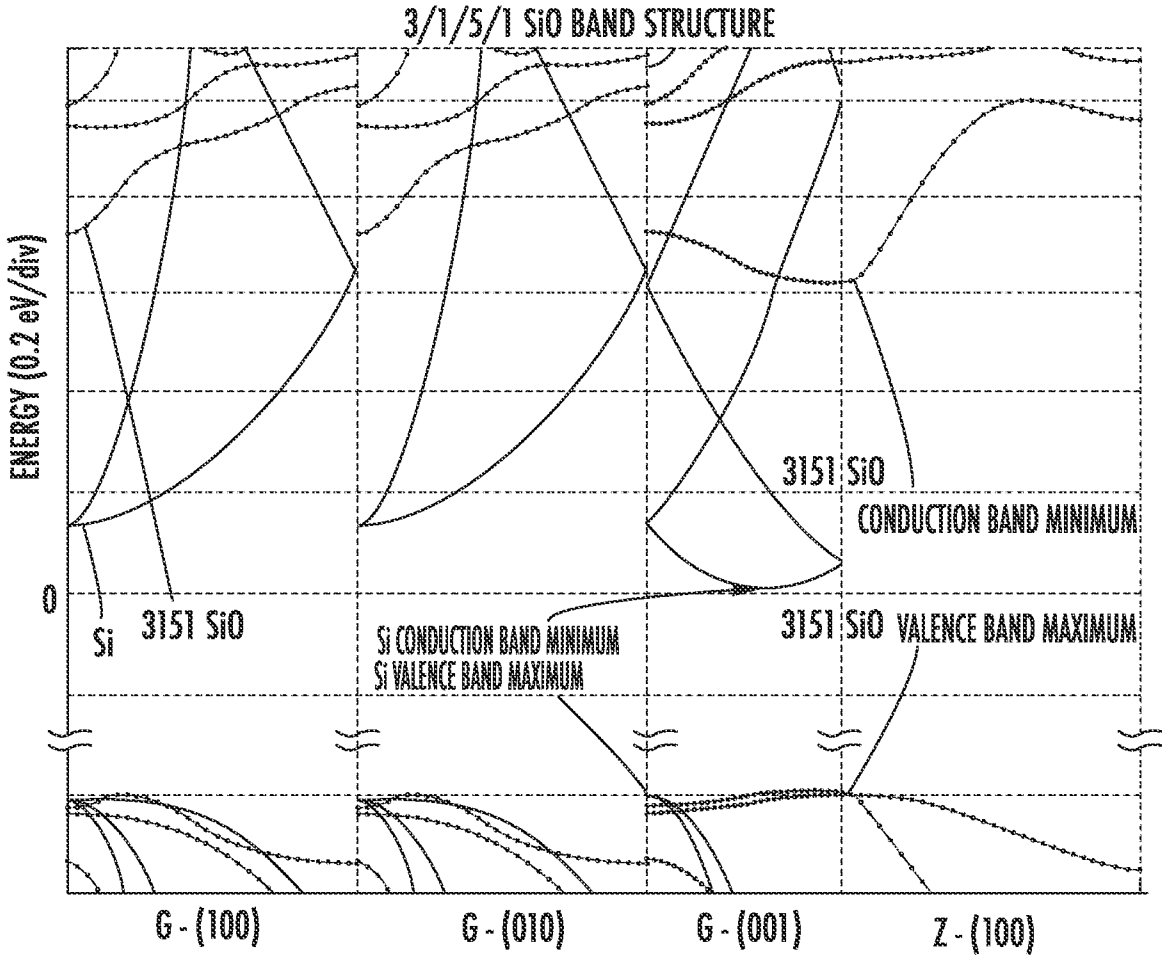

3/1/5/1 SiO BAND STRUCTURE
ENERGY (0.2 eV/div)
0
Si
3151 SiO
Si CONDUCTION BAND MINIMUM
Si VALENCE BAND MAXIMUM
3151 SiO
CONDUCTION BAND MINIMUM
3151 SiO
VALENCE BAND MAXIMUM
G - (100)
G - (010)
G - (001)
Z - (100)

FIG. 4C

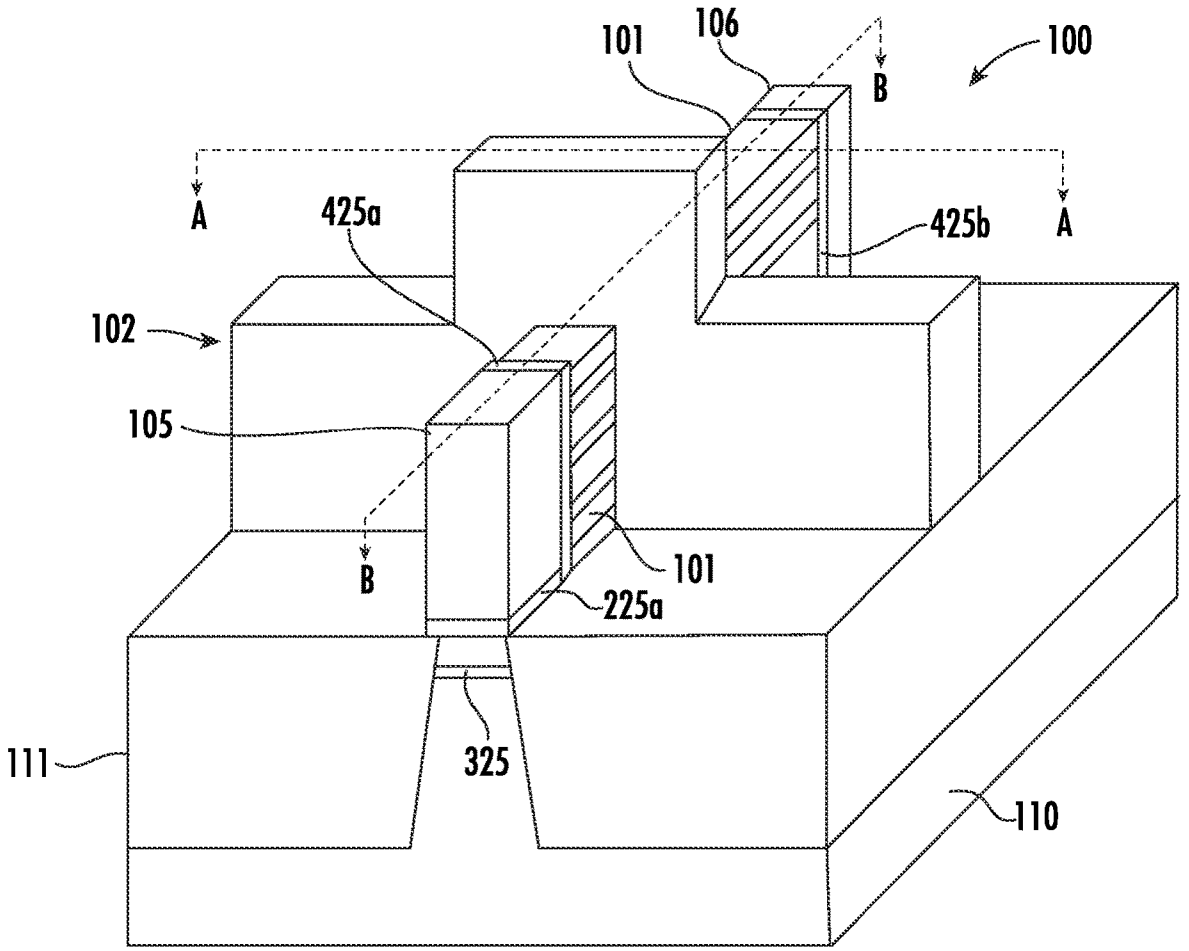


FIG. 5

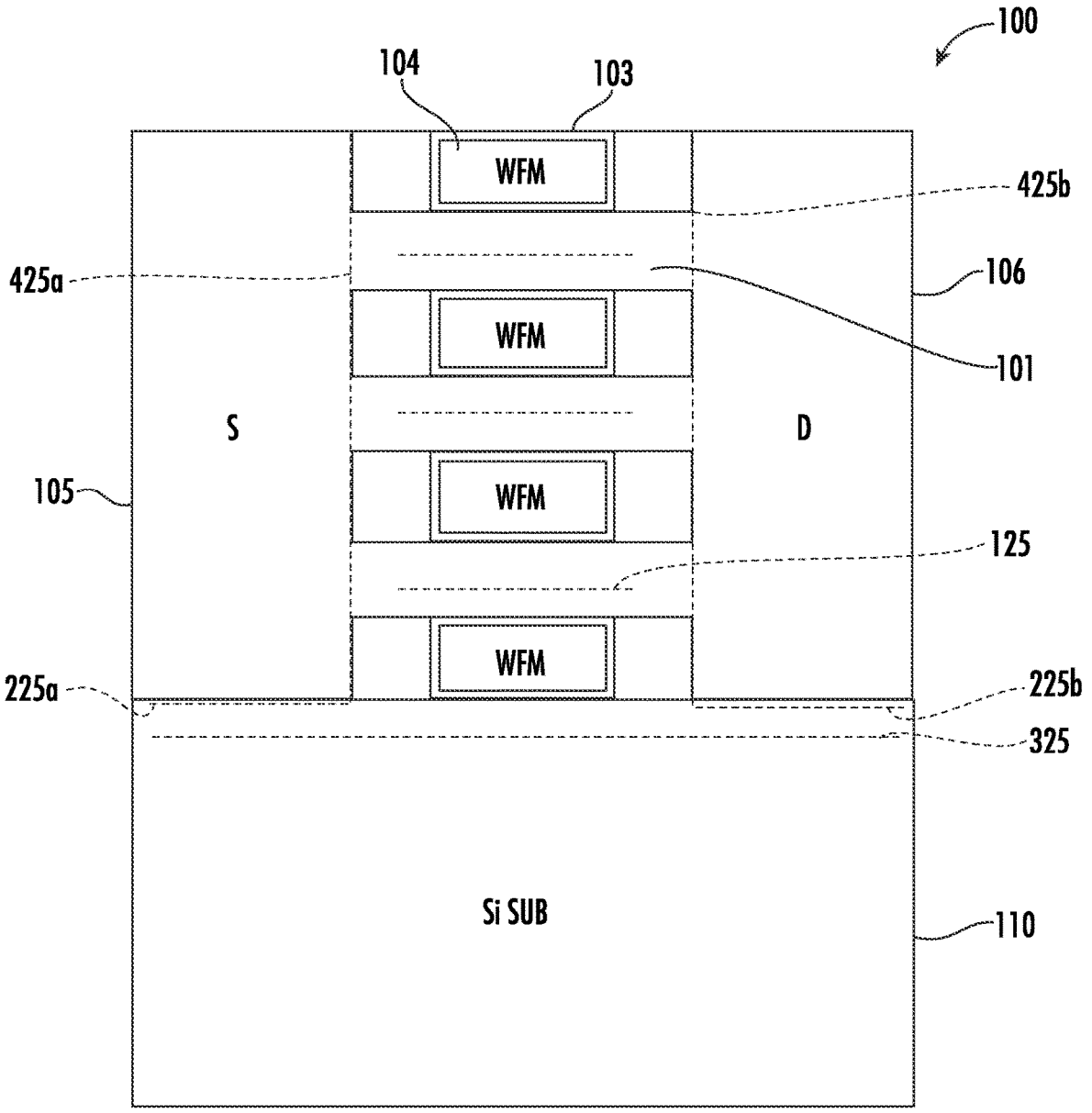

100
104
103
WFM
425b
425a
106
WFM
101
S
D
105
WFM
125
WFM
225a
225b
325
Si SUB
110

FIG. 6

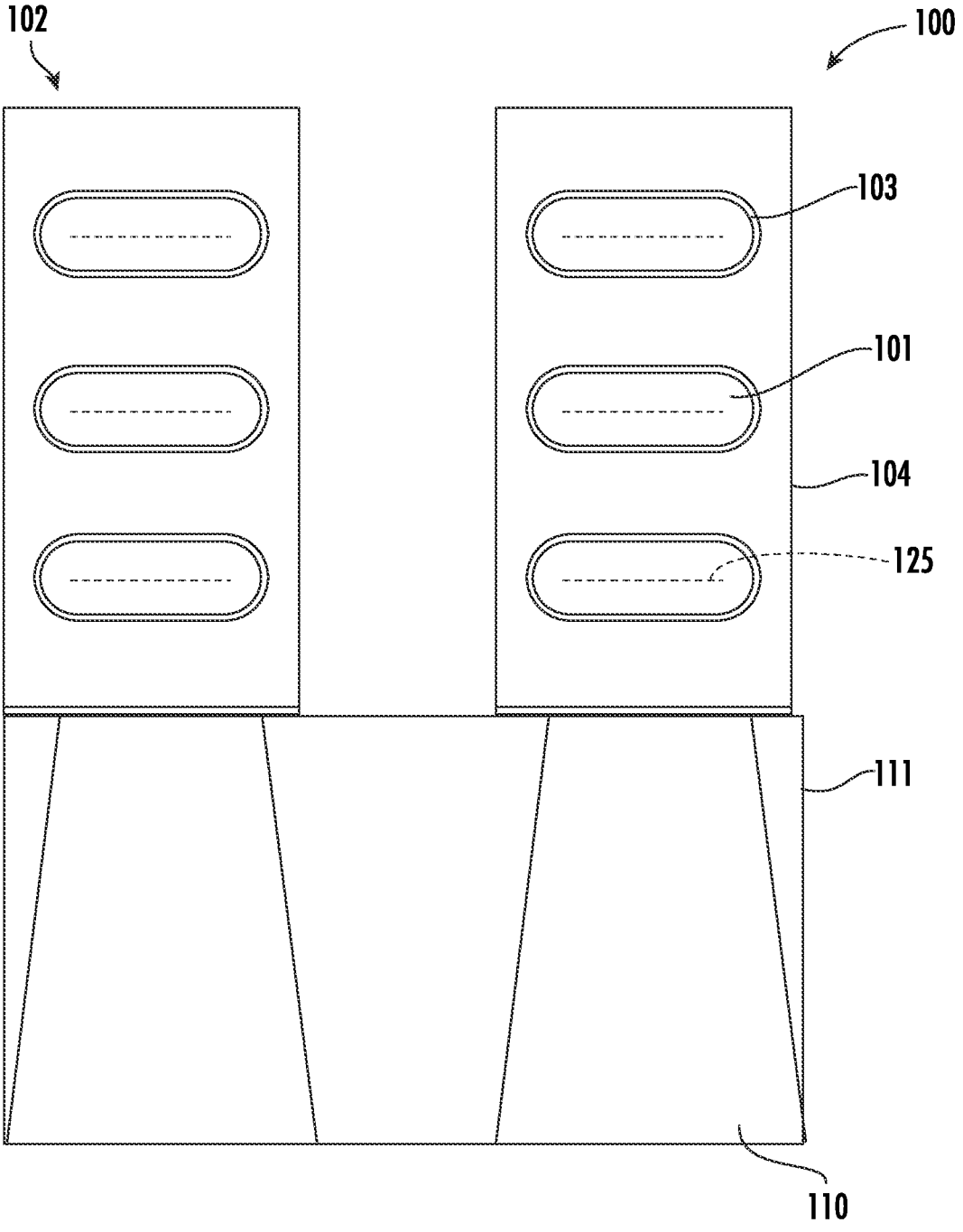


FIG. 7

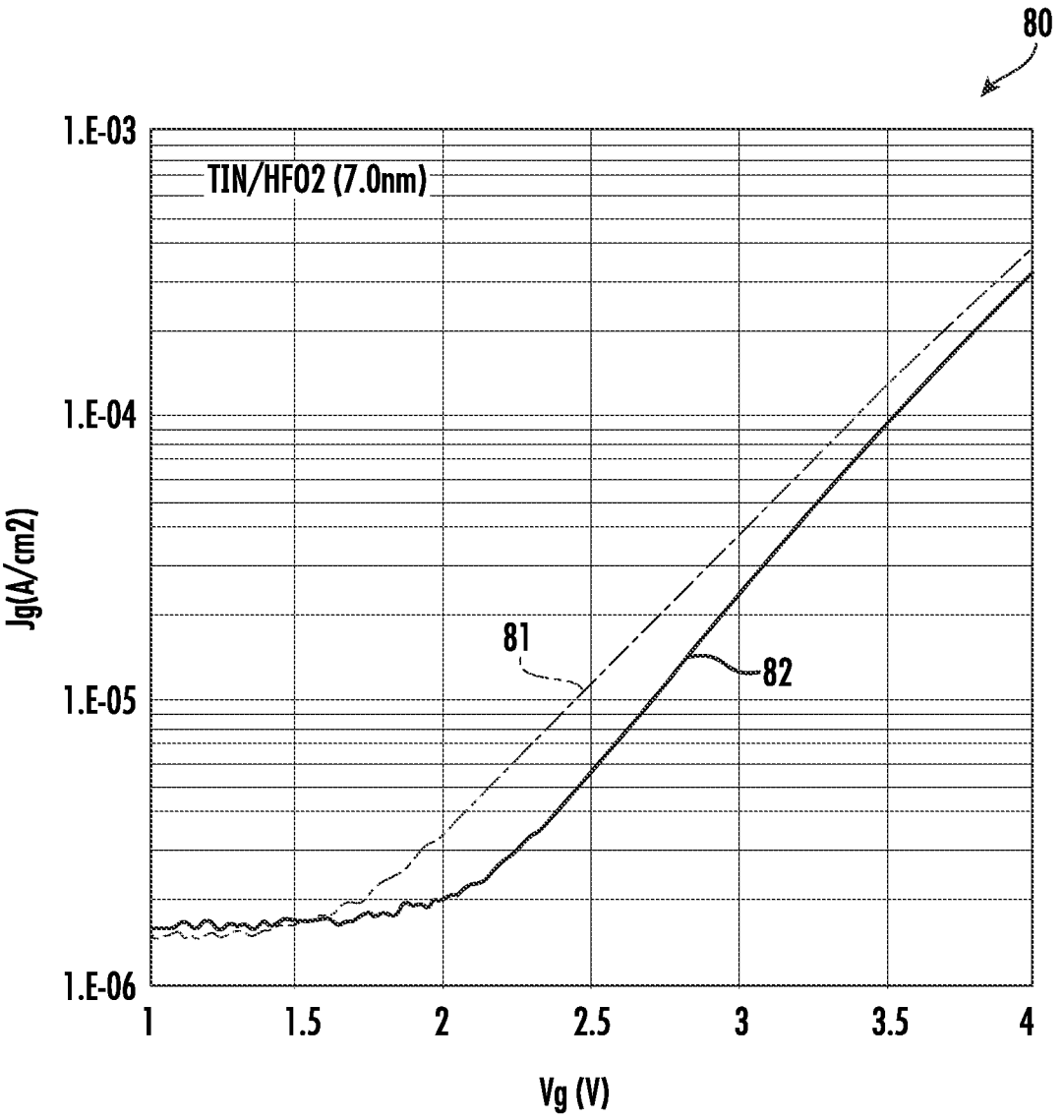

80
1.E-03
TIN/HFO2 (7.0nm)
1.E-04
1.E-05
1.E-06
Jg(A/cm2)
81
82
1
1.5
2
2.5
3
3.5
4
Vg (V)

FIG. 8

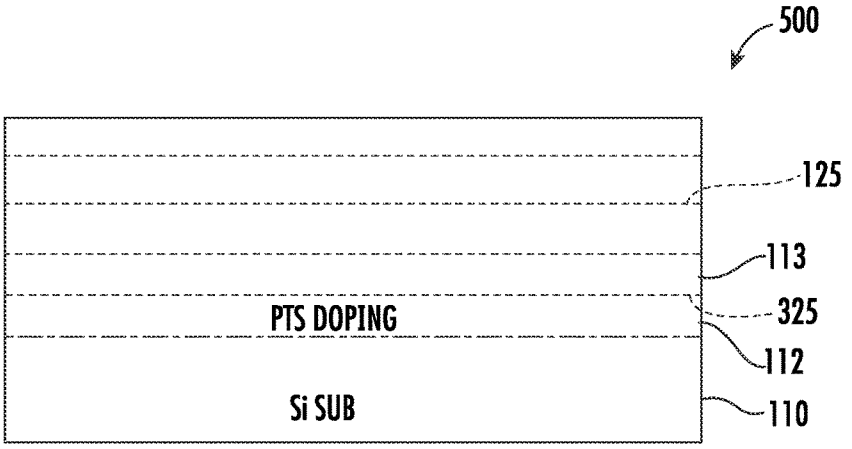


FIG. 9A

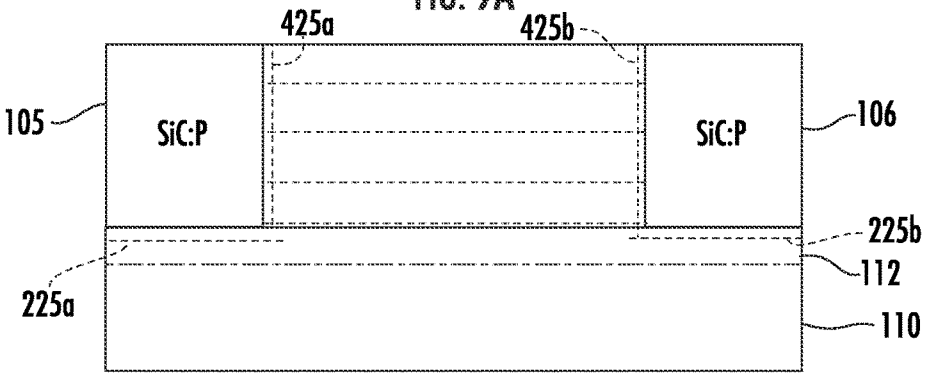


FIG. 9B

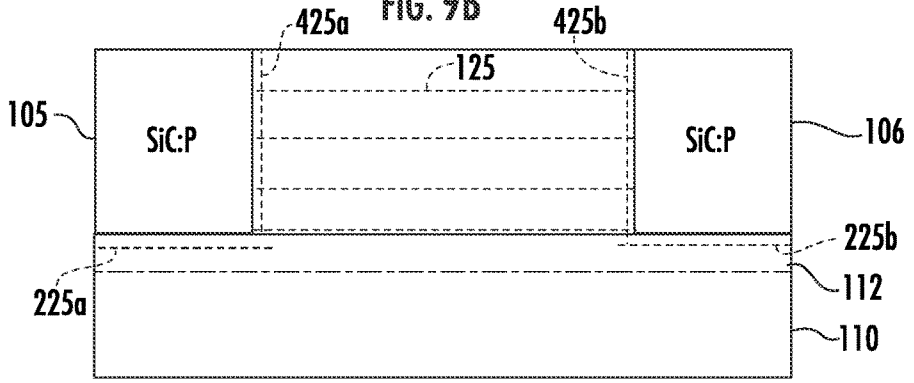


FIG. 9C

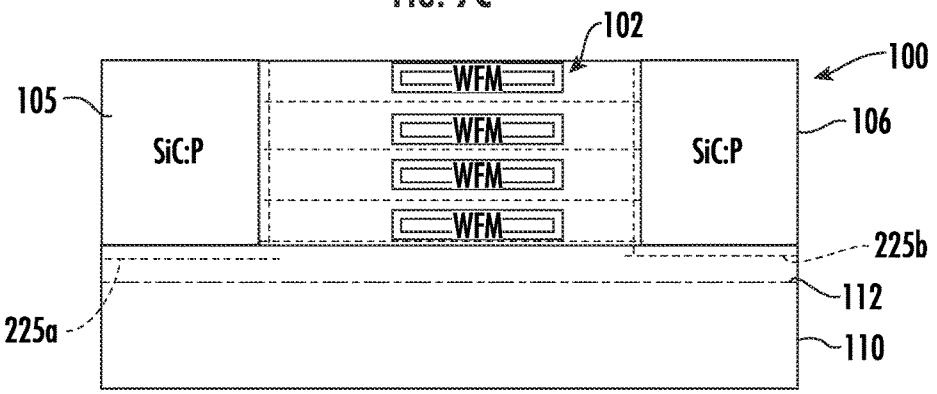


FIG. 9D

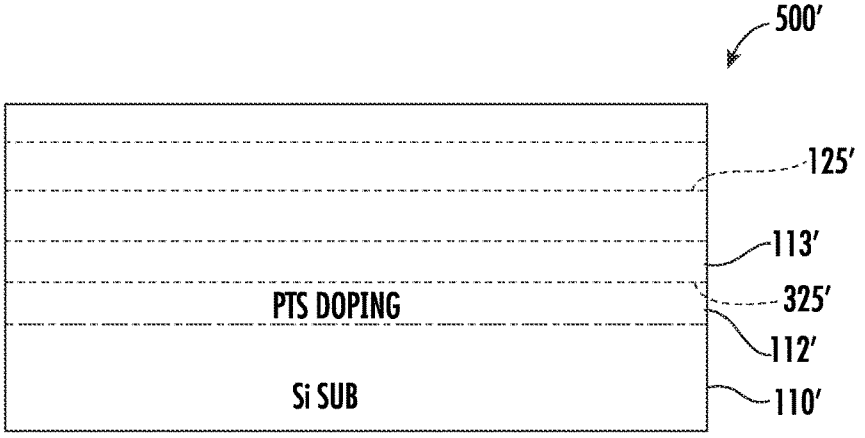


FIG. 10A

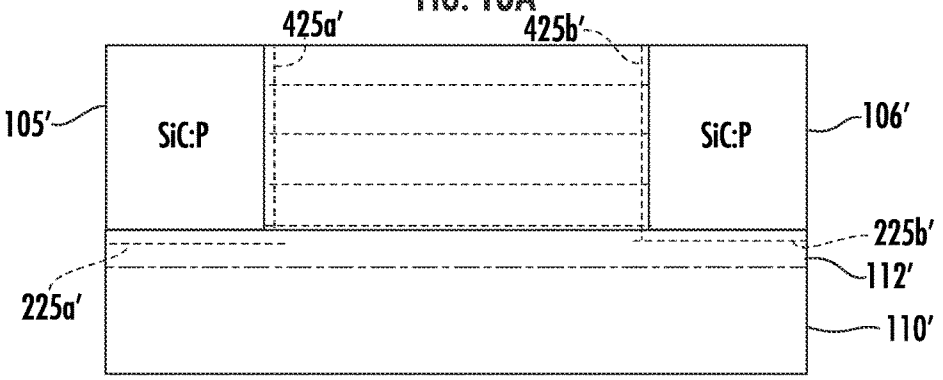


FIG. 10B

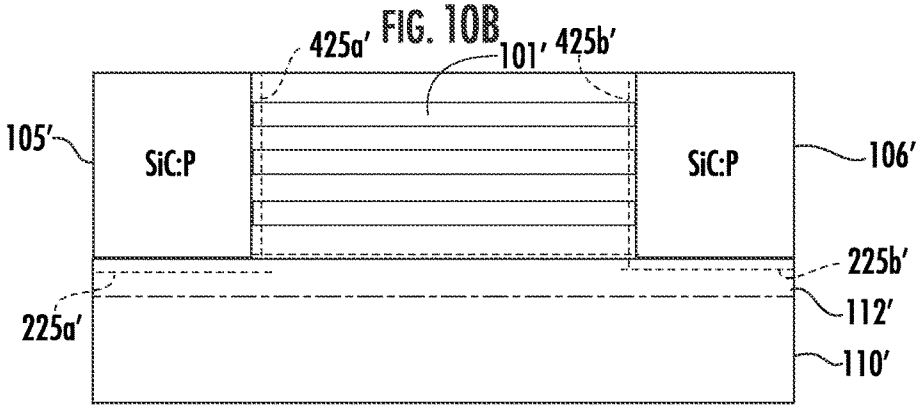


FIG. 10C

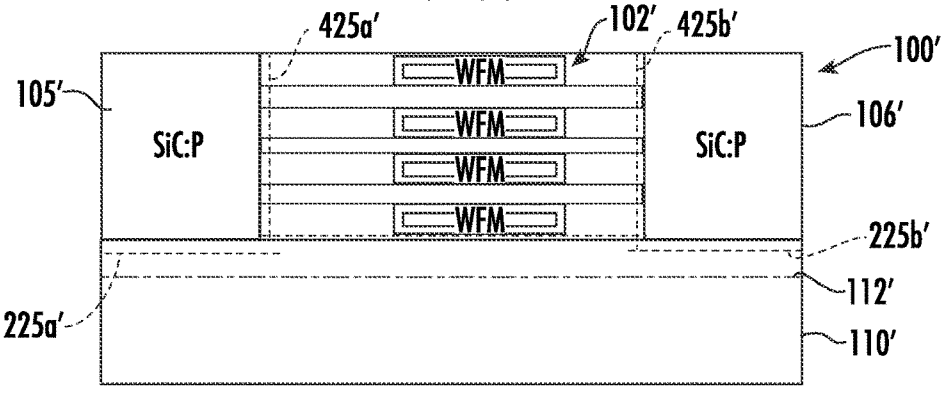


FIG. 10D

METHOD FOR MAKING SEMICONDUCTOR DEVICE INCLUDING A SUPERLATTICE PROVIDING METAL WORK FUNCTION TUNING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. provisional application Nos. 63/189,909 filed May 18, 2021; 63/211,174 filed Jun. 16, 2021; and 63/212,292 filed Jun. 18, 2021, all of which are hereby incorporated herein in their entireties by reference.

TECHNICAL FIELD

[0002] The present disclosure generally relates to semiconductor devices and, more particularly, to semiconductor devices including nanostructures and related methods.

BACKGROUND

[0003] Structures and techniques have been proposed to enhance the performance of semiconductor devices, such as by enhancing the mobility of the charge carriers. For example, U.S. Patent Application No. 2003/0057416 to Currie et al. discloses strained material layers of silicon, silicon-germanium, and relaxed silicon and also including impurity-free zones that would otherwise cause performance degradation. The resulting biaxial strain in the upper silicon layer alters the carrier mobilities enabling higher speed and/or lower power devices. Published U.S. Patent Application No. 2003/0034529 to Fitzgerald et al. discloses a CMOS inverter also based upon similar strained silicon technology.

[0004] U.S. Pat. No. 6,472,685 B2 to Takagi discloses a semiconductor device including a silicon and carbon layer sandwiched between silicon layers so that the conduction band and valence band of the second silicon layer receive a tensile strain. Electrons having a smaller effective mass, and which have been induced by an electric field applied to the gate electrode, are confined in the second silicon layer, thus, an n-channel MOSFET is asserted to have a higher mobility.

[0005] U.S. Pat. No. 4,937,204 to Ishibashi et al. discloses a superlattice in which a plurality of layers, less than eight monolayers, and containing a fractional or binary or a binary compound semiconductor layer, are alternately and epitaxially grown. The direction of main current flow is perpendicular to the layers of the superlattice.

[0006] U.S. Pat. No. 5,357,119 to Wang et al. discloses a Si—Ge short period superlattice with higher mobility achieved by reducing alloy scattering in the superlattice. Along these lines, U.S. Pat. No. 5,683,934 to Candelaria discloses an enhanced mobility MOSFET including a channel layer comprising an alloy of silicon and a second material substitutionally present in the silicon lattice at a percentage that places the channel layer under tensile stress.

[0007] U.S. Pat. No. 5,216,262 to Tsu discloses a quantum well structure comprising two barrier regions and a thin epitaxially grown semiconductor layer sandwiched between the barriers. Each barrier region consists of alternate layers of SiO2/Si with a thickness generally in a range of two to six monolayers. A much thicker section of silicon is sandwiched between the barriers.

[0008] An article entitled "Phenomena in silicon nanostructure devices" also to Tsu and published online Sep. 6, 2000 by Applied Physics and Materials Science & Processing, pp. 391-402 discloses a semiconductor-atomic superlattice (SAS) of silicon and oxygen. The Si/O superlattice is disclosed as useful in a silicon quantum and light-emitting devices. In particular, a green electroluminescence diode structure was constructed and tested. Current flow in the diode structure is vertical, that is, perpendicular to the layers of the SAS. The disclosed SAS may include semiconductor layers separated by adsorbed species such as oxygen atoms, and CO molecules. The silicon growth beyond the adsorbed monolayer of oxygen is described as epitaxial with a fairly low defect density. One SAS structure included a 1.1 nm thick silicon portion that is about eight atomic layers of silicon, and another structure had twice this thickness of silicon. An article to Luo et al. entitled "Chemical Design of Direct-Gap Light-Emitting Silicon" published in Physical Review Letters, Vol. 89, No. 7 (Aug. 12, 2002) further discusses the light emitting SAS structures of Tsu.

[0009] U.S. Pat. No. 7,105,895 to Wang et al. discloses a barrier building block of thin silicon and oxygen, carbon, nitrogen, phosphorous, antimony, arsenic or hydrogen to thereby reduce current flowing vertically through the lattice more than four orders of magnitude. The insulating layer/barrier layer allows for low defect epitaxial silicon to be deposited next to the insulating layer.

[0010] Published Great Britain Patent Application 2,347,520 to Mears et al. discloses that principles of Aperiodic Photonic Band-Gap (APBG) structures may be adapted for electronic bandgap engineering. In particular, the application discloses that material parameters, for example, the location of band minima, effective mass, etc., can be tailored to yield new aperiodic materials with desirable band-structure characteristics. Other parameters, such as electrical conductivity, thermal conductivity and dielectric permittivity or magnetic permeability are disclosed as also possible to be designed into the material.

[0011] Furthermore, U.S. Pat. No. 6,376,337 to Wang et al. discloses a method for producing an insulating or barrier layer for semiconductor devices which includes depositing a layer of silicon and at least one additional element on the silicon substrate whereby the deposited layer is substantially free of defects such that epitaxial silicon substantially free of defects can be deposited on the deposited layer. Alternatively, a monolayer of one or more elements, preferably comprising oxygen, is absorbed on a silicon substrate. A plurality of insulating layers sandwiched between epitaxial silicon forms a barrier composite.

[0012] Despite the existence of such approaches, further enhancements may be desirable for using advanced semiconductor materials and processing techniques to achieve improved performance in semiconductor devices.

SUMMARY

[0013] A method for making a semiconductor gate-all-around (GAA) device may include forming source and drain regions on a semiconductor substrate, forming a plurality of semiconductor nanostructures extending between the source and drain regions, forming a gate surrounding the plurality of semiconductor nanostructures in a gate-all-around arrangement, and forming a dopant diffusion liner adjacent at least one of the source and drain regions and comprising a first superlattice. The first superlattice may include a plurality of stacked groups of layers, with each group of layers including a plurality of stacked base semiconductor

monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

[0014] In an example embodiment, the dopant diffusion liner may comprise respective portions adjacent each of the source and drain regions. In some embodiment, the method may also include forming a second superlattice within at least one of the nanostructures, the second superlattice including a plurality of stacked groups of layers, with each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

[0015] In another example embodiment, the method may include forming a third superlattice embedded in the semiconductor substrate extending between the source and drain regions. The third superlattice may include a plurality of stacked groups of layers, with each group of layers including a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

[0016] In still another example embodiment, the method may also include forming a fourth superlattice on the semiconductor substrate beneath the source region. The fourth superlattice may include a plurality of stacked groups of layers, with each group of layers including a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

[0017] In some embodiments, the method may also include forming a fifth superlattice on the semiconductor substrate beneath the drain region. The fifth superlattice may include a plurality of stacked groups of layers, with each group of layers including a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

[0018] By way of example, the gate may comprise a metal. Also by way of example, the base semiconductor portion may comprise silicon, and the at least one non-semiconductor monolayer may comprise oxygen.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. **1** is a greatly enlarged schematic cross-sectional view of a superlattice for use in a semiconductor device in accordance with an example embodiment.

[0020] FIG. **2** is a perspective schematic atomic diagram of a portion of the superlattice shown in FIG. **1**.

[0021] FIG. **3** is a greatly enlarged schematic cross-sectional view of another embodiment of a superlattice in accordance with an example embodiment.

[0022] FIG. **4**A is a graph of the calculated band structure from the gamma point (G) for both bulk silicon as in the prior art, and for the 4/1 Si/O superlattice as shown in FIGS. **1-2**.

[0023] FIG. **4**B is a graph of the calculated band structure from the Z point for both bulk silicon as in the prior art, and for the 4/1 Si/O superlattice as shown in FIGS. **1-2**.

[0024] FIG. **4**C is a graph of the calculated band structure from both the gamma and Z points for both bulk silicon as in the prior art, and for the 5/1/3/1 Si/O superlattice as shown in FIG. **3**.

[0025] FIG. **5** is a schematic block diagram of a gate all around (GAA) semiconductor device in accordance with an example embodiment.

[0026] FIG. **6** is a cross-sectional diagram of the GAA device of FIG. **5** taken along line B-B.

[0027] FIG. **7** is a cross-sectional diagram of the GAA device of FIG. **5** taken along line A-A.

[0028] FIG. **8** is a diagram of atomic concentration vs. voltage illustrating example threshold voltage reductions for a metal gate semiconductor device such as the GAA device of FIG. **5** in accordance with an example embodiment.

[0029] FIG. **9** is a series of cross-sectional diagrams illustrating a method for making the GAA device of FIG. **5** with superlattices in the GAA nanostructures.

[0030] FIG. **10** is a series of cross-sectional diagrams illustrating a method for making an alternative embodiment of the GAA device of FIG. **5** without superlattices in the GAA nanostructures.

DETAILED DESCRIPTION

[0031] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings, in which the example embodiments are shown. The embodiments may, however, be implemented in many different forms and should not be construed as limited to the specific examples set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete. Like numbers refer to like elements throughout, and prime notation is used to indicate similar elements in different embodiments.

[0032] Generally speaking, the present disclosure relates to gate-all-around (GAA) semiconductor devices having one or more enhanced semiconductor superlattices therein to provide performance enhancement characteristics. The enhanced semiconductor superlattice may also be referred to as an "MST" layer or "MST technology" in this disclosure.

[0033] More particularly, the MST technology relates to advanced semiconductor materials such as the superlattice **25** described further below. Applicant theorizes, without wishing to be bound thereto, that certain superlattices as described herein reduce the effective mass of charge carriers and that this thereby leads to higher charge carrier mobility. Effective mass is described with various definitions in the literature. As a measure of the improvement in effective mass Applicants use a "conductivity reciprocal effective mass tensor", M_e^{-1} and M_h^{-1} for electrons and holes respectively, defined as:

$$M_{e,ij}^{-1}(E_F, T) = \frac{\sum_{E>E_F} \int_{B.Z.} (\nabla_k E(k,n))_i (\nabla_k E(k,n))_j \frac{\partial f(E(k,n), E_F, T)}{\partial E} d^3k}{\sum_{E>E_F} \int_{B.Z.} f(E(k,n), E_F, T) d^3k}$$

for electrons and:

$$M_{h,ij}^{-1}(E_F, T) = \frac{-\sum_{E<E_F} \int_{B.Z.} (\nabla_k E(k, n))_i (\nabla_k E(k, n))_j \frac{\partial f(E(k, n), E_F, T)}{\partial E} d^3k}{\sum_{E<E_F} \int_{B.Z.} (1 - f(E(k, n), E_F, T)) d^3k}$$

for holes, where f is the Fermi-Dirac distribution, E_F is the Fermi energy, T is the temperature, E(k,n) is the energy of an electron in the state corresponding to wave vector k and the n^{th} energy band, the indices i and j refer to Cartesian coordinates x, y and z, the integrals are taken over the Brillouin zone (B.Z.), and the summations are taken over bands with energies above and below the Fermi energy for electrons and holes respectively.

[0034] Applicant's definition of the conductivity reciprocal effective mass tensor is such that a tensorial component of the conductivity of the material is greater for greater values of the corresponding component of the conductivity reciprocal effective mass tensor. Again Applicant theorizes without wishing to be bound thereto that the superlattices described herein set the values of the conductivity reciprocal effective mass tensor so as to enhance the conductive properties of the material, such as typically for a preferred direction of charge carrier transport. The inverse of the appropriate tensor element is referred to as the conductivity effective mass. In other words, to characterize semiconductor material structures, the conductivity effective mass for electrons/holes as described above and calculated in the direction of intended carrier transport is used to distinguish improved materials.

[0035] Applicant has identified improved materials or structures for use in semiconductor devices. More specifically, Applicant has identified materials or structures having energy band structures for which the appropriate conductivity effective masses for electrons and/or holes are substantially less than the corresponding values for silicon. In addition to the enhanced mobility characteristics of these structures, they may also be formed or used in such a manner that they provide piezoelectric, pyroelectric, and/or ferroelectric properties that are advantageous for use in a variety of different types of devices, as will be discussed further below.

[0036] Referring now to FIGS. **1** and **2**, the materials or structures are in the form of a superlattice **25** whose structure is controlled at the atomic or molecular level and may be formed using known techniques of atomic or molecular layer deposition. The superlattice **25** includes a plurality of layer groups **45***a*-**45***n* arranged in stacked relation, as perhaps best understood with specific reference to the schematic cross-sectional view of FIG. **1**.

[0037] Each group of layers **45***a*-**45***n* of the superlattice **25** illustratively includes a plurality of stacked base semiconductor monolayers **46** defining a respective base semiconductor portion **46***a*-**46***n* and an energy band-modifying layer **50** thereon. The energy band-modifying layers **50** are indicated by stippling in FIG. **1** for clarity of illustration.

[0038] The energy band-modifying layer **50** illustratively includes one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. By "constrained within a crystal lattice of adjacent base semiconductor portions" it is meant that at least some semiconductor atoms from opposing base semiconductor portions **46***a*-**46***n* are chemically bound together through the non-semiconductor monolayer **50** therebetween, as seen in FIG. **2**. Generally speaking, this configuration is made possible by controlling the amount of non-semiconductor material that is deposited on semiconductor portions **46***a*-**46***n* through atomic layer deposition techniques so that not all (i.e., less than full or 100% coverage) of the available semiconductor bonding sites are populated with bonds to non-semiconductor atoms, as will be discussed further below. Thus, as further monolayers **46** of semiconductor material are deposited on or over a non-semiconductor monolayer **50**, the newly deposited semiconductor atoms will populate the remaining vacant bonding sites of the semiconductor atoms below the non-semiconductor monolayer.

[0039] In other embodiments, more than one such non-semiconductor monolayer may be possible. It should be noted that reference herein to a non-semiconductor or semiconductor monolayer means that the material used for the monolayer would be a non-semiconductor or semiconductor if formed in bulk. That is, a single monolayer of a material, such as silicon, may not necessarily exhibit the same properties that it would if formed in bulk or in a relatively thick layer, as will be appreciated by those skilled in the art.

[0040] Applicant theorizes without wishing to be bound thereto that energy band-modifying layers **50** and adjacent base semiconductor portions **46***a*-**46***n* cause the superlattice **25** to have a lower appropriate conductivity effective mass for the charge carriers in the parallel layer direction than would otherwise be present. Considered another way, this parallel direction is orthogonal to the stacking direction. The band modifying layers **50** may also cause the superlattice **25** to have a common energy band structure, while also advantageously functioning as an insulator between layers or regions vertically above and below the superlattice.

[0041] Moreover, this superlattice structure may also advantageously act as a barrier to dopant and/or material diffusion between layers vertically above and below the superlattice **25**. These properties may thus advantageously allow the superlattice **25** to provide an interface for high-K dielectrics which not only reduces diffusion of the high-K material into the channel region, but which may also advantageously reduce unwanted scattering effects and improve device mobility, as will be appreciated by those skilled in the art.

[0042] It is also theorized that semiconductor devices including the superlattice **25** may enjoy a higher charge carrier mobility based upon the lower conductivity effective mass than would otherwise be present. In some embodiments, and as a result of the band engineering achieved by the present invention, the superlattice **25** may further have a substantially direct energy bandgap that may be particularly advantageous for opto-electronic devices, for example.

[0043] The superlattice **25** also illustratively includes a cap layer **52** on an upper layer group **45***n*. The cap layer **52** may comprise a plurality of base semiconductor monolayers **46**. The cap layer **52** may have between 2 to 100 monolayers of the base semiconductor, and, more preferably between 10 to 50 monolayers.

[0044] Each base semiconductor portion **46***a*-**46***n* may comprise a base semiconductor selected from the group consisting of Group IV semiconductors, Group III-V semiconductors, and Group II-VI semiconductors. Of course, the

term Group IV semiconductors also includes Group IV-IV semiconductors, as will be appreciated by those skilled in the art. More particularly, the base semiconductor may comprise at least one of silicon and germanium, for example.

[0045] Each energy band-modifying layer **50** may comprise a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, carbon and carbon-oxygen, for example. The non-semiconductor is also desirably thermally stable through deposition of a next layer to thereby facilitate manufacturing. In other embodiments, the non-semiconductor may be another inorganic or organic element or compound that is compatible with the given semiconductor processing as will be appreciated by those skilled in the art. More particularly, the base semiconductor may comprise at least one of silicon and germanium, for example

[0046] It should be noted that the term monolayer is meant to include a single atomic layer and also a single molecular layer. It is also noted that the energy band-modifying layer **50** provided by a single monolayer is also meant to include a monolayer wherein not all of the possible sites are occupied (i.e., there is less than full or 100% coverage). For example, with particular reference to the atomic diagram of FIG. **2**, a 4/1 repeating structure is illustrated for silicon as the base semiconductor material, and oxygen as the energy band-modifying material. Only half of the possible sites for oxygen are occupied in the illustrated example.

[0047] In other embodiments and/or with different materials this one-half occupation would not necessarily be the case as will be appreciated by those skilled in the art. Indeed it can be seen even in this schematic diagram, that individual atoms of oxygen in a given monolayer are not precisely aligned along a flat plane as will also be appreciated by those of skill in the art of atomic deposition. By way of example, a preferred occupation range is from about one-eighth to one-half of the possible oxygen sites being full, although other numbers may be used in certain embodiments.

[0048] Silicon and oxygen are currently widely used in conventional semiconductor processing, and, hence, manufacturers will be readily able to use these materials as described herein. Atomic or monolayer deposition is also now widely used. Accordingly, semiconductor devices incorporating the superlattice **25** in accordance with the invention may be readily adopted and implemented, as will be appreciated by those skilled in the art.

[0049] It is theorized without Applicant wishing to be bound thereto that for a superlattice, such as the Si/O superlattice, for example, that the number of silicon monolayers should desirably be seven or less so that the energy band of the superlattice is common or relatively uniform throughout to achieve the desired advantages. The 4/1 repeating structure shown in FIGS. **1** and **2**, for Si/O has been modeled to indicate an enhanced mobility for electrons and holes in the X direction. For example, the calculated conductivity effective mass for electrons (isotropic for bulk silicon) is 0.26 and for the 4/1 SiO superlattice in the X direction it is 0.12 resulting in a ratio of 0.46. Similarly, the calculation for holes yields values of 0.36 for bulk silicon and 0.16 for the 4/1 Si/O superlattice resulting in a ratio of 0.44.

[0050] While such a directionally preferential feature may be desired in certain semiconductor devices, other devices may benefit from a more uniform increase in mobility in any direction parallel to the groups of layers. It may also be beneficial to have an increased mobility for both electrons and holes, or just one of these types of charge carriers as will be appreciated by those skilled in the art.

[0051] The lower conductivity effective mass for the 4/1 Si/O embodiment of the superlattice **25** may be less than two-thirds the conductivity effective mass than would otherwise occur, and this applies for both electrons and holes. Of course, the superlattice **25** may further comprise at least one type of conductivity dopant therein, as will also be appreciated by those skilled in the art.

[0052] Indeed, referring now additionally to FIG. **3**, another embodiment of a superlattice **25'** in accordance with the invention having different properties is now described. In this embodiment, a repeating pattern of 3/1/5/1 is illustrated. More particularly, the lowest base semiconductor portion **46***a*' has three monolayers, and the second lowest base semiconductor portion **46***b*' has five monolayers. This pattern repeats throughout the superlattice **25'**. The energy band-modifying layers **50'** may each include a single monolayer. For such a superlattice **25'** including Si/O, the enhancement of charge carrier mobility is independent of orientation in the plane of the layers. Those other elements of FIG. **3** not specifically mentioned are similar to those discussed above with reference to FIG. **1** and need no further discussion herein.

[0053] In some device embodiments, all of the base semiconductor portions of a superlattice may be a same number of monolayers thick. In other embodiments, at least some of the base semiconductor portions may be a different number of monolayers thick. In still other embodiments, all of the base semiconductor portions may be a different number of monolayers thick.

[0054] In FIGS. **4**A-**4**C, band structures calculated using Density Functional Theory (DFT) are presented. It is well known in the art that DFT underestimates the absolute value of the bandgap. Hence all bands above the gap may be shifted by an appropriate "scissors correction." However the shape of the band is known to be much more reliable. The vertical energy axes should be interpreted in this light.

[0055] FIG. **4**A shows the calculated band structure from the gamma point (G) for both bulk silicon (represented by continuous lines) and for the 4/1 Si/O superlattice **25** shown in FIG. **1** (represented by dotted lines). The directions refer to the unit cell of the 4/1 Si/O structure and not to the conventional unit cell of Si, although the (001) direction in the figure does correspond to the (001) direction of the conventional unit cell of Si, and, hence, shows the expected location of the Si conduction band minimum. The (100) and (010) directions in the figure correspond to the (110) and (−110) directions of the conventional Si unit cell. Those skilled in the art will appreciate that the bands of Si on the figure are folded to represent them on the appropriate reciprocal lattice directions for the 4/1 Si/O structure.

[0056] It can be seen that the conduction band minimum for the 4/1 Si/O structure is located at the gamma point in contrast to bulk silicon (Si), whereas the valence band minimum occurs at the edge of the Brillouin zone in the (001) direction which we refer to as the Z point. One may also note the greater curvature of the conduction band minimum for the 4/1 Si/O structure compared to the curvature of the conduction band minimum for Si owing to the band splitting due to the perturbation introduced by the additional oxygen layer.

[0057] FIG. **4**B shows the calculated band structure from the Z point for both bulk silicon (continuous lines) and for the 4/1 Si/O superlattice **25** (dotted lines). This figure illustrates the enhanced curvature of the valence band in the (100) direction.

[0058] FIG. **4**C shows the calculated band structure from both the gamma and Z point for both bulk silicon (continuous lines) and for the 5/1/3/1 Si/O structure of the superlattice **25'** of FIG. **3** (dotted lines). Due to the symmetry of the 5/1/3/1 Si/O structure, the calculated band structures in the (100) and (010) directions are equivalent. Thus the conductivity effective mass and mobility are expected to be isotropic in the plane parallel to the layers, i.e. perpendicular to the (001) stacking direction. Note that in the 5/1/3/1 Si/O example the conduction band minimum and the valence band maximum are both at or close to the Z point.

[0059] Although increased curvature is an indication of reduced effective mass, the appropriate comparison and discrimination may be made via the conductivity reciprocal effective mass tensor calculation. This leads Applicant to further theorize that the 5/1/3/1 superlattice **25'** should be substantially direct bandgap. As will be understood by those skilled in the art, the appropriate matrix element for optical transition is another indicator of the distinction between direct and indirect bandgap behavior.

[0060] Referring now to FIGS. **5-8**, the above-described superlattice structures may advantageously be used to provide enhanced metal work function tuning in semiconductor devices, such as a gate-all-around (GAA) device **100**, for example. More particularly, in the illustrated GAA device **100**, nanostructures (here nanosheets **101**) are surrounded on all sides by a gate **102** including a high K dielectric **103** and a metal electrode **104**. In other embodiments, the nanostructures may take the form of nanoparticles, nanowires, nanofibers, nanotubes, nanobelts, nanoribbons, nanodiscs, nanoplatelets, or nanohorns, and such nanostructures generally have a thickness or diameter in a range of 0.5 nm to 100 nm, for example, although other dimensions may be used in different embodiments. The channel of the GAA device **100** extends through the nanosheets **101** between source and drain regions **105**, **106**.

[0061] Generally speaking, GAA devices not only provide for more efficient utilization of device real estate for higher device densities, they may also help reduce problems associated with channel width variations, such as variability and mobility loss. However, in conventional GAA devices, the threshold voltage (Vt) may need to be controlled by the metal work function of the electrode metal. Typically, this involves adjusting the thickness of the metal, with thicker metal providing higher Vt values, and thinner metal providing lower Vt values. However, GAA structures may be space constrained, such that there is not enough room available for low Vt (high thickness) metals, as this would limit the number of nanosheets **101** that could otherwise be placed in the gate stack. Since drive current is proportional to the number of nanosheets **101** present, use of low Vt (high thickness) metal may otherwise lead to an undesirable decrease in drive current for low Vt devices. By way of background, U.S. Pat. Pub. No. 2021/0126018 to Zhang et al., which is hereby incorporated herein in its entirety by reference, discloses one approach to implementing a GAA device in which the Vt is shifted based on a thickness of a portion of the dielectric layer.

[0062] In the present example, one or more inserted non-semiconductor (e.g., oxygen) monolayers **50** or full MST films **125** may be incorporated within the nanosheets of a GAA device to advantageously provide desired work function tuning (see FIGS. **6** and **7**). As shown in the diagram **80** of FIG. **8**, simulation results establish that incorporation of one or more non-semiconductor monolayers within a nanosheet advantageously lowers Vt vs. a pure silicon nanosheet, such that a relatively thin metal thickness may be used without resulting in the otherwise high Vt that would accompany the relatively low metal thickness. In the illustrated example, respective plots **81**, **82** illustrate voltage per atomic area using an MST film vs. straight silicon with a TiN/HfO2 gate configuration having a 7 nm thickness for the simulations. However, it will be appreciated that other gate materials and configurations may be used in different embodiments.

[0063] In this way, for integrated circuits where both high and low Vt devices are required, similar structures may be used for both, just with the inclusion of an inserted oxygen (or MST) layer within the nanosheets of the low Vt devices. Processes for making high and low Vt GAA devices with and without inserted oxygen/MST layers in the nanosheets **100** will be discussed below with reference to FIGS. **9** and **10**, respectively. It should be noted that one or more inserted oxygen (or MST) layers may be at different locations within the nanosheets, such as at the top and/or bottom interfaces, as well as in the middle of the nanosheet. Further details regarding the incorporation of inserted oxygen/MST layers in nanostructures are provided in U.S. Pat. Pub. No. 2022/0005926 to Weeks et al., which is assigned to the present Applicant and hereby incorporated herein in its entirety by reference.

[0064] As also seen in FIG. **6**, inserted oxygen (or MST) layers **225***a* and/or **225***b* may additionally (or instead) be incorporated on the surface of the substrate **110** (here a silicon substrate) below the source and/or drain **105**, **106**, respectively, to advantageously provide a punch through stop (PTS) layer to help avoid source/drain dopant punch through. Moreover, an inserted oxygen (or MST) layer **325** may additionally (or instead) be positioned in the substrate **110** as a PTS layer extending between the source and drain **105**, **106**, either individually or in conjunction with the layers **225***a* and/or **225***b*. In the illustrated example, shallow trench isolation (STI) regions **111** (e.g., SiO_2) are used to electrically isolate different devices across the substrate **110**.

[0065] Also in the illustrated example, a respective dopant diffusion liner **425***a*, **425***b* (which may be an inserted oxygen or MST layer) is located between the source **105** and the gate **102** and/or between the drain **106** and the gate, respectively, as shown to advantageously help prevent dopant diffusion from the source/drain regions to the nanosheets **101**. Further information regarding the use of MST layers as PTS layers and for dopant diffusion blocking are set forth in U.S. Pat. Nos. 9,941,359 and 9,899,479, which are both assigned to the present Applicant and hereby incorporated herein in their entireties by reference. MST films used for the various layers **125**, **225***a*, **225***b*, **325**, **425***a*, and **425***b* may be similar to those described above with reference to FIGS. **1-4***c*, as well as in U.S. Pat. Pub. No. 2022/0005926 noted above, for example.

[0066] Referring now additionally to the process flow diagrams **500**, **500'** of FIGS. **9** and **10**, example methods for fabricating low and high Vt GAA devices **100**, **100'** with

superlattices **125** in the nanosheets **101** and without, respectively, are now described. In step (a) of both process flows, a PTS implant **112** or **112'** is formed in the substrate **110** or **110'**. This is followed by the formation of the PTS layer **325** or **325'** and nanosheet epitaxy with epitaxial silicon germanium (SiGe) **113** or **113'** deposition with vertically spaced silicon/oxygen superlattice layers **125** or **125'** therein. In step (b), the regions where the sources **105** or **105'** and drains **106** or **106'** are to be formed may then be etched away to define the nanosheet "fin" and provide pattering for the formation of the STI regions **111**, as well as dummy gate patterning. The respective MST layers **225***a*, **225***b* or **225***a'*, **225***b'* may then be formed on the surface of the substrate **110** or **110'**, and the vertical MST dopant diffusion liners **425***a*, **425***b* or **425***a'*, **425***b'* may be formed on the source or drain side of the SiGe **113** or **113'**, respectively, followed by growth of the source/drain regions **105**, **106** or **105'**, **106'**. In the illustrated example, a doped SiC:P epitaxy may be performed to grow the source and drain regions **105**, **106** or **105'**, **106'**. This may be performed using a cluster tool to perform the etch+ash+clean operations, as well as the epitaxial growth, as will be appreciated by those skilled in the art.

[0067] In step (c) of both process flows **500**, **500'**, the SiGe sacrificial layer **113** or **113'** is removed. However, for the high Vt GAA device **100'**, a high temperature anneal (e.g., 5 s-120 s at 800-1000 C in N_2 or O_2 or UHV) is also performed to cause the oxygen from the MST layers **125'** to diffuse out (i.e., the MST layers are no longer present in the nanosheets **101'**). Further details on annealing to out-diffuse oxygen from an MST layer may be found in U.S. Pat. No. 10,109,479 to Mears et al., which is assigned to the present Applicant and hereby incorporated herein in its entirety by reference. Here again, this processing may also be performed using a cluster tool. Both process flows conclude with the formation of the high K metal gate (HKMG) gate **102** or **102'** in step (d).

[0068] Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included.

1. A method for making a semiconductor gate-all-around (GAA) device comprising:

forming source and drain regions on a semiconductor substrate;

forming a plurality of semiconductor nanostructures extending between the source and drain regions;

forming a gate surrounding the plurality of semiconductor nanostructures in a gate-all-around arrangement; and

forming a dopant diffusion liner adjacent at least one of the source and drain regions and comprising a first superlattice, the first superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

2. The method of claim **1** wherein the dopant diffusion liner comprises respective portions adjacent each of the source and drain regions.

3. The method of claim **1** further comprising forming a second superlattice within at least one of the nanostructures, the second superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

4. The method of claim **1** further comprising forming a third superlattice embedded in the semiconductor substrate extending between the source and drain regions, the third superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

5. The method of claim **1** further comprising forming a fourth superlattice on the semiconductor substrate beneath the source region, the fourth superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

6. The method of claim **1** further comprising forming a fifth superlattice on the semiconductor substrate beneath the drain region, the fifth superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

7. The method of claim **1** wherein the gate comprises a metal.

8. The method of claim **1** wherein the base semiconductor portion comprises silicon.

9. The method of claim **1** wherein the at least one non-semiconductor monolayer comprises oxygen.

10. A method for making a semiconductor gate-all-around (GAA) device comprising:

forming source and drain regions on a semiconductor substrate;

forming a plurality of semiconductor nanostructures extending between the source and drain regions;

forming a gate surrounding the plurality of semiconductor nanostructures in a gate-all-around arrangement;

forming source and drain dopant diffusion liners adjacent respective portions of the source and drain regions and each comprising a first superlattice, the first superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions; and

forming a second superlattice within at least one of the nanostructures, the second superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

11. The method of claim **10** further comprising forming a third superlattice embedded in the semiconductor substrate extending between the source and drain regions, the third superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

12. The method of claim **10** further comprising forming a fourth superlattice on the semiconductor substrate beneath the source region, the fourth superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

13. The method of claim **10** further comprising forming a fifth superlattice on the semiconductor substrate beneath the drain region, the fifth superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

14. The method of claim **10** wherein the gate comprises a metal.

15. A method for making a semiconductor gate-all-around (GAA) device comprising:

forming source and drain regions on a semiconductor substrate;

forming a plurality of semiconductor nanostructures extending between the source and drain regions;

forming a gate surrounding the plurality of semiconductor nanostructures in a gate-all-around arrangement; and

forming a dopant diffusion liner adjacent at least one of the source and drain regions and comprising a first superlattice, the first superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked silicon monolayers defining a base silicon portion, and at least one oxygen monolayer constrained within a crystal lattice of adjacent base silicon portions.

16. The method of claim **15** wherein the dopant diffusion liner comprises respective portions adjacent each of the source and drain regions.

17. The method of claim **15** further comprising forming a second superlattice within at least one of the nanostructures, the second superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base silicon monolayers defining a base semiconductor portion, and at least one oxygen monolayer constrained within a crystal lattice of adjacent base silicon portions.

18. The method of claim **15** further comprising forming a third superlattice embedded in the semiconductor substrate extending between the source and drain regions, the third superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base silicon monolayers defining a base silicon portion, and at least one oxygen monolayer constrained within a crystal lattice of adjacent base silicon portions.

19. The method of claim **15** further comprising forming a fourth superlattice on the semiconductor substrate beneath the source region, the fourth superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base silicon monolayers defining a base silicon portion, and at least one oxygen monolayer constrained within a crystal lattice of adjacent base silicon portions.

20. The method of claim **15** further comprising forming a fifth superlattice on the semiconductor substrate beneath the drain region, the fifth superlattice comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base silicon monolayers defining a base silicon portion, and at least one oxygen monolayer constrained within a crystal lattice of adjacent base silicon portions.

21. The method of claim **15** wherein the gate comprises a metal.

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