United States Patent [19]

Fulton et al.

[11] **3,719,781**

[45] **March 6, 1973**

[54] CONTROL SYSTEM FOR HIGH SPEED PRINTER

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[73] Assignee: **Extel Corporation,** Chicago, Ill.

[22] Filed: **March 19, 1971**

[21] Appl. No.: **126,004**

[52] **U.S. Cl.** **178/30**

[51] **Int. Cl.** **H04l 21/00**

[58] **Field of Search** ..... 178/24, 23 R, 23 A, 25, 26 R, 178/26 A, 30

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[57] **ABSTRACT**

An all-electronic control system for a high-speed dot matrix printer, using a permutation code input signal comprising individual code words each including a fixed number of data pulses preceded by a start pulse. The control system comprises a line relay for receiving the input signal, an input clock triggered by the start pulse in each code word and developing a clock signal at a frequency equal to a predetermined multiple of the input pulse frequency, and an electronic shift register as a buffer store for recording each pulse, in a code word, in sequence as received, on a given count of the clock. The system further comprises an operational store, a load detector for stopping the input clock and transferring recorded data from the buffer store to the operational store whenever the data pulses of a complete code word have been recorded in the buffer store, and operational control means to actuate the printer in accordance with data in the operational store while a further code word is recorded in the buffer store. The operational control means includes a print clock, started upon transfer of data to the operational store, for timing the functions of the printer, including carriage advance or return, print rod actuation, line feed, and others.

16 Claims, 11 Drawing Figures

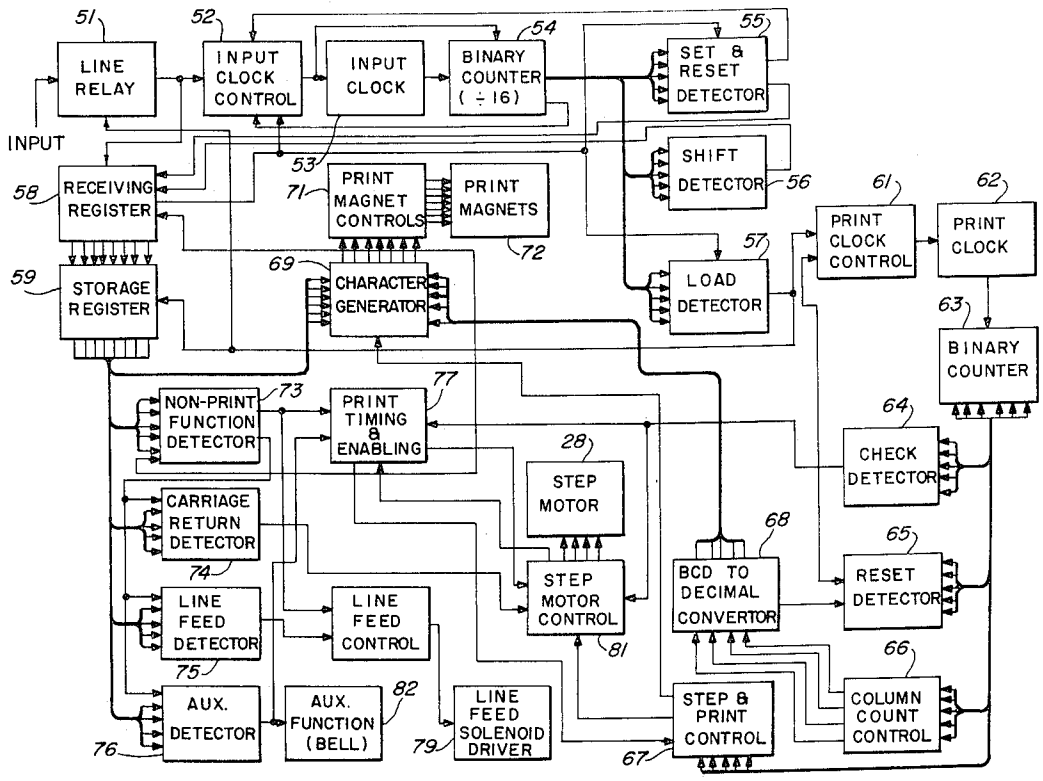

FIG. 1

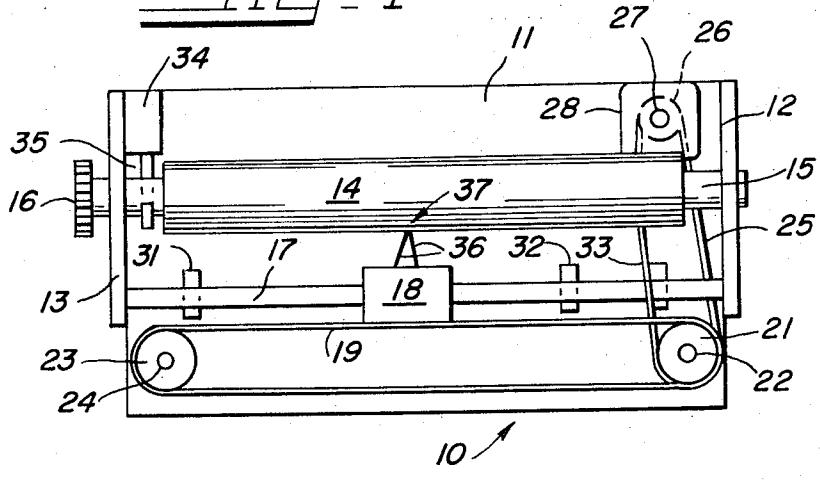

FIG. 2

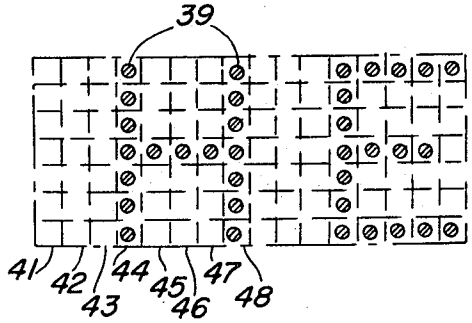

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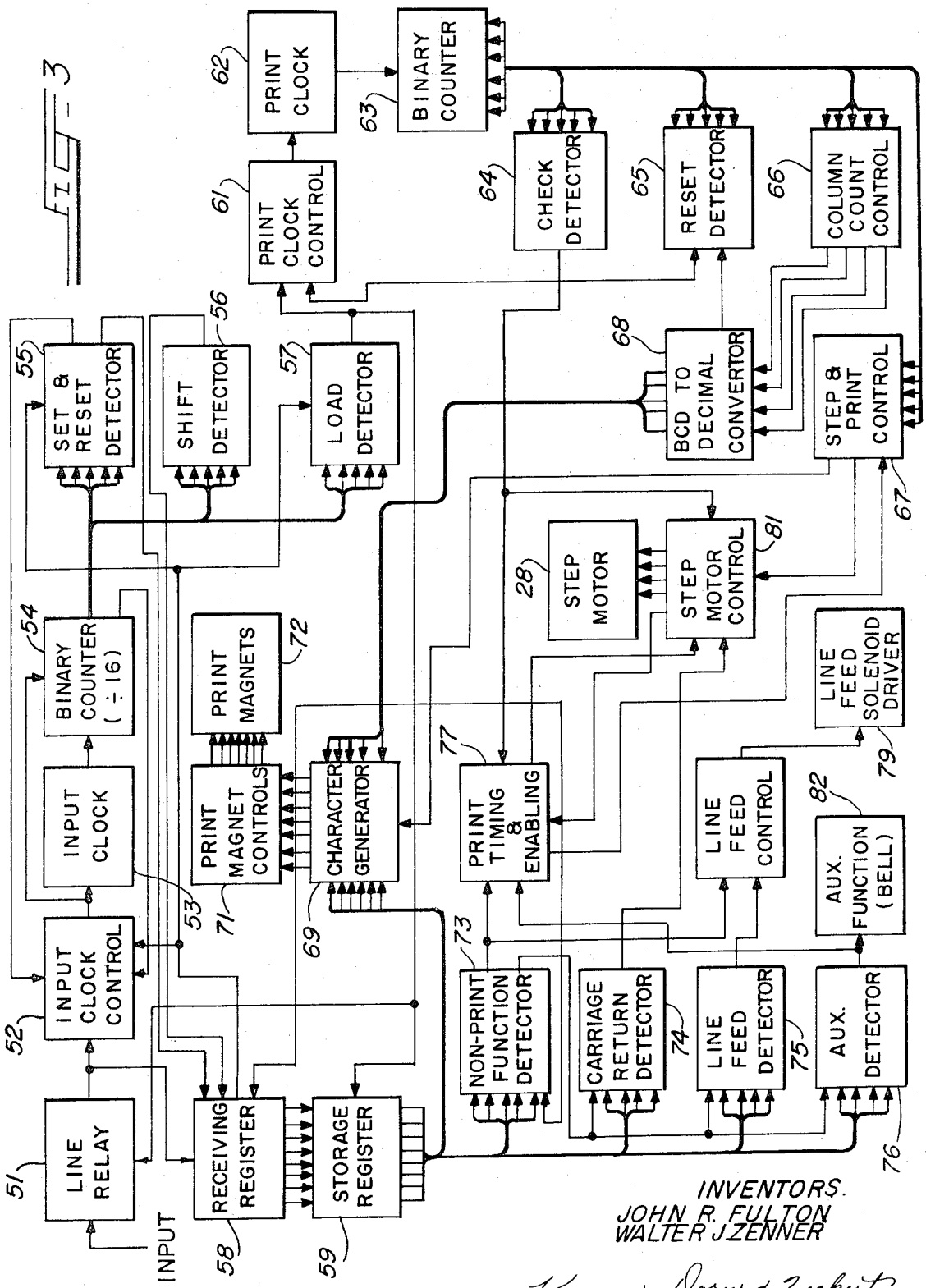
FIG - 3



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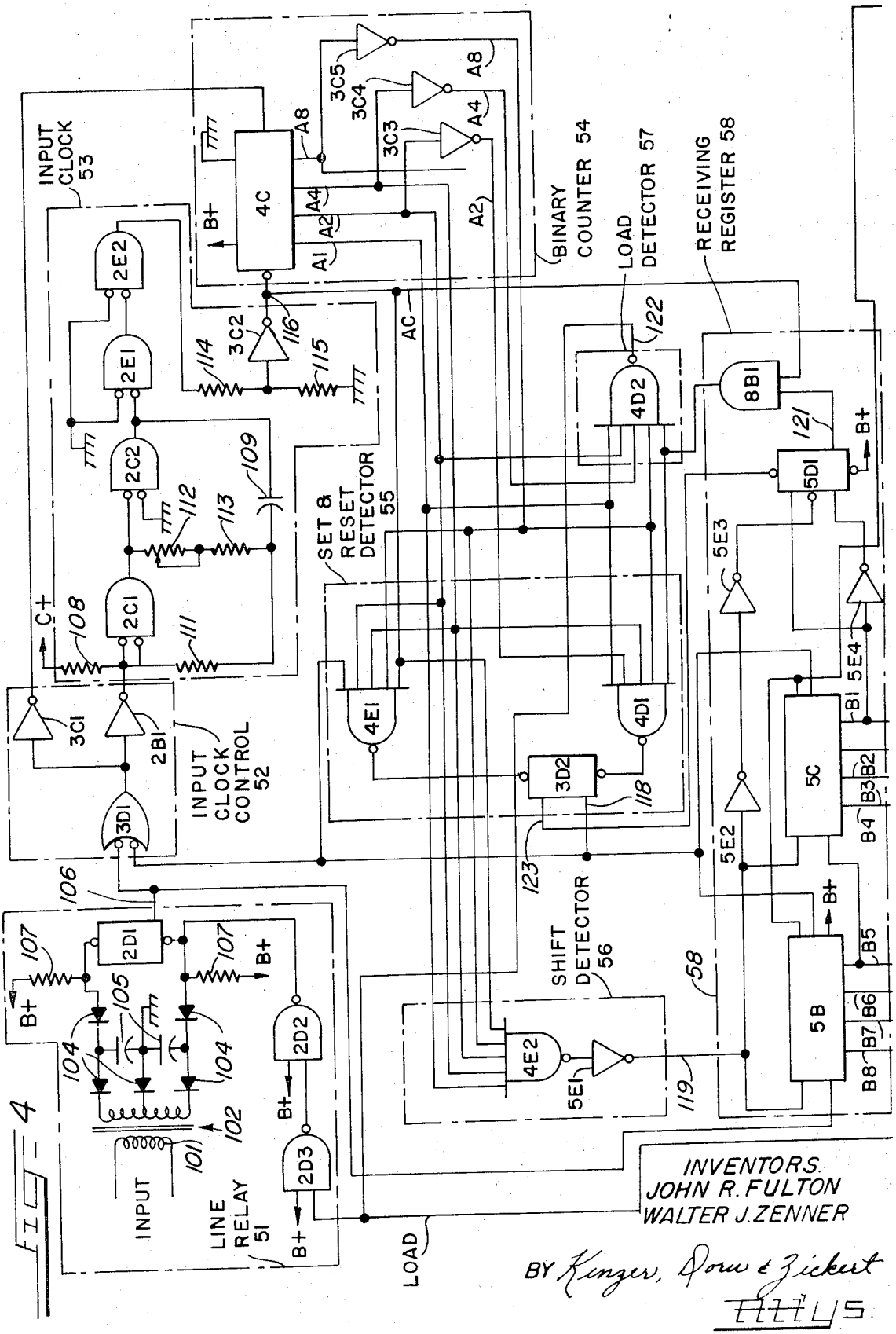

FIG. 4

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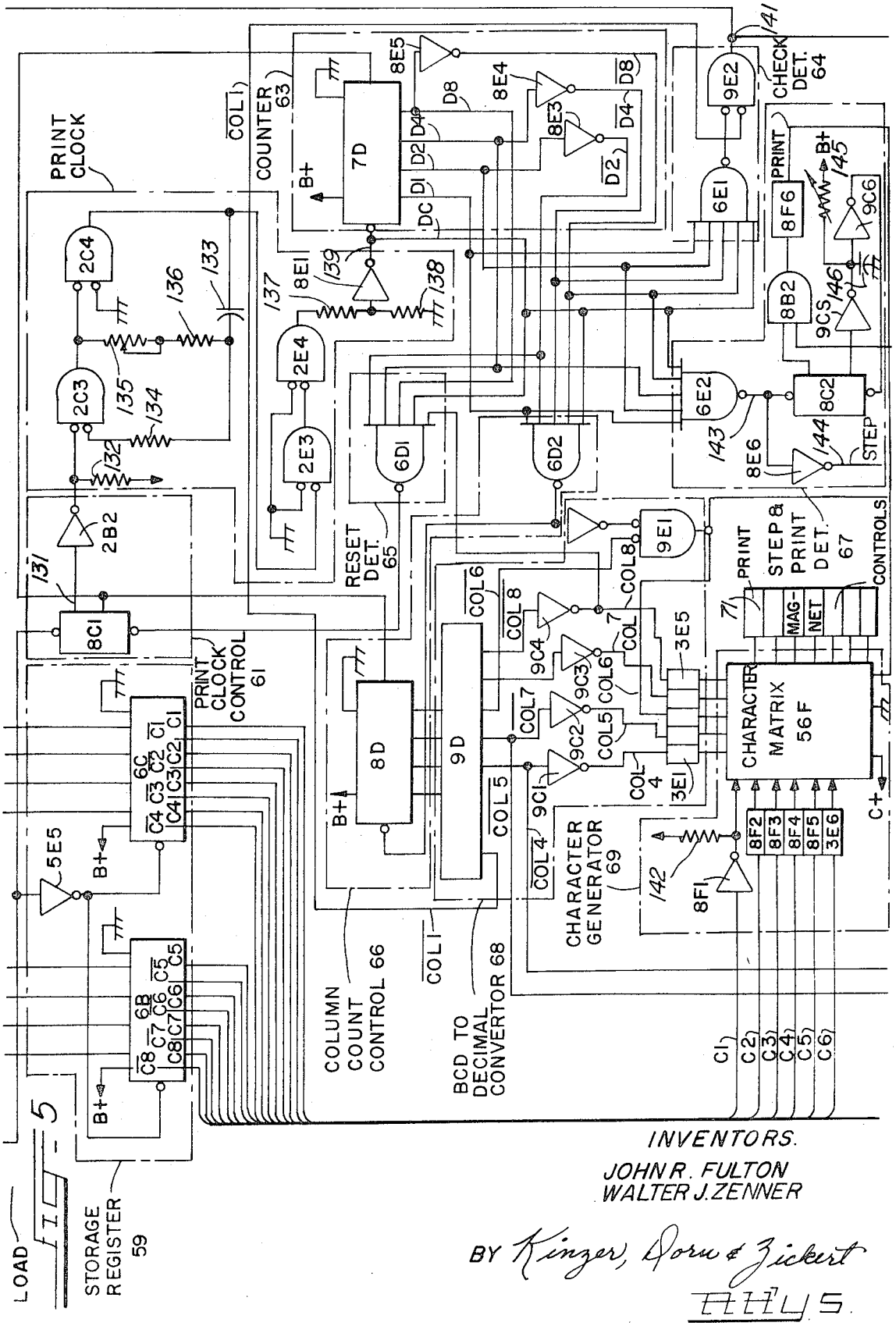

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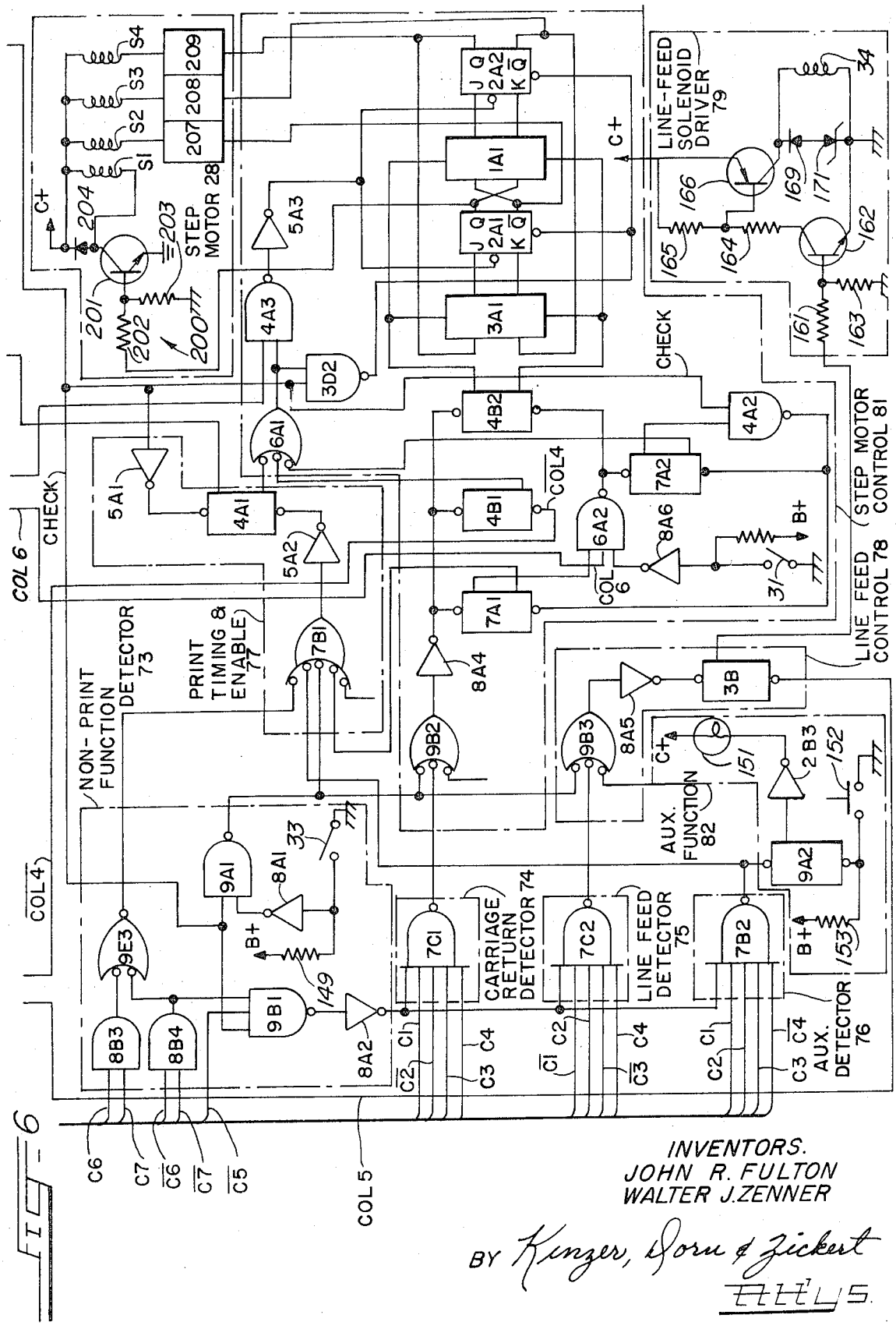

FIG-6

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FIG. 7A

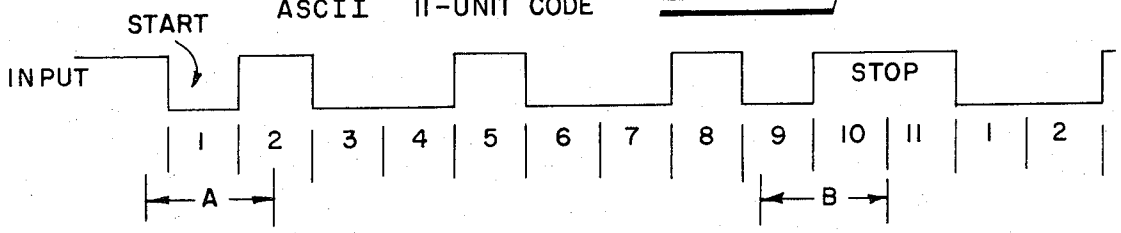

FIG. 7B

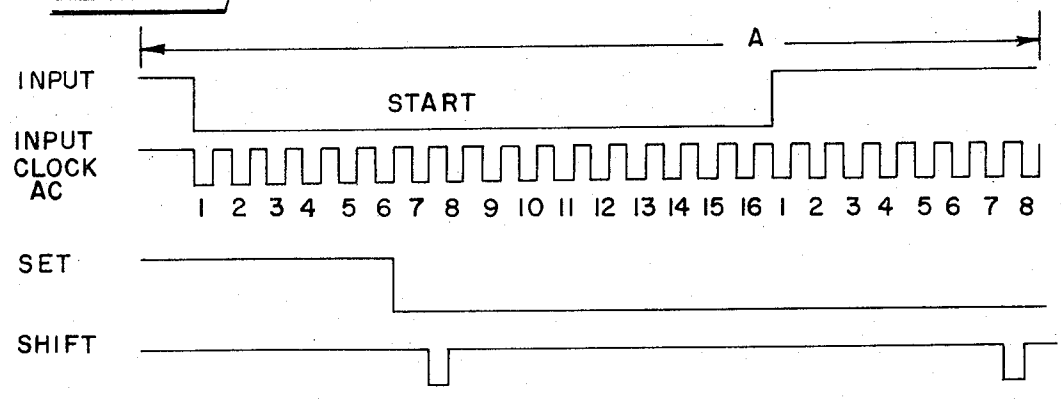

FIG. 7C

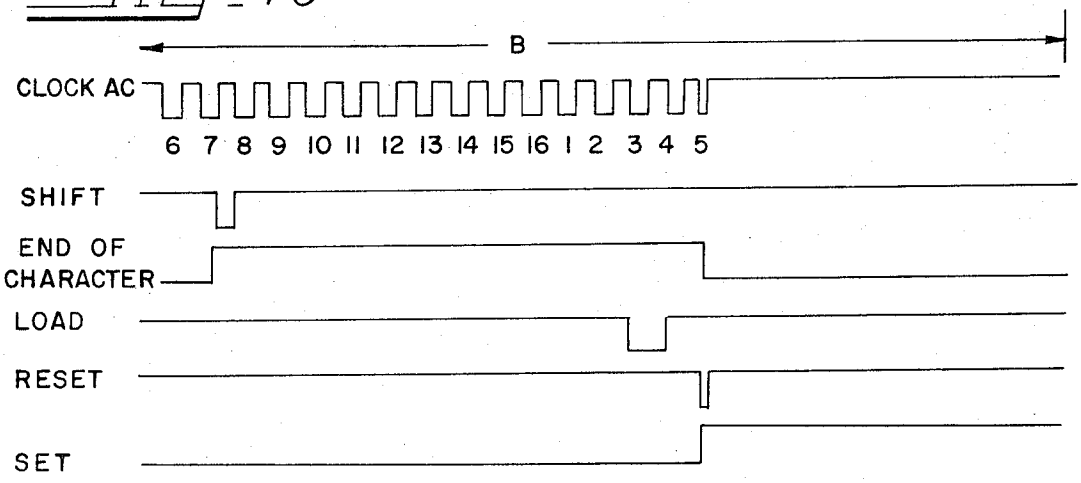

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FIG. 8A

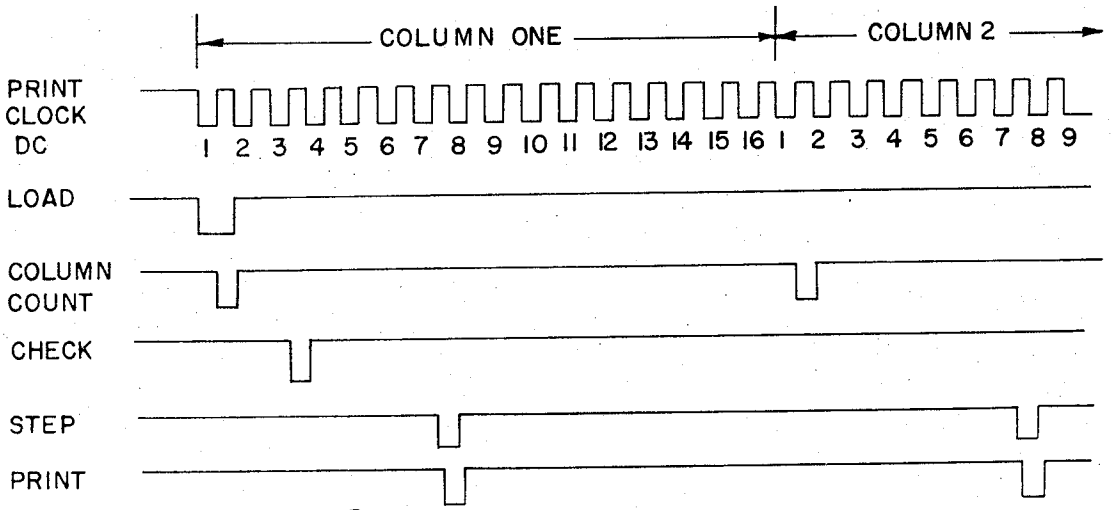
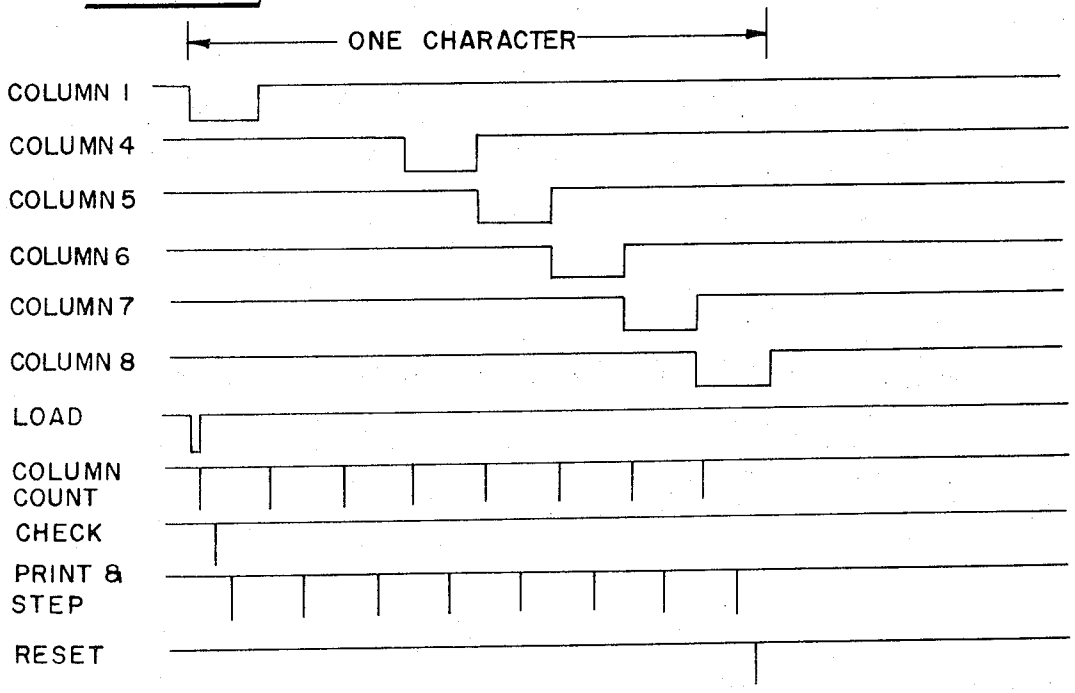


FIG. 8B



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CONTROL SYSTEM FOR HIGH SPEED PRINTER

BACKGROUND OF THE INVENTION

The basic timing for high-speed printers controlled by permutation code input signals, such as the American Standard Code for Information Interchange (ASCII), is established by the received signal. In a dot matrix printer, particularly the kind in which each character is reproduced in a series of individual columns of dots imprinted sequentially, timing of the printer operations is quite critical. Each code word, as received, must be translated into a form usable in control of the printer, and the translated information must be presented to the printer with precise timing and at a speed sufficient to permit multiple functions of the printer mechanism before a new code word is received. Conventional timing controls have not been notably efficient, as applied to dot matrix printers of the sequential kind, leading to continuing difficulties in maintaining accurate reproduction in synchronism with the received signal.

These timing difficulties are also prevalent in connection with non-print functions of the printer, such as carriage return, line feed, and other auxiliary operations. Immediate recognition of a non-print function is essential to accurate operation of the printer; if the printer begins to step through a character-reproduction cycle in response to a non-print function code word, an error of substantial magnitude can result. This is particularly true when the non-print function is one that entails no advance of the printer carriage (line feed, etc.) or even a reverse movement of the carriage. Overprinting, distorted characters, erroneous characters and other errors can easily result from any discrepancies in timing or in code recognition.

SUMMARY OF THE INVENTION

It is a principal object of the invention, therefore, to provide a new and improved timing control for a high-speed dot matrix printer actuated by a conventional permutation code input signal such as the ASCII code.

A specific object of the invention is to provide a dual clock control system, with a buffer store, for a high-speed dot matrix telegraph printer.

Another object of the invention is to afford a new and improved all-electronic "stunt box" for rapid and accurate recognition and control of non-print functions in a high-speed dot matrix telegraph printer.

A further object of the invention is to afford a new and improved all-electronic code converter for converting a received permutation code signal, such as the 11-unit ASCII code, to a form suitable for actuation of a sequential-column dot matrix printer.

An additional object of the invention is to afford a new and improved timing control for a step motor carriage drive in a high-speed dot matrix printer actuated by a permutation code input signal.

Accordingly, the invention relates to an electronic control system for controlling a high-speed dot matrix printer in accordance with a permutation code signal of given pulse rate, in which each code word representative of a character to be printed or of a non-print function contains a fixed number of data pulses preceded by a start pulse. The control system comprises an input circuit, for receiving the permutation code signal, and input clock means, connected to the input circuit. The input clock means generates a clock signal having a frequency equal to a predetermined multiple of the input pulse rate upon receipt of a start pulse by the input circuit. The system includes buffer storage means, comprising a receiving register, having a capacity sufficient to store all data pulses in a code word, connected to the input circuit and to the input clock means, for recording the individual pulses in each code word in sequence, as received, at a given clock count. An operational storage means having a capacity sufficient to store all data pulses in a code word is connected to the buffer storage means. Load means, connected to the storage means and to the input clock means, are provided for transferring recorded data from the buffer storage means to the operational storage means, and for interrupting the input clock means, upon completion of recording of the data pulses of a complete code word in the buffer storage means. Operational control means are provided to actuate the printer to perform a function determined by the data recorded in the operational storage means during the succeeding time interval in which a further code word may be recorded in the buffer storage means. In the preferred construction, the operational control means includes a print timing clock that times the reading and translation of data from the operational storage means, the detection of non-print function codes, and the operation of a step motor that actuates the carriage of the printer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified plan view of a high speed dot matrix printer of the general kind to which the control system of the present invention may be applied;

FIG. 2 illustrates the form of the characters printed by the printer of FIG. 1;

FIG. 3 is a block diagram of a high speed printer control system constructed in accordance with the present invention;

FIGS. 4, 5 and 6, together, constitute a detailed schematic and logic diagram for a preferred form of the control system illustrated in FIG. 3;

FIGS. 7A, 7B and 7C are timing charts illustrating the sequence of operations followed in entering data in the control systems of FIGS. 3-6; and

FIGS. 8A and 8B are timing charts illustrating the sequence of operations followed in a print cycle in the control systems of FIGS. 3–6.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 illustrates, in simplified form, a high speed printing machine 10 in which the control system of the present invention may be employed; the printer 10 produces characters in dot matrix form as shown in FIG. 2. Printer 10 comprises a base 11 with two vertical frame members 12 and 13 affixed to the opposite sides of the base. A platen 14 is incorporated in printer 10 and is mounted upon a shaft 15 that extends between and is journalled in suitable bearings in the two side frame members 12 and 13. A knob 16 may be mounted on one end of shaft 15 to provide for manual rotation of the platen.

A carriage guide rail 17 is mounted at the front end of printer 10, extending transversely of the printer

between frame members 12 and 13 parallel to platen 14. A carriage 18 is mounted upon guide rail 17 and is connected to a carriage positioning belt 19. Preferably, belt 19 is a toothed belt of the kind sometimes referred to as a timing belt or gear belt. The carriage positioning belt 19, at its right-hand end, extends around a drive pulley or sprocket 21 mounted upon a shaft 22 that projects vertically upwardly from base 11. The opposite end of belt 19 engages an idler pulley 23 mounted upon a vertical shaft 24 that projects upwardly from base 11 at the left-hand side of the printer.

Shaft 22 is connected to another pulley, not shown, that is engaged by a drive belt 25. The drive belt 25 extends around a sprocket or drive pulley 26 mounted upon the shaft 27 of a stepping motor 28. Motor 28 is a reversible motor that rotates through a discrete angle of rotation each time an electrical signal pulse is applied to the windings of the motor.

There are three control switches 31, 32 and 33 mounted on base 11 in position to be actuated by engagement with carriage 18. Switch 31 is located at the left-hand side of printer 10 and constitutes a left-hand margin control switch. Switch 33 is located at the right-hand side of the printer and comprises a right-hand margin control switch. Switch 32 is located intermediate switches 31 and 33, but substantially nearer to switch 33, and may be utilized for control of the right-hand margin, during printing operations, for material that has not been grouped in specific line groupings.

Printer 10 also includes a line feed solenoid 34 mounted in the rear left-hand corner of the printer on base 11. Solenoid 34 is connected to a line feed linkage 35, shown as a simple line feed lever, for rotating platen 14 through a discrete angular distance to achieve a line feed operation. In operation, a sheet or web of paper extends around platen 14 and is imprinted by impact from a plurality of printing rods or needles 36 that extend from carriage 18 toward platen 14. In a typical printer, there are seven rods 36 arranged in vertical alignment with each other at the printing station 37 adjacent the surface of platen 14, each provided with an individual drive magnet (not shown).

Printer 10 is, essentially, a simplified illustration of the high speed printer described and claimed in the copending application of Walter J. Zenner and Raymond E. Kranz, Ser. No. 71,051 filed Sept. 10, 1970, now U.S. Pat. No. 3,670,861, to which reference may be made for a more complete and comprehensive description of the mechanical construction and operation of the printer. Details of some of the mechanical linkages in the printer, such as a return spring for return of carriage 18 to the left-hand margin and a clutch to release the carriage drive for return movement, have been omitted as unnecessary for an understanding of the present invention. The preferred construction for carriage 18, including print rods 36 and the print rod magnets, is described and illustrated in detail in the copending application of Messrs. Zenner and Kranz, Ser. No. 85,675, filed Oct. 30, 1970. Only a brief description of the mechanical operation of printer 10 is necessary in this specification.

In the operation of printer 10, as noted above, a sheet or web of impact-sensitive paper is extended around platen 14, between the platen and the print rods 36 of the printer. If preferred, ordinary paper and a carbon ribbon or carbon sheet can be employed. The starting position for carriage 18 is at the left-hand end of its travel on guide 17, in alignment with the left-hand margin switch 31. For the first character to be imprinted, such as the character H illustrated in FIG. 2, carriage 18 advances P discrete steps from left to right, the carriage being driven by its positioning belt 19 through the drive afforded by stepping motor 28, drive belt 25, and pulley 21; in the illustrated embodiment, P = 8. During the first three steps or column movements of carriage 18, no impression is made on the paper. In the next five steps of the carriage, the complete character is imprinted by selective actuation of rods 36 into driving impact with the surface of the paper on platen 14.

As shown in FIG. 2, the initial advancing movement of carriage 18 leaves three blank columns 41, 42 and 43 preceding the first character to be imprinted. In the first character column 44, all seven of the print rods 36 are driven into impact with the paper, producing seven vertical dot impressions 39. On the next incremental step in the advancing movement of carriage 18, only one dot impression 39 is formed, at the fourth or center level. That is, on the fifth step 45 in the formation of the character, only the fourth level print rod 36 is driven into impact with the paper to produce a dot impression. This action is repeated in the next two columns 46 and 47 in the advancing movement of carriage 18. In the eighth and final stage of movement of carriage 18, all seven of the prints rods 36 are again actuated, producing seven dot impressions in the final column 48 for the first character imprinted. This results in formation of the letter H as illustrated in FIG. 2. In this same manner, a complete line of characters is imprinted across the paper on platen 14 with carriage 18 moving from left to right a total of eight steps for each individual character.

As carriage 18 approaches the right-hand end of platen 14, it first engages switch 32. Switch 32 may be utilized to actuate a return mechanism (not shown) to return carriage 18 to the left-hand side of printer 10 and initiate printing of a new line. Under other operational circumstances, discussed more fully hereinafter, carriage 18 may continue its movement until it engages switch 33, at which time the carriage return and line feed mechanisms of printer 10 are mandatorily actuated to return the carriage to the initial line position and to feed the paper. When a new line of print is initiated, solenoid 34 is actuated to rotate platen 14 through one or more feed increments, placing a fresh line segment of the paper web or sheet on the platen in alignment with the carriage and thereby permitting the printing of a subsequent line of characters on the paper.

In the preferred form of printer, the carriage return operation is effected by reverse rotation of motor 28 through a discrete number of steps, which reverse movement operates a spring-return mechanism that performs the necessary carriage return operation. In the carriage drive for the printer described in the aforementioned Zenner and Kranz application, Ser. No. 71,051, the carriage return action is initiated by reverse rotation of motor 28 through four steps, but a different number of reverse rotational steps for initiation of carriage return could be employed if desired.

Ordinarily, each carriage return operation is initiated by a carriage return function code incorporated in a telegraph signal that controls printer **10**. On the other hand, if the telegraph signal does not include carriage return codes suitable to operation of printer **10**, the control system of the present invention can be utilized to effectuate a carriage return operation upon the occurrence of any space code occurring after carriage **18** has actuated switch **32**, thus affording an automatic carriage return and line feed operation. A separate line feed code is utilized to actuate the line feed mechanism comprising solenoid **34** and linkage **35**. Other non-print function codes may be included in the received signal and can be utilized in control of printer **10**.

FIG. **3** illustrates, in block diagram form, a printer control system **50** constructed in accordance with one embodiment of the present invention. The input stage of control system **50** is a line relay circuit **51** to which a conventionally coded telegraph signal is supplied. In the following description, and particularly in connection with the specific circuits illustrated in FIGS. **4–6**, it is assumed that the incoming signal is encoded in accordance with the standard 11-unit ASCII code (see FIG. 7A), but other similar permutation codes can be employed with appropriate modifications in the control system to interpret the input code.

The output of line relay **51** is connected to an input clock control circuit **52**. Clock control circuit **52** is in turn coupled to an input clock **53**. Clock **53** may comprise a start-stop multivibrator or other oscillator of constant frequency. The input clock frequency is taken as n times the pulse rate of the input signal; for the control described herein, $n = 16$. For the ASCII permutation code, which is an 11 unit code comprising one start pulse, eight data pulses, and two stop pulses, the frequency for clock **53** is 1760 hz, assuming an input rate of one hundred words per minute and a pulse rate of 110 pulses per second. The relationship between the input signal and the input clock signal is best shown in FIG. 7B.

The output of clock **53** is applied to a binary counter **54**, which also has an input derived from clock control **52**. Counter **54** is a 16 stage counter and thus cycles once for each pulse in the input signal. The final stage of binary counter **54** is connected back to the input clock control circuit **52**. The outputs from individual stages in the binary counter are connected to a set and reset detector circuit **55**, to a shift detector circuit **56**, and to a load detector circuit **57**. Control circuit **52**, clock **53** and counter **54** are sometimes referred to conjointly as the input clock means.

The output of the input circuit **51** of control system **50** is also connected to a receiving data storage register **58** serving as a buffer storage unit for the control system. Receiving register **58**, comprising an all-electronic shift register, also receives control signals from the set and reset detector **55** and from the shift detector **56**. Another output from the set and reset detector **55** is connected back to the input of clock control circuit **52**.

The individual stages of receiving register **58** are connected in parallel to individual stages in an operational storage means comprising a storage register **59**. A control input to storage register **59** is supplied from load detector **57**. The output of load detector **57** is also connected in a control circuit to line relay **51** and to a print clock control circuit **61**.

The output of the print clock control circuit **61** is connected to a print clock **62** which is in turn connected to a binary counter **63**. The clock control, clock, and counter circuits **61–63** constitute a print clock means essentially similar to circuits **52–54**; however, print clock **62** operates at a different frequency from input clock **53**. The operating frequency for print clock **62** is determined by the printing pulse rate for printer **10** and is made equal to at least n times the printing pulse rate. The printing rate is faster than the incoming signal pulse rate but the print clock frequency is actually lower because the printer requires only eight pulses per character, as described above in connection with FIG. **2**, instead of the 11 pulses per character in the input signal. Thus, the minimum frequency for print clock **62** is **1280** hz; to assure effective operation, a somewhat higher frequency is preferably employed. In a typical installation, the print clock frequency is 1330 hz.

The outputs from the various levels of binary counter **63** are connected to a check signal detector **64**, a reset detector **65**, a column count control circuit **66**, and a step and print control circuit **67**. Detector **64** produces a check signal that is applied to receiving register **58** and to a number of other circuits in control system **50** as described more fully hereinafter. The output of reset detector **65** is connected to the print clock control circuit **61** to reset that circuit at the end of each character code or other code word. The column count control circuit **66** has a plurality of output circuits individually connected to the several stages of a code converter **68** for conversion of the column count signals from binary coded decimal (BCD) form to decimal form. Converter **68** has a plurality of output circuits individually connected to a character generator **69**, and one output connected to reset detector **65**.

Character generator **69** has an input circuit connected to an output of the step and print control circuit **67**. In addition, character generator **69** has a plurality of input circuits that are connected to the individual stages of the operational storage register **59**. Character generator **69** is a commercially available signal translation matrix of integrated circuit construction as identified more fully hereinafter.

Character generator **69** affords seven output circuits, one for each of the printing rods **36** of the high speed printer **10** (FIG. **1**). Each output of character generator **69** is individually connected to one of seven print magnet control circuits **71**. Each print magnet control is in turn connected to an individual magnet or solenoid **72** for actuating one of the print rods **36**.

Of course, there are a number of codes in the input signal to system **50** that apply to printer functions other than the imprinting of individual characters. The occurrence of any of these non-print function codes is identified in a detector **73** having a plurality of inputs connected to the outputs of individual stages in storage register **59**. In addition, separate detector circuits are provided for the specific non-print function codes necessary to operation of the printer. These include a carriage return detector **74**, a line feed detector **75**, and an auxiliary function detector **76**. Each of the individual function code detectors **74**, **75** and **76** is pro-

vided with an input from the non-print function detector **73** as well as a plurality of inputs from individual stages of storage register **59**.

One output from the non-print function detector **73** is connected to a print timing and enabling circuit **77** and to a line feed control circuit **78**. Circuit **78** has a second input derived from the output of the line feed detector **75**. The output of the line feed control circuit **78** is connected to a line feed solenoid driver circuit **79** for energizing the line feed solenoid **34** of the printer (FIG. **1**).

The output of the auxiliary function detector **76**, FIG. **3**, is connected to an auxiliary function circuit **82**, which may comprise a buzzer, a bell, or other auxiliary device. The output of detector **76** is also connected to a second input for the print timing and enabling circuit **77**. The print timing and enabling circuit **77** has one output that is connected to the step and print control **67**. Another output from the enabling circuit **77** is connected to a step motor control circuit **81**. The step motor control circuit **81** has a second input derived from the output of carriage return detector **74** and a third input taken from the output of check detector circuit **64**. The check signal developed in detector **64** is also supplied to the print timing and enabling circuit **77** and to the non-print function detector **73**.

The step motor control circuit **81** has four outputs individually connected to four motor windings in step motor **28**. It is the step motor control **81** that determines the direction of rotation of step motor **28** and that controls the number of steps through which the motor is driven in any given operational sequence.

In considering operation of control system **50**, it should be remembered that the initial pulse in each code word, in the ASCII telegraph signal supplied to line relay **51**, is a start pulse of given polarity (FIG. **7A**), sometimes referred to as a "space" pulse. The next eight pulses in each code word are data pulses identifying a particular character or a specific printer function; these eight data pulses may be "space" pulses or may be "mark" pulses, which are opposite in polarity to the "space" pulses. The final two pulses in the code word are stop pulses; both are "mark" pulses. In the following description, and particularly in connection with the description of FIGS. **4–6**, it is assumed that the "space" pulses in the incoming signal are negative-going signals and that the "mark" pulses are positive-going signals.

OPERATION IN RESPONSE TO A CHARACTER CODE

When a signal transmission to control system **50** is initiated, the first code pulse or baud in the input signal is a "space" signal pulse which actuates line relay **51**, producing an output signal that triggers the input clock control circuit **52** to start input clock **53** in operation. As noted above, clock **53** produces a clock signal at a frequency of sixteen times the pulse rate of the input signal; this clock signal is supplied to binary counter **54**. From the frequency relations given above, and as shown in FIGS. **7A** and **7B**, it can be seen that binary counter **54** produces sixteen output signal pulses during the time interval prior to occurrence of the next pulse in the incoming signal, which may be either a "space" or a "mark" pulse, depending upon the character or function code being transmitted.

When counter **54** reaches a count of six, the set and reset detector **55** is actuated, producing a set signal (FIG. **7B**) that is supplied back to the input clock control **52** (FIG. **3**) to maintain input clock **53** in operation for the full period of time required for receipt of a given character or other code word. That is, the set signal from circuit **55** maintains the input clock means **52–54** in operation until reset upon receipt of all of the data pulses in a complete code word.

When counter **54** reaches a count of seven, shift detector **56** produces a shift pulse (FIG. **7B**) that is supplied to receiving register **58** (FIG. **3**). The shift pulse causes receiving register **58** to record the "space" signal appearing at the output of line relay **51** in the initial stage of the receiving register. When counter **54** reaches a count of sixteen, indicating completion of one pulse of the input signal, the final stage of counter **54** produces an output signal that is supplied to the input clock control **52**; at this time, however, this does not alter the operating condition of the input clock control and the input clock **53** continues to run.

During the second cycle of operation of the input clock means **52–54**, the second input signal pulse is received in line relay **51**. This is the first data pulse; it may be a "mark" signal, as shown in FIG. **7A**, or it may be a "space" signal. At count seven of counter **54**, during this first data signal pulse, a shift signal is again supplied to receiving register **58**. This shifts the initially recorded "space" pulse to the second stage of the receiving register and records the present output of line relay **51** in the first stage of receiving register **58**. This process continues, with the shift detector **56** producing a shift pulse in each cycle and recording the incoming data from line relay **51** sequentially in the individual stages of receiving register **58**.

When the initial "space" pulse that started the transmission reaches the final stage of receiving register **58**, the receiving register produces an end-of-character signal (FIG. **7C**) that is supplied to the set and reset detector **55**, to the load detector **57**, and to the input clock control **52**. This is an enabling signal that conditions the system for subsequent operations.

In the next cycle of the input clock means **52–54** on the count of three in counter **54**, a "load" signal (FIG. **7C**) is developed by load detector **57**. This load signal is supplied to storage register **59** and is utilized to transfer the information that has been recorded in receiving register **58** into the operational storage register **59**. The transfer of data between registers **58** and **59** is accomplished in a single input clock pulse, the transfer being effected on a parallel basis between individual stages of the two registers. The load signal is also applied to line relay **51** to reset the line relay to the mark condition to prevent running of the printer on an "open line" condition.

On the count of five in counter **54**, after a complete set of data pulses for a code word has been stored in receiving register **58**, and transferred to storage register **59**, the set and reset detector **55** develops a reset signal. This reset signal is supplied to input clock control **52** to interrupt operation of input clock **53** until a further code signal is received from line relay **51**. The reset signal is also supplied to receiving register **58** to clear the shift register, recording "mark" bits in all stages of the receiving register in preparation for recording a new character or function code word therein. The

resetting of register **58** also serves to reset the end-of-character circuits in receiving register **58**, so that the enabling signal previously supplied from register **58** to clock control **52** and to detectors **55** and **57** is no longer present.

The output signal from load detector **57**, in addition to the functions described above, is also supplied to print clock control circuit **61** to initiate operation of print clock **62** (see FIGS. **8A**, **8B**). Thus, almost immediately after a complete character or function code has been stored in register **59**, the print clock **62** is started, affording a clock signal for timing all of the operational control circuits **59–82**. The output pulses from print clock **62** are counted in binary counter **63** which, like counter **54**, counts in groups of 16. On each count of one in the input of binary counter **63**, control **66** is actuated to produce a column count signal (FIGS. **8A**, **8B**) that is supplied to converter **68** for conversion from binary coded decimal to decimal notation. For each complete character (or function) code, there are eight pulses in the column count signal (FIG. **8B**).

On each count of three in the output of binary counter **63**, a "check" signal is produced by the detector **64**. This check signal is supplied to receiving register **58** to assure resetting of that register to an all "-marking" condition. The check signal developed by detector **64** is also supplied to the non-print function detector **73**, to the print timing and enabling circuit **77**, and to the step motor control circuit **81**.

As described above, printer **10** uses a total of eight columns for each character, but the first three columns are utilized for spacing between characters and only the last five columns are actually employed for printing. Consequently, only five output signal connections are provided from the BCD-decimal converter **68** to character generator **69**; the signals from the converter are employed in the character generator as column strobe signals. The first column signal output from converter **68** is supplied to column count control **66** for check pulse gating. Additional outputs from converter **68** are available but are not used.

Each stage in storage register **59** is coupled to an individual input for character generator **69**. This information is continuously available to the character generator until new code data is shifted into the storage register by another load pulse from detector **57**. The character generator develops a series of output signals, in response to the column strobe signals from converter **68**, that are utilized to actuate the individual print magnets **72** for the print rods **36** of printer **10**.

When counter **63** reaches a count of seven, near the mid-point of the counter cycle, the step and print control circuit **67** is actuated to develop a "step" signal that is supplied to step motor control **81**. This step signal (FIGS. **8A**, **8B**) is utilized, in control **81**, to develop appropriate drive signals to advance step motor **28** one step. This action occurs once for each of the eight columns entailed in reproduction of a single character. The step and print control **67** also receives a timing signal from the print timing and enabling circuit **77** and develops a "print" pulse timing signal that occurs shortly after the step signal (FIG. **8A**). The print pulse timing signal is supplied to character generator **69** to control timing of energization of the print magnets **72**, so that the print magnets are always energized immediately after step motor **28** has advanced one step.

As noted above, character generator **69** is a commercially available integrated circuit matrix suitable for generating actuating signals in response to the code data signals in storage register **59**, the column count signals from converter **68**, and the print signals from control **67**. In the reproduction of a single character (FIG. **8B**), only the column count signals for columns four through eight (columns **44–48** in FIG. **2**) are supplied to character generator **69**. Upon the receipt of one column count signal pulses, character generator **69** (FIG. **3**) develops from zero to seven actuating signals, depending upon the particular print magnets that are to be energized for each given column of the character being reproduced. These signals are supplied to the individual print magnets **72**, through appropriate drive circuits in the print magnet control **71**, reproducing the desired character as described above in connection with FIGS. **1** and **2**.

After completion of printing of the character, on the occurrence of a count of twelve in the output of binary counter **63** and with a column eight signal available from converter **68**, reset detector **65** is actuated to produce a reset signal that is supplied to print clock control **61**. This effectively stops print clock **62**, readying control system **50** for printing of another character or for any other function dictated by the next code word received by line relay **51**.

OPERATION IN RESPONSE TO A FUNCTION CODE

The initial operation of control system **50** in response to a non-print function code word is basically the same as for a character code word. Thus, the initial "space" pulse at the beginning of the function code word initiates operation of input clock **53**. The code word is stored in receiving register **58**, pulse by pulse, in the same manner as described above, under control of the shift signal from detector **56**. When all data pulses from the complete code word are stored in receiving register **58**, the end-of-character circuits in the receiving register are actuated and initiate the transfer of the complete code data from receiving register **58** to storage register **59**. The load signal from detector **57** that initiates transfer operations between registers **58** and **59** again starts print clock **62** by actuation of control **61**. As before, on count five of binary counter **54**, a reset signal is generated by detector **55** to condition the input circuits for receipt of a new code word.

With print clock **62** in operation, column count control **66** is again actuated to develop a column count signal comprising eight equally spaced pulses (FIG. **8B**). Moreover, when counter **63** reaches a count of three, check detector **64** again develops a check pulse that is supplied to motor control **81** and to the print timing and enabling circuit **77**. The check signal is also applied to the non-print function detector **73**, which identifies the code data now stored in register **59** as pertaining to a non-print function rather than to a character to be imprinted. Thus, detector **73** utilizes the check signal from detector **64** and the data signals stored in register **59** to develop a non-print function signal that is supplied to the print timing and enabling circuit **77**, the line feed control **78**, and each of the several different function detectors **74**, **75** and **76**.

If the data in register **59** constitutes the code for a carriage return operation, detector **74** is actuated to develop a carriage return signal that is supplied to step motor control **81**. The carriage return signal is utilized by control **81** to initiate a reverse stepping movement of motor **28**, where reverse movement of the motor constitutes the mechanical action necessary to begin a carriage return operation in printer **10**. In the preferred form of the control system, motor **28** is stepped four steps in the reverse direction to release carriage **18** and allow it to return to the initial line position at the left-hand side of printer **10**. In this arrangement, the left-hand margin switch **31** is connected to step motor control **81** to step the motor **28** forward four steps and restore the normal driving conditions for carriage **18** once the carriage has reached its initial position at the left-hand side of the printer.

The selection of the number of reverse steps of motor **28** required to initiate a carriage return movement is subject to substantial variation. Three, five, or even eight steps could be utilized for this purpose if desired. On a practical basis, four steps of reverse movement for motor **28** is adequate and effective in relation to the carriage return operation. It will be recognized, of course, that with a different mechanism for carriage return, the output of carriage return detector **74** could be applied to a separate carriage return device as required.

In the event that the data in storage register **59** represents a line feed code, line feed detector **75** is actuated by the output signal from the non-print function detector **73** and by the data signals from register **59**, producing a line feed signal that is supplied to the line feed control **78** together with the non-print function signal from detector **73**. Control **78** supplies an actuating signal to the line feed solenoid driver circuit **79**, energizing solenoid **34** and initiating a line feed operation. During the line feed operation, operation of step motor **28** is inhibited.

If the data stored in register **59** is a separate auxiliary code for a non-print function, it is detected in auxiliary detector circuit **76**. Detector **76** produces an output signal that is supplied to the print timing and enabling circuit **77** to preclude actuation of step motor **28** through control **81**. The output signal from auxiliary detector **76** is also supplied to auxiliary function circuit **82** to ring a bell, sound a buzzer or perform such other auxiliary function as may be required.

For each non-print function code, just as for each character code, column count control **66** is operated and supplies the column count signal to converter **68**. When the column eight stage of converter **68** is actuated, it produces an output signal that is supplied to reset detector **65**. Detector **65** produces a reset signal that is applied to the print clock control **61** to interrupt operation of print clock **62** and thus condition system **50** for the next received code word.

From the foregoing description, it can be seen that each received character or function code is first stored in the buffer register **58** by the distributor circuits comprising the line relay **51**, the input clock means **52–54**, and detectors **55**, **56** and **57**. Once all of the data pulses of a complete character or function code word are stored in register **58**, the data is transferred from the receiving register to storage register **59**. The load signal from detector **57** that initiates the transfer of data between registers **58** and **59** also initiates the next operational phase of system **50**, which may be the printing of a character or may comprise some other machine function. During the time that a character is printed or some other machine function is effected, a further character or function code can be received and stored in the buffer store comprising receiving register **58**. The overall operating cycle for the printing and function circuits of system **50**, controlled by the print clock means **61–63**, is somewhat shorter than the data input cycle controlled by the input clock means **52–54**. Accordingly, printing of a character or accomplishment of another machine function dictated by data in storage register **59** is accomplished before it is necessary to transfer new data into register **59** from receiving register **58**.

SPECIFIC CONTROL CIRCUITS

A specific form of control system is illustrated in detail in FIGS. **4**, **5** and **6**, which fit together vertically with FIG. **4** on top and FIG. **6** on the bottom. The permutation code telegraph signal for controlling printer **10** is applied to the primary winding **101** of an input transformer **102** in line relay **51**. The secondary winding **103** of transformer **102** is connected by a balanced circuit, comprising the diodes **104** and the capacitors **105**, to the inputs of a flip-flop circuit **2D1**. Each input to flip-flop **2D1** is biased to a positive polarity, indicative of a "marking" state, by connection to a B+ supply through a resistor **107**. A start signal (FIG. **7A**) applied to the input winding **101** of transformer **102** induces a negative voltage in the secondary winding **103** that actuates flip-flop **2D1** to cause the output **106** of the flip-flop to go to a "low" or negative-going state.

The low signal from line relay output **106** is supplied to one input of an OR circuit **3D1** in input clock control **52**. This drives the output of OR gate **3D1** positive; the output signal is inverted in an amplifier **2B1** and is applied to one input of an AND gate **2C1** in input clock **53**. This input to AND gate **2C1** is normally biased positive by a connection to a supply C+ through a resistor **108**. The positive-going output from OR gate **3D1** is also inverted in an amplifier **3C1** and is applied to an integrated circuit binary counter **4C** to condition the counter for operation.

In clock **53**, the output of AND gate **2C1** is connected to one input of a second AND gate **2C2**, the other input to gate **2C2** being grounded. The output of gate **2C2** is connected back to the second input of gate **2C1** through a capacitor **109**, in series with a resistor **111**. A potentiometer **112** and a resistor **113** are connected in series from the output of gate **2C1** to the common terminal of capacitor **109** and resistor **111**.

The output of gate **2C2** in clock **53** is connected to one input of an AND gate **2E1** in turn connected to one input of an AND gate **2E2**; the second input to each of gates **2E1** and **2E2** is grounded. The output of AND gate **2E2** is connected to a voltage divider comprising a resistor **114** and a resistor **115** that is returned to ground. The common terminal of resistors **114** and **115** is connected to the input of an inverting amplifier **3C2**. The clock signal AC (FIGS. **7B**, **7C**) appears at the output **116** of amplifier **3C2**.

Binary counter **54**, in addition to the integrated circuit counter **4C**, includes three inverting amplifier **3C3**,

3C4 and 3C5 connected to the outputs A2, A4 and A8, respectively, of circuit 4C. It is thus seen that binary counter 54 affords a total count of 16 and that signals of both polarities are provided for counts of two, four and eight in the output of the binary counter.

When the count in binary counter 54 reaches six, an output signal is developed by an AND gate 4E1 included in the set and reset detector circuit 55 and having input connections from the AC, $\overline{A8}$, A4 and A2 outputs of clock 53 and binary counter 54. This is a negative-going or "low" signal that is supplied to a clock control flip-flop 3D2. This drives the output 118 of flip-flop 3D2 negative, affording a continuing "low" input signal to the OR gate 3D1 in input clock control 52. This is the set signal (FIGS. 7B, 7C) that maintains input clock 53 in operation until all of the data pulses in a complete code word have been received by the control system.

On the seventh count of binary counter 54, the output of an AND gate 4E2 in shift detector 56 is momentarily driven low or negative. The output from AND gate 4E2 is inverted in an amplifier 5E1, producing a shift signal (FIG. 7B) at the output terminal 119 of shift detector 56 (FIG. 4). This shift signal is supplied to one input of each of two four-stage integrated circuit shift registers 5B and 5C. Shift register 5B has four stages B5 through B8, and register 5C has four stages B1 through B4; the B5 stage of circuit 5B is connected to the B4 stage of circuit 5C. Stage B8 of register 5B is connected to the output terminal 106 of line relay 51 so that the initial shift signal from detector 56 records the start pulse (FIG. 7A) from line relay 51 in the first stage of circuit 5B in receiving register 58.

As each succeeding input signal pulse is supplied to line relay 51, FIG. 4, it is recorded in receiving register 58, and more specifically in shift register circuits 5B and 5C, by the shift signals from shift detector 56. Recording of the incoming data always occurs on the seventh pulse from binary counter 54. Each shift pulse also advances previously recorded information from left to right through the shift registers 5B and 5C until the initial information bit, the start pulse, reaches stage B1 of register 5C.

When the start pulse has reached stage B1 in receiving register 58, a "low" signal is supplied from stage B1 to the input of an inverting amplifier 5E4 connected to one input of a flip-flop circuit 5D1. The low signal from stage B1 of register 58 is also supplied directly to another input of flip-flop 5D1. The next succeeding shift pulse is applied to flip-flop circuit 5D1 through a series connected pair of inverting amplifiers 5E2 and 5E3. When this occurs, the output 121 of flip-flop 5D1 develops an enabling signal that is supplied to one input of an enabling AND gate 8B1. The other input to gate 8B1 is derived from the clock output terminal 116 so that, on the next clock pulse, gate 8B1 supplies an enabling signal to load detector 57 and to set and reset detector 55. Thus, flip-flop circuit 5D1, in conjunction with AND gate 8B1, produces the end-of-character signal described above in connection with the simplified system of FIG. 3.

Load detector 57 (FIG. 4) comprises an AND gate 4D2. Once enabled by an output signal from gate 8B1, load detector 57 develops a load signal at its output terminal 122 (FIG. 7C). This load signal is applied to one input of an AND gate 2D3 in line relay 51. The output of AND gate 2D3 is supplied to one input of a further AND gate 2D2 that is in turn connected to one input of the line relay flip-flop 2D1. Thus, the load signal resets line relay 51 to the condition corresponding to a positive or "mark" input, ready for reception of the next permutation code word.

The load signal from output terminal 122 of detector 57 is also connected to the input of an inverting amplifier 5E5 in storage register 59 (FIG. 5). Storage register 59 includes two integrated circuit storage devices 6B and 6C each including four stages; each stage has two output terminals of opposite polarity, identified as outputs C1 through C8 and $\overline{C1}$ through $\overline{C8}$. Each stage of circuit 6B has an input connection from one of the stages B8 through B5 of storage register circuit 5B in receiving register 58. The inputs to the four stages in circuit 6C are derived from stages B4 through B1 of receiving register circuit 5C. The inverted load signal from amplifier 5E5 is applied to each of the storage devices 6B and 6C to transfer recorded data from receiving register 58 to storage register 59.

Referring again to FIG. 4, once the end-of-character enabling signal is available from AND gate 8B1 in receiving register 58, and binary counter 54 reaches a count of five, an AND gate 4D1 in the set and reset detector 55 is actuated to produce a preliminary reset signal that is supplied to flip-flop circuit 3D2. This flops circuit 3D2 back to its original condition, interrupting the "set" signal that had been supplied from terminal 118 to OR gate 3D1 in input clock control 52, and thus effectively interrupts operation of input clock 53. At the same time, the reset signal from terminal 118 is supplied to devices 5B and 5C to condition receiving register 58 for reset to an all "marking" condition. At the same time, an auxiliary reset signal from the other output 123 of flip-flop 3D2 is supplied to flip-flop 5D1 to interrupt the end-of-character signal (see FIG. 7C).

The load signal from detector 57 (FIG. 4) is also applied to one input of a flip-flop circuit 8C1 in the print clock control 61 (FIG. 5). This produces a positive-going output signal, at the output terminal 131 of flip-flop 8C1, that is applied to an inverting amplifier 2B2. The output from amplifier 2B2 is applied to one input of an AND gate 2C3 in print clock 62; this input for AND gate 2C3 is normally biased positive by a connection through a resistor 132 to the C+ supply.

The output of AND gate 2C3 is connected to one input of an AND gate 2C4, the second input to AND gate 2C4 being grounded. The output of AND gate 2C4 is connected back to the second input of AND gate 2C3 by the series combination of a capacitor 133 and a resistor 134. The output of AND gate 2C3 is connected to the common terminal of capacitor 133 and resistor 134 by the series combination of an adjustable resistor 135 and a fixed resistor 136.

The output stage of print clock 62 includes two series-connected AND gates 2E3 and 2E4, each having one grounded input. The output of gate 2E4 is connected to a voltage divider, comprising a resistor 137 in series with a resistor 138, that is returned to ground. The common terminal of the resistors 137 and 138 is connected to the input of an inverting amplifier 8E1. The clock signal DC (FIG. 8A) appears at the output terminal 139 of amplifier 81 (FIG. 5). The clock signal

from terminal 139 is supplied to the input of an integrated circuit binary counter 7D, having four outputs D1, D2, D4 and D8. Circuit 7D is a part of the print clock counter 63, which also includes three inverting amplifiers 8E3, 8E4, and 8E5, having output terminals $\overline{D2}$, $\overline{D4}$ and $\overline{D8}$, respectively.

When a count of one is reached, in counter 63, an AND gate 6D2 in the column count control 66 is actuated and momentarily produces a "low" output signal that is supplied to the input of an integrated circuit counter 8D that is also a part of column count control 66. The output of gate 6D2 is the column count signal (FIGS. 8A and 8B). The several outputs of counter 8D are connected to an integrated circuit decoder 9D that has individual outputs for each of eight columns; however, only the column outputs $\overline{COL\ 1}$ and $\overline{COL\ 4}$ through $\overline{COL\ 8}$ are used. The output signals from decoder 9D, which is a part of the converter 68, are individual column signals, but require inversion in polarity. Thus, converter 68 includes four inverting amplifiers 9C1 through 9C4 that develop the column signals for columns four, five, seven and eight. The COL 6 signal is developed by an AND gate 9E1 that has one input connection from the $\overline{COL\ 6}$ output of decoder 9D and another input connection from gate 6D2 through an inverter 8E2. The column signals for columns four through eight are supplied to a matrix 56F in character generator 69 through individual drive circuits 3E1 through 3E5.

The $\overline{COL\ 1}$ output from decoder 9D is connected to one input of an AND gate 9E2 incorporated in check detector 64 (FIG. 5). The other input to AND gate 9E2 is taken from the output of an AND gate 6E1 that is connected to the appropriate outputs of counter 63 indicative of a print clock count of three. The signal at the output terminal 141 of gate 9E2 is the "check" signal described above and shown in FIGS. 8A and 8B. This check signal is fed back to shift registers 5B and 5C to reset the receiving register 58 for recording of a subsequent code word.

The outputs C1 through C6 from storage register 59 are individually connected to matrix 56F in character generator 69 through separate interface circuits employed to maintain fixed voltage levels at the matrix inputs. The C1 input connection to the character generator matrix is shown in detail and comprises an inverter amplifier 8F1 with a bias connection to the C+ supply through a resistor 142. This circuit is typical of the construction used for the interface circuits 8F2, 8F3, 8F4, 8F5 and 3E6 employed for the data inputs C2 through C6. The interface circuit illustrated for the C1 input is also the same as those used for the column signal inputs, circuits 3E1 through 3E5. The inputs to matrix 56F from storage register 59 remain constant until new data is transferred into the storage register from receiving register 58 by a new load pulse from load detector 57.

When counter 63 reaches a count of seven, an AND gate 6E2 is actuated in detector 67, producing a step output signal at its output terminal 143. This step signal (see FIGS. 8A and 8B) is applied to the input of an inverting amplifier 8E6 having its output terminal 144 connected to the step motor control 81. The step signal is also applied to one input of a flip-flop circuit 8C2 that is utilized to develop a print timing signal. One of the outputs of flip-flop circuit 8C2 is connected to the input of an inverting amplifier 9C5. The output of amplifier 9C5 is connected to a timing circuit comprising a resistor 145 that is connected to the B+ supply and a capacitor 146 that is returned to ground. The timing circuit is connected to the input of an inverting amplifier 9C6 that is connected back to another input of flip-flop circuit 8C2 to reset the flip-flop circuit after a predetermined time.

The other output of the print pulse timing flip-flop 8C2 is connected to one input of an AND circuit 8B2 having a second input derived from the print timing and enabling circuit 77 (FIG. 6). As shown in FIG. 5, the output from AND gate 8B2 is connected through an interface circuit 8F6 to the matrix 56F in character generator 69. This is a print signal that enables operation of the character generator, but inhibits printing during non-print functions such as a carriage return, line feed, or the like.

The electronic "stunt box" comprising the non-print function detector 73, shown in FIG. 6, includes an AND gate 8B3 that determines when both of the outputs C6 and C7 of storage register 59 are marking pulses. Detector 73 also includes an AND gate 8B4 that identifies the occurrence of space pulses in both the sixth and seventh code levels for the data storage in storage register 59. Either of these conditions indicates the occurrence of a non-print function in the ASCII code. The outputs of both AND gates 8B3 and 8B4 are connected to an OR gate 9E3 that supplies a non-print output signal to the print timing and enabling circuit 77.

In the non-print function detector 73, the check signal from check detector 64 (FIG. 5) is connected to one input of each of two AND gates 9A1 and 9B1. The second input to gate 9A1 is connected to the output of an amplifier 8A1. The input for amplifier 8A1 is connected to the right-hand margin switch 33, the switch 33 being returned to ground. A resistor 149 connected from the B+ supply to the input of amplifier 8A1 normally biases the amplifier off. The closing of switch 33 produces an output signal from gate 9A1, coincident with the check signal, that is supplied to the print timing and enabling circuit 77 to the line feed control 78.

In the non-print function detector 73, AND gate 9B1 receives additional input signals from the $\overline{C5}$ output of storage register 59 and from the output of AND gate 8B4. An output from gate 9B1 signifies the occurrence of a carriage return, a line feed, or other non-print function; this signal is supplied to the detectors 74, 75 and 76 through an inverter amplifier 8A2. Gate 8B4 in detector 73 senses all of the control functions that are actually used by the printer 10; additional unused codes are rejected by gate 9B1 through use of the $\overline{C5}$ connection. Because the output from AND gate 9B1 occurs in coincidence with the check pulse, there is sufficient time for the function detectors 74–76 to operate their respective controls before carriage advance or printing are initiated.

In FIG. 6, the auxiliary detector 76 comprises a single AND gate 7B2 that detects the auxiliary function code word when stored in register 59, and produces an output signal to actuate a flip-flop circuit 9A2 in the auxiliary function device 82. The output of flip-flop circuit 9A2, including an amplifier 2B3, may be used to

energize a lamp **151**, to actuate a buzzer, or for other control purposes. A separate actuation circuit comprising a switch **152** and a resistor **153** may be utilized to reset flip-flop **9A2** and turn off the lamp or the buzzer.

In the circuit of FIG. **6**, the line feed detector **75** comprises an AND gate **7C2** that is responsive to a line feed code word stored in register **59**. The output signal from line feed detector **75** is applied to a line feed flip-flop **3B** through the series combination of an OR gate **9B3** and an inverting amplifier **8A5**. The circuits **9B3**, **8A5**, and **3B** constitute the line feed control **78**. A line feed signal is supplied from flip-flop **3B** to the line feed solenoid drive circuit **79**. The resetting of flip-flop **3B** is accomplished by the $\overline{\text{COL 5}}$ signal from circuit **9D** in converter **68** (FIG. **5**).

The line feed solenoid drive circuit **79** (FIG. **6**) comprises a series input resistor **161** connected to the base of a transistor **162**. The base of transistor **162** is also connected to a resistor **163** that is returned to ground. The emitter of transistor **162** is grounded. The collector of transistor **162** is connected to a load resistor **164** that is in turn connected to a resistor **165** which is connected to the C+ supply.

The common terminal of the resistors **164** and **165** is connected to the base of a transistor **166**. The emitter of transistor **166** is connected to the C+ supply. The collector of transistor **166** is connected to one terminal of the line feed solenoid **34**. The other terminal of solenoid **34** is connected to ground. A diode **169** and a zener diode **171** are connected in series from the collector of transistor **166** to ground.

The specific circuit shown for the line feed solenoid driver **79** affords an efficient and inexpensive drive for the solenoid. Essentially identical circuits can be used for the individual print magnet controls **71** (FIGS. **3** and **5**).

In FIG. **6**, the input to the print timing and enabling circuit **77** is an OR circuit **7B1** having several different input connections. Thus, one input to OR gate **7B1** is taken from gate **9E3** in the non-print function detector **73**. Another input to gate **7B1** is derived from gate **9A1** in detector **73**. A third input to gate **7B1** is taken from the AND gate **7B2** in auxiliary detector **76**. A fourth input to OR gate **7B1** is derived from a flip-flop **7A1** in the step motor control **81**. Any one of these inputs is indicative of a condition in which the function required of printer **10** is a non-print operation so that printing should be inhibited.

The output of OR gate **7B1** is supplied to a flip-flop **4A1** through an inverting amplifier **5A2**. Flip-flop **4A1** also has a second input, the check signal, applied to the flip-flop through an inverting amplifier **5A1**. One output of flip-flop **4A1** is connected back to AND gate **8B2** in the step and print circuit **67** (FIG. **5**) to inhibit the print signal supplied to character generator **69**. The other output of flip-flop **4A1** is connected to an OR gate **6A1** in the step motor control **81**.

Carriage return detector **74**, in the circuit of FIG. **6**, comprises an AND gate **7C1** that develops an output signal in time coincidence with the check pulse whenever a carriage return code word is stored in storage register **59**. This carriage return signal is supplied to an OR gate **9B2** in the step motor control **81**. The OR gate **9B2** also receives a non-print function signal from the output of gate **9A1** in detector **73**. The carriage return signal is applied, through gate **9B2** and an amplifier **8A4**, to one input of flip-flop circuit **7A1**.

As shown in FIG. **6**, step motor **28** comprises four individual field windings **S1**, **S2**, **S3** and **S4**. The energizing circuit **200** for winding **S1** comprises a transistor **201** having its base electrode connected to a series input resistor **202** and returned to ground through a shunt resistor **203**. The emitter of transistor **201** is connected to system ground and the collector is connected to the C+ supply through a diode **204**. The collector of transistor **201** is also connected to one terminal of motor winding **S1**. The other terminal of the motor winding is returned to the C+ supply. The energizing circuits **207**, **208** and **209** for windings **S2**, **S3** and **S4**, respectively, are the same construction as illustrated in drive circuit **200**.

In the step motor control **81**, the basic sequencing control for energization of motor windings **S1-S4** comprises a pair of conventional J-K flip-flop circuits **2A1** and **2A2**, each equipped with a clearing input as well as a central clock input. The Q output of flip-flop **2A1** is connected to the input resistor **202** in the drive circuit **200** for motor winding **S1**. The Q output of flip-flop **2A2** is similarly connected to the drive circuit **207** for the motor winding **S2**. The $\overline{Q}$ output of flip-flop **2A2** is connected to the drive circuit **208** for motor winding **S3** and the $\overline{Q}$ output of flip-flop **2A1** actuates the drive circuit **209** for motor winding **S4**. The Q output of flip-flop **2A2** is connected in a feedback circuit to the J input of flip-flop **2A1**, with an AND-OR-INVERT gate **3A1** interposed in the feedback circuit. Similarly, the $\overline{Q}$ output of flip-flop **2A2** is connected in a feedback circuit to the K input of flip-flop **2A1**, through gate **3A1**. There is also a feedback circuit from the Q output of flip-flop **2A1** to the K input of flip-flop **2A2**, through an AND-OR-INVERT gate **1A1**, with another feedback connection from the $\overline{Q}$ output of flip-flop **2A1** to the J input of flip-flop **2A2** through gate **1A1**.

In the normal operation of step motor **28**, in reproducing a printed character or in forming a blank space in a line of print, the step signal from step and print circuit **67** (FIG. **5**) is supplied to the clock inputs of both of the flip-flops **2A1** and **2A2** through an AND gate **4A3** and an inverting amplifier **5A3**. Gate **4A3** is normally enabled by a second signal from the OR gate **6A1**, in turn actuated by an enabling signal from flip-flop **4A1** in circuit **77**. The step pulses actuate flip-flop circuits **2A1** and **2A2** to energize motor windings **S1** through **S4** in the following sequence:

FORWARD STEPPING SEQUENCE

	Motor Windings			
Step Pulse	S1	S2	S3	S4
1	0	1	1	0
2	0	1	0	1
3	1	0	0	1
4	1	0	1	0
5	0	1	1	0
6	0	1	0	1
7	1	0	0	1
8	1	0	1	0

As described above, there are a total of eight column steps through which motor **28** must move the printer carriage in the reproduction of each character (FIG. **2**). Following the eighth step signal, print clock **62** is interrupted in its operation by reset detector **65**, comprising gate **6D1** (FIG. **5**); accordingly, no more step

signals are generated and the stepping of motor **28** in a forward direction ceases. At the beginning of the next operational cycle, the check signal from check detector **64** (FIG. **5**) is supplied to a reset gate **3D2** in motor control **81** (FIG. **6**) in coincidence with an enabling signal from gate **6A1**. This reset signal is supplied to the clearing inputs of each of the two flip-flop circuits **2A1** and **2A2**, resetting the two flip-flops to the operating conditions required for the beginning of the forward stepping sequence in the preceding table. This reset arrangement also assures correct operational states for the two flip-flops **2A1** and **2A2** when the printer and its control system are first placed in operation.

On a carriage return operation, as indicated above, stepping motor **28** is first stepped in a reverse direction through a predetermined number of steps. The recording of a carriage return code word in operational storage means **59** is detected by the non-print function detector **73**. The non-print function signal from detector **73** is utilized, in circuits **7B1** and **5A2**, to develop an actuating signal that triggers flip-flop circuit **4A1** to cut off the normal enabling signal to the input OR gate **6A1** in motor control **81**. Upon occurrence of the check signal, however, the carriage return code is detected by detector **74**. This produces a carriage return signal that is supplied to OR gate **9B2** and amplified in inverter **8A4**, flipping each of three flip-flop circuits **7A1**, **4B1** and **4B2**. The actuation of flip-flop **7A1** results in the application of a continuing inhibit signal to the OR gate **7B1** in the print timing and enabling circuit **77**, effectively maintaining flip-flop circuit **4A1** in the desired operating condition for non-print functions. Circuit **7A1** also supplies an enabling signal to an AND gate **6A2** for subsequent use.

The actuation of flip-flop circuit **4B1** causes that circuit to supply an output signal to OR gate **6A1** to again enable AND gates **3D2** and **4A3**. Thus, the step motor control **81** is conditioned for reception of stepping signals and for the utilization of those signals in actuation of motor **28**, even though a non-print function (carriage return) is entailed. The triggering of flip-flop **4B2** to its alternate condition, on the other hand, results in the application of actuating signals to the inverting AND-OR gates **3A1** and **1A1** to reverse the feedback connections for the two flip-flops **2A1** and **2A2** that control energization of the windings in step motor **28**. As a consequence, on the step pulses that are subsequently received from detector **67** (FIG. **5**) during the carriage return cycle, the stepping motor **28** (FIG. **6**) is actuated to step in a reverse direction in accordance with the following sequence:

CHARACTER RETURN STEPPING

	Motor Windings			
Step Pulse	S1	S2	S3	S4
1	0	1	1	0
2	1	0	1	0
3	1	0	0	1
4	0	1	0	1

The column count proceeds as described above, during a carriage return cycle. At a column count of four, the column count signal $\overline{\text{COL 4}}$ is supplied to flip-flop circuit **4B1** (FIG. **6**) and returns that circuit to its original operating condition. This cuts off the enabling signal to gate **6A1** and interrupts the stepping movement of motor **28**. The particular column count used to actuate circuit **4B1** can be varied, depending upon the mechanical inertia of the printer and similar factors; ordinarily, three to five reverse steps for motor **28** will be sufficient to actuate the carriage return mechanism and release the carriage to return to its starting position at the left-hand side of the printer.

When the carriage is returned to its original position, switch **31** is closed, supplying an input signal to an amplifier **8A6** that is connected to one input of AND circuit **6A2**. On the next count of column **6**, either during the carriage return cycle or in a following line feed cycle, gate **6A2** is fully enabled and produces an output signal that resets flip-flop circuit **4B2**, again conditioning the step motor control **81** for forward stepping movement of motor **28**. The output signal from gate **6A2** also flips a flip-flop circuit **7A2**. This applies an enabling signal to an AND gate **4A2**. In the next print cycle or other function cycle of the control, upon occurrence of the check signal, gate **4A2** produces an output signal that resets both of the flip-flop circuits **7A1** and **7A2**. This completes the restoration of the step motor control **81** to the operating condition necessary for printing another character.

In the timing of operations of control system **50**, certain characteristics should be maintained. The sampling of the input signal, controlled by shift detector **56**, should be timed as nearly as possible to the middle of every incoming signal pulse. Thus, the shift signal should occur approximately at a count of $n/2$ of the input clock signal. The same relation should be observed with respect to the step and print operations, which are preferably timed at a count of approximately $n/2$ for the print clock. A slight advance of the count is often desirable, as shown in FIGS. **7** and **8**. Precise timing of the system assures accurate and complete printing of the incoming data.

The buffer storage afforded by control system **50**, in conjunction with the precision timing incorporated therein, allows high-speed operation with an accurate print out in an all-electronic control. There is no need to store more than one code word at a time; on the other hand, the buffer store can be expanded to two or more words if necessary, as in a printer having a relatively long carriage-return or other non-print cycle. The all-electronic stunt box of the system effectively precludes errors and misprints on non-character code words. The step motor control, with its positive-acting flip-flop circuits, allows both forward and reverse movement with no loss of control.

In order to afford a more complete example of the invention, specific circuit parameters for much of FIGS. **4–6** are presented below; it should be understood that this information is presented solely by way of illustration and in no sense as a limitation on the invention.

Integrated Circuits

Number	Type
1A, 3A	7451
2A	74107
2B, 3C, 3E, 5E, 8A, 8E, 8F, 9C	7405
2C, 2E	CD4001D
2D, 3B, 3D, 4A, 4B, 7A, 8C, 9A	7400
4C, 7D, 8D	7493
4D, 4E, 6D, 6E, 7B, 7C	1800
5B, 5C	7495
5D	7472
6A, 9B	7410
6B, 6C	7475

9D	7442
9E	7402

Other Semiconductor Devices

Transistor **162, 201**	T1592
Transistor **166**	TIP32A
Diode **169**	1N4001
Diode **171**	1N5250
Diode **204**	1N914
Other diodes	

Capacitors

105	0.033 microfarads
109	510 microfarads
133	470 microfarads
146	20 microfarads

Resistors

107, 108, 132, 142	2.7 kilohms
111, 134	1 megohm
112	25 kilohms
113	487 kilohms
114, 137	2.2 kilohms
115, 138, 202	620 ohms
135	50 kilohms
136	688 kilohms
149	10 kilohms
161	7.5 kilohms
163	22 kilohms
164	68 ohms
165, 203	4.7 kilohms

Operating Voltages

B+	5 volts D.C.
C+	14 volts D.C.

We claim:

1. An all-electronic control system for controlling a high-speed dot matrix printer in accordance with a permutation code signal of given pulse rate in which each code word representative of a character or of a non-print function includes a start pulse followed by a given fixed number of data pulses, comprising:

an input circuit for receiving said permutation code signal;

input clock means, connected to said input circuit, for generating an input clock signal having a frequency equal to a predetermined multiple of n times said pulse rate upon receipt of a start pulse by said input circuit;

buffer storage means, comprising a receiving register having a capacity sufficient to store all data pulses in a code word, connected to said input circuit;

shift means, connected to said input clock means, for recording the individual pulses in each code word in said buffer storage means in sequence, as received, at a given clock count;

operational storage means, having a capacity sufficient to store all data pulses in a code word, connected to said buffer storage means;

load means, connected to said storage means and to said input clock means, for applying a load signal to said storage means to transfer recorded data from said buffer storage means to said operational storage means, at a given clock count, upon completion of recording of the data pulses of a complete code word in said buffer storage means; and

operational control means, actuated by said load means, for actuating said printer to perform a function determined by data recorded in said operational storage means during a time interval shorter than that required to record a further code word in said buffer storage means, said operational control means comprising:

print clock means, actuated by said load signal, for generating a print clock signal having a frequency equal to a predetermined multiple of n times the printing rate of said printer;

a step motor for stepping a dot matrix carriage through a predetermined number of column steps in reproducing each printed character;

a step motor control for said step motor;

a character generator connected to said operational storage means;

step and print control means, connected to said print clock means, said step motor control, and said character generator, for actuating said step motor and said character generator, in timed relation to each other, at a print clock count of approximately $n/2$;

print reset means for interrupting operation of said print clock means upon completion of a time interval corresponding to a complete character reproduction cycle; and

column signal generating means, connected to said print clock means, for generating a series of distinct column signals and for applying said column signals to said character generator in sequence, to actuate a corresponding series of separate stages in said character generator, corresponding to different print columns, in the reproduction of each character.

2. A control system for a high-speed dot matrix printer, according to claim **1**, in which said shift means operates on an input clock count of approximately $n/2$, and in which said load means operates on an input clock count substantially smaller than $n/2$.

3. A control system for a high-speed dot matrix printer, according to claim **2**, and further comprising input reset means, connected to said load means and to said input clock means, for applying an input reset signal to said input clock means to interrupt said input clock means after occurrence of said load signal and on an input clock count of less than $n/2$.

4. A control system for a high-speed dot matrix printer, according to claim **3**, in which said input reset signal is applied to said buffer storage means to condition said buffer storage means for recording of a new code word.

5. A control system for a high-speed dot matrix printer, according to claim **1**, in which said column signal generating means comprises a column counter of several stages, connected to said print clock means, and a BCD-decimal converter connected to said column counter.

6. A control system for a high-speed dot matrix printer, according to claim **1**, in which said operational control means further comprises:

a non-print function detector, coupled to said operational storage means, for generating a non-print control signal upon recording of a non-print code word in said operational storage means;

and print enabling means for utilizing said non-print control signal to inhibit operation of said character generator for a non-print code word.

7. A control system for a high-speed dot matrix printer, according to claim **6**, in which said non-print control signal is also utilized by said enabling means to inhibit normal column stepping operation of said motor in response to a non-print code word.

8. A control system for a high-speed dot matrix printer, according to claim **6**, in which said operational control means further comprises:

a plurality of individual function detectors, each connected to said non-print function detector and to said operational storage means, for detecting specific printer functions; and

check means, connected to said print clock means, for developing a check signal at a given print clock count of less than $n/2$, and for applying said check signal to said individual function detectors to actuate the same.

9. A control system for a high-speed dot matrix printer, according to claim **8**, in which said check signal is also applied to said buffer storage means to reset said buffer storage means for recording a new code word.

10. An all-electronic control system for controlling a high-speed dot matrix printer for operation at a given printing pulse rate in accordance with a permutation code signal in which each code word representative of a character or of a non-print function includes a start pulse followed by a fixed number of data pulses, comprising:

operational storage means having a capacity sufficient to store all data pulses in a code word;

input means for recording the data pulses of each received code word of said permutation code signal in said operational storage means;

load means, included in said input means, for developing a load signal indicative of recording of a code word in said operational storage means;

print clock means, actuated by said load signal, for generating a print clock signal having a frequency equal to a predetermined multiple of n times said printing pulse rate;

a step motor for stepping a dot matrix carriage through a predetermined number of column steps in reproducing each printed character;

a step motor control for said step motor;

a character generator connected to said operational storage means;

step and print control means, connected to said print clock means, said step motor control, and said character generator, for generating a step signal actuating said step motor and said character generator, in timed relation to each other, at a print clock count of approximately $n/2$;

column signal generating means, connected to said print clock means, for generating a series of distinct column signals and for applying said column signals to said character generator, in sequence, to actuate a corresponding series of separate stages in said character generator, corresponding to different print columns, in the reproduction of each character, and

reset means for interrupting operation of said print clock means upon completion of a time interval corresponding to a complete character reproduction cycle;

all of the operations of said printer and said control system, subsequent to said input means, being timed solely by said print clock signal.

11. A control system for a high-speed dot matrix printer, according to claim **10**, in which said column signal generating means comprises a column counter of several stages, connected to said print clock means, and a BCD-decimal converter connected to said column counter.

12. A control system for a high-speed dot matrix printer, according to claim **10**, and further comprising:

a non-print function detector, coupled to said operational storage means, for generating a non-print control signal upon recording of a non-print code word in said operational storage means;

and print enabling means for utilizing said non-print control signal to inhibit operation of said character generator for a non-print code word,

said non-print control signal also being utilized by said enabling means to inhibit normal column stepping operation of said motor in response to a non-print code word.

13. A control system for a high-speed dot matrix printer, according to claim **12**, and further comprising:

a plurality of individual function detectors, each connected to said non-print function detector and to said operational storage means, for detecting specific printer functions; and

check means, connected to said print clock means, for developing a check signal at a given print clock count of less than $n/2$, and for applying said check signal to said individual function detectors to actuate the same.

14. An all-electronic control system for a high-speed dot matrix printer, according to claim **10**, in which said step motor includes four field windings and in which said step motor control comprises two flip-flop circuits each having two unidirectional inputs, a clock input, and two complementary outputs, one output of each flip-flop being connected in an energizing circuit for a respective individual motor winding, and four feedback circuits each connecting one output of one flip-flop circuit to a respective unidirectional input of the other flip-flop circuit;

and means for applying said step signal to the clock inputs of both flip-flop circuits to actuate said flip-flop circuits in a fixed sequence.

15. An all-electronic control system for controlling a high-speed dot matrix printer including a carriage, a plurality of print rods and print rod actuators mounted on the carriage, and a stepping motor, having four field windings, for rapidly advancing said carriage along a given path, in minute incremental column steps, with a given number p of column steps for each produced character, comprising:

step and print control means for generating a series of p step signal pulses for each character to be reproduced;

a step motor control including two flip-flop circuits each having two unidirectional inputs, a clock input, and two complementary outputs, one output of each flip-flop being connected in an energizing circuit for one of said step motor windings, and four feedback circuits each connecting one output of one flip-flop circuit to a respective unidirectional input of the other flip-flop circuit;

and means for applying said step signal pulses to the clock inputs of said two flip-flop circuits to actuate said flip-flop circuits in a fixed sequence and thereby step said motor in a given direction through *p* column steps for each character.

16. An all-electronic control system for a high-speed dot matrix printer, according to claim **15**, in which each of said feedback circuits includes an inverting AND-OR gate, and further comprising means to actuate said AND-OR gates to effect reverse stepping movement of said stepping motor for a given non-print function of said printer.

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