US 20060255444A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2006/0255444 A1**

(43) **Pub. Date: Nov. 16, 2006**

Moshayedi

(54) **SYSTEM AND METHOD FOR VERTICALLY STACKING COMPUTER MEMORY COMPONENTS**

(75) Inventor: **Mark Moshayedi**, Orange, CA (US)

Correspondence Address:
SimpleTech, Inc.
c/o S. Jalal Sadr, Esq.
3001 Daimler Street
Santa Ana, CA 92705 (US)

(73) Assignee: **SimpleTech, Inc.**

(21) Appl. No.: **11/404,464**

(22) Filed: **Apr. 13, 2006**

Related U.S. Application Data

(63) Continuation of application No. 10/853,865, filed on May 25, 2004, now Pat. No. 7,057,270, which is a continuation of application No. 10/127,343, filed on Apr. 19, 2002, now Pat. No. 6,762,487.

(60) Provisional application No. 60/285,089, filed on Apr. 19, 2001.

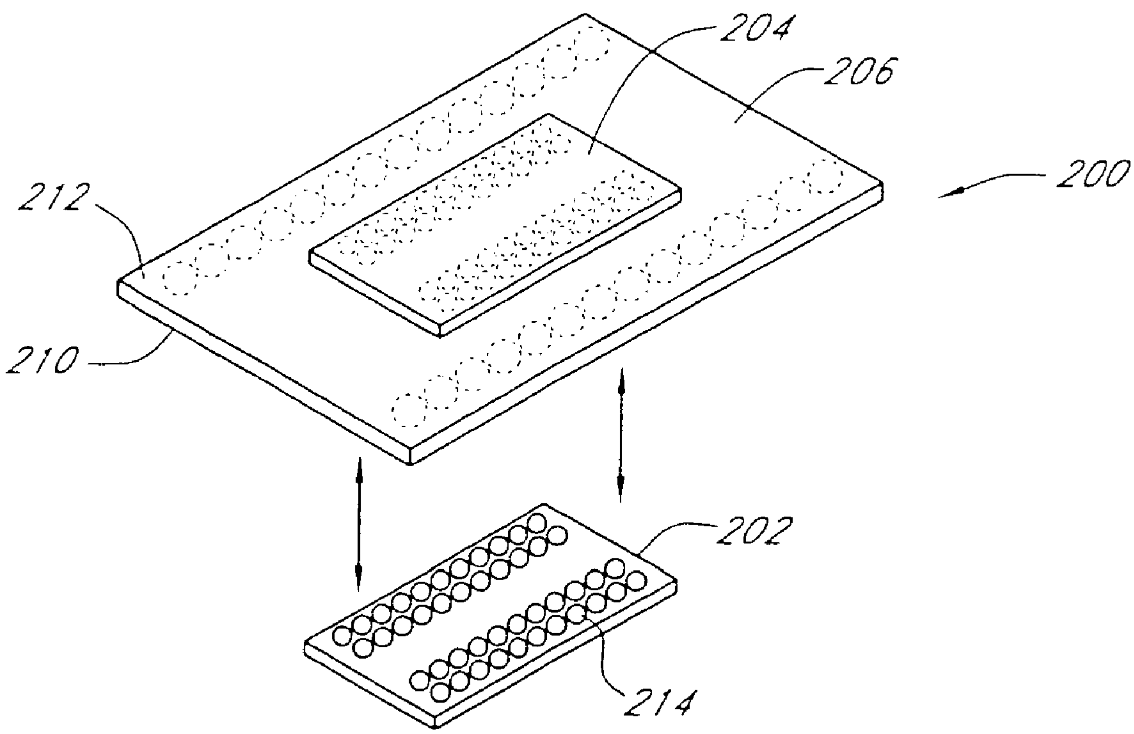
Publication Classification

(51) **Int. Cl.**
H01L 23/02 (2006.01)
H01L 21/00 (2006.01)

(52) **U.S. Cl.** **257/686**; 438/109; 257/E23

(57) **ABSTRACT**

System and method for vertically interconnecting a plurality of chips to provide increased volume circuit density for a given surface chip footprint. One embodiment provides a chip stack where two smaller chips are interconnected to a larger third chip on both sides thereof with the lower smaller chip flipped and connected below the larger chip. Further, in another embodiment, interconnecting structures extend from the larger chip beyond the extent of the lower smaller chip to facilitate the electronic connection of the chip stack with other computer components or circuit board. Another embodiment provides a method for stacking chips where two smaller chips are interconnected to a larger third chip on both sides thereof with the lower smaller chip flipped and connected below the larger chip.



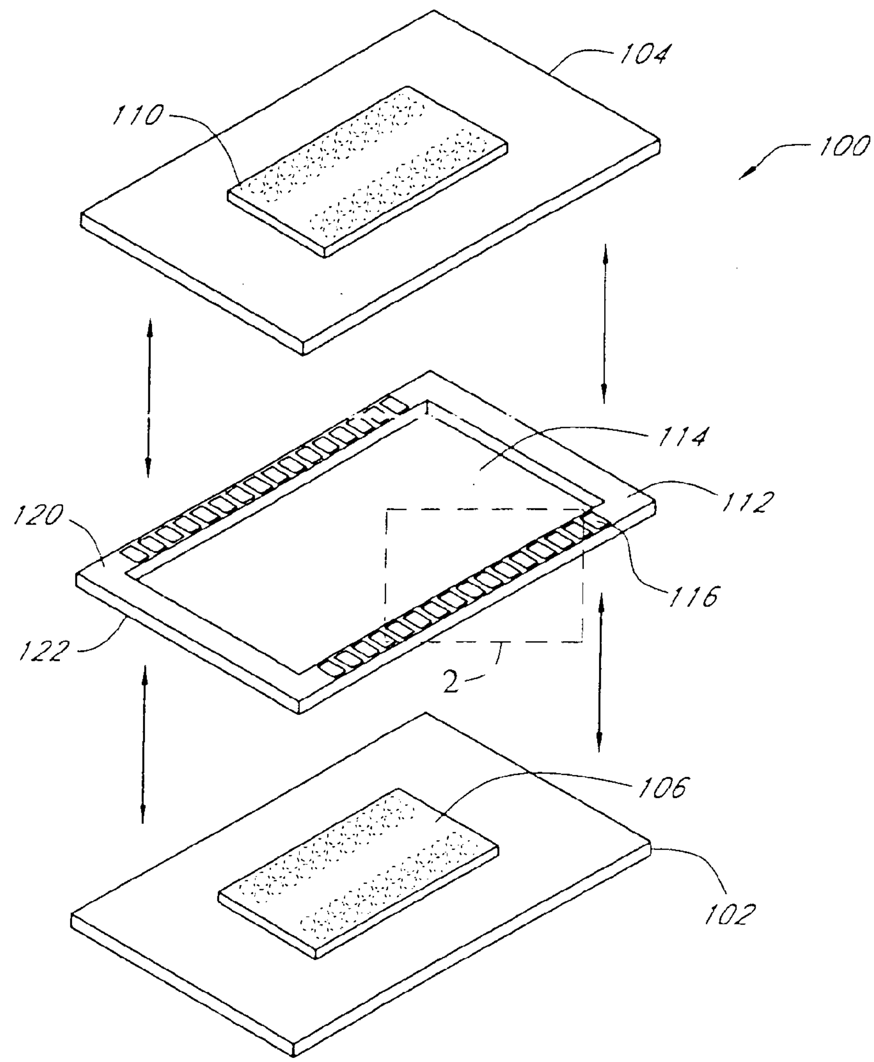


FIG. 1

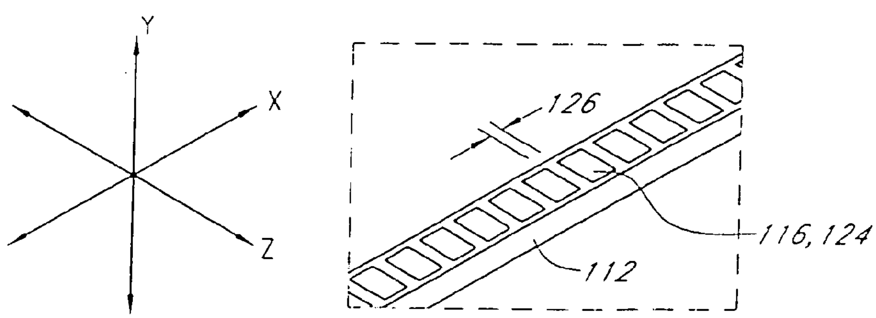


FIG. 2

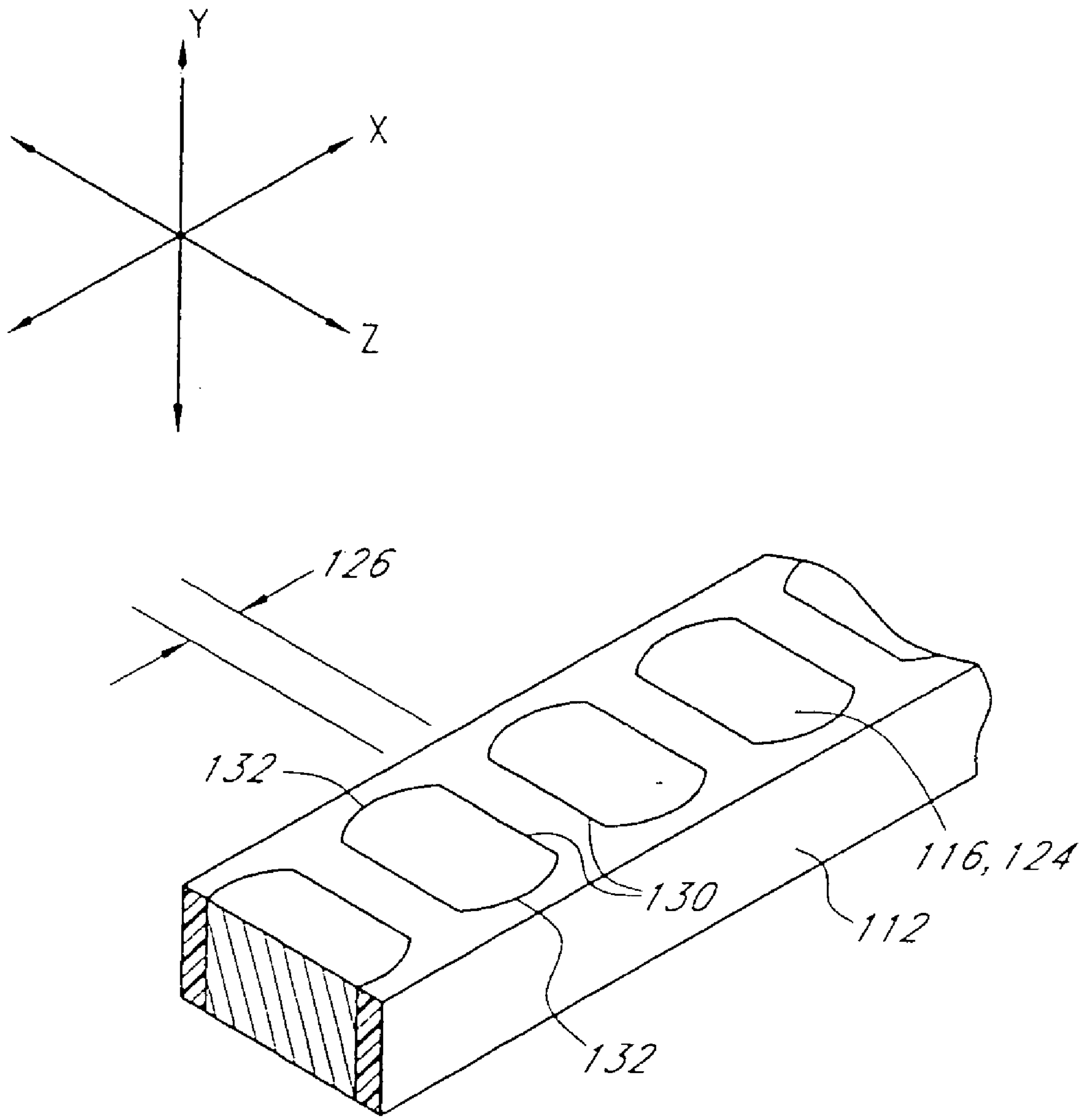


FIG. 3

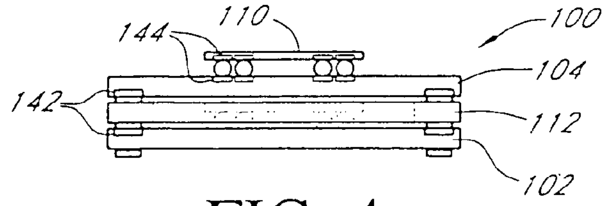


FIG. 4

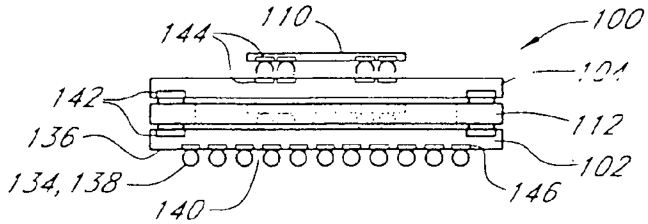


FIG. 5

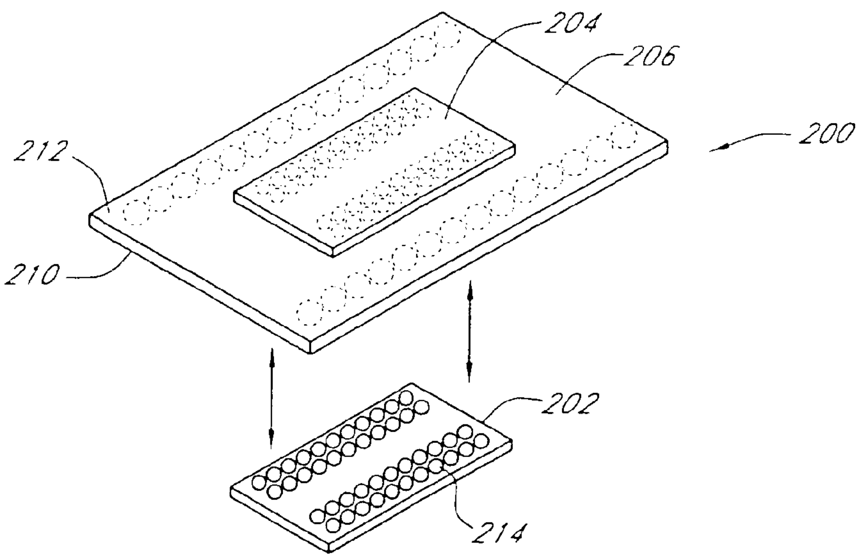


FIG. 6

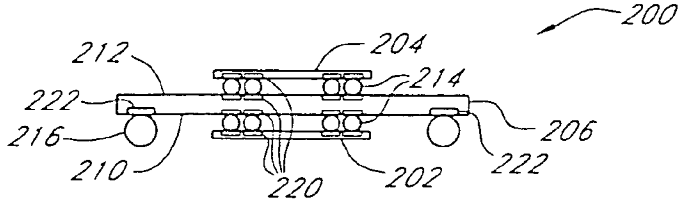


FIG. 7

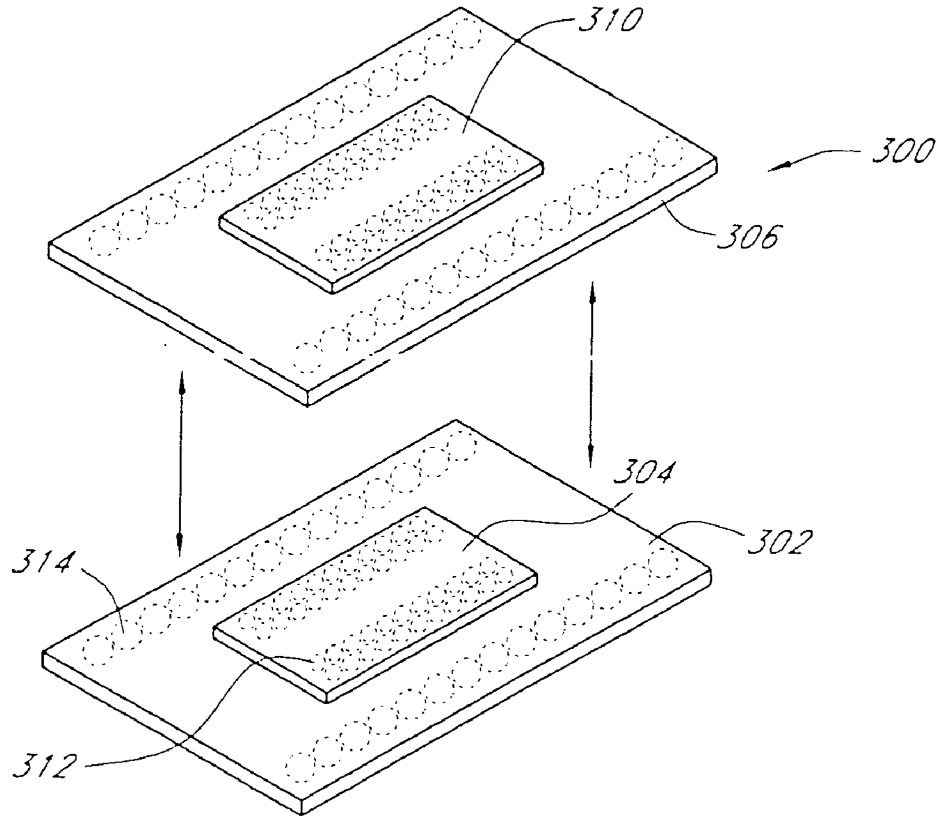

310
300
306
304
302
314
312

FIG. 8

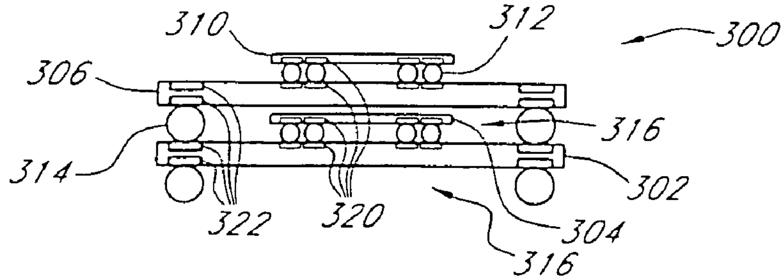

310
312
300
306
316
314
302
322
320
304
316

FIG. 9

SYSTEM AND METHOD FOR VERTICALLY STACKING COMPUTER MEMORY COMPONENTS

RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application No. 10/853,865, filed May 25, 2004, which is a continuation of U.S. application No. 10/127,343, filed Apr. 19, 2002, which claimed the benefit of U.S. Provisional Application No. 60/285,089 filed Apr. 19, 2001.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates to the field of integrated circuit interconnections and, in particular, to structures and methods for vertically stacking chips for increased volume density without increased footprint.

[0004] 2. Description of the Related Art

[0005] Modern electronic devices, such as computers and the like, typically include integrated circuits encapsulated in packages generally referred to generically as "chips". Chips are generally planar structures and typically include a plurality of conducting pads disposed as surface contacts about a surface of the chip and/or "pins" along an edge thereof. The conducting pads generally interconnect to a plurality of interconnecting conductive traces that extend from the pads to the electronic devices within the chip and allow interconnection of the electronic devices to external circuits to allow a system level circuit.

[0006] With advances in semiconductor device processing has come a continuing increase in device count and density within chips and this has driven a corresponding increase in the count and density of the external conducting pads. Current technology places a limit on how small external contacts can be made and how closely they can be placed adjacent one another while still maintaining circuit integrity. Limits are imposed both by the limitations of machinery to form ever smaller conductive elements and the reduction in production yield as the limits are pushed.

[0007] An additional concern is an overall system level consideration of packaging. As previously mentioned, chips are generally planar structures with relatively thin, flat profile. A common practice has been to interconnect chips on another generally planar support structure often referred to as a "mother board". However, the desire to provide the capability of integrated circuits to relatively small devices limits the extent to which multiple chips can be laterally interconnected while still fitting within the device. In addition, lateral extension and interconnection of chips tends to lead to relatively long interconnects between chips and thus between circuit components thus introducing propagation delays that can limit the practical speed of operation of the system level circuits.

[0008] From the foregoing, it can be appreciated that there is an ongoing need for structures and methods for interconnecting chips to increase circuit density without increasing the chip footprint and with minimal increase in interconnection length.

SUMMARY OF THE INVENTION

[0009] The aforementioned needs are satisfied by the invention which in one aspect is various structures and methods for interconnecting a plurality of generally planar chips in a vertical stack such that the stack chips define interstitial spaces that provide clearance for additional chips to be placed therein. The various structures and methods include the aspect that the total footprint of the stack does not exceed the footprint of the single largest component chip.

[0010] A certain aspect of the invention is a chip stack of a preformed support structure vertically interconnecting a first chip to a second chip with a third chip interposed therebetween wherein the support structure comprises a rigid annular housing defining an opening adapted to provide clearance for the third chip and a plurality of conductor cavities disposed about the periphery of the housing and extending between a first face and an opposite second face of the housing and a plurality of conductive elements positioned within the conductor cavities such that a portion of each conductive element extends slightly beyond the first and second faces of the housing so as to interconnect the first and second chips and such that each of the conductive element extends substantially flush with the edges of the conductor cavities on the first and second faces of the housing so as to substantially fill the corresponding conductor cavity. A particular aspect therein is wherein the conductor cavities of the support structure are substantially rectangular in horizontal cross-section or more particularly wherein the conductor cavities of the support structure are substantially square in horizontal cross-section.

[0011] Other aspects of the invention are wherein walls of the conductor cavities are substantially parallel to other conductor cavity walls along their adjacency to the adjacent conductor cavities and/or wherein the conductor cavities define first opposing walls facing adjacent conductor cavities and second opposing walls between the first walls wherein the first walls are generally planar and parallel to the first walls of adjacent conductor cavities and wherein the second walls are generally convexly curved.

[0012] The invention also includes the aspects of a preformed support structure for vertically interconnecting a first chip to a second chip with a third chip interposed therebetween wherein the support structure comprises a rigid annular housing defining an opening adapted to provide clearance for the third chip and a plurality of conductor cavities disposed about the periphery of the housing and extending between a first face and an opposite second face of the housing and a plurality of conductive elements positioned within the conductor cavities such that a portion of each conductive element extends slightly beyond the first and second faces of the housing and such that each of the conductive element extends substantially flush with the edges of the conductor cavities on the first and second faces of the housing so as to substantially fill the corresponding conductor cavity. A particular aspect therein is wherein the conductor cavities of the support structure are substantially rectangular in horizontal cross-section and more particularly wherein the conductor cavities of the support structure are substantially square in horizontal cross-section.

[0013] The invention further includes the aspect wherein walls of the conductor cavities are substantially parallel to other conductor cavity walls along their adjacency to the adjacent conductor cavities and wherein the conductor cavities define first opposing walls facing adjacent conductor cavities and second opposing walls between the first walls wherein the first walls are generally planar and parallel to the first walls of adjacent conductor cavities and wherein the second walls are generally convexly curved.

[0014] The invention is also a method of interconnecting chips having surface contacts comprising forming a generally annular support structure with a plurality of conductor cavities extending between opposite faces of the support structure and aligned with the surface contacts, filling the conductor cavities with conductive material such that the conductive material substantially fills the conductor cavities and extends slightly beyond the opposite faces of the support structure, placing chips on the support structure such that the surface contacts are adjacent and aligned with the conductor cavities so as to form a stack of the chips and the support structure, and processing the stack so as to induce the conductive material to connect to the surface contacts.

[0015] Yet another aspect of the invention is a chip stack of at least a first, a second, and a third chip and conductive interconnecting structures of at least a first size and a second smaller size interconnecting the chips wherein the third chip has a smaller footprint than either of the first or second chips and wherein the first conductive structures interconnect the first and second chips so as to define an interstitial space therebetween and the third chip is connected to at least one of the first and the second chips via the second conductive structures and is positioned within the interstitial space such that the vertical extent of the first conductive support structures is greater than the combined vertical extent of the third chip and the second conductive support structures. Particularly therein, the invention includes wherein the third chip is connected to one of the first or the second chips via the second conductive structures.

[0016] An additional aspect of the invention is a chip stack of at least a first, a second, and a third chip and conductive interconnecting structures of a first size interconnecting the first and second chips to the third chip wherein the third chip has a larger footprint than either of the first or second chips and further comprising second conductive support structures connected to the third chip such that the vertical extent of the second conductive support structures is greater than the combined vertical extent of either the first or second chips and the associated first conductive support structures.

[0017] These and other objects and advantages of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] **FIG. 1** is an exploded, perspective view of one embodiment of a preformed support structure vertically interconnecting a first chip to a second chip with a third chip interposed therebetween;

[0019] **FIG. 2** is a detail, perspective view of a portion of one embodiment of the preformed support structure of FIG. I wherein conductor cavities of the support have a generally square cross-section;

[0020] **FIG. 3** is a detail, perspective view of a portion of another embodiment of the preformed support structure of FIG. I wherein conductor cavities of the support have generally planar walls generally parallel to the walls of adjacent cavities and a generally convex outward curve on the sides between the planar sides;

[0021] **FIG. 4** is a side view of one embodiment of a preformed support structure vertically interconnecting a first chip to a second chip with a third chip interposed therebetween;

[0022] **FIG. 5** is a side view of another embodiment of a preformed support structure vertically interconnecting a first chip to a second chip with a third chip interposed therebetween;

[0023] **FIG. 6** is an exploded perspective view of one embodiment of a chip stack of at least a first, a second, and a third chip and conductive interconnecting structures of at least a first size and a second smaller size interconnecting the chips;

[0024] **FIG. 7** is a side view of the chip stack of **FIG. 6**;

[0025] **FIG. 8** is an exploded perspective view of one embodiment of a chip stack of at least a first, a second, and a third chip and conductive interconnecting structures of a first size interconnecting the first and second chips to the third chip; and

[0026] **FIG. 9** is a side view of the chip stack of **FIG. 8**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0027] Reference will now be made to the drawings wherein like numerals refer to like parts throughout. **FIG. 1** is an exploded, perspective view of one embodiment of a chip stack **100** of the invention. The chip stack **100**, in this embodiment, comprises a first chip **102**, a second chip **104** and a third chip **106**. The chip stack **100** as illustrated in **FIG. 1** further comprises a fourth chip **110**. The chips **102**, **104**, **106**, **110** comprise packaged integrated circuits with exposed contacts of types generally well known in the art.

[0028] The chip stack **100** also comprises a preformed support **112** vertically interconnecting the first chip **102** and the second chip **104**. The support **112** in this particular embodiment is generally rectangular and is sized to generally match the shape and size of the first **102** and second **104** chips. The support **112** is also annular, defining an internal opening **114**. The opening **114** in this particular embodiment is also generally rectangular and sized to provide clearance for the third chip **106** within the opening **114**. The support **112** is made of a rigid, non-conducting material.

[0029] The support **112** also includes a plurality of conductor cavities **116**. The conductor cavities **116** extend generally vertically between a first face **120** and an opposite second face **122** of the support **112**. The conductor cavities **116** are substantially filled with a conductive material **124**. In certain embodiments, the conductive material **124** comprises a metal of relatively low melting point, such as solder and in alternative embodiments, the conductive material **124** comprises a conductive adhesive material, such as epoxy. An advantageous aspect of this embodiment is that the support **112** is provided in a preformed manner with the conductor cavities **116** substantially filled with the conductive material **124**. This aspect of this embodiment facilitates alignment of the conductive material **124** within the rigid support **112** and maintains the alignment as the first **102** and second **104** chips are interconnected via the support **112** in a manner that will be described in greater detail below.

[**0030**] The conductor cavities **116** are disposed mutually aligned with contacts **142** of the first **102** and second **104** chips arrayed in a first pattern about the periphery of the support **112** (corresponding to the periphery of the first **102** and second **104** chips) with a spacing **126** as shown in **FIGS. 2 and 3**. As understood herein, the spacing **126** is the lateral separation between adjacent conductor cavities **116** as filled with the conductive material **124** as considered generally orthogonal to the generally vertical orientation of the conductor cavities **116**. It is to be understood that the terms "vertical" and "vertically" as used herein refer to a generally orthogonal orientation with respect to the major plane of the chips.

[**0031**] As shown in **FIGS. 2 and 3**, the conductor cavities **116** extend generally along the y-axis and have generally planar first walls **130** aligned generally along the y-z plane. The conductor cavities **116** also have second walls **132** between the first walls **130**. In the embodiment shown in **FIG. 2**, the first walls **130** and second walls **132** are generally planar and respectively parallel to each other. The first walls **130** are also perpendicular to the second walls **132** such that the conductor cavities **116** are generally rectangular in cross-section as considered along the horizontal x-z plane. In certain embodiments, the conductor cavities **116** are square in cross-section. It should also be understood that in further embodiments, the conductor cavities **116** can be circular, oval, or other cross-sectional shapes without detracting from the spirit of the invention.

[**0032**] It will be understood that the conductor cavities **116** filled with the conductive material **124** define signal lines conducting signals between the various electronic devices of the various chips **102**, **104**, **106**, **110**. It is generally essential to proper circuit operation that each of the plurality of conductive cavities **116** filled with conductive material **124** maintain signal integrity. Cross-talk between the conductor cavities **116** should preferably be inhibited. Cross-talk can arise because of conductive material **124** bridging across conductor cavities or excessive electric field intensity causing arcing across adjacent conductor cavities. Thus, the spacing **126** between adjacent conductor cavities **116** as filled with the conductive material **124** is subject to lower limits. In particular, a lower limit to the spacing **126** will be imposed by process limitations to forming smaller conductor cavities **116** or closer spacing **126** while maintaining reliable conductive integrity therethrough.

[**0033**] However, there is also a desire to increase conductivity of the conductor cavities **116** filled with conductive material **124** to reduce signal loss. One manner of increasing the conductivity is to increase the cross-sectional area of the conductor cavities **116**, thereby increasing the available volume for filling the cavities **116** with the conductive material **124**. Within a given width and thickness envelope, i.e. along the x and z directions, for placement of the conductor cavities **116**, a square cross-sectional aspect of the conductor cavities **116** as shown in **FIG. 2** will increase the available conductive material **124** for signal transmission and thus increase the conductance thereof.

[**0034**] **FIG. 3** illustrates an alternative embodiment of configuration for the conductor cavities **116** that may be advantageous in certain applications. In particular, the conductor cavities **116** of **FIG. 3** have first walls **130** that are generally planar and mutually parallel. The second walls **132**, positioned between the first walls **130**, in this embodiment, are convexly curved. This embodiment offers the advantage that the junction between the first **130** and second **132** walls has a larger radius of curvature, i.e. is less sharp. Thus a potential difference between conductor cavities **116** filled with conductive material **124** will result in a lower electric field intensity adjacent the conductor cavities **116** than an otherwise equivalent case with sharper corners thus reducing the likelihood of arcing across conductor cavities **116** of reduced dimensions and smaller spacing **126**. In certain applications, the embodiment of conductor cavities illustrated in **FIG. 3** may also offer advantages in manufacturing ease as opposed to embodiments with sharper comers between first **130** and second **132** walls.

[**0035**] In order to form the chip stack **100**, the chips **102**, **104**, **106**, **110** are preferably provided with a plurality of surface mount contacts **142**, **144** comprising solder balls or bumps of types generally well known in the art such that the solder balls or bumps are positioned mutually aligned with respect to each other such that the third chip **106** is generally centered on a face of the first chip **102** and that contacts **144** of the first **102** and third **106** chips are aligned in a second pattern as well as contacts **142** of the first **102** and second **104** chips aligned in a first pattern. The third chip **106** is attached to the first chip **102** by positioning the first chip **102** adjacent the third chip **106** so as to achieve alignment between the plurality of solder balls/bumps thereof. The first **102** and third **106** chips are then processed to induce the solder balls/bumps to partially liquefy and reflow and subsequently the first **102** and third **106** chips are further processed to induce the solder to resolidify thereby mutually affixing and interconnecting the first **102** and third **106** chips via the contacts **144**.

[**0036**] The support **112** is then placed between the first **102** and second **104** chips such that the third chip **106** is positioned within the internal opening **114** of the support **112** and such that the contacts **142** disposed about the periphery of the first **102** and second **104** chips are aligned with the conductor cavities **116**. In embodiments wherein the conductive material **124** is solder, the support **112** and first **102** and second **104** chips are then exposed to a heat process to induce the solder to partially liquefy and then allowed to cool to form a solder joint between the first **102** and second **104** chips at the contacts **142** via the support **112** with the preformed conductive material **124** in the conductor cavities **116**. In embodiments wherein the conductive material **124** comprises a conductive adhesive, the support **112** and first **102** and second **104** chips are maintained in alignment until the adhesive components of the conductive material **124** set.

[**0037**] **FIG. 4** illustrates an embodiment of the invention wherein the fourth chip **110** is attached to the second chip **104** in a similar manner to the connection of the third chip **106** to the first chip **102**. The fourth chip **100** can be attached to the second chip **104** in the manner previously described for the first **102** and third **106** chips either before or after the interconnection of the first **102** and second **104** chips. It will be appreciated that in additional embodiments, additional layers of supports **112** and chips could be formed to extend the height of and number of chips in the chip stack **100** in the manner previously described.

[0038] **FIG. 5** illustrates a further embodiment of the invention otherwise similar to the embodiments described with respect to **FIGS. 1-4** and further comprising a plurality of conductive supports **134** are attached to a lower face **136** of the first chip **102** at contacts **146**. In certain embodiments, the conductive supports **134** comprise balls or bumps of solder and, in other embodiments, a conductive, adhesive material such as conductive epoxy **138**. As can be seen in **FIG. 5**, the conductive supports **134** extend beyond the lower face **136** a vertical distance. In embodiments wherein the conductive supports **134** are generally positioned about the periphery of the lower face **136** of the first chip **102**, the conductive supports **136** define an interstitial space **140**. The interstitial space **140** provides clearance for the attachment of additional chips to the lower face **136** of the first chip **102** in a similar manner to that in which the internal opening **114** of the support **112** provides clearance for the third chip **106** on an upper face **142** of the first chip **102**.

[0039] The conductive supports **134** also provide mechanism for attaching the lower face of the first chip **102** to other chips or structures that have a footprint at least generally as large as that of the first chip **102**. It will be appreciated that the various electronic devices of the chips **102**, **104**, **106**, **110** can thus be interconnected to underlying circuits or structures without exceeding the footprint of the single first chip **102**. These aspects of the invention facilitate efficient attachment of the first chip **102** and thus the chip stack **100** to other electronic structures or devices.

[0040] **FIG. 6** is an exploded, perspective view of another embodiment of a chip stack **200**. The chip stack **200** comprises a first chip **202**, a second chip **204**, and a third chip **206**. The chips **202**, **204**, and **206** are similar to the chips **102**, **104**, **106**, **110** previously described being encapsulated integrated circuits of types generally well known in the art. The chips **202**, **204**, **206** are also provided with a plurality of contacts **220**, **222** of types well known in the art as previously described for the chip stack **100**. The contacts **220** of the first **202** and second **204** chips are arrayed in a first pattern aligned with contacts **220** on a lower **210** and an upper **212** face respectively of the third chip **206**.

[0041] In this embodiment, the first **202** and second **204** chips have smaller footprints than that of the third chip **206**. The first contacts **220** of the third **206** chips are positioned generally centrally on the lower **210** and upper **212** faces of the third chip **206**.

[0042] The chip stack **200** also comprises a plurality of first conductive interconnecting structures **214**. The first interconnecting structures **214** in this embodiment comprise balls/bumps of solder arrayed about a face of the first **202** and second **204** chips and aligned with the contacts **222** thereof. The first interconnecting structures **214** are aligned between the contacts **220** of the first chip **202** and the first contacts **220** on the lower face **210** of the third chip **206** and between the contacts **220** of the second chip **204** and the first contacts **220** on the upper face **212** of the third chip **206**. The first interconnecting structures **214** and the chips **202**, **204**, **206** are processed to induce the first interconnecting structures **214** to partially liquefy and then allowed to cool so as to form a solder joint between the first **202** and third **206** and the second **204** and third **206** chips at the contacts **220**.

[0043] The third chip **206** also comprises a plurality of second contacts **222** disposed about the lower face **210** and positioned outside the attachment of the first chip **202** to the third chip **206**. The chip stack **200** also comprises a plurality of second interconnecting structures **216** similar in composition and form to the first interconnecting structures **214**. However, the first interconnecting structures **214** are of a first size and the second interconnecting structures **216** are of a larger second size. In particular, the vertical dimension of the second interconnecting structures **216** is greater than the combined vertical dimension of the first chip **202** and the first interconnecting structures **214** as interconnecting the first **202** and the third **206** chips.

[0044] Thus, as can be seen in **FIG. 7**, the second interconnecting structures extend vertically beyond the first chip **202** as interconnected to the third chip **206**. The second interconnecting structures **216** facilitate interconnection of the third chip **206**, and thus as desired, the first **202** and second **204** chips, via the third chip **206**, to an underlying chip or structure. These aspects provide alternative efficient interconnection mechanism for connecting a plurality of chips **202**, **204**, **206** to an underlying structure without exceeding the footprint of the largest single (third **206**) chip.

[0045] **FIGS. 8 and 9** illustrate an additional alternative embodiment of a chip stack **300**. The chip stack **300** comprises a first chip **302**, a second chip **304**, a third chip **306**, and a fourth chip **310**. The chips **302**, **304**, **306**, **310** are generally planar encapsulated integrated circuits of types well known in the art. In this embodiment, the first **302** and the third **306** chips and the second **304** and the fourth **310** chips respectively have substantially similar footprints. The chip stack **300** also comprises first **312** and second **314** interconnecting structures. The interconnecting structures **312**, **314** comprise solder balls/bumps and the first interconnecting structures **312** are of a first size and the second interconnecting structures **314** are of a second larger size. In particular, the second interconnecting structures **314** are larger in vertical dimension than the combined vertical dimension of the first interconnecting structures **312** and one of the chips **304** and **310**.

[0046] The chips **302**, **304**, **306**, **310** comprise contacts **320**, **322** disposed about faces of the chips **302**, **304**, **306**, **310**. In this embodiment, first contacts **320** are disposed on upper faces of the first **302** and third **306** chips and on lower faces of the second **304** and fourth **310** chips such that the first contacts **320** are aligned between the respective faces of the first **302** and second **304** chips and between the third **306** and fourth **310** chips.

[0047] The chips **302**, **306** also comprise second contacts **322** disposed on vertically corresponding positions on opposing upper and lower faces of the chips **302**, **306**. The second contacts **322** are disposed generally about the periphery of the chips **302**, **306** and outside the footprint of the chips **304** and **310**.

[0048] The chip stack **300** is formed by positioning first interconnecting structures **312** so as to be aligned between the first contacts **320** of the first **302** and second **304** chips as well as between the third **304** and the fourth **310** chips. Second interconnecting structures **314** are further positioned so as to be aligned between the second contacts **322** of the first **302** and third **306** chips. The chips **302**, **304**, **306**, **310** and first **312** and second **314** interconnecting structures are then processed so as to induce the first **312** and second **314** interconnecting structures to partial liquefy and then allowed to cool so as to resolidify and form solder joints between the chips **302**, **304**, **306**, **310** via the contacts **320**, **322**.

[**0049**] It can be seen in **FIG. 9**, that as the second interconnecting structures **314** are greater in vertical dimension than the combined vertical dimension of either the second **304** or fourth **310** chips plus the vertical dimension of a first interconnecting structure **312**, the attachment of the first **302** and third **306** chips via the second interconnecting structures **314** defines an interstitial space **316**. The interstitial space **316** provides clearance for the second chip **304** between the first **302** and third **306** chips. It can be appreciated that additional layers of chips and first **312** and second **314** interconnecting structures can be added to the chip stack **300** creating additional interstitial spaces **316** in alternative embodiments of the invention.

[**0050**] Although the foregoing description of the preferred embodiment of the present invention has shown, described, and pointed out the fundamental novel features of the invention, it will be understood that various omissions, substitutions, and changes in the form of the detail of the apparatus as illustrated, as well as the uses thereof, may be made by those skilled in the art without departing from the spirit of the present invention.

What is claimed is:

1-21. (canceled)

43. A chip stack comprising:

a first chip having a first and a second side, wherein a first plurality of contacts are formed on the first side in a first pattern and a second plurality of contacts are formed on the second side in a second pattern;

a second chip having a first and a second side, wherein the first side of the second chip includes a first plurality of contacts arranged in the first pattern, wherein the second chip is located proximate the first side of the first chip, and wherein the second chip is positioned so that the first plurality of contacts on the second chip are aligned with the first plurality of contacts on the first chip;

a third chip having a first and a second side wherein the third chip includes a first plurality of contacts arranged in the second pattern on the first side wherein the third chip is located proximate the second side of the first chip such that the first chip is interposed between the second and third chips and so that the first plurality of contacts on the third chip are aligned with the second plurality of contacts on the first chip;

a first set of interconnecting structures having a first length that are interposed between the first plurality of contacts on the first chip and the first plurality of contacts on the second chip so as to interconnect the first plurality of contacts on the first chip and the first plurality of contacts on the second chip; and

a second set of interconnecting structures having a second length that are interposed between the second plurality of contacts on the first chip and the first plurality of contacts on the third chip so as to interconnect the second plurality of contacts on the first chip and the first plurality of contacts on the third chip.

44. The chip stack of claim 43, wherein the first pattern is a substantially similar pattern as the second pattern.

45. The chip stack of claim 43, wherein the first chip further comprises a third plurality of contacts arranged in a third pattern on the second side.

46. The chip stack of claim 45, further comprising a third set of interconnecting structures having the second length interconnected to the third plurality of contacts.

47. The chip stack of claim 46, wherein the first chip and the third set of interconnecting structures are arranged in a modular unit defining an interstitial space around the third chip.

48. The chip stack of claim 46, wherein the first chip defines a platform over the third chip and wherein the third set of interconnecting structures define side struts supporting the platform.

49. The chip stack of claim 46, wherein the first chip and the third set of interconnecting structures are arranged in contiguous non-conductive material.

50. The chip stack of claim 46, wherein the first chip and the third set of interconnecting structures define a carrier for positioning one or more chips above the second chip.

51. The chip stack of claim 46, wherein the first chip and the third set of interconnecting structures are arranged within a modular unit that can accept one or more chips, and the modular unit further provides an interstitial space around the third chip.

52. The chip stack of claim 46, wherein the first chip comprises a preformed support structure.

53. A method of stacking chips comprising:

providing a first chip having a first and a second side, wherein a first plurality of contacts are formed on the first side in a first pattern and a second plurality of contacts are formed on the second side in a second pattern;

providing a second chip having a first and a second side, wherein the first side of the second chip includes a first plurality of contacts arranged in the first pattern, wherein the second chip is located proximate the first side of the first chip, and wherein the second chip is positioned so that the first plurality of contacts on the second chip are aligned with the first plurality of contacts on the first chip;

providing a third chip having a first and a second side wherein the third chip includes a first plurality of contacts arranged in the second pattern on the first side, and wherein the third chip is located proximate the second side of the first chip such that the first chip is interposed between the second and third chips and so that the first plurality of contacts on the third chip are aligned with the second plurality of contacts on the first chip;

providing a first set of interconnecting structures having a first length that are interposed between the first plurality of contacts on the first chip and the first plurality of contacts on the second chip so as to interconnect the first plurality of contacts on the first chip and the first plurality of contacts on the second chip; and

providing a second set of interconnecting structures having a second length that are interposed between the second plurality of contacts on the first chip and the first plurality of contacts on the third chip so as to interconnect the second plurality of contacts on the first chip and the first plurality of contacts on the third chip.

54. The method of stacking chips of claim 53, wherein the first pattern is a substantially similar pattern as the second pattern.

55. The method of stacking chips of claim 53, wherein the first chip further comprises a third plurality of contacts arranged in a third pattern on the second side.

56. The method of stacking chips of claim 55, further comprising providing a third set of interconnecting structures having a third length interconnected to the third plurality of contacts.

57. The method of stacking chips of claim 56, wherein the first chip and the third set of interconnecting structures are arranged in a modular unit defining an interstitial space around the third chip.

58. The method of stacking chips of claim 56, wherein the first chip defines a platform over the third chip and wherein the third set of interconnecting structures define side struts supporting the platform.

59. The method of stacking chips of claim 56, wherein the first chip and the third set of interconnecting structures are arranged in contiguous non-conductive material.

60. The method of stacking chips of claim 56, wherein the first chip and the third set of interconnecting structures define a carrier for positioning one or more chips above the second chip.

61. The method of stacking chips of claim 56, wherein the first chip and the third set of interconnecting structures are arranged within a modular unit that can accept one or more chips, and the modular unit further provides an interstitial space around the third chip.

62. A chip stack comprising:

a first chip having a first and a second side, wherein a first plurality of contacts are formed on the first side in a first pattern and a second plurality of contacts are formed on the second side in a second pattern;

a second chip having a first and a second side and a selected thickness, wherein the first side of the second chip includes a first plurality of contacts arranged in the first pattern, wherein the second chip is located proximate the first side of the first chip, and wherein the second chip is positioned so that the first plurality of contacts on the second chip are aligned with the first plurality of contacts on the first chip;

a third chip having a first and a second side wherein the third chip includes a first plurality of contacts arranged in the second pattern on the first side wherein the third chip is located proximate the second side of the first chip such that the first chip is interposed between the second and third chips and so that the first plurality of contacts on the third chip are aligned with the second plurality of contacts on the first chip;

means for interconnecting the first plurality of contacts on the first chip and the first plurality of contacts on the second chip; and

means for interconnecting the second plurality of contacts on the first chip and the first plurality of contacts on the third chip, wherein the first chip is interposed between the first side of the second chip and the first side of the third.

* * * * *